1.5°C ACCURATE PROGRAMMABLE DIGITAL TEMPERATURE SENSORS WITH SPI™ INTERFACE

FEATURES

- **Digital Output: SPI-Compatible Interface**
- **Programmable Resolution: 9 to 12 Bits + Sign**
- **Aaccuracy: ±1.5°C from -25°C to 85°C (max)**
  ±2.0°C from -55°C to 125°C (max)
- **Low Quiescent Current: 50 μA**
- **Wide Supply Range: 2.7 V to 5.5 V**
- **Tiny SOT23-6 Package**
- **Operation to 150°C**
- **Programmable High/Low Setpoints**

APPLICATIONS

- **Power-Supply Temperature Monitoring**
- **Computer Peripheral Thermal Protection**
- **Notebook Computers**
- **Cell Phones**
- **Battery Management**
- **Office Machines**
- **Thermostat Controls**
- **Environmental Monitoring and HVAC**
- **Electromechanical Device Temperature**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

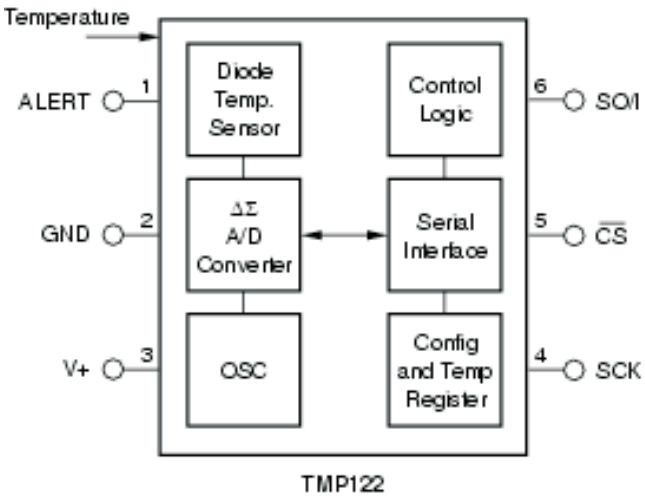
- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Additional temperature ranges are available - contact factory

DESCRIPTION

The TMP122 is an SPI-compatible temperature sensor available in an SOT23-6 package. Requiring only a pull-up resistor for complete function, the TMP122 temperature sensor is capable of measuring temperatures within 2°C of accuracy over a temperature range of -55°C to 125°C, with operation up to 150°C. Programmable resolution, programmable set points and shut down function provide versatility for any application. Low supply current and a supply range from 2.7 V to 5.5 V make the TMP122 an excellent candidate for low-power applications.

The TMP122 is ideal for extended thermal measurement in a variety of communication, computer, consumer, environmental, industrial, and instrumentation applications.



TMP122

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SPI is a trademark of Motorola.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOT23-6	Tape and reel of 250	TMP122AMDBVTEP	122E

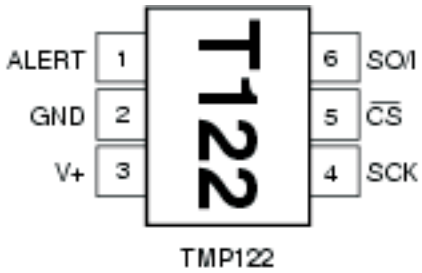
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V+	Power supply	7	V
V_I	Input voltage	-0.3 to 7	V
	Inout current	10	mA
	Operating temperature range	-55 to 150	°C
	Storage temperature range	-60 to 150	°C
T_J (max)	Junction temperature	150	°C
	Lead temperature (soldering)	300	°C

PIN CONFIGURATION



TMP122

ELECTRICAL CHARACTERISTICS

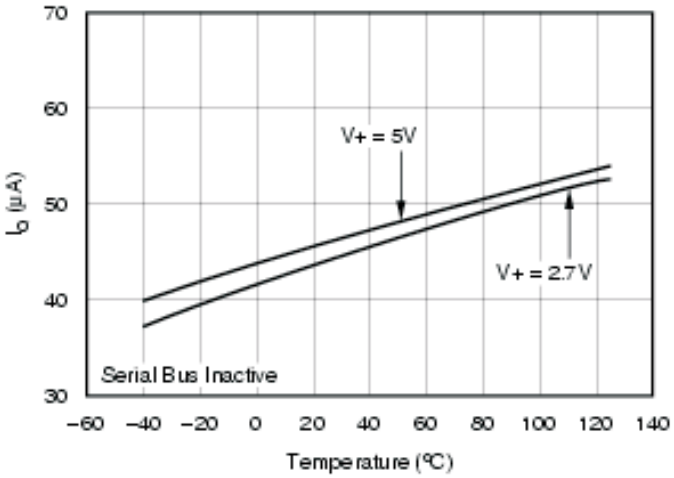
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Temperature input	Range		-55		125	°C
	Accuracy (temperature error)	-25°C to 85°C		±0.5	±1.5	°C
		-55°C to 125°C		±1.0	±2.0	
		-55°C to 150°C		±1.5		
	vs supply			0.1		°C/V
	Resolution(1)	Selectable		±0.0625		°C
Digital input/output	V_{IH}		0.7 (V+)			V
	V_{IL}				0.3 (V+)	V
	Input current, SO/I, SCK, $\overline{CS}$	0 V ≤ V_{IN} ≤ V+			±1	µA
	V_{OL} SO/I	I_{SINK} = 3mA			0.4	V
	V_{OH} SO/I	I_{SOURCE} = 2mA	(V+) - 0.4			V
	V_{OL} ALERT	I_{SINK} = 4mA			0.4	V
	Leakage current ALERT	0 V ≤ V_{IN} ≤ 6 V			±1	µA
	Input capacitance, SO/I, SCK, $\overline{CS}$, ALERT			2.5		pF
	Reolution	Selectable		9 to 12 + sign		bits
	Conversion time	9 bit + sign		30	40	ms
		10 bit + sign		60	80	
		11 bit + sign		120	160	
		12 bit + sign		240	320	
Power supply	Operating range		2.7		5.5	V
	Quiescent current I_Q	Serial bus inactive		50	75	µA
	Shutdown current I_{SD}	Serial bus inactive		0.1	1	
Temperature range	Specified range		-55		125	°C
	Operating range		-55		150	
	Storage range		-60		150	
	Thermal resistance, θ_{JA}	SOT23-6 surface-mount		200		°C/W

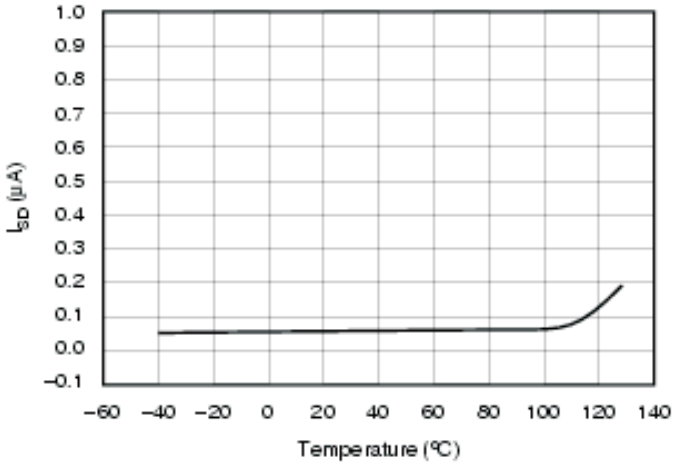
(1) Specified for 12-bit resolution.

TYPICAL CHARACTERISTICS

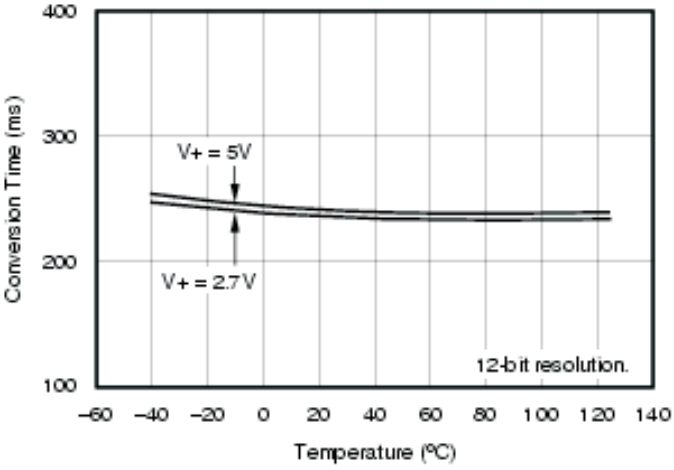
QUIESCENT CURRENT vs TEMPERATURE



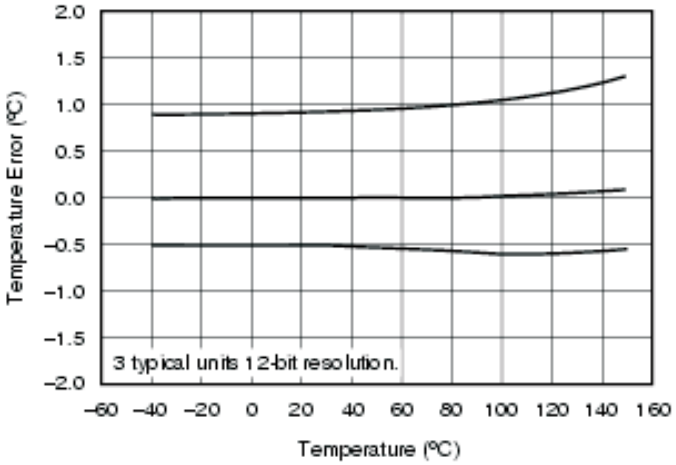
SHUTDOWN CURRENT vs TEMPERATURE



CONVERSION TIME vs TEMPERATURE



TEMPERATURE ACCURACY vs TEMPERATURE



APPLICATION INFORMATION

The TMP122 digital temperature sensor is optimal for thermal management and thermal protection applications. The TMP122 is SPI interface-compatible and specified for a temperature range of -55°C to 125°C.

The TMP122 requires minimal external components for operation, needing only a pullup resistor on the ALERT pin and a bypass capacitor on the supply. Bypass capacitors of 0.1 µF is recommended. Figure 1 shows typical connections for the TMP122.

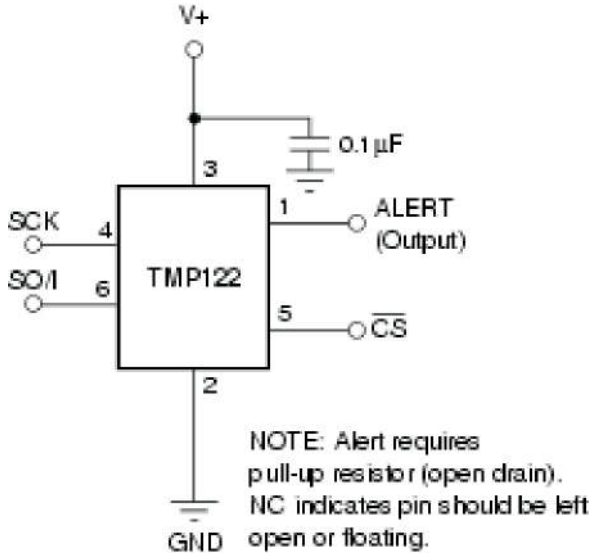


Figure 1. Typical Connections

To maintain accuracy in applications requiring air or surface temperature measurement, care should be taken to isolate the package and leads from ambient air temperature.

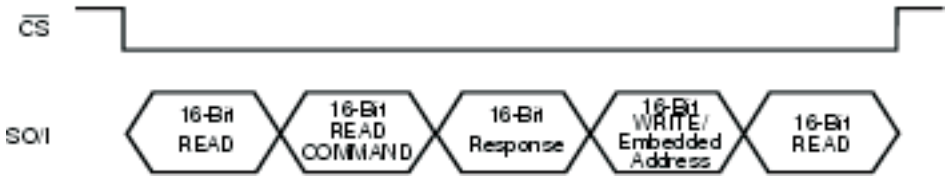


Figure 2. Multiple Command Sequence

COMMUNICATING WITH THE TMP122

The TMP122 converts continuously. If $\overline{CS}$ is brought low during a conversion the conversion process continues, but the last completed conversion is available at the output register. Communication with the TMP122 is initiated by pulling $\overline{CS}$ low. The first 16 clocks of data transfer will return temperature data from the temperature sensors. The 16-bit data word is clocked out sign bit first, followed by the MSB. Any portion of the 16-bit word may be read before raising $\overline{CS}$. If the user wishes to continue with $\overline{CS}$ low, the following 16 clocks transfer in a READ or WRITE command. READ and WRITE commands are described in Table 1 and Table 2.

The READ command contains an embedded address in bits D4 and D3 to identify which register to read. Bits D4 and D3 are internally registered and will hold their value following a READ command until an entire 16-bit read is completed by the user. The completion of the 16-bit READ acknowledges that the READ command has been completed. If the user issues a READ command and then raises $\overline{CS}$ with less than 16 subsequent clocks, the data from that register will be available at the next fall of $\overline{CS}$. Teh registered READ address will remain in effect until a full 16 clocks have been received. After the compleation of a 16-bit READ from the part, the READ address is reset to return data from the Temperature Register. A WRITE command to a register will not change the READ address registered. For further discussion on the READ address register, see the *Read Address Register* section.

Multiple commands may be strung together as illustrated in Figure 2. The TMP122 accepts commands alternating with 16-bit response data. On lowering $\overline{CS}$, the part always responds with a READ from the address location indicated by the READ address register. If the next command is a READ command then data is returned from the address specified by the READ command with the 16th clock resetting the READ address register to the default temperature register. The TMP122 then expects a 16-bit command. If the command is a WRITE command, then the 16 clocks following the command will again return temperature data.

Figure 3, Figure 4, Figure 5, and Figure 6 detail the communication sequences.

Table 1. READ Command

READ Command	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Temperature	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Configuration register	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
Low temperature threshold	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
High temperature threshold	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

Table 2. WRITE Command

WRITE Command	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Temperature	0	0	0	0	D1	D0	R1	R0	F1	F0	POL	TM1	TM0	0	1	0
Low temperature threshold	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	1	0	0
High temperature threshold	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	1	1	0
Shutdown command	x	x	x	x	x	x	x	x	1	1	1	1	1	1	1	1

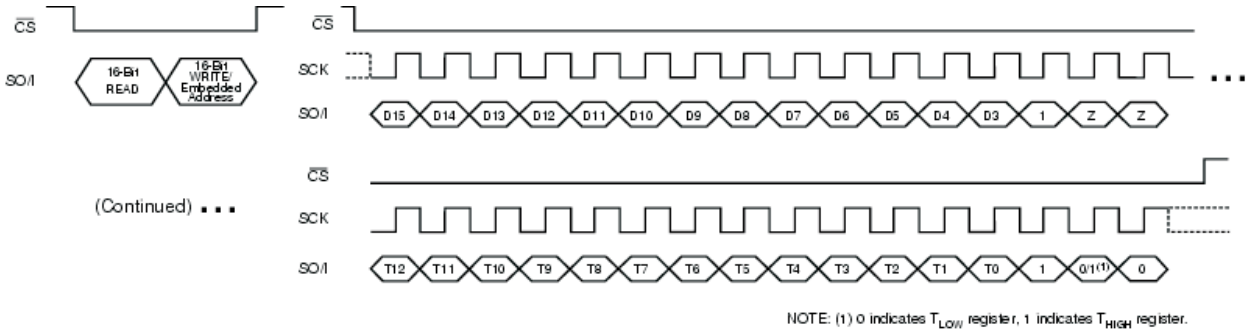


Figure 3. READ followed by WRITE Command to T_{LOW}/T_{HIGH} Register

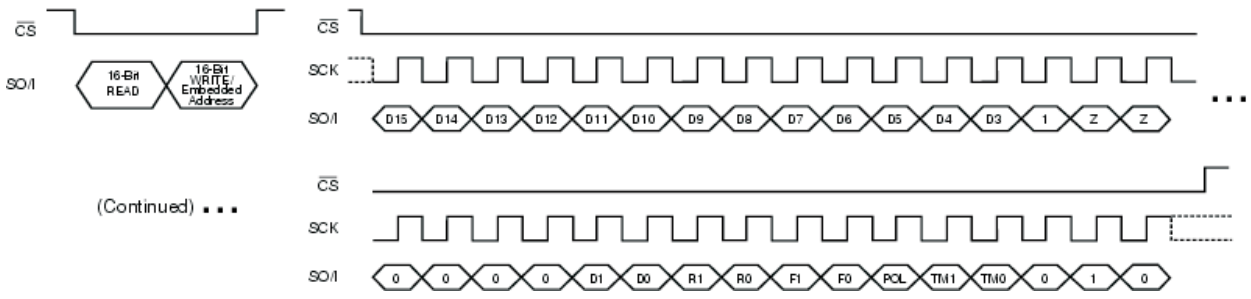


Figure 4. READ followed by WRITE Command to Configuration Register

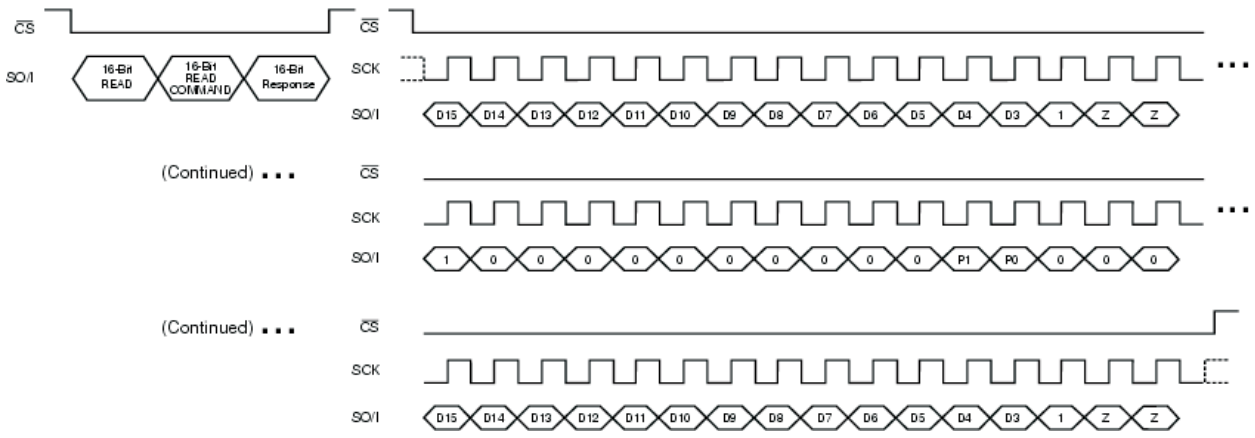


Figure 5. READ followed by READ Command and Response

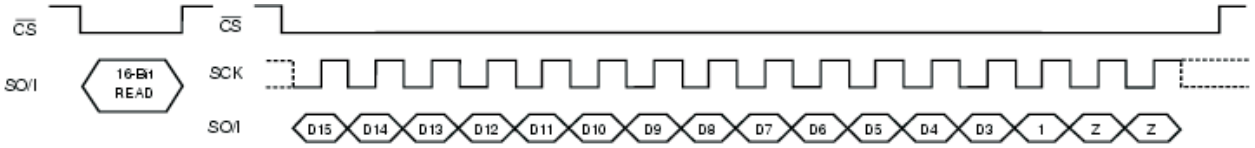


Figure 6. Data READ

READ ADDRESS REGISTER

Figure 7 shows the internal register structure of the TMP122/TMP124. Table III describes the addresses of the registers available. The READ address register uses the two bits to identify which of the data registers should respond to a read command. Following a complete 16-bit read, the READ address register is reset to the default power-up state of P1/P0 equal 0/0.

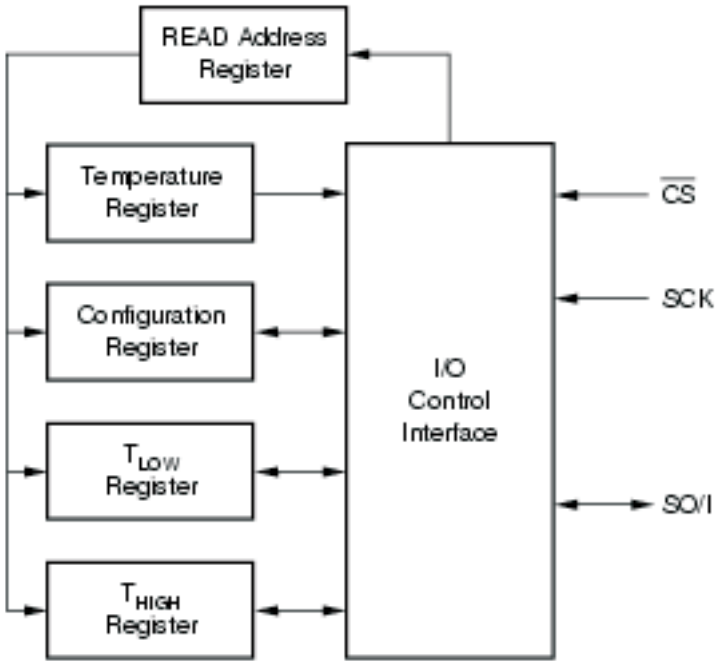


Figure 7. Internal Register Structure

Table 3. Pointer Addresses

P1	P0	REGISTER
0	0	Temperature Register (READ only)
0	1	Configuration Register (READ/WRITE)
1	0	T_{LOW} Register (READ/WRITE)
1	1	T_{HIGH} Register (READ/WRITE)

TEMPERATURE REGISTER

The Temperature Register of the TMP122 is a 16-bit, signed read-only register that stores the output of the most recent conversion. The TMP122 is specified for the temperature range of -55°C to 125°C with operation from -55°C to 150°C. Up to 16 bits can be read to obtain data and are described in Table 4. The first 13 bits are used to indicate temperature where bit D2 is 1, and D1, D0 are in a high impedance state. Data format for temperature is summarized in Table 5. Following power-up or reset, the Temperature Register will read 0°C until the first conversion is complete.

Table 4. Temperature Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	1	Z	Z

Table 5. Temperature Data Format

TEMPERATURE (°c)	DIGITAL OUTPUT(1) (BINARY)	HEX
150	0100 1011 0000 0111	4B07
125	0011 1110 1000 0111	3E87
25	0000 1100 1000 0111	0C87
0.0625	0000 0000 0000 1111	000F
0	0000 0000 0000 0111	0007
-0.0625	1111 1111 1111 1111	FFFF
-25	1111 0011 1000 0111	F387
-55	1110 0100 1000 0111	E487

(1) The last two bits are high impedance and are shown as 11 in the table.

The user can obtain 9, 10, 11, or 12 bits of resolution by addressing the Configuration Register and setting the resolution bits accordingly. For 9-, 10-, or 11-bit resolution, the most significant bits in the Temperture Register are used with the unused LSBs set to zero.

CONFIGURATION REGISTER

The Configuration Register is a 16-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read/write operations are performed MSB first. The format of the Configuration Register for the TMP122 is shown in Table 6, followed by a break-down of the register bits. The power-up/reset value of the Configuration Register bits R1/R0 equal 1/1, all other bits equal zero.

Table 6. Configuration Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	D1	D0	R1	R0	F1	F0	POL	TM1	TM0	0	1	0

SHUTDOWN MODE (SD)

The Shutdown Mode of the TMP122 can be used to shut down all device circuitry except the serial interface. Shutdown mode occurs when the last 8 bits of the WRITE command are equal to 1, and will occur once the current conversion is completed, reducing current consumption to less than 1 μA. To take the part out of shutdown, send any command or pattern after the 16-bit read with the last 8 bits not equal to one. Power on default is in active mode.

THERMOSTAT MODE (TM1/TM0)

The Thermostat Mode bits of the TMP122 indicate to the device whether to operate in Comparator Mode, Interrupt Mode or Interrupt Comparator Mode. For more information on Comparator and Interrupt Mode, see text HIGH and LOW limit registers. The bit assignments for thermostat mode are described in Table 7. Power on default is comparator mode.

Table 7. Mode Settings

TM1	TM0	MODE OF OPERATION
0	0	Comparator mode
0	1	Interrupt mode
1	0	Interrupt comparator mode
1	1	Reserved

POLARITY (POL)

The Polarity Bit of the TMP122 adjusts the polarity of the ALERT pin output. By default, POL = 0 and the ALERT pin will be active LOW, as shown in Figure 8. For POL = 1 the ALERT Pin will be active HIGH, and the state of the ALERT Pin is inverted.

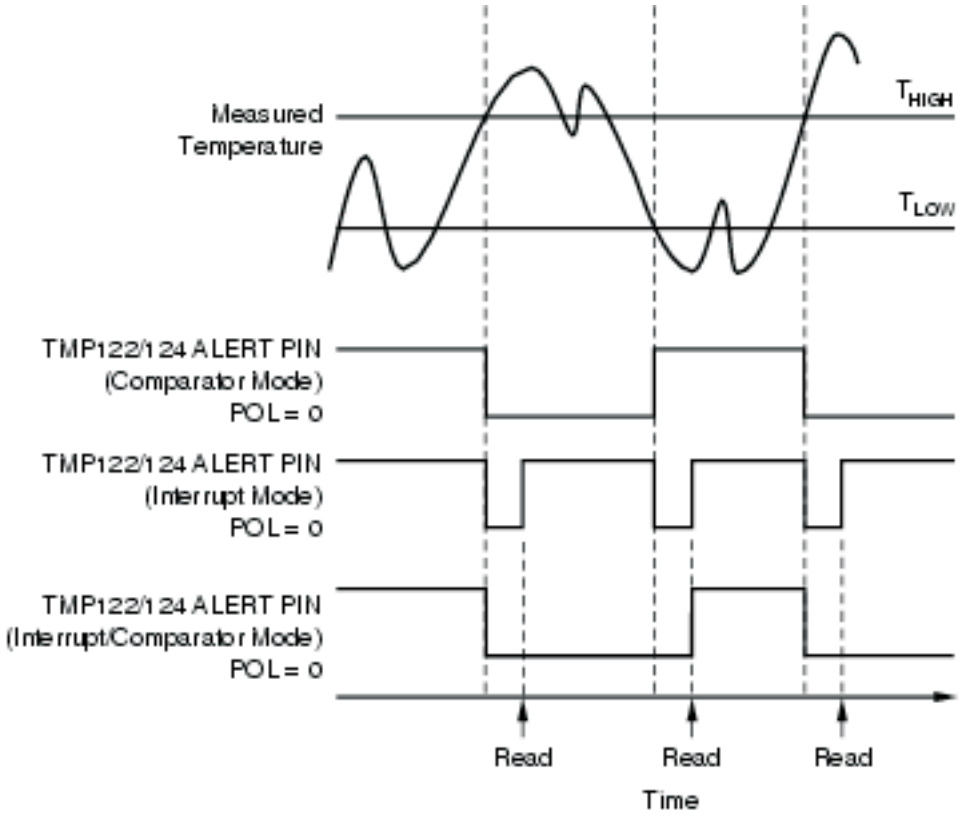


Figure 8. ALERT Output Transfer Function Diagrams

FAULT QUEUE (F1/F0)

A fault condition occurs when the measured temperature exceeds the limits set in the T_{HIGH} and T_{LOW} registers. The Fault Queue is provided to prevent a false alert due to environmental noise and requires consecutive fault measurements to trigger the alert function of the TMP122. Table 8 defines the number of consecutive faults required to trigger a consecutive alert condition. Power-on default for F1/F0 is 0/0.

Table 8. Fault Settings

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2
1	0	4
1	1	6

HIGH AND LOW LIMIT REGISTERS

In Comparator Mode (TM1/TM0 = 0/0), the ALERT Pin of the TMP122 becomes active when the temperature equals or exceeds the value in T_{HIGH} and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin will remain active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

In Interrupt Mode (TM1/TM0 = 0/1) the ALERT pin becomes active when the temperature equals or exceeds T_{HIGH} for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs. The ALERT pin will also be cleared if the device is placed in Shutdown Mode. Once the ALERT pin is cleared, it will only become active again by the temperature falling below T_{LOW}. When the temperature falls below T_{LOW}, the ALERT pin becomes active and remains active until cleared by a read operation of any register. Once the ALERT pin is cleared, the above cycle will repeat with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH}.

In Interrupt/Comparator Mode (TM1/TM0 = 1/0), the ALERT Pin of the TMP122 becomes active when the temperature equals or exceeds the value in T_{HIGH} and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin will remain active until the temperature falls below the indicated T_{LOW} value for the same number of faults and a communication with the device has occurred after that point.

Operational modes are represented in Figure 8. Table 9 and Table 10 describe the format for the T_{HIGH} and T_{LOW} registers. Power-up reset values for T_{HIGH} and T_{LOW} are: T_{HIGH} = 80°C and T_{LOW} = 75°C. The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature Register. TABLE IX. T_{HIGH} Register.

All 13 bits for the Temperature, T_{HIGH}, and T_{LOW} registers are used in the comparisons for the ALERT function for all converter resolutions. The three LSBs in T_{HIGH} and T_{LOW} can affect the ALERT output even if the converter is configured for 9-bit resolution.

Table 9. T_{HIGH} Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
H12	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0	1	1	0

Table 10. T_{LOW} Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0	1	0	0

CONVERTER RESOLUTION (R1/R0)

The Converter Resolution Bits control the resolution of the internal analog-to-digital (A/D) converter. This allows the user to maximize efficiency by programming for higher resolution or faster conversion time. Table 11 identifies the resolution bits and the relationship between resolution and conversion time. The TMP122 has a default resolution of 12 bits.

Table 11. Resolution

R1	R2	RESOLUTION	CONVERSION TIME (TYPICAL)
0	0	9 bits (0.5°C) + sign	30 ms
0	1	10 bits (0.25°C) + sign	60 ms
1	0	11 bits (0.125°C) + sign	120 ms
1	1	12 bits (0.0625°C) + sign	240 ms

DELAY TIME

The Delay Bits control the amount of time delay between each conversion. This feature allows the user to maximize power savings by eliminating unnecessary conversions, and minimizing current consumption. During active conversion the TMP122 typically requires 50 μA of current for approximately 0.25s conversion time, and approximately 20 μA for idle times between conversions. Delay settings are identified in Table 12 as conversion time and period, and are shown in Figure 9. Default power up is D1/D0 equal 0/0. Conversion time and conversion periods scale with resolution. Conversion period denotes time between conversion starts.

Table 12. Conversion Delay for 12-Bit Resolution

D1	D2	CONVERSION TIME	CONVERSION PERIOD
0	0	0.25 s	0.25 s
0	1	0.25 s	0.5 s
1	0	0.25 s	1 s
1	1	0.25 s	8 s

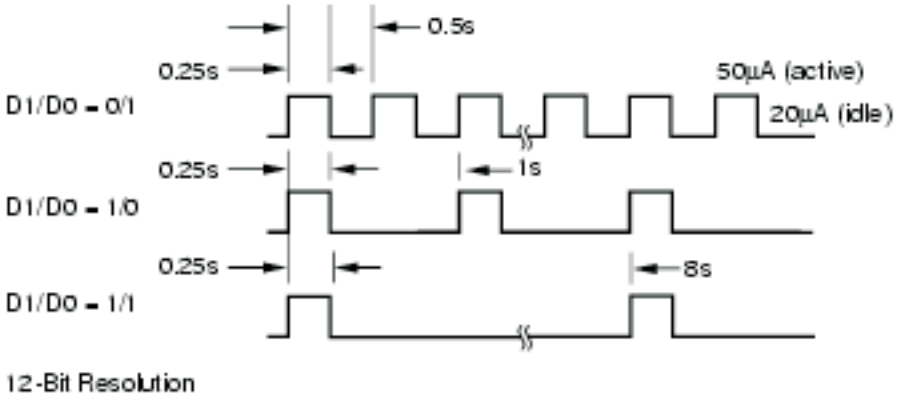


Figure 9. Conversion Time and Period Description

TIMING DIAGRAMS

The TMP122 is SPI compatible. Figure 10 to Figure 12 describe the various timing parameters of the TMP122 with timing definitions in Table 13.

Table 13. Timing Description

	PARAMETER	MIN	MAX	UNIT
t_1	SCK period	100		ns
t_2	Data in to rising edge SCK setup time	20		ns
t_3	SCK falling edge to output data delay		30	ns
t_4	SCK rising edge to input data hold time	20		ns
t_5	$\overline{CS}$ to rising edge SCK set-up time	40		ns
t_6	$\overline{CS}$ to output data delay		30	ns
t_7	$\overline{CS}$ rising edge to output high impedance		30	ns

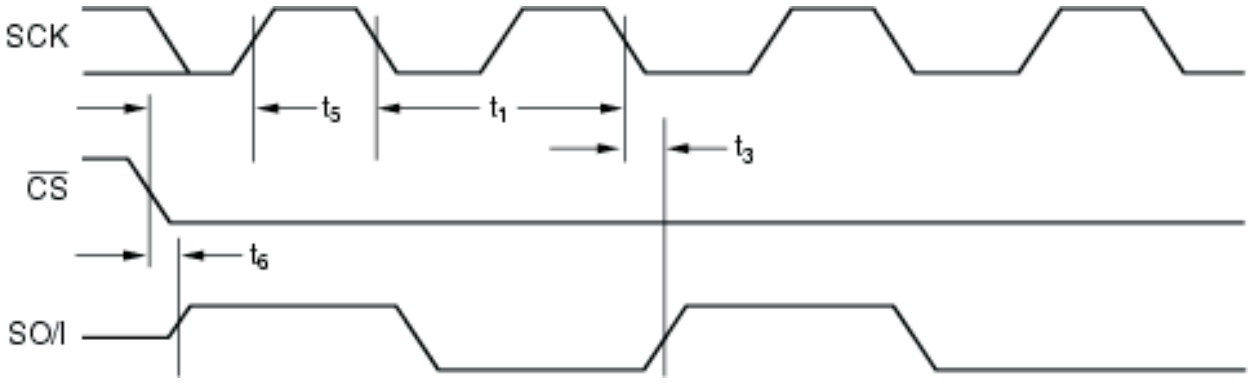


Figure 10. Output Data Timing Diagram

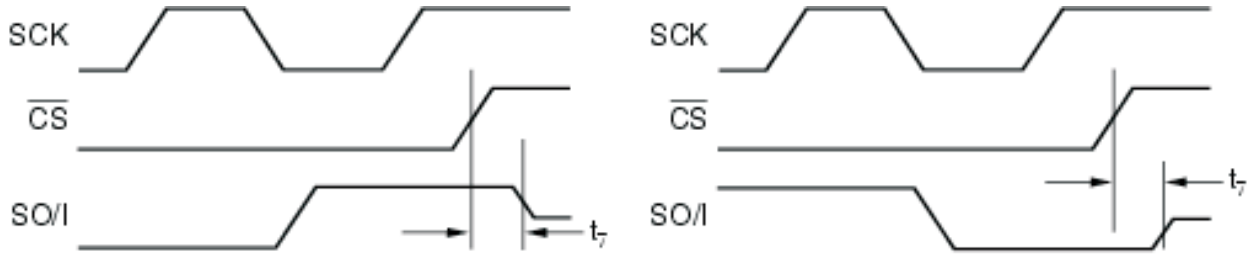


Figure 11. High Impedance Output Timing Diagram

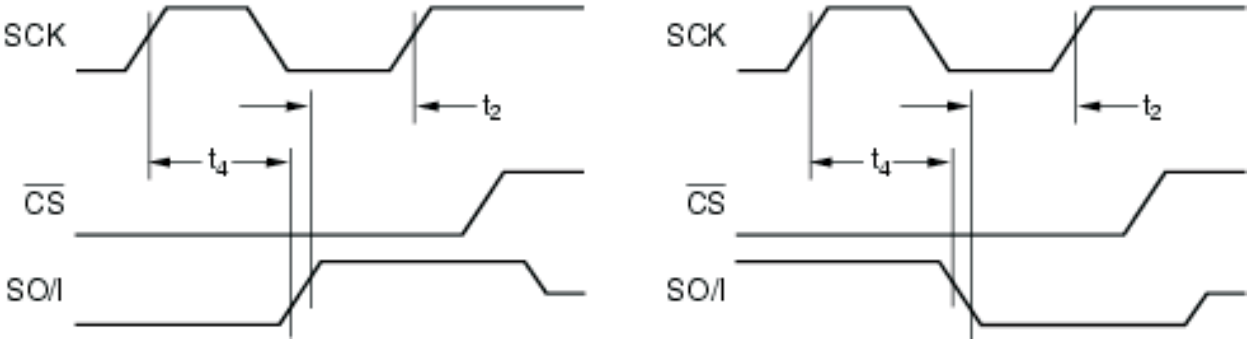


Figure 12. Input Data Timing Diagram

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP122AMDBVTEP	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	122E	Samples
V62/09607-01XE	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	122E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

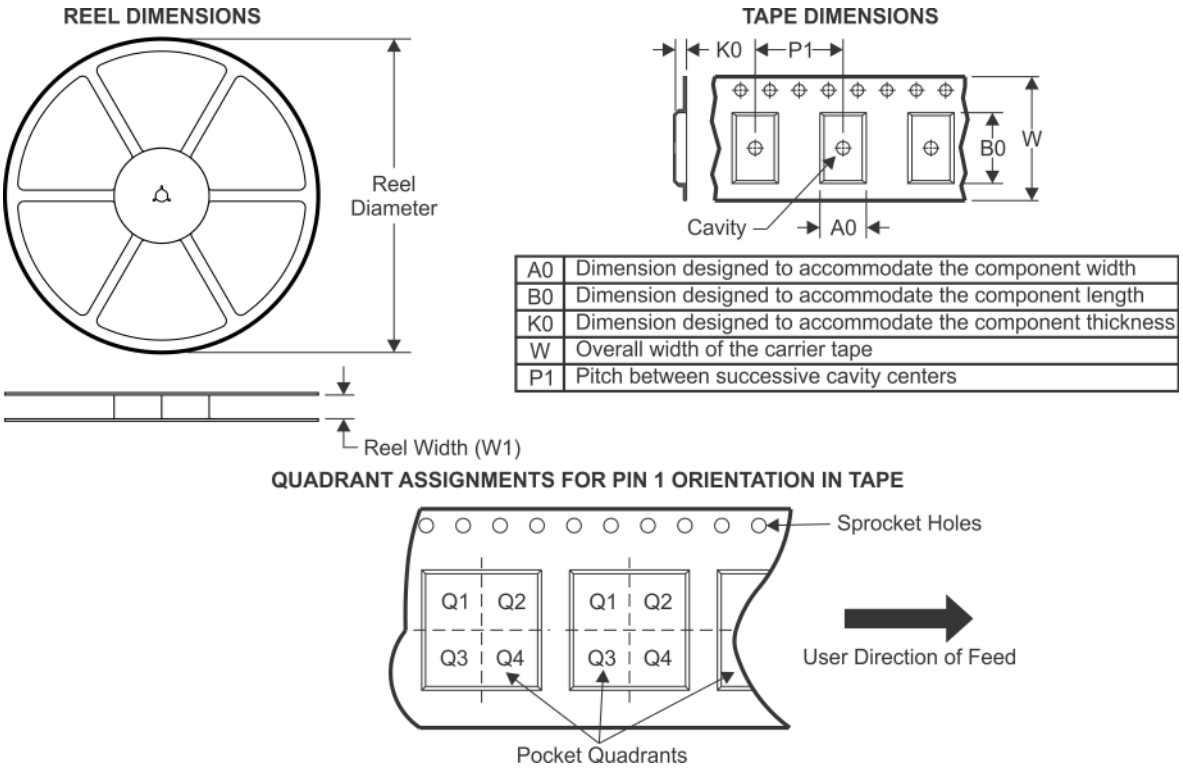
OTHER QUALIFIED VERSIONS OF TMP122-EP :

- Catalog: TMP122

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

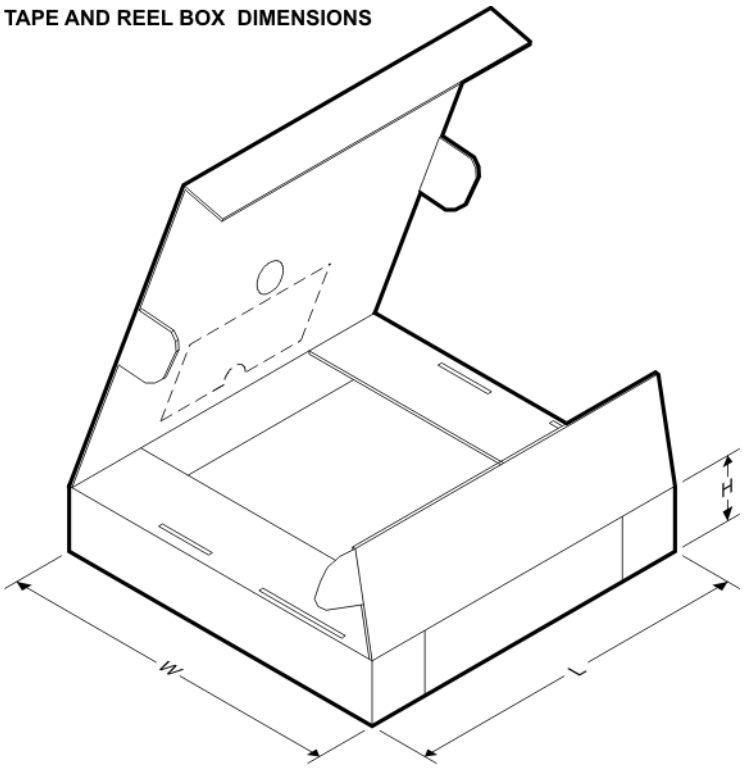


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP122AMDBVTEP	SOT-23	DBV	6	250	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

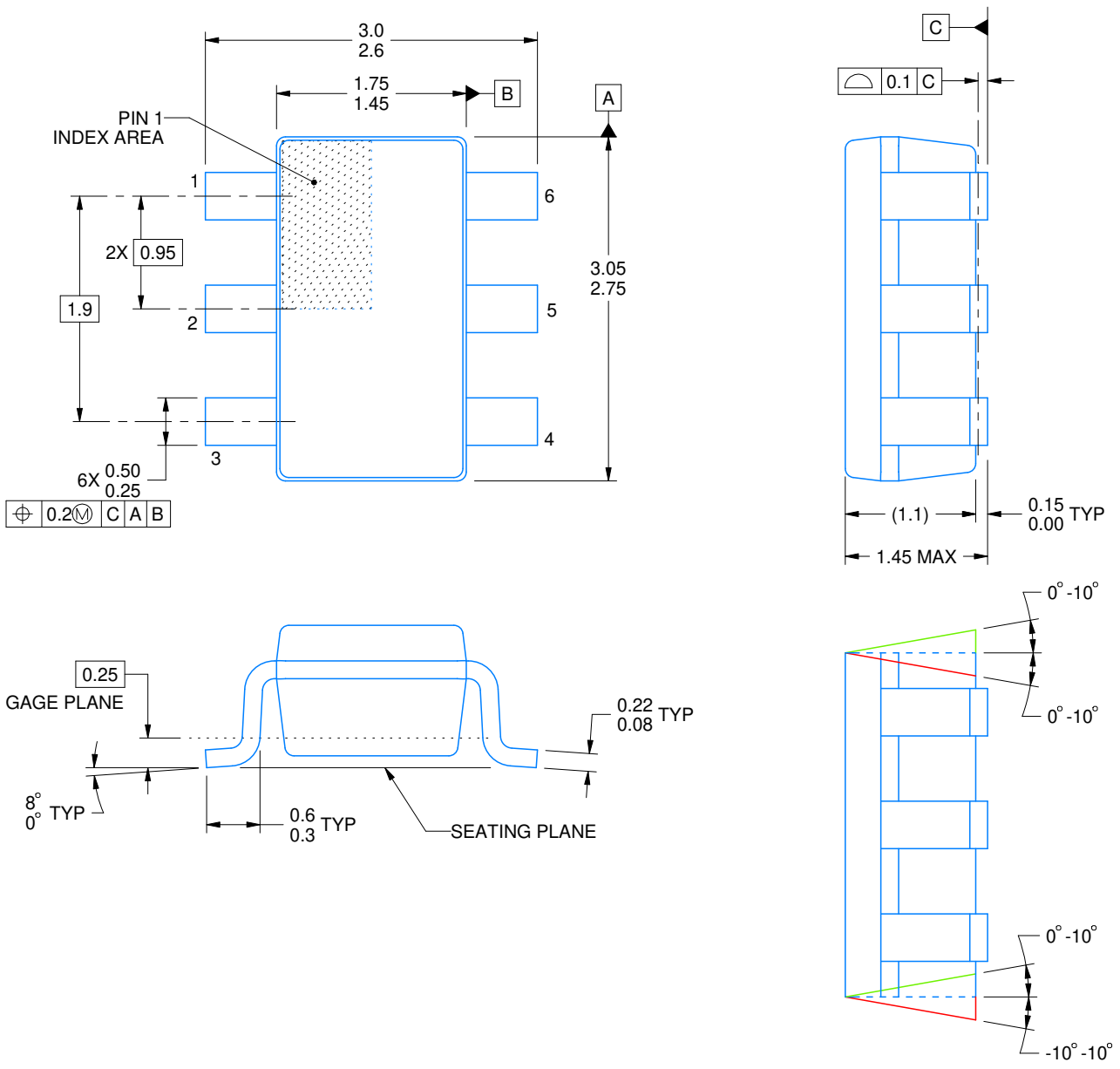
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP122AMDBVTEP	SOT-23	DBV	6	250	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

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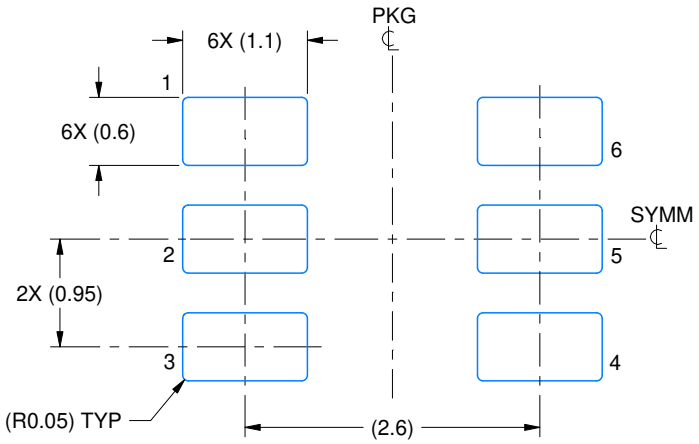
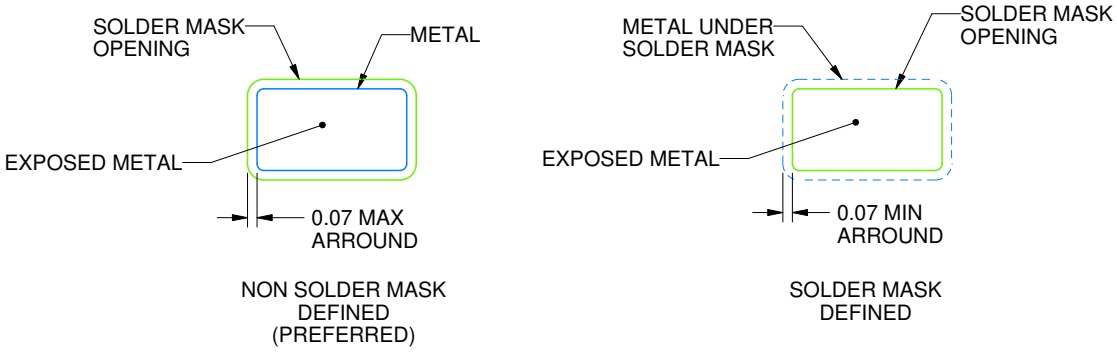
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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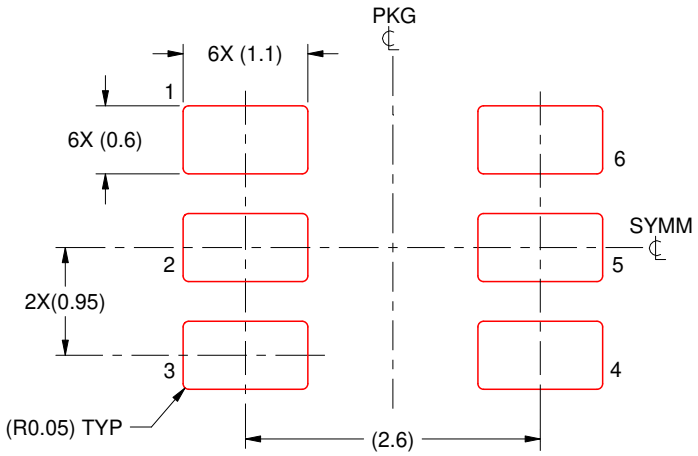
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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