MICREL

FEATURES

- 2:1 PECL/ECL multiplexer
- Guaranteed AC-performance over temperature/ voltage
  - >3GHz f_{MAX} (toggle)
  - <200ps rise/fall time
  - <420ps propagation delay (D-to-Q)
- Low jitter performance
  - <1ps$_{RMS}$ random jitter
  - <15ps$_{PP}$ deterministic jitter
  - <10ps$_{PP}$ total jitter (clock)
- Flexible supply voltage: 3V to 5.5V
- 100k ECL/PECL compatible output
- Wide operating temperature range: –40°C to +85°C
- Available in ultra-small 8-pin MLF™ (2mm x 2mm) package

APPLICATIONS

- SONET
- Gig Ethernet
- Fibre Channel
- Transponders

Precision Edge®

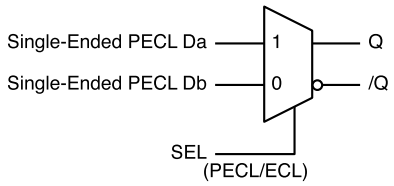
DESCRIPTION

The SY89208V is a 3.3V/5V precision high-speed 2:1 multiplexer. It is functionally equivalent to the SY100EP58V but in an ultra-small 8-lead MLF™ package that features a 70% smaller footprint. The signal-path inputs (Da and Db) are single-ended PECL/ECL compatible, and can accept a signal swing as low as 150mV. All I/O pins are 10k/100k EP ECL/PECL compatible.

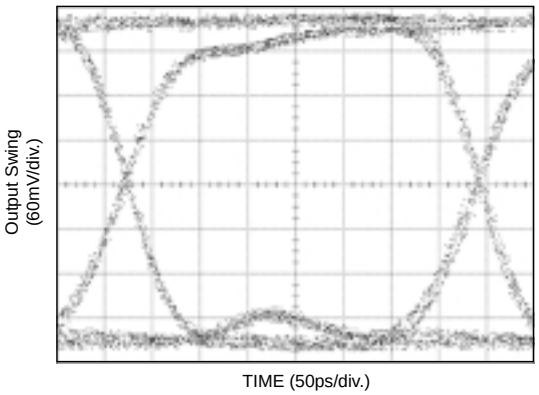
AC-performance is guaranteed over the industrial –40°C to +85°C temperature range and 3.0V to 5.5V supply voltage range. Maximum throughput (f_{MAX}) is guaranteed to be 3GHz with a differential output swing ≥400mV. In addition, these multiplexers are optimized for low-jitter applications. The SY89208V is designed to operate in either ECL/PECL or PECL/LVPECL mode. The SY89208V is internally temperature compensated, thus is 100k EP ECL/PECL compatible—I/O logic levels remain constant over temperature.

The SY89208V is part of Micrel's high-speed, Precision Edge™ timing and distribution family. For applications that require a differential I/O combination, consult the Micrel website at: www.micrel.com, and choose from a comprehensive product line of high-speed, low skew fanout buffers, translators, and clock dividers.

FUNCTIONAL BLOCK DIAGRAM

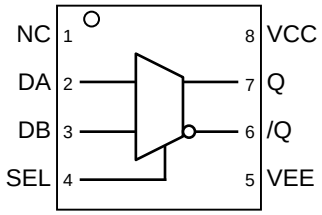


TYPICAL PERFORMANCE



2.7Gbps, 2^{23} – 1PRBS

PACKAGE/ORDERING INFORMATION



8-Pin MLF™
Ultra-Small Outline (2mm x 2mm)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89208VMITR[2]	MLF-8	Industrial	208	Sn-Pb
SY89208VMGTR[2]	MLF-8	Industrial	208 with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.

PIN DESCRIPTION

Pin Number	Pin Name	Type	Pin Function
2, 3	DA, DB	100k ECL Input	Single-ended PECL/ECL Inputs: The signal inputs include internal 75kΩ pull-down resistors. Default condition is LOW when left floating. The input signal should be terminated externally.
4	SEL	100k ECL Input	Single-ended PECL/ECL Input: PECL/ECL compatible 2:1 mux select. See Truth Table. Includes internal 75kΩ pull-down resistor. Default condition is LOW when left floating.
5	VEE Exposed Pad	Negative Power Supply	Negative Power Supply: VEE and Exposed pad must be tied to most negative supply. For PECL/LVPECL connect to ground.
6, 7	/Q, Q	100k ECL Output	Differential PECL/LVPECL Output: 100k ECL/ output defaults to LOW if D inputs left open. See *"Output Interface Applications"* section for recommendations on terminations.
8	VCC	Power	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors.
1	NC		Not connected.

MUX SELECT TRUTH TABLE

SEL	DATA OUT (Q, /Q)
L	DB Input Selected
H	DA Input Selected

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC}) ..... –0.5V to + 6.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Input Current
  Source or sink current on D, /D ..... ±50mA
Lead Temperature (soldering, 10 sec.) ..... +220°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings(Note 2)

Supply Voltage ($|V_{CC}–V_{EE}|$) .. LVPECL/LVECL 3.0V to 3.6V
..... PECL/ECL 4.5V to 5.5V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance **Note 3**
MLF™ (θ_{JA})
  Still-Air ..... 93°C/W
  500lfpm ..... 87°C/W
MLF™ (Ψ_{JB}),
  Junction-to-Board ..... 60°C/W

DC ELECTRICAL CHARACTERISTICS(Note 4)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage (PECL) (LVPECL) (ECL) (LVECL)		4.5 3.0 –5.5 –3.6	5.0 — –5.0 –3.3	5.5 3.6 –4.5 –3.0	V V V V
I_{EE}	Supply Current	No load	—	35	50	mA
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH}$	—	—	80	µA
I_{IL}	Input LOW Current All Inputs	$V_{IN} = V_{IL}$	0.5	—	—	µA
C_{IN}	Input Capacitance		—	1.0	—	pF

PECL/ECL (100K) DC ELECTRICAL CHARACTERISTICS(Note 4)

V_{CC} = +3.3V±10% or +5V±10% and V_{EE} = 0V; V_{CC} = 0V and V_{EE} = –3.3V±10% or –5V±10%; T_A = –40°C to +85°C unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	**Note 5**	V_{CC}–1.145	—	V_{CC}–0.895	V
V_{OL}	Output LOW Voltage	**Note 5**	V_{CC}–1.945	—	V_{CC}–1.695	V
V_{IH}	Input HIGH Voltage		V_{CC}–1.225	—	V_{CC}–0.88	V
V_{IL}	Input LOW Voltage		V_{CC}–1.945	—	V_{CC}–1.625	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range	**Note 6**	V_{EE}+2.0	—	V_{CC}	V
V_{BB}	Bias Voltage		V_{CC}–1.525	V_{CC}–1.425	V_{CC}–1.325	V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V±10% or +5V±10% and V_{EE} = 0V; V_{CC} = 0V and V_{EE} = –3.3V±10% or –5V±10%; T_A = –40°C to +85°C unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Max. Toggle Frequency	**Note 7**	3	—	—	GHz
t_{pd}	Propagation Delay (Differential) SEL to Q, /Q; D to Q, /Q		170	230	420	ps
t_{SKEW}	Part-to-Part Skew	**Note 8**	—	—	200	ps
t_{JITTER}	Cycle-to-Cycle Jitter (rms)	**Note 9**	—	—	1	ps_{RMS}
	Random Jitter	**Note 10**	—	—	1	ps_{RMS}
	Deterministic Jitter @1.25Gbps @2.5Gbps	 **Note 11** **Note 10**	 — —	 7 10	 — —	 ps_{PP} ps_{PP}
	Total Jitter	**Note 12**	—	—	10	ps_{PP}
V_{IN}	Differential Input Voltage Range		150	800	1200	mV
t_r, t_f	Output Rise/Fall Time Q, /Q (20% to 80%)		90	140	200	ps

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.

Note 4. The device is guaranteed to meet the DC specifications, shown in the table above, after thermal equilibrium has been established.

Note 5. Output loaded with 50Ω to V_{CC}–2V.

Note 6. V_{IHCMR}(min) varies 1:1 with V_{EE}, (max) varies 1:1 with V_{CC}.

Note 7. Measured with 750mV input signal, 50% duty cycle. Output swing ≥ 400mV. All loading with a 50Ω to V_{CC} –2.0V.

Note 8. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

Note 9. The variation in period between adjacent cycles over a random sample of adjacent cycle pairs. $t_{JITTER\_CC} = t_n - t_n + 1$, where t is the time between rising edges of the output signal.

Note 10. Random jitter is measured with a K28.7 comma detect character pattern, measured at 1.25Gbps and 2.5Gbps.

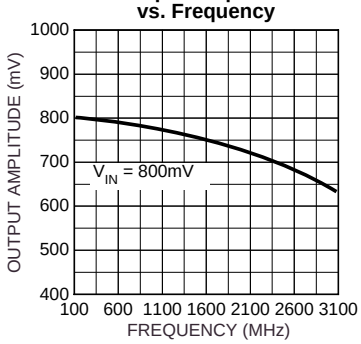
Note 11. Deterministic jitter is measured at 1.25Gbps and 2.5Gbps, with both K28.5 and 2^{23}–1 PRBS pattern.

Note 12. Total Jitter definition with an ideal clock input, no more than 1 output edge in 10^{12} output edges will deviate by more than specified peak-to-peak jitter value.

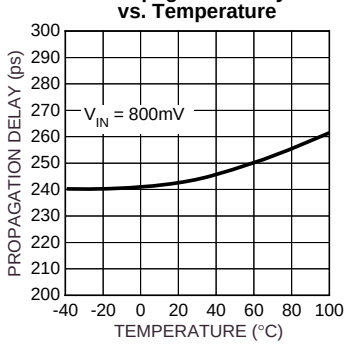
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, V_{EE} = GND, T_A = 25°C, unless otherwise stated.

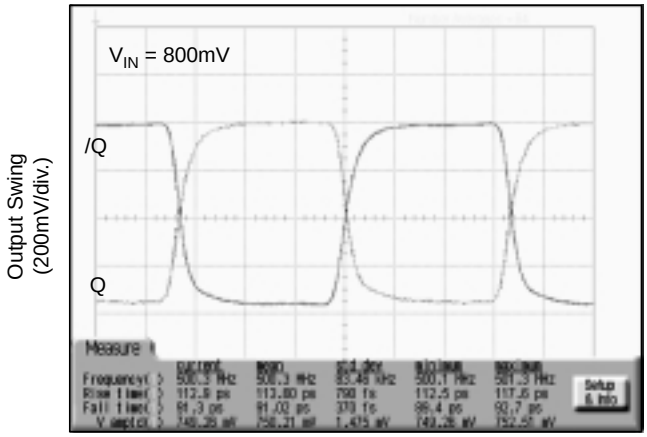
Output Amplitude vs. Frequency



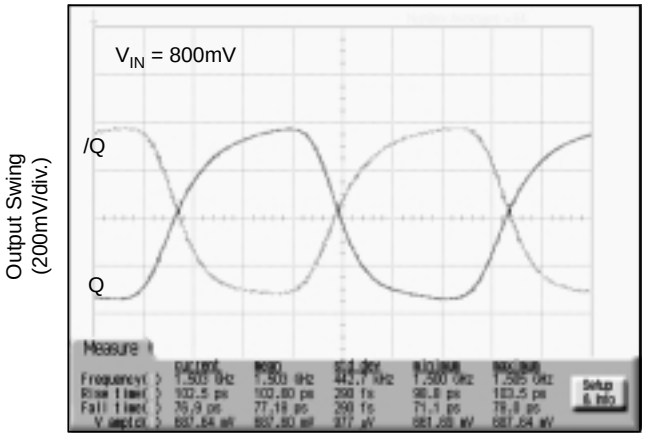
Propagation Delay vs. Temperature



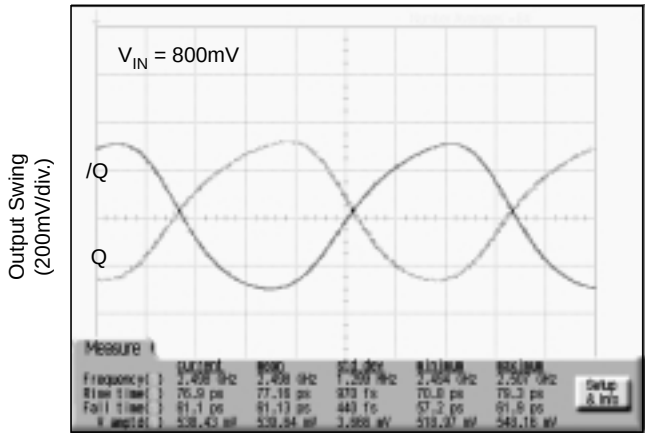
500MHz Output



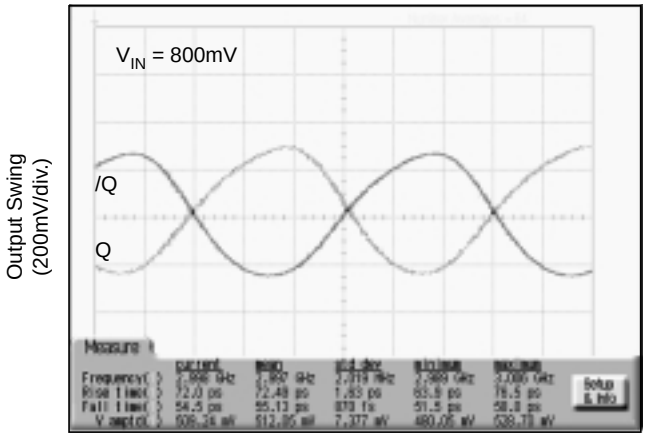
1.5GHz Output



2.5GHz Output



3.0GHz Output



LVPECL OUTPUT INTERFACE APPLICATIONS

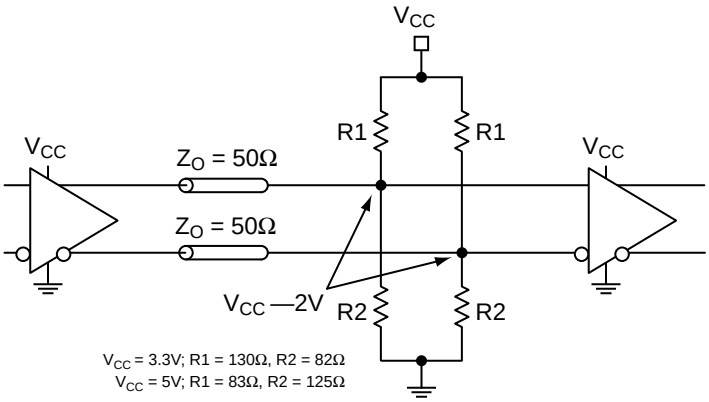


Figure 1a. Parallel Thevenin-Equivalent Termination

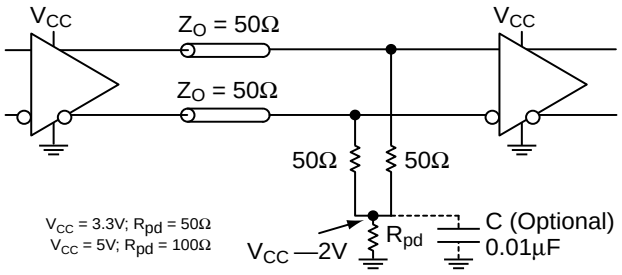


Figure 1b. Three Resistor "Y Termination"

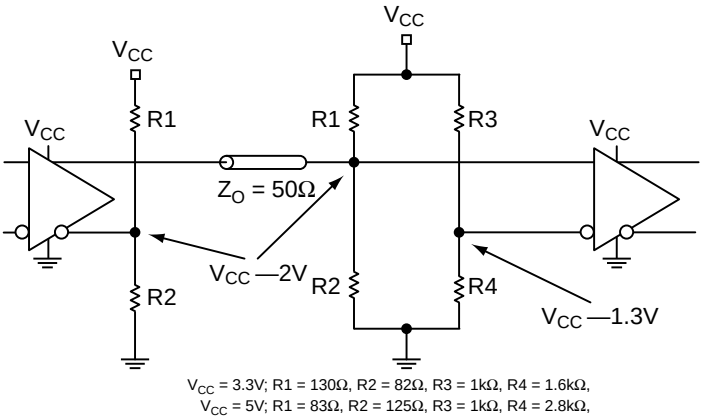
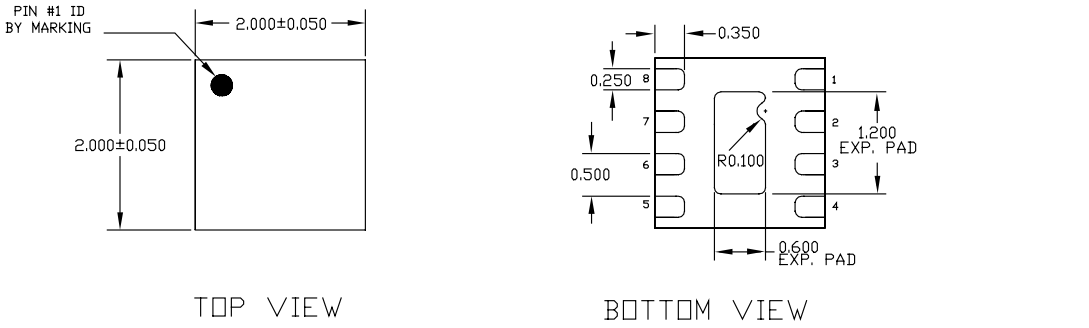
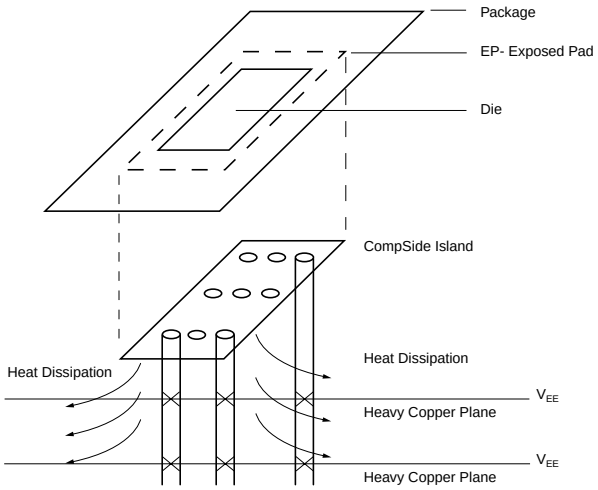


Figure 1c. Terminating Unused I/O

8 LEAD ULTRA-SMALL EPAD-*Micro*LeadFrame™ (MLF-8)



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 8-Pin MLF™ Package

Package Notes:

Note 1. Package meets Level 2 qualification.

Note 2. All parts are dry-packaged before shipment.

Note 3. Exposed pads must be soldered to the most negative supply plane, equivalent to V_{EE} for proper thermal management.

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