

1 Ω Typical On Resistance, ± 5 V, +12 V, +5 V, and +3.3 V, 4:1 Multiplexer

Data Sheet ADG1604

FEATURES

1 Ω typical on resistance
0.2 Ω on resistance flatness
±3.3 V to ±8 V dual-supply operation
3.3 V to 16 V single-supply operation
No V_L supply required
3 V logic-compatible inputs
Rail-to-rail operation
Continuous current per channel
LFCSP: 504 mA
TSSOP: 315 mA

14-lead TSSOP and 16-lead, 4 mm × 4 mm LFCSP

APPLICATIONS

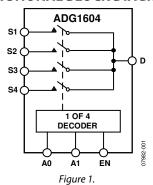
Communication systems
Medical systems
Audio signal routing
Video signal routing
Automatic test equipment
Data acquisition systems
Battery-powered systems
Sample-and-hold systems
Relay replacements

GENERAL DESCRIPTION

The ADG1604 is a complementary metal-oxide semiconductor (CMOS) analog multiplexer and switches one of four inputs to a common output, D, as determined by the 3-bit binary address lines, A0, A1, and EN. Logic 0 on the EN pin disables the device. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

The ultralow on resistance of these switches make them ideal solutions for data acquisition and gain switching applications where low on resistance and distortion is critical. The on resistance profile is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching audio signals.

FUNCTIONAL BLOCK DIAGRAM



The CMOS construction ensures ultralow power dissipation, making the devices ideally suited for portable and battery-powered instruments.

PRODUCT HIGHLIGHTS

- 1. 1.6Ω maximum on resistance over temperature.
- 2. Minimum distortion: THD + N = 0.007%.
- 3. 3 V logic-compatible digital inputs: $V_{INH} = 2.0 \text{ V}$, $V_{INL} = 0.8 \text{ V}$.
- 4. No V_L logic power supply required.
- 5. Ultralow power dissipation: <16 nW.
- 6. 14-lead TSSOP and 16-lead, $4 \text{ mm} \times 4 \text{ mm}$ LFCSP.

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REVISION HISTORY
3/16—Rev. A to Rev. B
Changed CP-16-13 to CP-16-26Throughout
Changes to Figure 2, Figure 3, and Table 7
Updated Outline Dimensions
Changes to Ordering Guide
9/09—Rev. 0 to Rev. A
Changes to On Resistance (R _{ON}) Parameter, On Resistance
Match Between Channels (ARON) Parameter, and On Resistance

1/09—Revision 0: Initial Version

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SPECIFICATIONS

±5 V DUAL SUPPLY

 V_{DD} = +5 V \pm 10%, V_{SS} = -5 V \pm 10%, GND = 0 V, unless otherwise noted.

Table 1.

1.2	Parameter	25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
On Resistance (R _{PM}) 1 1.2 1.4 1.6 Ω rmax V ₅ = ±4.5 V, k ₅ = −10 mA; see Figure 2 v ₅ = ±4.5 V, v ₅ = −10 mA On Resistance Flatness (R _{FLATICNI}) 0.08 0.09 0.1 Ω rmax V ₅ = ±4.5 V, k ₅ = −10 mA LEAKAGE CURRENTS 0.2 0.29 0.34 Ω rmax V ₅ = ±4.5 V, k ₅ = −10 mA Source Off Leakage, l ₅ (Off) ±0.1 nA typ nA typ V ₅ = ±4.5 V, V ₅ = ∓4.5 V; see Figure 2 Channel On Leakage, l ₅ (Off) ±0.1 nA typ nA typ V ₅ = ±4.5 V; v ₅ = ∓4.5 V; see Figure 24 Channel On Leakage, l ₅ (b (On) ±0.2 ±1 ±8 nA typ V ₅ = ±4.5 V; v ₅ = ∓4.5 V; see Figure 24 DIGITAL INPUTS 10.4 ±2 ±16 nA max V ₇ = ±4.5 V; see Figure 24 Digital Input Capacitance, V ₅ (ML Input Low Voltage, V ₁₀) 10.4 ±2 ±16 nA typ V ₇ = V ₂₀₀ or V ₂₀ DYNAMIC CHARACTERISTICS¹ 150 ns typ ns typ R ₆ 300 Ω, C ₆ = 35 pF Torr (EN) 186 ns typ ns typ	ANALOG SWITCH					
On Resistance (Row)	Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance Match Between Channels (ΔRou) 1.2 1.4 1.6 Ω max Ot typ V ₅₀ = ±4.5 V, V ₅₀ = −10 mA On Resistance Flatness (R _{FLATION}) 0.2 0.29 0.34 Ω typ V ₅₀ = ±4.5 V, V ₅₀ = −10 mA LEAKAGE CURRENTS V ₀₀ = ±4.5 V, V ₅₀ = −1.0 mA Ω max V ₅₀ = ±4.5 V, V ₅₀ = −1.5 V Source Off Leakage, I ₅ (Off) ±0.1 nA typ nA typ V ₅ = ±4.5 V, V ₅₀ = −4.5 V; see Figure Drain Off Leakage, I ₅ (Off) ±0.1 nA typ nA max N ₅ = ±4.5 V, V ₅₀ = −4.5 V; see Figure Channel On Leakage, I ₅ (Off) ±0.1 nA max N ₅ = ±4.5 V, V ₅₀ = −4.5 V; see Figure Channel On Leakage, I ₅ (Off) ±0.1 nA max N ₅ = ±4.5 V, V ₅₀ = −4.5 V; see Figure DIGITAL INPUTS 1.0 nA max N ₅ = ±4.5 V, V ₅₀ = ±4.5 V; see Figure V ₅ = ±4.5 V; V ₅₀ = ±4.5 V; see Figure DIGITAL INPUTS 1.0 0.8 V max V ₅ = ±4.5 V; V ₅₀		1			Ωtyp	$V_S = \pm 4.5 \text{ V}, I_S = -10 \text{ mA}$; see Figure 22
On Resistance Match Between Channels (ΔR _{CN}) On Resistance Flatness (R _{ELATICON}) I		1.2	1.4	1.6		$V_{DD} = \pm 4.5 \text{ V}, V_{SS} = \pm 4.5 \text{ V}$
On Resistance Flatness (Relations) 0.2 0.2 0.2 0.29 0.34 Ω typ Vs = ±4.5 V, Is = −10 mA Ct typ Vs = ±4.5 V, Is = −10 mA LEAKAGE CURRENTS Source Off Leakage, Is (Off) ±0.1 ±0.2 ±1 ±8 nA max Drain Off Leakage, Is (Off) ±0.1 ±0.2 ±2 ±16 nA max Channel On Leakage, Is, Is (On) ±0.2 Channel On Leakage, Is, Is (On) ±0.4 ±0.4 ±2 ±16 nA max DiGITAL INPUTS Input High Voltage, V _{INI} Input Low Voltage, V _{INI} Input Low Voltage, V _{INI} Input Current, I _{INI} or I _{INI} Digital Input Capacitance, C _{IN} 8 DYNAMIC CHARACTERISTICS¹ Transition Time, t _{TRANSHION} 150 278 336 376 ns max Vs = 2.5 V, Vse = 7.5 V, Vse = −5.5 V Ns = ±4.5 V, Vse = ₹4.5 V; see Figure 24 Ns = Vs = ±4.5 V; see Figure 24 Ns = Vs = ±4.5 V; see Figure 24 Ns = Vs = Vs = ±4.5 V; see Figure 24 Ns = Vs = Vs = ±4.5 V; see Figure 24 Ns = Vs = Vs = ±4.5 V; see Figure 24 Ns = Vs = Vs = ±4.5 V; see Figure 24 Ns = Vs = Vs = ±4.5 V; see Figure 24 Ns = Vs = Vs = ±4.5 V; see Figure 24 Ns = Vs = Vs = ±4.5 V; see Figure 24 Ns = Vs = Vs = ±4.5 V; see Figure 24 Ns = Vs = Vs = ±4.5 V; see Figure 24 Ns = Vs = Vs = ±4.5 V; see Figure 24 Ns = Vs = Vs = ±4.5 V; see Figure 24 Ns = Vs = Vs = ±4.5 V; see Figure 24 Ns = Vs = Vs = ±4.5 V; see Figure 24 Ns = Vs = Vs = ±4.5 V; see Figure 24 Ns = Vs = Vs = ±4.5 V; see Figure 24 Ns = Vs = Vs = ±4.5 V; see Figure 24 Ns = Vs = Vs = ±4.5 V; see Figure 24 Ns = Vs = ±4.5 V; see Figure 24 Ns = Vs = ±4.5 V; see Figure 24 Ns = Vs = ±4.5 V; see Figure 24 Ns = Vs = ±4.5 V; see Figure 24 Ns = Vs = ±4.5 V; see Figure 25 Ns = Vs = ±4.5 V; see Figure 25 Ns = Vs = ±4.5 V; see Figure 26 Ns = Vs = ±4.5 V; see Figure 26 Ns = Vs = ±4.5 V; see Figure 26 Ns = Vs = ±4.5 V; see Figure 27 Ns = Vs = ±4.5 V; see Figure 26 Ns = Vs = ±4.5 V; see Figure 26 Ns = Vs = ±4.5 V; see Figure 26 Ns = Vs = ±4.5 V; see Figure 26 Ns = Vs = ±4.5 V; see Figure 26 Ns = Vs = ±4.5 V; see Figure 27 Ns = Vs = ±4.5 V; see Figure 28 Ns = Vs = ±4.5 V; see Figure 26 Ns = Vs = ±4.5 V; see Figure 26 Ns = Vs = ±4.5 V; se	On Resistance Match Between Channels (ΔR _{ON})				Ωtyp	-
On Resistance Flatness (R _{FLATIONO}) 0.2 o.25 o.29 o.34 one Ω typ Ω max Vs = ±4.5 V, ks = −10 mA LEAKAGE CURRENTS ±0.1	•	0.08	0.09	0.1		
LEAKAGE CURRENTS Source Off Leakage, Is (Off) ±0.1 ±0.2 ±1 ±8 nA max nA typ Vs = ±4.5 V, Vo = ∓4.5 V; see Figure 1.0.2 ±0.1 ±0.2 ±1 1.0.3 nA typ Vs = ±4.5 V, Vo = ∓4.5 V; see Figure 1.0.2 thannel On Leakage, Io, Is (On) DIGITAL INPUTS Input High Voltage, Vnns Input Low Voltage, Vnns Input Current, Insu or Insu Digital Input Capacitance, Cn Digital Input Capacitance, Cn Transition Time, transsmon 150 278 336 376 ns max Vs = 2.5 V; see Figure 29 ton (EN) 116 107 116 108 117 109 116 109 116 109 117 109 1186 109 1186 109 119 119 110 110 110 110 1110 1110	On Resistance Flatness (R _{FLAT(ON)})	0.2			Ωtyp	$V_S = \pm 4.5 \text{ V, } I_S = -10 \text{ mA}$
Source Off Leakage, Is (Off)	, <i>"</i>		0.29	0.34		
Source Off Leakage, Is (Off)	LEAKAGE CURRENTS					$V_{DD} = +5.5 \text{ V}, V_{SS} = -5.5 \text{ V}$
Drain Off Leakage, Io (Off)		±0.1			nA tvp	
Drain Off Leakage, Io (Off)	g-,,		±1	±8		
Channel On Leakage, Io, Is (On) ±0.2 ±16 nA max nA typ nA typ nA max nA typ nA max nA typ nA max nA typ nA max nA max nA typ nInput High Voltage, Visit Input High Voltage, Visit Input Low Voltage, Visit Input Low Voltage, Visit Input Current, Isit Or Isit Input Current, Isit Or Isit Input Current, Isit Input Current, Isit Input Capacitance, Civit Input Capacitanc	Drain Off Leakage, In (Off)					$V_S = \pm 4.5 \text{ V}$. $V_D = \pm 4.5 \text{ V}$: see Figure 23
Channel On Leakage, I _o , I _o (On)	2.a 2 20aa.g.c, 15 (2,		+2	+16		13
±0.4 ±2 ±16	Channel On Leakage, Ip. Is (On)		_ _			$V_S = V_D = +4.5 \text{ V: see Figure 24}$
DIGITAL INPUTS Input High Voltage, V _{INH}	e.ia.ie. e.i _eailage, ie, ie (e.i.,		±2	±16		
Input High Voltage, V _{INH}	DIGITAL INPUTS					
Input Low Voltage, V _{INL} 0.005				2.0	V min	
Input Current, I _{NL} or I _{NH} 0.005						
Digital Input Capacitance, C _{IN} 8		0.005		0.0		$V_{IN} = V_{CND} \text{ or } V_{DD}$
Digital Input Capacitance, C _{IIN} S	input current, fine or fine	0.003		+0.1		VIIN VGIND OF VDD
DYNAMIC CHARACTERISTICS¹ 150 ns typ R _L = 300 Ω, C _L = 35 pF Transition Time, t _{TRANSITION} 150 ns max V _S = 2.5 V; see Figure 29 to _N (EN) 116 ns typ R _L = 300 Ω, C _L = 35 pF 146 166 177 ns max V _S = 2.5 V; see Figure 29 to _{FF} (EN) 146 166 177 ns max V _S = 2.5 V; see Figure 31 ns typ R _L = 300 Ω, C _L = 35 pF ns typ R _L = 300 Ω, C _L = 35 pF 234 277 310 ns max V _S = 2.5 V; see Figure 31 ns typ R _L = 300 Ω, C _L = 35 pF ns typ R _L = 300 Ω, C _L = 35 pF 234 277 310 ns max V _S = 2.5 V; see Figure 31 ns typ R _L = 300 Ω, C _L = 35 pF ns typ R _L = 300 Ω, C _L = 35 pF Charge Injection 140 pC typ V _S = 0 V, R _S = 0 Ω, C _L = 1 nF; see Figure 20 Off Isolation 70 dB typ R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 25 Channel-to-Channel Crosstalk 70 dB typ R _L = 50 Ω, C _L = 5 pF, f = 20 Hz to 20 kr see Figure 25	Digital Input Capacitance, C _{IN}	8		20.1	·	
Transition Time, trransition 150 ns typ R _L = 300 Ω, C _L = 35 pF ton (EN) 116 ns typ R _L = 300 Ω, C _L = 35 pF ns typ R _L = 300 Ω, C _L = 35 pF R _L = 300 Ω, C _L = 35 pF ns typ R _L = 300 Ω, C _L = 35 pF R _L = 300 Ω, C _L = 35 pF ns max V _S = 2.5 V; see Figure 31 ns typ R _L = 300 Ω, C _L = 35 pF ns max V _S = 2.5 V; see Figure 31 ns typ R _L = 300 Ω, C _L = 35 pF ns max V _S = 2.5 V; see Figure 31 ns typ R _L = 300 Ω, C _L = 35 pF ns max V _S = 2.5 V; see Figure 31 ns typ R _L = 300 Ω, C _L = 35 pF ns max V _S = 2.5 V; see Figure 31 ns typ R _L = 300 Ω, C _L = 35 pF ns max V _S = 2.5 V; see Figure 31 ns typ R _L = 300 Ω, C _L = 35 pF ns max V _S = 2.5 V; see Figure 31 ns typ R _L = 300 Ω, C _L = 35 pF ns typ R _L = 300 Ω, C _L = 35 pF ns typ R _L = 300 Ω, C _L = 35 pF ns typ R _L = 300 Ω, C _L = 35 pF ns typ R _L = 50 Ω, C _L = 5 pF; f = 1 MHz; see Figure 26 Charge Injection R _L = 50 Ω, C _L = 5 pF; f = 1 MHz; see Figure 25 N _L = 50 Ω, C _L = 5 pF; see Figure 26					p. 0)p	
ton (EN) 278 336 376 ns max V ₅ = 2.5 V; see Figure 29 ton (EN) 116 ns typ R _L = 300 Ω, C _L = 35 pF 146 166 177 ns max V ₅ = 2.5 V; see Figure 31 toff (EN) 186 ns typ R _L = 300 Ω, C _L = 35 pF Break-Before-Make Time Delay, t _D 50 ns max V ₅ = 2.5 V; see Figure 31 Charge Injection 140 pC typ V ₅ = 0Ω, C _L = 35 pF Charge Injection 140 pC typ V ₅ = 0Ω, C _L = 1 nF; see Figure 30 Off Isolation 70 dB typ R _L = 50 Ω, C _L = 1 nF; see Figure 30 Channel-to-Channel Crosstalk 70 dB typ R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 25 Channel-to-Channel Crosstalk 70 dB typ R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 26 Total Harmonic Distortion + Noise (THD + N) 0.007 % typ R _L = 50 Ω, C _L = 5 pF; see Figure 26 C ₅ (Off) 63 pF typ V ₅ = 0 Ω, C _L = 5 pF; see Figure 26 C ₅ (Off) 270 pF typ V ₅ = 0 Ω, f = 1 MHz C ₀ (C ₀ (F) 270 pF typ V ₅ = 0 Ω, f = 1 MHz		150			ns typ	R ₁ = 300 O C ₁ = 35 pF
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Transition Time, transition		336	376		•
$t_{OFF} (EN) \\ 186 \\ 234 \\ 277 \\ 310 \\ ns \ max \\ Ns \ typ \\ R_L = 300 \ \Omega, \ C_L = 35 \ pF \\ Ns \ max \\ Ns \ typ \\ R_L = 300 \ \Omega, \ C_L = 35 \ pF \\ Ns \ max \\ Ns \ typ \\ R_L = 300 \ \Omega, \ C_L = 35 \ pF \\ Ns \ min \\ Ns \ typ \\ R_L = 300 \ \Omega, \ C_L = 35 \ pF \\ Ns \ min \\ Ns \ typ \\ Ns = 2.5 \ V; \ see \ Figure 31 \\ Ns \ typ \\ Ns = 2.5 \ V; \ see \ Figure 30 \\ Ns \ typ \\ Ns = 2.5 \ V; \ see \ Figure 30 \\ Ns \ typ \\ typ \\ Ns \ typ \\ Ns$	ton (FN)		330	370		
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	CON (LIV)		166	177		·
Break-Before-Make Time Delay, t_D Break-Before-Make Time Delay, t_D Charge Injection Off Isolation Channel-to-Channel Crosstalk Total Harmonic Distortion + Noise (THD + N) Case (Off) Cas	torr (FN)		100	177		_
Break-Before-Make Time Delay, t_D 28.5 ns min $V_{S1} = V_{S2} = 2.5 \text{ V}$; see Figure 30 Charge Injection Off Isolation 70 $D_{S1} = V_{S2} = 2.5 \text{ V}$; see Figure 30 $D_{S2} = 0.0 \text{ N}$, $C_{S1} = 0.0 \text{ N}$, $C_{S2} = 0.0 \text{ N}$, $C_{S3} = 0.0 \text{ N}$, $C_{S4} = 0.0 $	COFF (LIV)		277	310		•
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Break-Refore-Make Time Delay to		277	310		_
Charge Injection 140 pC typ $V_S = 0 V$, $R_S = 0 \Omega$, $C_L = 1$ nF; see Figur Off Isolation 70 dB typ $R_L = 50 \Omega$, $C_L = 5$ pF, $f = 1$ MHz; see Figure 25 Channel-to-Channel Crosstalk 70 dB typ $R_L = 50 \Omega$, $C_L = 5$ pF, $f = 1$ MHz; see Figure 27 Total Harmonic Distortion + Noise (THD + N) 0.007 % typ $R_L = 110 \Omega$, $5 V$ p-p, $f = 20$ Hz to $20 K$ see Figure 28 -3 dB Bandwidth 15 MHz typ $R_L = 50 \Omega$, $C_L = 5$ pF; see Figure 26 $C_S (Off)$ 63 pF typ $V_S = 0 V$, $f = 1$ MHz $C_D (Off)$ 270 pF typ $V_S = 0 V$, $f = 1$ MHz $C_D (Off)$ 270 pF typ $V_S = 0 V$, $f = 1$ MHz POWER REQUIREMENTS I_{DD} 0.001 μA typ Digital inputs $= 0 V$ or V_{DD}	break before make time belay, to	30		28.5		•
Off Isolation 70 dB typ $R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; see Figure 25 Channel-to-Channel Crosstalk 70 dB typ $R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; see Figure 27 Total Harmonic Distortion + Noise (THD + N) 0.007 % typ $R_L = 110 \Omega$, 5 V p-p , $f = 20 \text{ Hz to } 20 \text{ kHz to } 20 \text{ kHz typ}$ $R_L = 50 \Omega$, $C_L = 5 pF$; see Figure 26 $C_S = 63 \Omega$,	Charge Injection	140		20.5		. 3
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	= -					_
Total Harmonic Distortion + Noise (THD + N) 0.007 % typ $R_L = 110 \Omega$, 5 V p-p, f = 20 Hz to 20 kF see Figure 28 -3 dB Bandwidth 15 MHz typ $R_L = 50 \Omega$, $C_L = 5$ pF; see Figure 26 C_S (Off) 63 pF typ $V_S = 0$ V, f = 1 MHz C_D (Off) 270 pF typ $V_S = 0$ V, f = 1 MHz C_D (On) 360 pF typ $V_S = 0$ V, f = 1 MHz						see Figure 25
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Channel-to-Channel Crosstalk	70			dB typ	<u> </u>
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	Total Harmonic Distortion + Noise (THD + N)	0.007			% typ	R_L = 110 Ω, 5 V p-p, f = 20 Hz to 20 kHz; see Figure 28
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	–3 dB Bandwidth	15			MHz typ	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	C _s (Off)	63			1	
$ \begin{array}{c cccc} C_D, C_S (On) & 360 & pF typ & V_S = 0 V, f = 1 MHz \\ \hline POWER REQUIREMENTS & & & V_{DD} = +5.5 V, V_{SS} = -5.5 V \\ I_{DD} & 0.001 & \mu A typ & Digital inputs = 0 V or V_{DD} \\ \hline \end{array} $	C _D (Off)	270				$V_S = 0 V, f = 1 MHz$
POWER REQUIREMENTS $I_{DD} \hspace{1cm} V_{DD} = +5.5 \text{ V, } V_{SS} = -5.5 \text{ V} \\ Digital inputs = 0 \text{ V or } V_{DD}$		360				
I_{DD} 0.001 $\mu A typ$ Digital inputs = 0 V or V_{DD}	POWER REQUIREMENTS					$V_{DD} = +5.5 \text{ V}, V_{SS} = -5.5 \text{ V}$
10 10 may		0.001		1.0		
V_{DD}/V_{SS} $\pm 3.3/\pm 8$ $V min/max$	V //			1.0	μA max	

 $^{^{\}rm 1}$ Guaranteed by design, not subject to production test.

12 V SINGLE SUPPLY

 V_{DD} = 12 V \pm 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH	23 C	103 C	1123 C	Onic	rest conditions, comments
Analog Signal Range			0 V to V _{DD}	V	
On Resistance (RoN)	0.95		0 4 10 400	Ωtyp	$V_s = 0 \text{ V to } 10 \text{ V}, I_s = -10 \text{ mA}; \text{ see Figure } 22$
on nesistance (non)	1.1	1.25	1.45	Ω max	$V_{DD} = 10.8 \text{ V}, V_{SS} = 0 \text{ V}$
On Resistance Match Between Channels (ΔR _{ON})	0.03	5		Ωtyp	$V_S = 10 \text{ V}, I_S = -10 \text{ mA}$
Chinesistance materials and manifest (21.60)	0.06	0.07	0.08	Ω max	
On Resistance Flatness (R _{FLAT(ON)})	0.2			Ωtyp	$V_s = 0 \text{ V to } 10 \text{ V, } I_s = -10 \text{ mA}$
()30(0.0)	0.23	0.27	0.32	Ω max	
LEAKAGE CURRENTS					$V_{DD} = 13.2 \text{ V}, V_{SS} = 0 \text{ V}$
Source Off Leakage, Is (Off)	±0.1			nA typ	$V_S = 1 \text{ V}/10 \text{ V}, V_D = 10 \text{ V}/1 \text{ V}; \text{ see Figure 23}$
-	±0.2	±1	±8	nA max	
Drain Off Leakage, ID (Off)	±0.1			nA typ	$V_S = 1 \text{ V}/10 \text{ V}, V_D = 10 \text{ V}/1 \text{ V}; \text{ see Figure 23}$
_	±0.2	±2	±16	nA max	_
Channel On Leakage, ID, Is (On)	±0.2			nA typ	$V_S = V_D = 1 \text{ V or } 10 \text{ V}$; see Figure 24
	±0.4	±2	±16	nA max	
DIGITAL INPUTS					
Input High Voltage, V _{INH}			2.0	V min	
Input Low Voltage, V _{INL}			0.8	V max	
Input Current, I _{INL} or I _{INH}	0.001			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C _{IN}	8			pF typ	
DYNAMIC CHARACTERISTICS ¹					
Transition Time, t _{TRANSITION}	100			ns typ	$R_L = 300 \Omega, C_L = 35 pF$
	161	192	220	ns max	$V_s = 8 \text{ V}$; see Figure 29
ton (EN)	80			ns typ	$R_L = 300 \Omega, C_L = 35 pF$
	95	104	111	ns max	$V_S = 8 \text{ V}$; see Figure 31
t _{OFF} (EN)	144			ns typ	$R_L = 300 \Omega, C_L = 35 pF$
	173	205	234	ns max	$V_s = 8 \text{ V}$; see Figure 31
Break-Before-Make Time Delay, t _D	25			ns typ	$R_L = 300 \Omega, C_L = 35 pF$
-			18	ns min	$V_{S1} = V_{S2} = 8 \text{ V}$; see Figure 30
Charge Injection	125			pC typ	$V_s = 6 \text{ V}, R_s = 0 \Omega, C_L = 1 \text{ nF; see Figure 32}$
Off Isolation	70			dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; see Figure 25
Channel-to-Channel Crosstalk	70			dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; see Figure 27
Total Harmonic Distortion + Noise	0.013			% typ	R_L = 110 Ω , 5 V p-p, f = 20 Hz to 20 kHz; see Figure 28
–3 dB Bandwidth	19			MHz typ	$R_L = 50 \Omega$, $C_L = 5 pF$; see Figure 26
C _s (Off)	60			pF typ	$V_S = 6 \text{ V, } f = 1 \text{ MHz}$
C _D (Off)	270			pF typ	$V_S = 6 \text{ V, } f = 1 \text{ MHz}$
C_D , C_S (On)	350			pF typ	$V_S = 6 V, f = 1 MHz$
POWER REQUIREMENTS					$V_{DD} = 12 V$
I _{DD}	0.001			μA typ	Digital inputs = 0 V or V _{DD}
			1	μA max	
IDD	230			μA typ	Digital inputs = 5 V
			360	μA max	
V_{DD}			3.3/16	V min/max	

 $^{^{\}mbox{\tiny 1}}$ Guaranteed by design, not subject to production test.

5 V SINGLE SUPPLY

 V_{DD} = 5 V \pm 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 3.

	−40°C to	−40°C to		
25°C	+85°C	+125℃	Unit	Test Conditions/Comments
		$0 V \text{ to } V_{DD}$		
			Ωtyp	$V_S = 0 \text{ V to } 4.5 \text{ V, } I_S = -10 \text{ mA; see Figure 22}$
	2.4	2.7	Ω max	$V_{DD} = 4.5 \text{ V}, V_{SS} = 0 \text{ V}$
0.05			Ω typ	$V_S = 0 \text{ V to } 4.5 \text{ V, } I_S = -10 \text{ mA}$
0.09	0.12	0.15	Ω max	
0.4			Ω typ	$V_S = 0 \text{ V to } 4.5 \text{ V, } I_S = -10 \text{ mA}$
0.53	0.55	0.6	Ω max	
				$V_{DD} = 5.5 \text{ V}, V_{SS} = 0 \text{ V}$
±0.05			nA typ	$V_S = 1 \text{ V}/4.5 \text{ V}, V_D = 4.5 \text{ V}/1 \text{ V}; \text{ see Figure 23}$
±0.2	±1	±8	nA max	
±0.05			nA typ	$V_S = 1 \text{ V}/4.5 \text{ V}, V_D = 4.5 \text{ V}/1 \text{ V}; \text{ see Figure 23}$
±0.2	±2	±16	nA max	
±0.1			nA typ	$V_S = V_D = 1 \text{ V or } 4.5 \text{ V; see Figure } 24$
±0.4	±2	±16	nA max	-
		2.0	V min	
		0.8	V max	
0.001			μΑ typ	$V_{IN} = V_{GND}$ or V_{DD}
		±0.1		
8				
			1 31	
175			ns typ	$R_L = 300 \Omega, C_L = 35 pF$
	337	380		$V_S = 2.5 \text{ V}$; see Figure 29
				$R_L = 300 \Omega$, $C_L = 35 pF$
	194	212		$V_S = 2.5 \text{ V}$; see Figure 31
				$R_L = 300 \Omega$, $C_L = 35 pF$
	342	385		$V_S = 2.5 \text{ V}$; see Figure 31
	3 12	303		$R_L = 300 \Omega$, $C_L = 35 pF$
		21		$V_{S1} = V_{S2} = 2.5 \text{ V}$; see Figure 30
70		21		$V_s = 2.5 \text{ V}$, $R_s = 0 \Omega$, $C_L = 1 \text{ nF}$; see Figure 32
				$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 100 kHz$;
70			ab typ	see Figure 25
70			dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 100 kHz$; see Figure 27
0.09			% typ	R _L = 110 Ω, f = 20 Hz to 20 kHz, V _S = 3.5 V p-p; see Figure 28
16			MHz typ	$R_L = 50 \Omega$, $C_L = 5 pF$; see Figure 26
70				$V_S = 2.5 \text{ V, } f = 1 \text{ MHz}$
300				$V_S = 2.5 \text{ V, } f = 1 \text{ MHz}$
400			pF typ	$V_S = 2.5 \text{ V, } f = 1 \text{ MHz}$
			۲۰ ۰٫۲	
				$1 \text{ V}_{DD} = 5.5 \text{ V}$
0.001			uA typ	$V_{DD} = 5.5 \text{ V}$ Digital inputs = 0 V or V_{DD}
0.001		1	μΑ typ μΑ max	$V_{DD} = 5.5 \text{ V}$ Digital inputs = 0 V or V_{DD}
	0.09 0.4 0.53 ±0.05 ±0.2 ±0.1 ±0.4 0.001 8 175 283 135 174 228 288 30 70 70 0.09 16 70 300	1.7 2.15 0.09 0.12 0.4 0.53 0.55 ±0.05 ±0.2 ±1 ±0.05 ±0.2 ±0.1 ±0.4 ±2 0.001 8 175 283 337 135 174 194 228 288 342 30 70 70 70 70 0.09 16 70 300	25°C +85°C +125°C 0 V to V _{DD} 1.7 2.15 2.4 2.7 0.09 0.12 0.15 0.4 0.53 0.55 0.6 ±0.05 ±0.2 ±1 ±8 ±0.05 ±0.2 ±2 ±16 ±0.1 ±0.4 ±2 ±16 2.0 0.8 0.001 ±0.1 8 337 380 380 135 174 194 212 228 288 342 385 30 21 70 70 70 70 0.09 16 70 300 300 16	25°C +85°C +125°C Unit 1.7 Ω typ Ω typ 2.15 2.4 2.7 Ω max 0.05 Ω typ Ω typ 0.09 0.12 0.15 Ω max 0.4 Ω typ Ω typ Ω typ 0.53 0.55 0.6 Ω max ±0.05 πA max nA typ nA max ±0.05 πA typ nA max nA typ ±0.1 πA max nA max ±0.1 μA max nA max ±0.1 μA max pF typ 175 πs typ ns max 135 ns typ ns max 135 ns max ns typ 174 194 212 ns max 30 ns max ns typ

 $^{^{\}mbox{\tiny 1}}$ Guaranteed by design, not subject to production test.

3.3 V SINGLE SUPPLY

 V_{DD} = 3.3 V, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 4.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			$0VtoV_{DD}$	V	
On Resistance (R _{ON})	3.2	3.4	3.6	Ωtyp	$V_S = 0 \text{ V to V}_{DD}$, $I_S = -10 \text{ mA}$, $V_{DD} = 3.3 \text{ V}$, $V_{SS} = 0 \text{ V}$; see Figure 22
On Resistance Match Between Channels (ΔR _{ON})	0.06	0.07	0.08	Ωtyp	$V_{S} = 0 \text{ V to } V_{DD}, I_{S} = -10 \text{ mA}$
On Resistance Flatness (R _{FLAT(ON)})	1.2	1.3	1.4	Ωtyp	$V_S = 0 \text{ V to } V_{DD}, I_S = -10 \text{ mA}$
LEAKAGE CURRENTS					$V_{DD} = 3.6 \text{ V}, V_{SS} = 0 \text{ V}$
Source Off Leakage, Is (Off)	±0.02			nA typ	$V_S = 0.6 \text{ V/3 V}, V_D = 3 \text{ V/0.6 V}; \text{ see Figure 23}$
	±0.25	±1	±8	nA max	_
Drain Off Leakage, ID (Off)	±0.02			nA typ	$V_S = 0.6 \text{ V/3 V}, V_D = 3 \text{ V/0.6 V}; \text{ see Figure 23}$
	±0.25	±2	±16	nA max	
Channel On Leakage, ID, Is (On)	±0.05			nA typ	$V_S = V_D = 0.6 \text{ V or 3 V; see Figure 24}$
-	±0.6	±2	±16	nA max	_
DIGITAL INPUTS					
Input High Voltage, V _{INH}			2.0	V min	
Input Low Voltage, V _{INL}			0.8	V max	
Input Current, I _{INL} or I _{INH}	0.001			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
·			±0.1	μA max	
Digital Input Capacitance, C _{IN}	8			pF typ	
DYNAMIC CHARACTERISTICS ¹					
Transition Time, trransition	280			ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$
	460	526	575	ns max	V _s = 1.5 V; see Figure 29
ton (EN)	227			ns typ	$R_L = 300 \Omega, C_L = 35 pF$
	308	332	346	ns max	V _s = 1.5 V; see Figure 31
t _{OFF} (EN)	357			ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$
	480	549	601	ns max	V _s = 1.5 V; see Figure 31
Break-Before-Make Time Delay, t _D	25			ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$
			20	ns min	$V_{S1} = V_{S2} = 1.5 \text{ V}$; see Figure 30
Charge Injection	60			pC typ	$V_S = 1.5 \text{ V}, R_S = 0 \Omega, C_L = 1 \text{ nF}; \text{ see Figure } 32$
Off Isolation	70			dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 100 kHz$; see Figure 25
Channel-to-Channel Crosstalk	70			dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 100 kHz$; see Figure 27
Total Harmonic Distortion + Noise	0.15			% typ	$R_L = 110 \Omega$, $f = 20 Hz$ to $20 kHz$, $V_S = 2 V p-p$; see Figure 28
–3 dB Bandwidth	15			MHz typ	$R_L = 50 \Omega$, $C_L = 5 pF$; see Figure 26
C _s (Off)	76			pF typ	$V_S = 1.5 \text{ V, } f = 1 \text{ MHz}$
C _D (Off)	316			pF typ	$V_S = 1.5 \text{ V, } f = 1 \text{ MHz}$
C_D , C_S (On)	420			pF typ	$V_S = 1.5 \text{ V, } f = 1 \text{ MHz}$
POWER REQUIREMENTS					$V_{DD} = 3.6 \text{ V}$
IDD	0.001			μA typ	Digital inputs = 0 V or V _{DD}
		1.0	1.0	μA max	- ·
V_{DD}			3.3/16	V min/max	

 $^{^{\}mbox{\tiny 1}}$ Guaranteed by design, not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, S OR D

Table 5.

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, S OR D				
$V_{DD} = +5 \text{ V}, V_{SS} = -5 \text{ V}$				
TSSOP ($\theta_{JA} = 150.4$ °C/W)	315	189	95	mA maximum
LFCSP ($\theta_{JA} = 48.7^{\circ}$ C/W)	504	259	112	mA maximum
$V_{DD} = 12 \text{ V}, V_{SS} = 0 \text{ V}$				
TSSOP ($\theta_{JA} = 150.4$ °C/W)	378	221	112	mA maximum
LFCSP ($\theta_{JA} = 48.7^{\circ}$ C/W)	627	311	126	mA maximum
$V_{DD} = 5 V$, $V_{SS} = 0 V$				
TSSOP ($\theta_{JA} = 150.4$ °C/W)	249	158	91	mA maximum
LFCSP ($\theta_{JA} = 48.7^{\circ}$ C/W)	403	224	105	mA maximum
$V_{DD} = 3.3 \text{ V}, V_{SS} = 0 \text{ V}$				
TSSOP ($\theta_{JA} = 150.4$ °C/W)	256	165	98	mA maximum
LFCSP ($\theta_{JA} = 48.7^{\circ}$ C/W)	410	235	116	mA maximum

ABSOLUTE MAXIMUM RATINGS

 $T_A = 25$ °C, unless otherwise noted.

Table 6.

14010 01	
Parameter	Rating
V _{DD} to V _{SS}	18 V
V _{DD} to GND	−0.3 V to +18 V
V _{ss} to GND	+0.3 V to −18 V
Analog Inputs ¹	V_{SS} – 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs ¹	GND $- 0.3 \text{ V}$ to $\text{V}_{DD} + 0.3 \text{ V}$ or 30 mA, whichever occurs first
Peak Current, S or D	1150 mA (pulsed at 1 ms, 10% duty-cycle maximum)
Continuous Current, S or D ²	Data + 15%
Operating Temperature Range	
Industrial (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
16-Lead TSSOP, 2-Layer Board	150.4°C/W
16-Lead LFCSP, 4-Layer Board	48.7°C/W
Reflow Soldering Peak Temperature, Pb free	260°C

 $^{^{\}rm 1}$ Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

² See Table 5.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

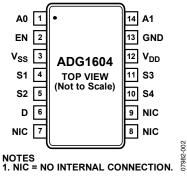


Figure 2. 14-Lead TSSOP Pin Configuration

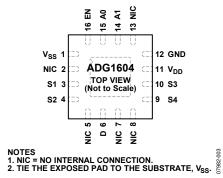


Figure 3. 16-Lead LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin	No.		
14-Lead TSSOP	14-Lead TSSOP 16-Lead LFCSP		Description
1	15	A0	Logic Control Input.
2	16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, the Ax logic inputs determine the on switch.
3	1	V _{SS}	Most Negative Power Supply Potential.
4	3	S1	Source Terminal. This pin can be an input or output.
5	4	S2	Source Terminal. This pin can be an input or output.
6	6	D	Drain Terminal. This pin can be an input or output.
7, 8, 9	2, 5, 7, 8, 13	NIC	No Internal Connection.
10	9	S4	Source Terminal. This pin can be an input or output.
11	10	S3	Source Terminal. This pin can be an input or output.
12	11	V_{DD}	Most Positive Power Supply Potential.
13	12	GND	Ground (0 V) Reference.
14	14	A1	Logic Control Input.
N/A ¹	0	EPAD	Exposed Pad. Tie the exposed pad to the substrate, Vss.

¹ N/A means not applicable.

Table 8. ADG1604 Truth Table

EN	A1	A0	S 1	S2	S3	S4	
0	Х	Χ	Off	Off	Off	Off	
1	0	0	On	Off	Off	Off	
1	0	1	Off	On	Off	Off	
1	1	0	Off	Off	On	Off	
1	1	1	Off	Off	Off	On	

TYPICAL PERFORMANCE CHARACTERISTICS

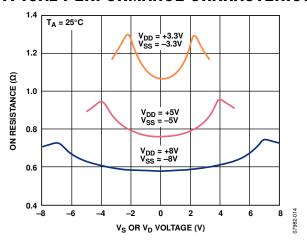


Figure 4. On Resistance as a Function of V_D (V_S) for Dual Supply

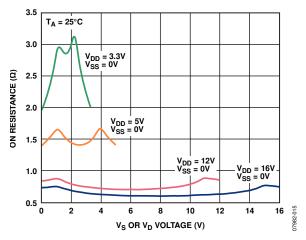


Figure 5. On Resistance as a Function of V_D (V_S) for Single Supply

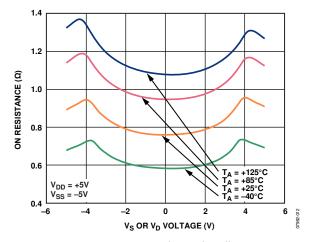


Figure 6. On Resistance as a Function of V_D (V_S) for Different Temperatures, ± 5 V Dual Supply

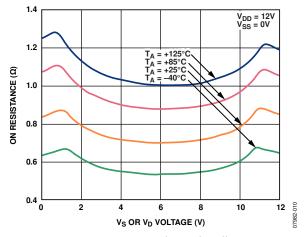


Figure 7. On Resistance as a Function of V_D (V_S) for Different Temperatures, 12 V Single Supply

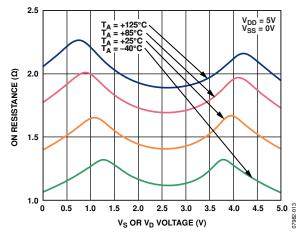


Figure 8. On Resistance as a Function of V_D (V_S) for Different Temperatures, 5 V Single Supply

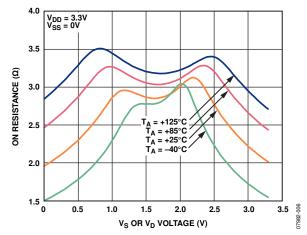


Figure 9. On Resistance as a Function of V_D (V_S) for Different Temperatures, 3.3 V Single Supply

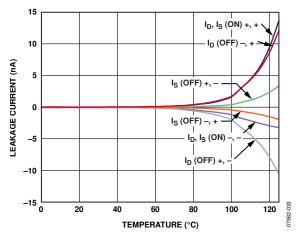


Figure 10. Leakage Currents as a Function of Temperature, ±5 V Dual Supply

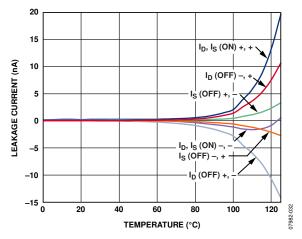


Figure 11. Leakage Currents as a Function of Temperature, 12 V Single Supply

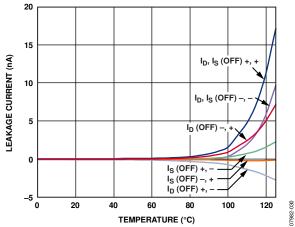


Figure 12. Leakage Currents as a Function of Temperature, 5 V Single Supply

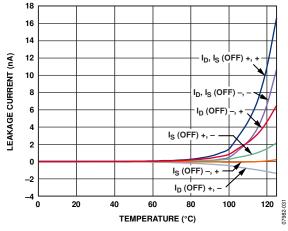


Figure 13. Leakage Currents as a Function of Temperature, 3.3 V Single Supply

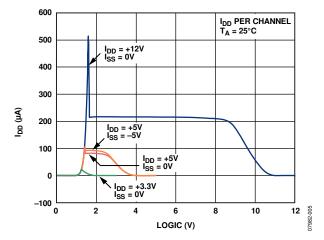


Figure 14. IDD vs. Logic Level

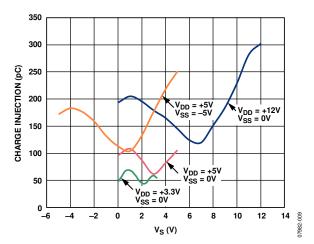


Figure 15. Charge Injection vs. Source Voltage

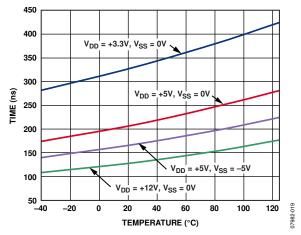


Figure 16. ton/toff Times vs. Temperature

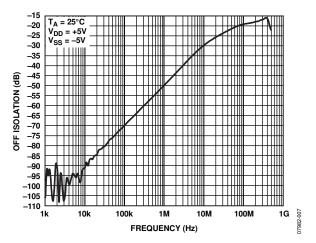


Figure 17. Off Isolation vs. Frequency

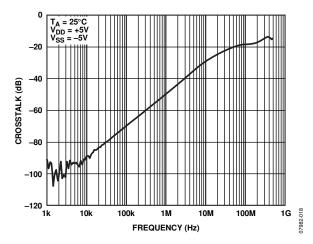


Figure 18. Crosstalk vs. Frequency

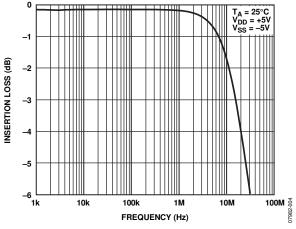


Figure 19. On Response vs. Frequency

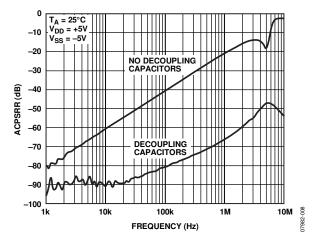


Figure 20. ACPSRR vs. Frequency

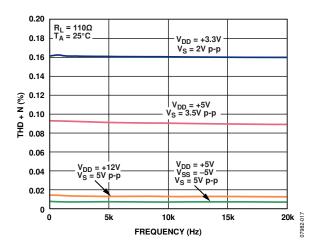
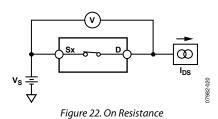


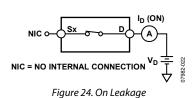
Figure 21. THD + N vs. Frequency

TEST CIRCUITS



 $V_{S} \stackrel{I_{S} \text{ (OFF)}}{=} V_{D} \stackrel{I_{D} \text{ (OFF)}}{=}$

Figure 23. Off Leakage



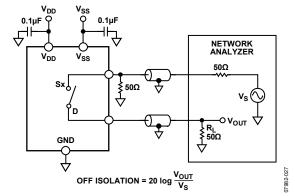


Figure 25. Off Isolation

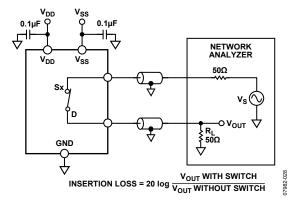


Figure 26. Bandwidth

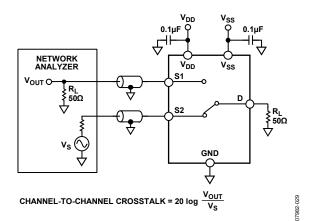


Figure 27. Channel-to-Channel Crosstalk

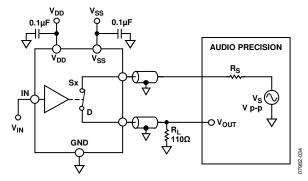


Figure 28. THD + Noise

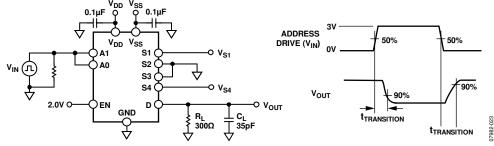


Figure 29. Address to Output Switching Times

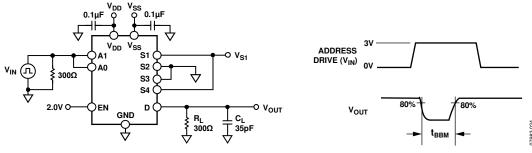


Figure 30. Break-Before-Make Time Delay

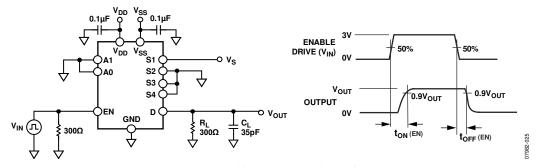


Figure 31. Enable-to-Output Switching Delay

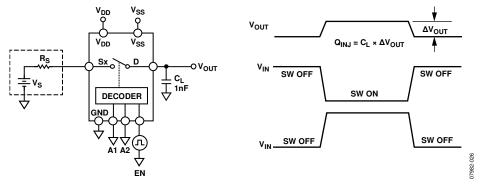


Figure 32. Charge Injection

TERMINOLOGY

 I_{DD}

The positive supply current.

 I_{ss}

The negative supply current.

 $V_D(V_S)$

The analog voltage on Terminal D and Terminal S.

Ron

The ohmic resistance between Terminal D and Terminal S.

R_{FLAT(ON)}

Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

Is (Off)

The source leakage current with the switch off.

I_D (Off)

The drain leakage current with the switch off.

 $I_D, I_S(On)$

The channel leakage current with the switch on.

 \mathbf{V}_{INI}

The maximum input voltage for Logic 0.

 \mathbf{V}_{INH}

The minimum input voltage for Logic 1.

I_{INL} (I_{INH})

The input current of the digital input.

Cs (Off)

The off switch source capacitance, which is measured with reference to ground.

CD (Off)

The off switch drain capacitance, which is measured with reference to ground.

 C_D , C_S (On)

The on switch capacitance, which is measured with reference to ground.

 C_{IN}

The digital input capacitance.

transition

The delay time between the 50% and 90% points of the digital input and switch on condition when switching from one address state to another. See Figure 29.

ton (EN)

The delay between applying the digital control input and the output switching on. See Figure 31.

toff (EN)

The delay between applying the digital control input and the output switching off. See Figure 31.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching. See Figure 32.

Off Isolation

A measure of unwanted signal coupling through an off switch. See Figure 25.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. See Figure 27.

Bandwidth

The frequency at which the output is attenuated by 3 dB. See Figure 26.

On Response

The frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

Total Harmonic Distortion + Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental. See Figure 28.

AC Power Supply Rejection Ratio (ACPSRR)

The ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

OUTLINE DIMENSIONS

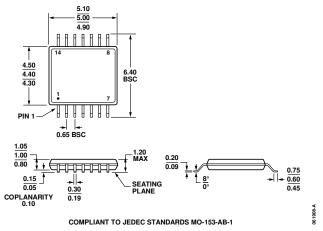


Figure 33. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14) Dimensions shown in millimeters

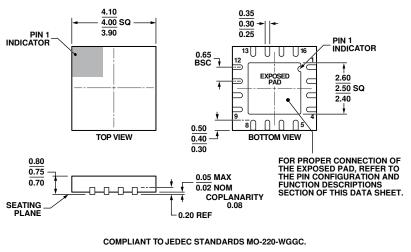


Figure 34. 16-Lead Lead Frame Chip Scale Package [LFCSP] 4 mm × 4 mm Body and 0.75 mm Package Height (CP-16-26) Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADG1604BRUZ	-40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
ADG1604BRUZ-REEL	-40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
ADG1604BRUZ-REEL7	-40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
ADG1604BCPZ-REEL	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-26
ADG1604BCPZ-REEL7	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-26

¹ Z = RoHS Compliant Part.

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