

## N- and P-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY				
	V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
N-Channel	12	0.040 at V <sub>GS</sub> = 4.5 V	4.5 <sup>a</sup>	4.5 nC
		0.048 at V <sub>GS</sub> = 2.5 V	4.5 <sup>a</sup>	
		0.063 at V <sub>GS</sub> = 1.8 V	4.5 <sup>a</sup>	
P-Channel	- 12	0.070 at V <sub>GS</sub> = - 4.5 V	- 4.5 <sup>a</sup>	5 nC
		0.100 at V <sub>GS</sub> = - 2.5 V	- 4.5 <sup>a</sup>	
		0.140 at V <sub>GS</sub> = - 1.8 V	- 4.5 <sup>a</sup>	

### FEATURES

- Halogen-free
- TrenchFET<sup>®</sup> Power MOSFETs
- New Thermally Enhanced PowerPAK<sup>®</sup> SC-70 Package
  - Small Footprint Area
  - Low On-Resistance

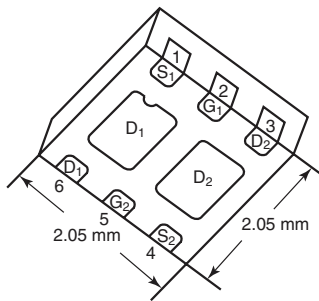


**RoHS**  
COMPLIANT

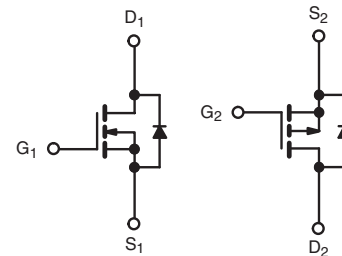
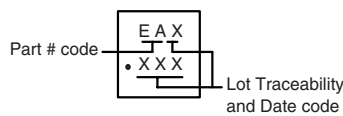
### APPLICATIONS

- Load Switch for Portable Devices

PowerPAK SC-70-6 Dual



Marking Code



Ordering Information: SiA511DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted					
Parameter	Symbol	N-Channel	P-Channel	Unit	
Drain-Source Voltage	V <sub>DS</sub>	12	- 12	V	
Gate-Source Voltage	V <sub>GS</sub>	± 8			
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	4.5 <sup>a</sup>	- 4.5 <sup>a</sup>	A
		T <sub>C</sub> = 70 °C	4.5 <sup>a</sup>	- 4.5 <sup>a</sup>	
		T <sub>A</sub> = 25 °C	4.5 <sup>a, b, c</sup>	- 4.3 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	4.5 <sup>a, b, c</sup>	- 3.4 <sup>b, c</sup>	
Pulsed Drain Current	I <sub>DM</sub>	20	- 10	A	
Source Drain Current Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	4.5 <sup>a</sup>		- 4.5 <sup>a</sup>
		T <sub>A</sub> = 25 °C	1.6 <sup>b, c</sup>	- 1.6 <sup>b, c</sup>	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	6.5	6.5	W
		T <sub>C</sub> = 70 °C	5	5	
		T <sub>A</sub> = 25 °C	1.9 <sup>b, c</sup>	1.9 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	1.2 <sup>b, c</sup>	1.2 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260			

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	N-Channel		P-Channel		Unit
		Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient <sup>b, f</sup>	R <sub>thJA</sub>	52	65	52	65	°C/W
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	12.5	16	12.5	16	

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- t = 5 s.
- See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 110 °C/W.



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	N-Ch	12			V
		$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-12			
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		12		mV/ $^\circ\text{C}$
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		-7		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		-2.8		
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		2.1		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	0.4		1	V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-0.4		-1	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$	N-Ch			$\pm 100$	nA
			P-Ch			$\pm 100$	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 12\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	$\mu\text{A}$
		$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-1	
		$V_{DS} = 12\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	N-Ch			10	
		$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	P-Ch			-10	
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	N-Ch	15			A
		$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	P-Ch	-8			
Drain-Source On-State Resistance <sup>b</sup>	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 4.2\text{ A}$	N-Ch		0.033	0.040	$\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -3.3\text{ A}$	P-Ch		0.058	0.070	
		$V_{GS} = 2.5\text{ V}, I_D = 3.8\text{ A}$	N-Ch		0.039	0.048	
		$V_{GS} = -2.5\text{ V}, I_D = -2.8\text{ A}$	P-Ch		0.082	0.100	
		$V_{GS} = 1.8\text{ V}, I_D = 1.6\text{ A}$	N-Ch		0.051	0.063	
		$V_{GS} = -1.8\text{ V}, I_D = -0.7\text{ A}$	P-Ch		0.111	0.140	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 4.2\text{ A}$	N-Ch		13		S
		$V_{DS} = -10\text{ V}, I_D = -3.3\text{ A}$	P-Ch		9		
<b>Dynamic<sup>a</sup></b>							
Input Capacitance	$C_{iss}$	N-Channel $V_{DS} = 6\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		400		pF
			P-Ch		400		
Output Capacitance	$C_{oss}$	P-Channel $V_{DS} = -6\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		120		
			P-Ch		140		
Reverse Transfer Capacitance	$C_{rss}$		N-Ch		70		
			P-Ch		100		
Total Gate Charge	$Q_g$	$V_{DS} = 6\text{ V}, V_{GS} = 8\text{ V}, I_D = 5.5\text{ A}$	N-Ch		7.5	12	nC
		$V_{DS} = -6\text{ V}, V_{GS} = -8\text{ V}, I_D = -4.3\text{ A}$	P-Ch		8	12	
Gate-Source Charge	$Q_{gs}$	N-Channel $V_{DS} = 6\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 5.5\text{ A}$	N-Ch		4.5	6.8	
			P-Ch		5	7.5	
Gate-Drain Charge	$Q_{gd}$	P-Channel $V_{DS} = -6\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -4.3\text{ A}$	N-Ch		0.6		
			P-Ch		0.8		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	N-Ch		2.5		$\Omega$
			P-Ch		7		

Notes:

- a. Guaranteed by design, not subject to production testing.  
b. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
<b>Dynamic<sup>a</sup></b>							
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 6\text{ V}$ , $R_L = 1.4\ \Omega$ $I_D \cong 4.4\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\ \Omega$	N-Ch		5	10	ns
Rise Time	$t_r$		P-Ch		15	25	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -6\text{ V}$ , $R_L = 1.8\ \Omega$ $I_D \cong -3.4\text{ A}$ , $V_{GEN} = -4.5\text{ V}$ , $R_g = 1\ \Omega$	N-Ch		35	55	
Fall Time	$t_f$		P-Ch		20	30	
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 6\text{ V}$ , $R_L = 1.4\ \Omega$ $I_D \cong 4.4\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	N-Ch		5	10	
Rise Time	$t_r$		P-Ch		5	10	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -6\text{ V}$ , $R_L = 1.8\ \Omega$ $I_D \cong -3.4\text{ A}$ , $V_{GEN} = -10\text{ V}$ , $R_g = 1\ \Omega$	N-Ch		10	15	
Fall Time	$t_f$		P-Ch		12	20	
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 6\text{ V}$ , $R_L = 1.4\ \Omega$ $I_D \cong 4.4\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	N-Ch		15	25	
Rise Time	$t_r$		P-Ch		20	30	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -6\text{ V}$ , $R_L = 1.8\ \Omega$ $I_D \cong -3.4\text{ A}$ , $V_{GEN} = -10\text{ V}$ , $R_g = 1\ \Omega$	N-Ch		10	15	
Fall Time	$t_f$		P-Ch		10	15	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	N-Ch			4.5	A
			P-Ch			-4.5	
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$		N-Ch			20	A
			P-Ch			-10	
Body Diode Voltage	$V_{SD}$	$I_S = 4.4\text{ A}$ , $V_{GS} = 0\text{ V}$	N-Ch		0.8	1.2	V
		$I_S = -3.4\text{ A}$ , $V_{GS} = 0\text{ V}$	P-Ch		-0.8	-1.2	
Body Diode Reverse Recovery Time	$t_{rr}$	N-Channel $I_F = 4.4\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	N-Ch		15	30	ns
			P-Ch		30	60	
Body Diode Reverse Recovery Charge	$Q_{rr}$	P-Channel $I_F = -3.4\text{ A}$ , $di/dt = -100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	N-Ch		8	20	nC
			P-Ch		12	24	
Reverse Recovery Fall Time	$t_a$	P-Channel $I_F = -3.4\text{ A}$ , $di/dt = -100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	N-Ch		8.5		ns
			P-Ch		14		
Reverse Recovery Rise Time	$t_b$	P-Channel $I_F = -3.4\text{ A}$ , $di/dt = -100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	N-Ch		8.5		
			P-Ch		16		

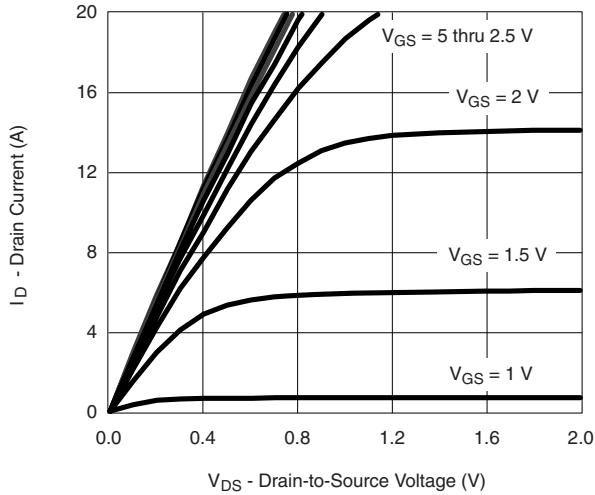
Notes:

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

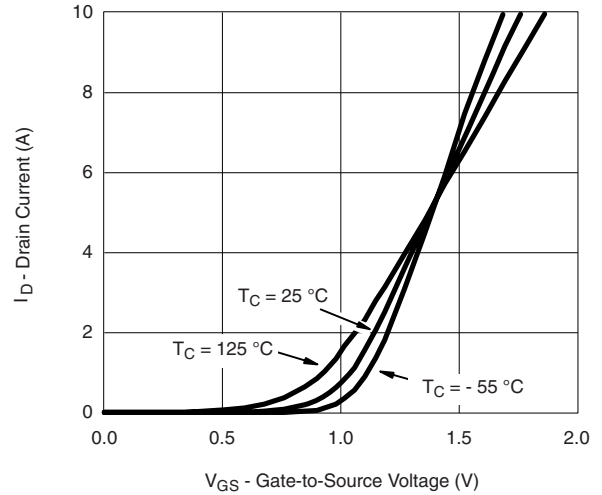
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



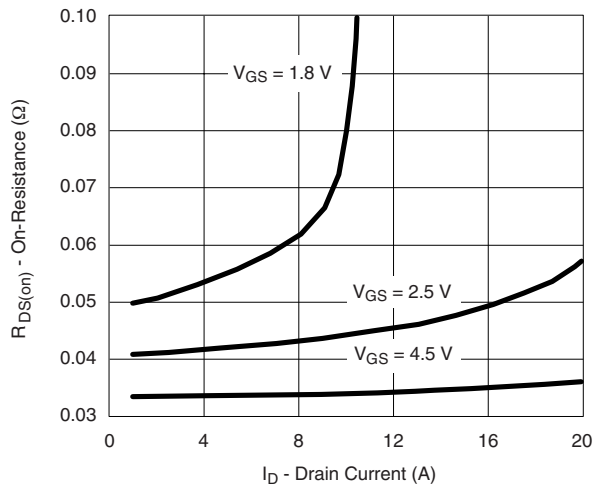
**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



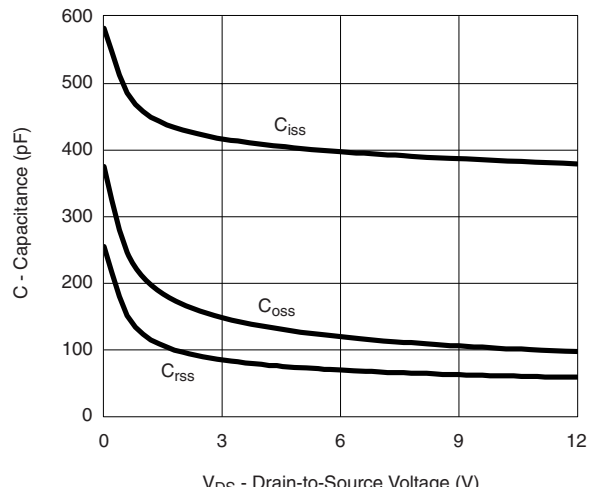
**Output Characteristics**



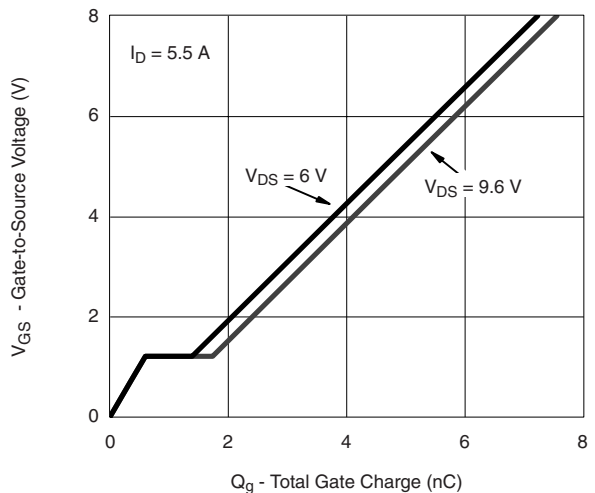
**Transfer Characteristics**



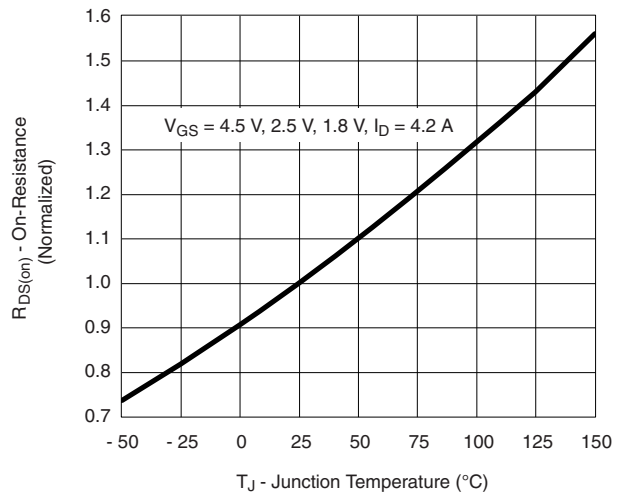
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**



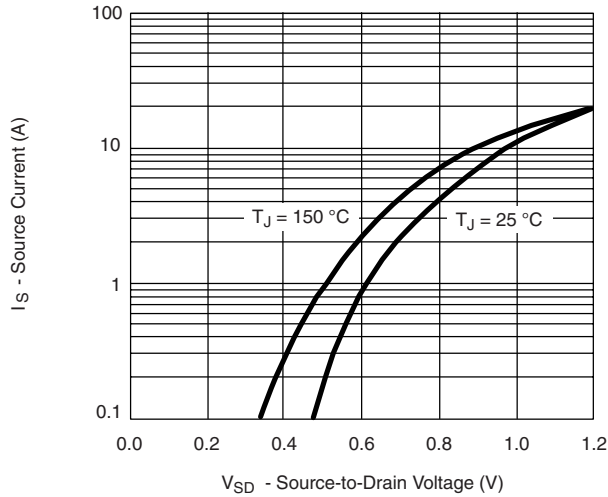
**Gate Charge**



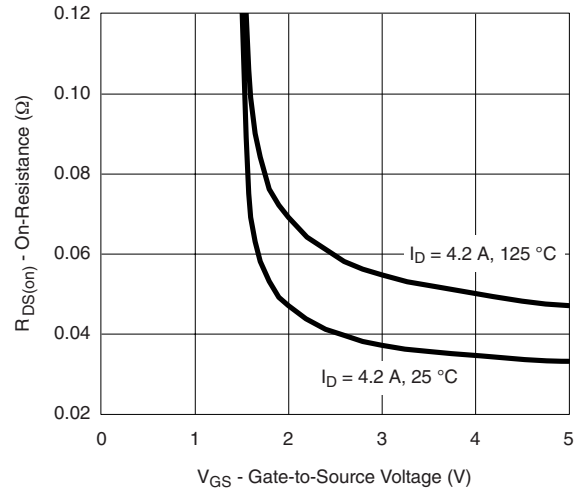
**On-Resistance vs. Junction Temperature**



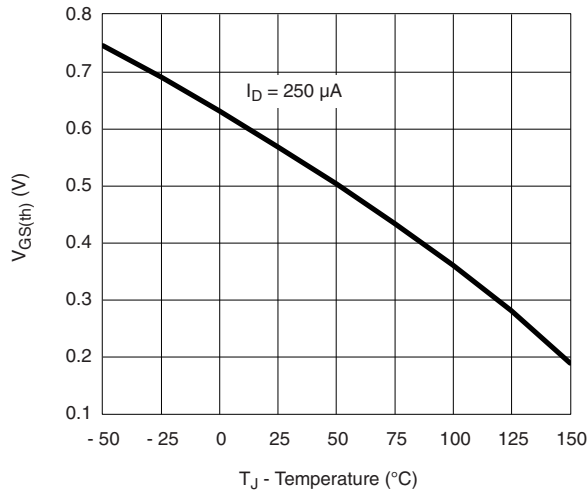
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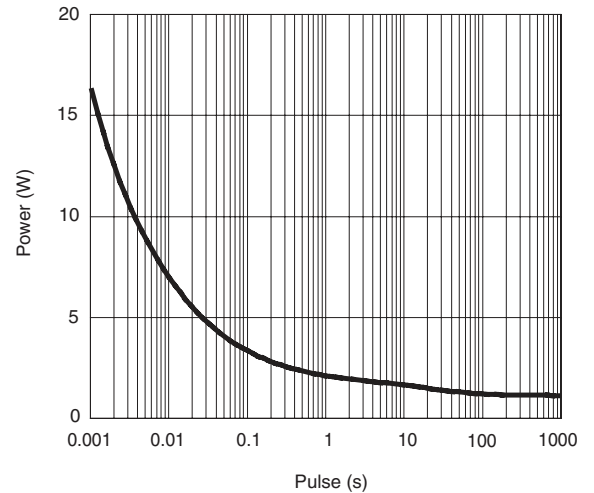
Source-Drain Diode Forward Voltage



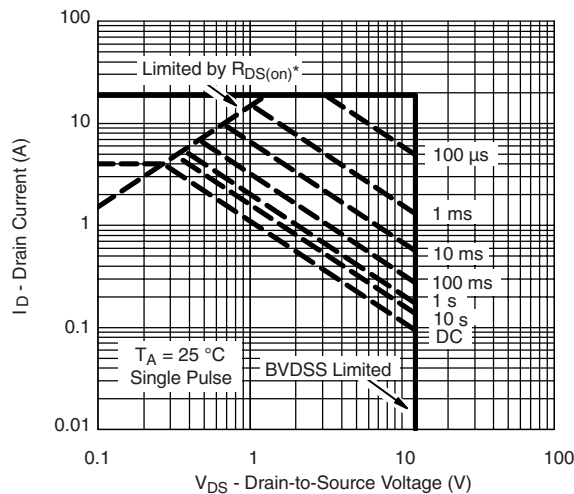
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power (Junction-to-Ambient)

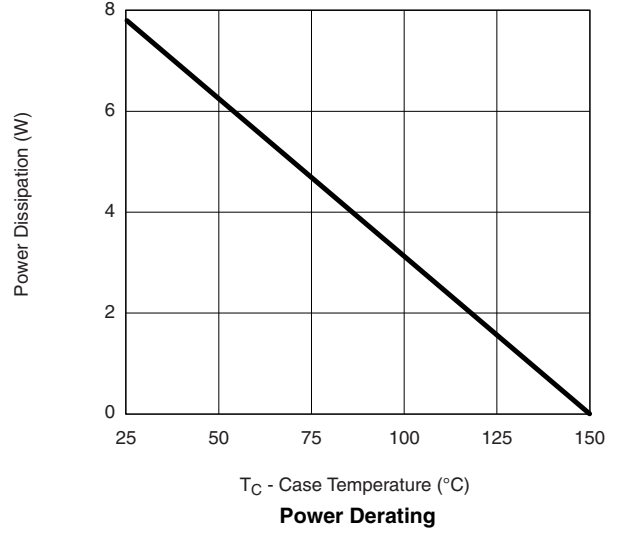
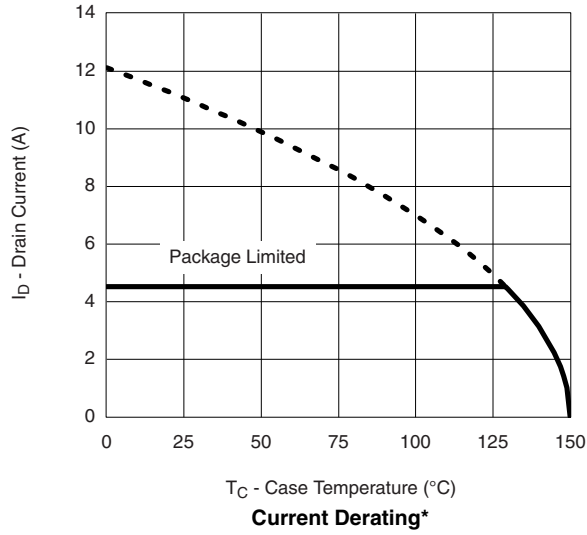


\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Ambient



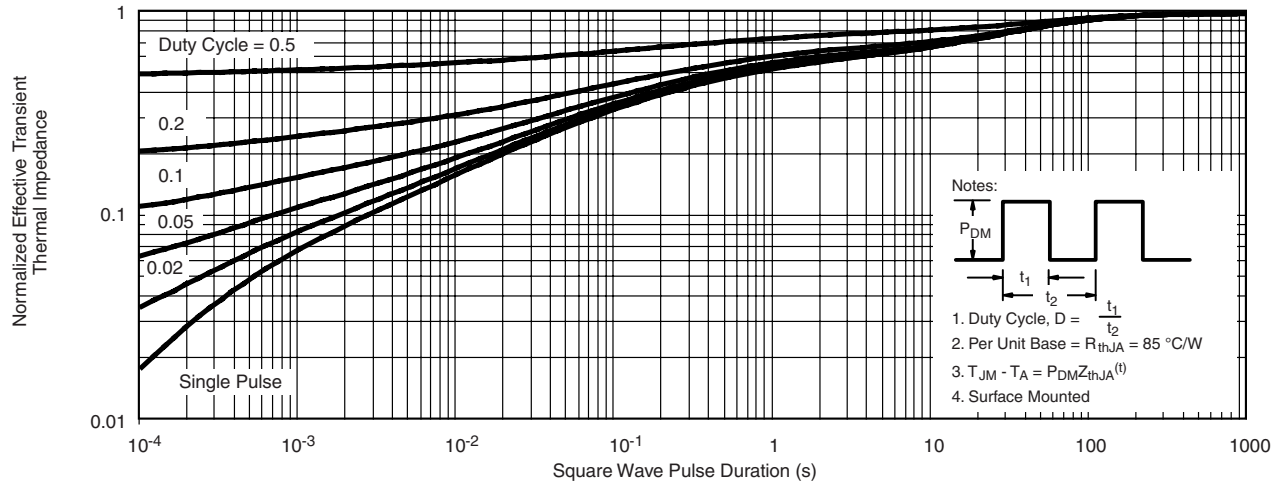
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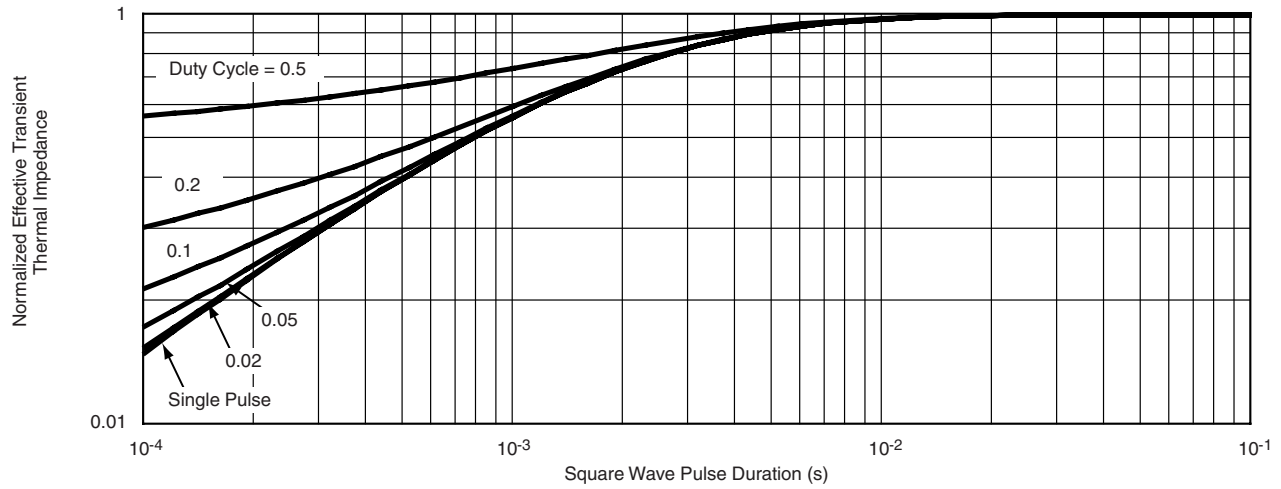
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



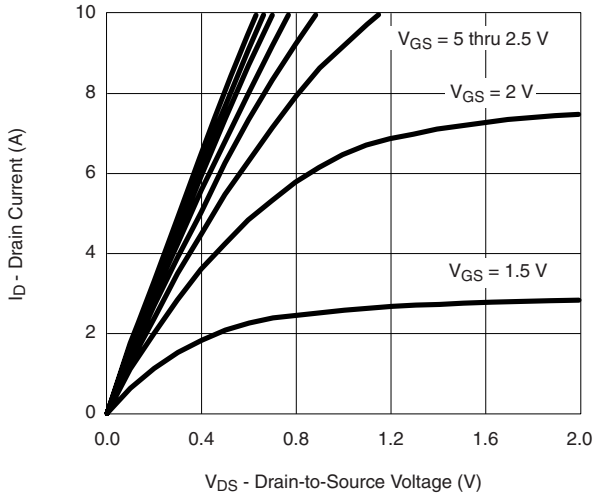
**Normalized Thermal Transient Impedance, Junction-to-Ambient**



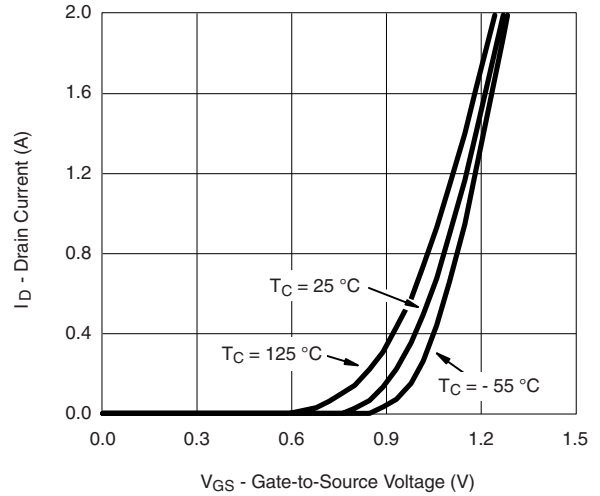
**Normalized Thermal Transient Impedance, Junction-to-Foot**



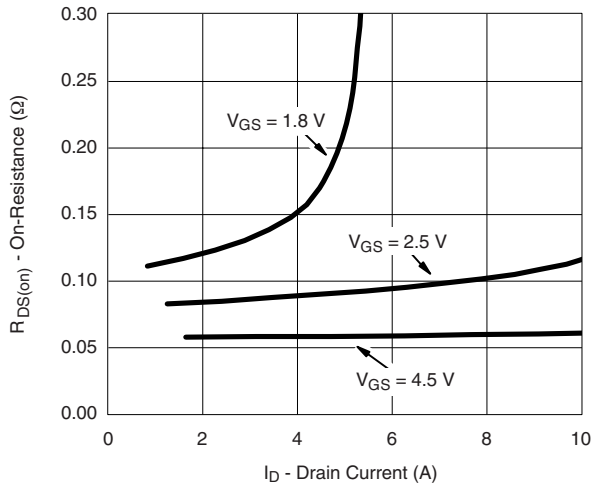
**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



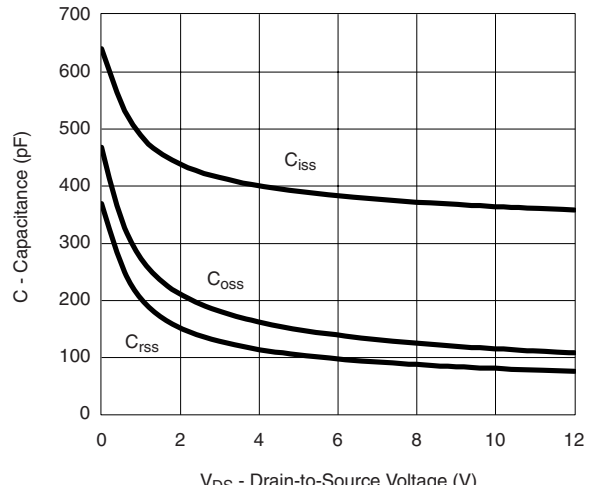
**Output Characteristics**



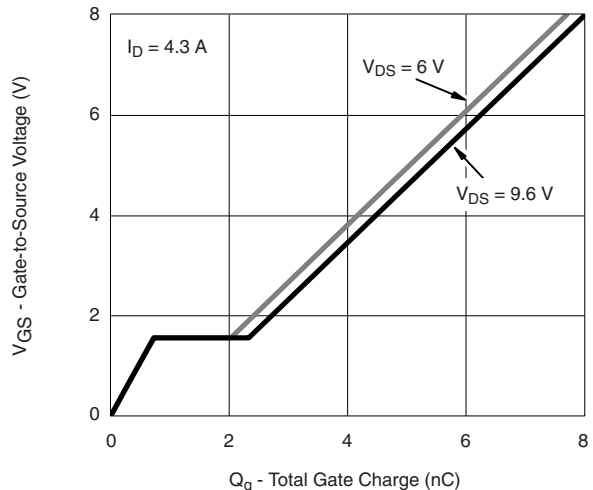
**Transfer Characteristics**



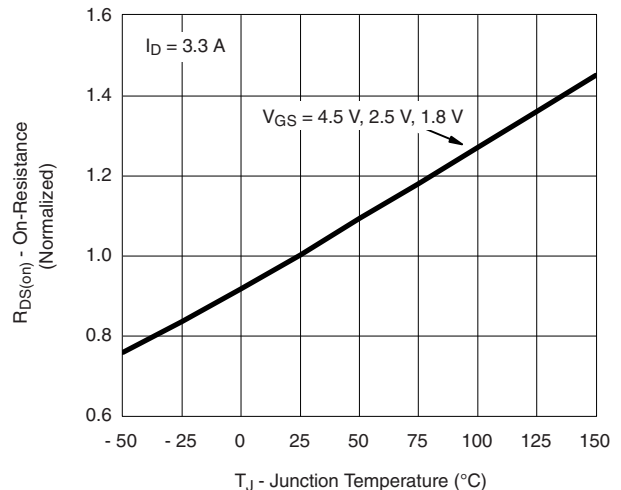
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**



**Gate Charge**

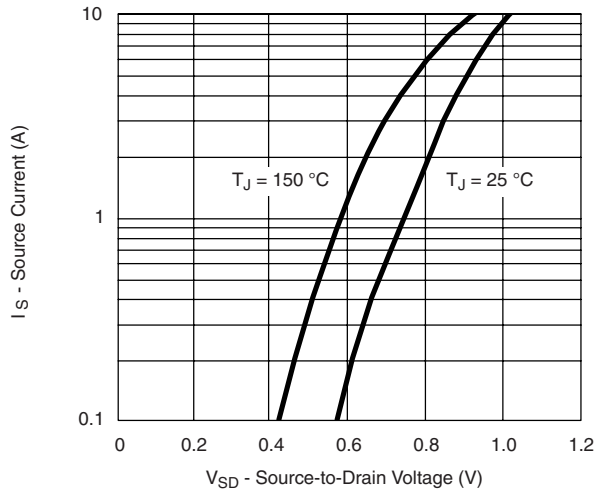


**On-Resistance vs. Junction Temperature**

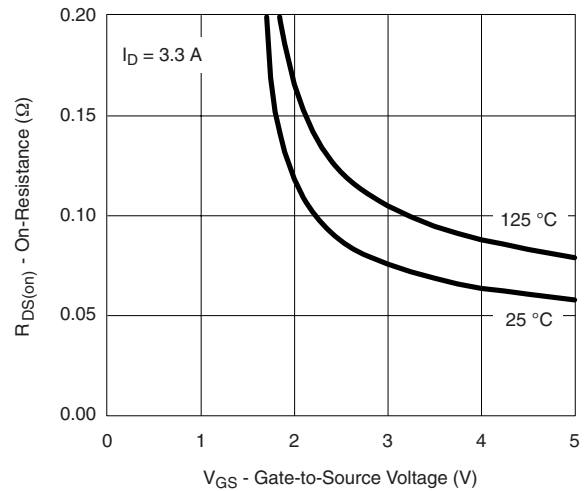




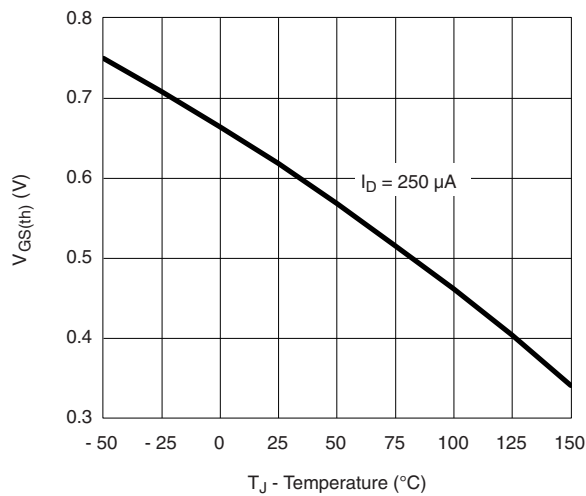
**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



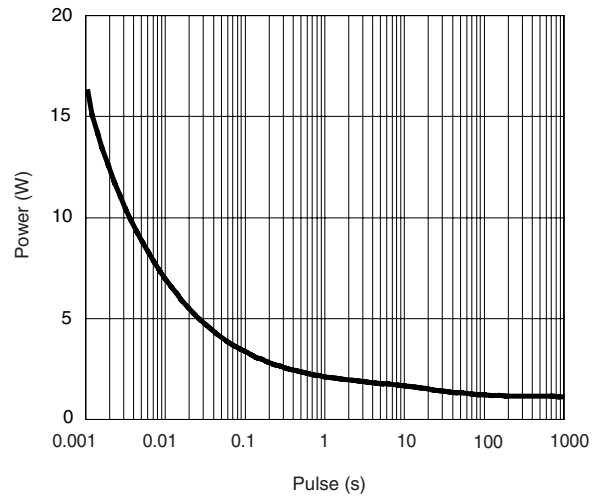
**Source-Drain Diode Forward Voltage**



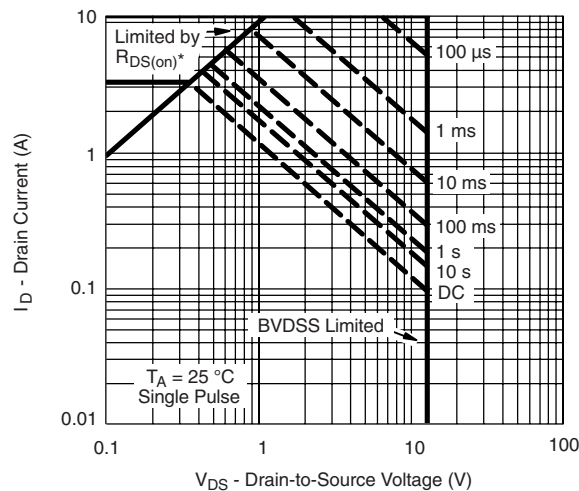
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



**Single Pulse Power, Junction-to-Ambient**

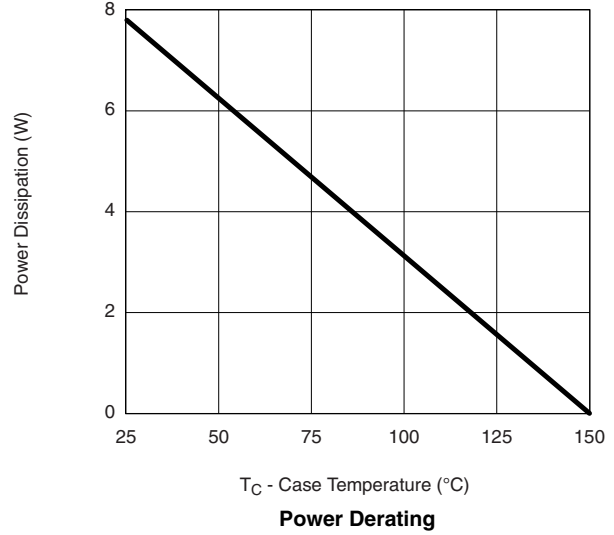
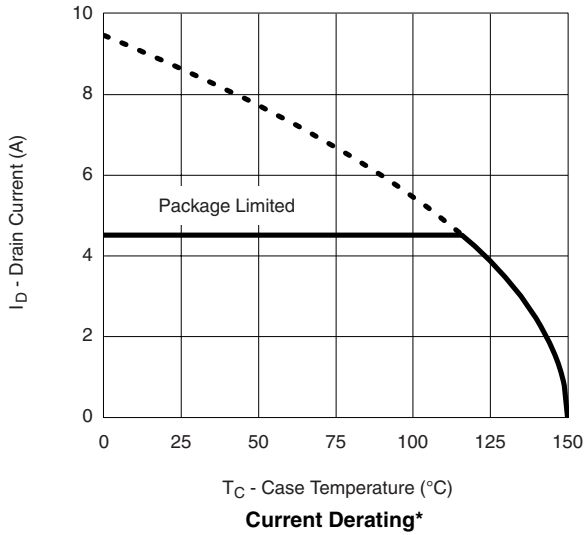


\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**Safe Operating Area, Junction-to-Ambient**



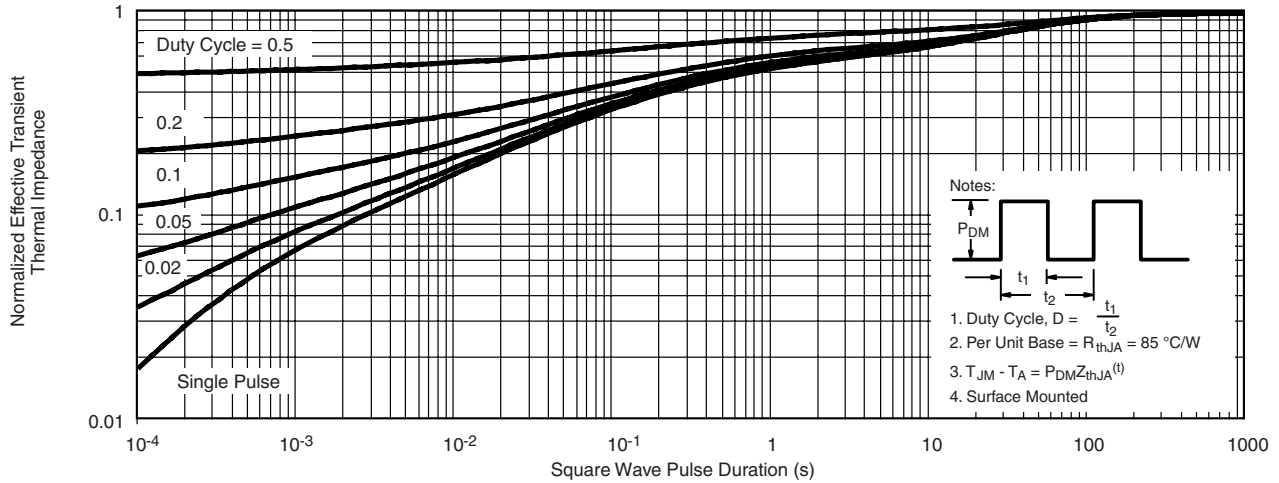
**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



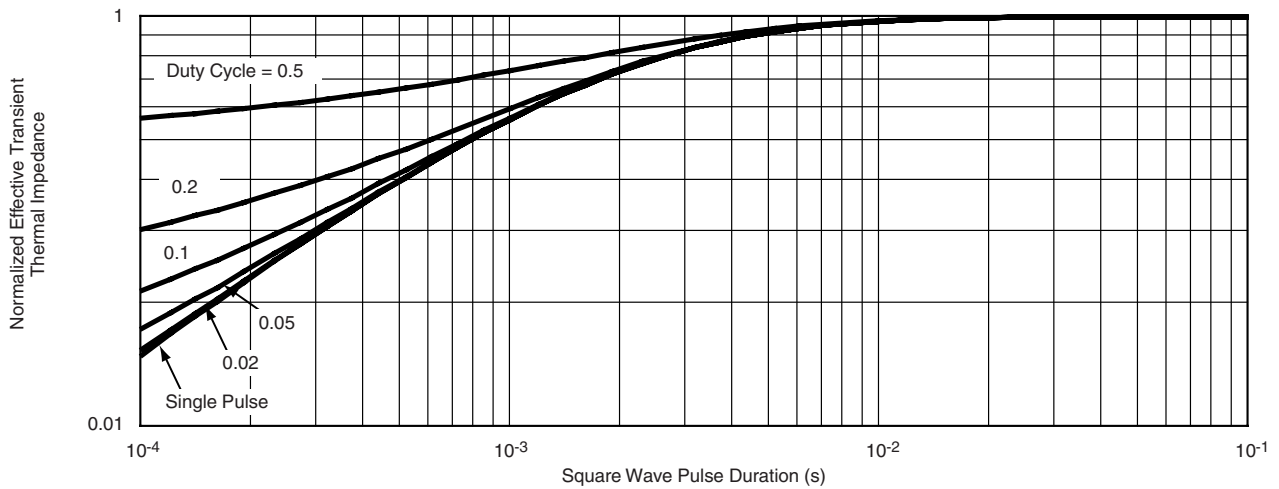
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**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?74592>.



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