

SN54ABT640, SN74ABT640 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS104A - D3778, FEBRUARY 1991 - REVISED OCTOBER 1992

- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (-32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

description

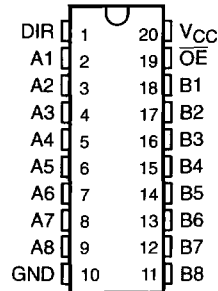
The 'ABT640 bus transceiver is designed for asynchronous communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

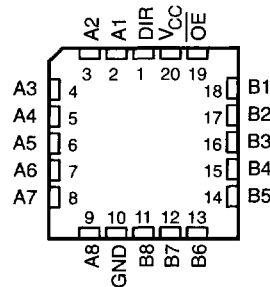
The SN74ABT640 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT640 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT640 is characterized for operation from -40°C to 85°C .

SN54ABT640 . . . J PACKAGE
SN74ABT640 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



SN54ABT640 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	\overline{B} data to A bus
L	H	\overline{A} data to B bus
H	X	Isolation

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UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

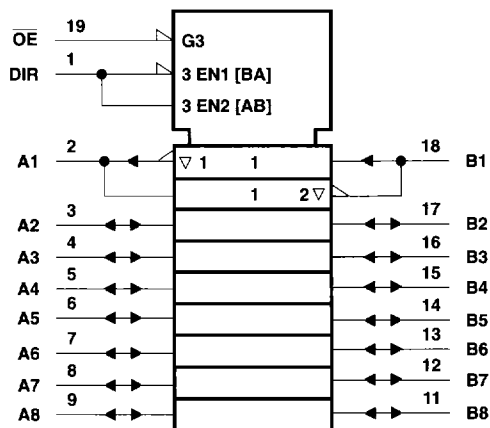
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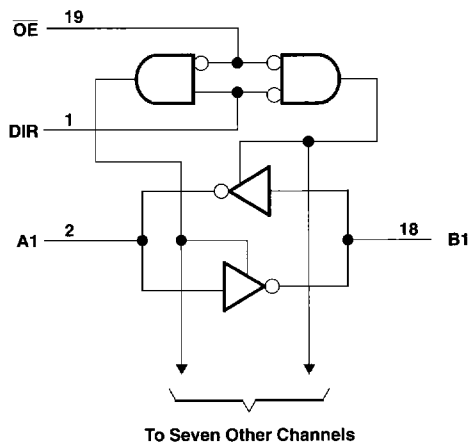
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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT640	96 mA
SN74ABT640	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.65 W
DW package	0.85 W
N package	1.3 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT640		SN74ABT640		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		-24		-32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5	5	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = 25°C			SN54ABT640		SN74ABT640		UNIT		
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX			
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA					-1.2		-1.2		V		
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA		2.5			2.5		2.5		V		
	V _{CC} = 5 V, I _{OH} = -3 mA		3			3		3				
	V _{CC} = 4.5 V, I _{OH} = -24 mA		2			2						
	V _{CC} = 4.5 V, I _{OH} = -32 mA		2‡					2				
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 48 mA					0.55				V		
	V _{CC} = 4.5 V, I _{OL} = 64 mA					0.55‡		0.55				
I _I	V _{CC} = 5.5 V, V _I = V _{CC} or GND		Control inputs		±1			±1		μA		
			A or B ports		±100			±100				
I _{OZH} §	V _{CC} = 5.5 V, V _O = 2.7 V		50			50		50		μA		
I _{OZL} §	V _{CC} = 5.5 V, V _O = 0.5 V		-50			-50		-50		μA		
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V		±100					±100		μA		
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V		Outputs high		50			50		μA		
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND		A or B ports		Outputs high		5		250		μA	
					Outputs low		24		30		30	mA
					Outputs disabled		0.5		250		250	
ΔI _{CC} #	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		Data inputs		Outputs enabled		1.5		1.5		mA	
					Outputs disabled		0.05		0.05			
			Control inputs				1.5		1.5		1.5	
C _i	V _I = 2.5 V or 0.5 V		Control inputs		4					pF		
C _{io}	V _O = 2.5 V or 0.5 V		A or B ports		7					pF		

† All typical values are at V_{CC} = 5 V.

‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

§ The parameters I_{OZH} and I_{OZL} include the input leakage current.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			SN54ABT640		SN74ABT640		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	1	2.7	4.2	1	5	1	4.9	ns
t _{PHL}			1.5	2.7	4.3	1.5	5	1.5	4.9	
t _{PZH}	OE	A or B	1.5	3.7	4.9	1.5	8.9	1.5	5.8	ns
t _{PZL}			1.3	5	5.9	1.3	7.4	1.3	7.3	
t _{PHZ}	OE	A or B	2.5	4.1	6.5	2.5	6.9	2.5	6.8	ns
t _{PLZ}			2	3.3	5.3	2	5.6	2	5.5	

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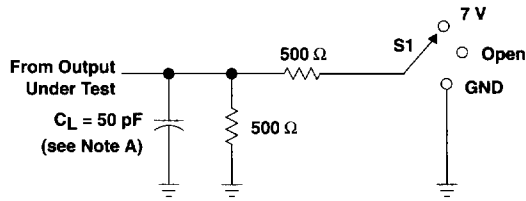


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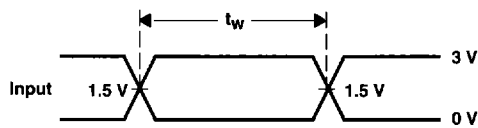
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PARAMETER MEASUREMENT INFORMATION

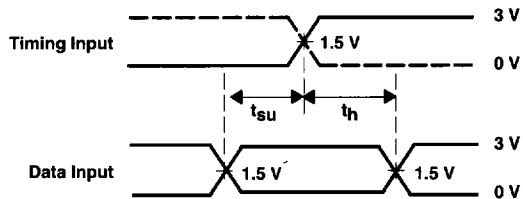


LOAD CIRCUIT FOR OUTPUTS

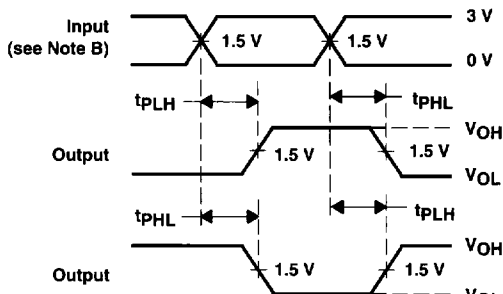
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



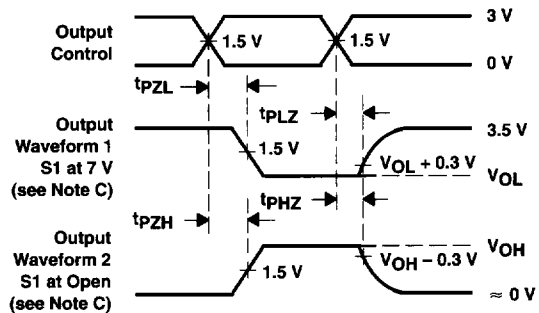
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms