



# High Speed CMOS Presettable Synchronous 4-Bit Binary Counters

QS54/74FCT191T

QS54/74FCT2191T

## FEATURES/BENEFITS

- Pin and function compatible to the 74F191 74FCT191 and 74FCT2191T
- CMOS power levels: <7.5 mW static
- Available in DIP, SOIC, QSOP, ZIP, HQSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

### FCT-T 191T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std., A, and C speed grades with 6.9 ns  $t_{PD}$  for C
- $I_{OL} = 48$  mA Com., 32 mA Mil.

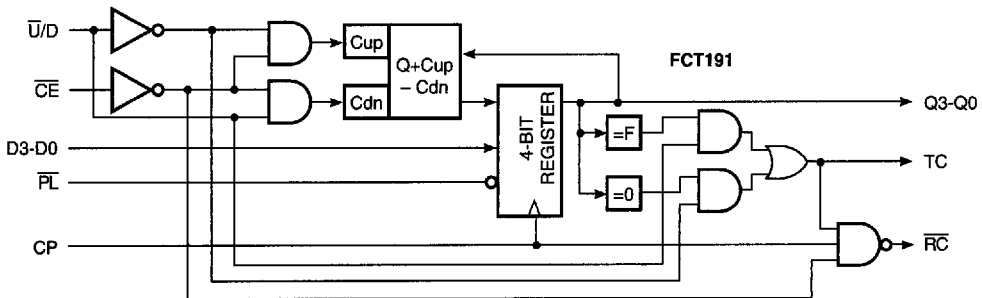
### FCT-T 2191T

- Built-in  $25\Omega$  series resistor outputs reduce reflection and other system noise
- Std., A, and C speed grades with 6.9 ns  $t_{PD}$  for C
- $I_{OL} = 12$  mA Com.

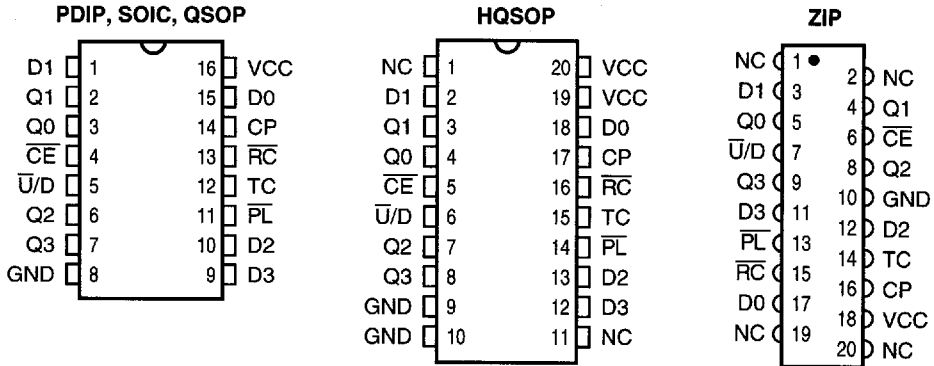
## DESCRIPTION

The QSFCT191T is a high speed CMOS 4-bit binary up/down counter. It has a single clock with clock enable and up/down control inputs and ripple carry output. The '191 has asynchronous preload inputs which override the count inputs. The '2191 is a  $25\Omega$  resistor output version of the '191 and is useful for driving transmission lines and reducing system noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001).

## FUNCTIONAL BLOCK DIAGRAM



**PIN CONFIGURATIONS (All Pins Top View)**



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**Note:**  
Available in both 150 mil wide SOIC (package code S1) and 300 mil SOIC (package code SO).

**PIN DESCRIPTION**

Name	I/O	Description
D3-D0	I	Data Inputs
Q3-Q0	O	Data Outputs
PL	I	Preload
$\overline{U/D}$	I	Up/Down Select

Name	I/O	Description
$\overline{CE}$	I	Count Enable
CP	I	Count Clock
TC	O	Terminal Count
$\overline{RC}$	O	Ripple Clock

**FUNCTION TABLE**

Inputs				Outputs				Function
PL	$\overline{U/D}$	CP	$\overline{CE}$	Di	Q3-Q0	TC	$\overline{RC}$	
L	X	X	X	D3-D0	D3-D0	X	X	Load Data
H	L	↑	L	X	Q+1	L	H	Count Up
H	H	↑	L	X	Q-1	L	H	Count Down
H	X	X	H	X	Q	X	X	Count Inhibit
H	L	H	L	X	F	H	H	Count Up = 1111
H	L	⎓	L	X	F	H	⎓	Count Up = 1111
H	L	X	X	X	0-E	L	H	Count Up ≠ 1111
H	H	H	L	X	0	H	H	Count Down = 0000
H	H	⎓	L	X	0	H	⎓	Count Down = 0000
H	H	X	X	X	1-F	L	H	Count Down ≠ 0000

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage to Ground .....	-0.5V to +7.0V
DC Output Voltage $V_{OUT}$ .....	-0.5V to +7.0V
DC Input Voltage $V_{IN}$ .....	-0.5V to +7.0V
AC Input Voltage (for a pulse width $\leq 20$ ns) .....	-3.0V
DC Input Diode Current with $V_{IN} < 0$ .....	-20 mA
DC Output Diode Current with $V_{OUT} < 0$ .....	-50 mA
DC Output Current Max. Sink Current/Pin .....	120 mA
Maximum Power Dissipation .....	0.5 watts
$T_{STG}$ Storage Temperature .....	-65° to +150°C

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

**CAPACITANCE**

$T_A = 25^\circ\text{C}$ ,  $f = 1$  MHz,  $V_{IN} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$

Pins	SOIC	QSOP	PDIP	ZIP	Unit
1, 4, 5, 9-11, 14, 15	4	4	5	7	pF
2, 3, 6, 7, 12, 13	6	6	7	9	pF
—	8	8	9	10	pF

**Note:** Capacitance is characterized but not tested.

**POWER SUPPLY CHARACTERISTICS**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min	Max	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ , $\text{freq} = 0$ $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
$\Delta I_{CC}$	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}$ , $V_{IN} = 3.4\text{V}$ , $\text{freq} = 0$ <sup>(2)</sup>	—	2.0	mA
$Q_{CCD}$	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$ , Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or $V_{CC}$ <sup>(3,4)</sup>	—	0.25	mA/ MHz

**Notes:**

- For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
- Per TTL driven input ( $V_{IN} = 3.4\text{V}$ ).
- For flip-flops,  $Q_{CCD}$  is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
- $I_C$  can be computed using the above parameters as explained in the Technical Overview section.

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ <sup>(1)</sup>	Max	Unit
$V_{IH}$	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
$V_{IL}$	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
$\Delta V_T$	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	5	$\mu\text{A}$
$I_{OS}$	Short Circuit Current (FCTXXX)	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$	-60	—	—	mA
$I_{OR}$	Current Drive (FCT2XXX)	$V_{CC} = \text{Max.}, V_{OUT} = 2.0\text{V}^{(3)}$	50	—	—	mA
$V_{IC}$	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}, T_A = 25^\circ\text{C}^{(3)}$	—	-0.7	-1.2	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -12 \text{ mA (MIL)}$ $I_{OH} = -15 \text{ mA (COM)}$	2.4 2.4	— —	— —	V
$V_{OL}$	Output LOW Voltage (FCTXXX)	$V_{CC} = \text{Min.}, I_{OL} = 32 \text{ mA (MIL)}$ $I_{OL} = 48 \text{ mA (COM)}$	— —	— —	0.50 0.50	V
$V_{OL}$	Output LOW Voltage (FCT2XXX- 25 $\Omega$ )	$V_{CC} = \text{Min.}, I_{OL} = 12 \text{ mA (MIL)}$ $I_{OL} = 12 \text{ mA (COM)}$	— —	— —	0.50 0.50	V
$R_{OUT}$	Output Resistance (FCT2XXX- 25 $\Omega$ )	$V_{CC} = \text{Min.}, I_{OL} = 12 \text{ mA (MIL)}$ $I_{OL} = 12 \text{ mA (COM)}$	— 20	25 28	— 40	$\Omega$

**Notes:**

1. Typical values indicate  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^\circ\text{C}$ .
2. Not more than one output should be shorted and the duration is  $\leq 1$  second.
3. These parameters are guaranteed by design but not tested.

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**QSFCT191T, QSFCT2191T**

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

$C_{LOAD} = 50\text{ pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted.

Symbol	Description <sup>(1)</sup>		191 2191		191A 2191A		191C 2191C		Unit
			Min	Max	Min	Max	Min	Max	
tcPQ	Propagation Delay CP to Qi	Com	2.5	12	2.5	7.8	2.0	6.9	ns
		Mil	1.5	16	1.5	10.5	1.5	9.0	
tcPTC	Propagation Delay CP to TC	Com	3.0	14	3.0	11.8	2.5	10.2	ns
		Mil	2.0	16	2.0	12.2	1.5	11.5	
tcPRC	Propagation Delay CP to RC	Com	2.5	8.5	2.5	8.5	2.0	8.0	ns
		Mil	1.5	12.5	1.5	10	2.0	9.2	
tcERC	Propagation Delay $\overline{CE}$ to $\overline{RC}$	Com	2.0	8.0	2.0	7.2	1.5	6.8	ns
		Mil	2.0	8.5	2.0	8.0	2.0	7.4	
tUDRC	Propagation Delay $\overline{U/D}$ to RC	Com	4.0	15	2.0	9.8	2.0	9.0	ns
		Mil	4.0	16.5	2.0	10.8	2.0	10	
tUDTC	Propagation Delay $\overline{U/D}$ to TC	Com	3.0	11	3.0	7.2	2.0	6.8	ns
		Mil	3.0	13	3.0	8.5	1.5	7.9	
tdQ	Propagation Delay Pi to Qi	Com	2.0	14	2.0	9.1	2.0	8.5	ns
		Mil	1.5	16	1.5	10.4	1.5	9.8	
tPLQ	Propagation Delay $\overline{PL}$ to Qi	Com	3.0	13	3.0	8.5	2.0	7.8	ns
		Mil	3.0	14	3.0	9.1	2.0	8.5	

**Notes:**

1. Minimums guaranteed but not tested.
2. See Test Circuit and Waveforms.

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**TIMING REQUIREMENTS OVER OPERATING RANGE**

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

$C_{LOAD} = 50\text{ pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted.

Symbol	Description		191 2191		191A 2191A		191C 2191C		Unit
			Min	Max	Min	Max	Min	Max	
tDPLS	Di to PL Setup	Com	5.0		4.0		4.0		ns
		Mil	6.0		5.0		5.0		
tDPLH	Di to $\overline{\text{PL}}$ Hold	Com	1.5		1.5		1.5		ns
		Mil	1.5		1.5		1.5		
tCS	$\overline{\text{CE}}$ to CP Setup	Com	10		9.0		9.0		ns
		Mil	10.5		9.5		9.5		
tCH	$\overline{\text{CE}}$ to CP Hold	Com	0		0		0		ns
		Mil	0		0		0		
tUDCPS	$\overline{\text{U/D}}$ to CP Setup	Com	12		10		10		ns
		Mil	12		10		10		
tUDCPH	$\overline{\text{U/D}}$ to CP Hold	Com	0		0		0		ns
		Mil	0		0		0		
tCPW	Clock Pulse <sup>(1)</sup> Width HIGH or LOW	Com	5.0		4.0		4.0		ns
		Mil	7.0		6.0		6.0		
tPL	$\overline{\text{PL}}$ LOW	Com	6.0		5.5		5.5		ns
		Mil	8.5		8.0		8.0		
tPLCPR	$\overline{\text{PL}}$ to CP Recovery	Com	6.0		5.0		5.0		ns
		Mil	7.5		6.5		6.5		

**Notes:**

1. This parameter is guaranteed by design but not tested.
2. See Test Circuit and Waveforms.

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