EVAL_6EDL7141_TRAP_1SH 18 V brushless DC motor drive board

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About this document

Scope and purpose

This document describes the functionalities of the **EVAL_6EDL7141_TRAP_1SH** 18 V motor drive board for battery-powered brushless DC (BLDC) motor drives with trapezoidal control, used in applications such as cordless power tools. This evaluation board operates with motors that include integrated Hall sensors for rotor position sensing. This solution combines an XMC1400 series microcontroller with the 6EDL7141 three-phase smart driver IC and Infineon OptiMOS™ 6 best-in-class power MOSFETs. The 6EDL7141 reduces system component count and development time-to-market, while at the same time significantly increasing the power density, system performance and peak power pulse capabilities. The graphical user interface (GUI) software tool designed for configuring the 6EDL7141 will also be introduced.

Intended audience

This document addresses the market for cordless power tool and other battery-powered motor drive applications, aimed at designers wishing to provide to a high-performance system solution as well as reduce system costs. It is intended for design engineers, applications engineers, and students.

Infineon components featured

- **BSC007N04LS6** (OptiMOS™ 6 40 V 0.7 mΩ 5x6 PQFN)
- **6EDL7141** three-phase half-bridge MOSFET gate driver and motor control IC
- **XMC1404-VQFN64-200 kB** 32-bit microcontroller with ARM® Cortex®-M0 (XMC™)

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1 Introduction

1.1 Brushless DC motors

BLDC motors are commutated by controlled switching of the inverter instead of using mechanical brushes. Windings are energized in a determined sequence to generate a rotating magnetic field. The rotor permanent magnet attempts to align with the stator field, producing torque and rotary motion. As with mechanical commutation, electronic commutation helps in achieving unidirectional torque similar to a conventional DC machine. In BLDC machines the rotor consists of permanent magnets, while the stator is wound with a specific number of poles. BLDC motors are often produced as outer-rotor type machines. Rotor position can be sensed using digital Hall effect sensors embedded in the stator.

1.2 EVAL_6EDL7141_TRAP_1SH motor drive board

This application note describes Infineon's EVAL_6EDL7141_TRAP_1SH motor drive evaluation board optimized for 18 V battery-powered tools operating with trapezoidal control. The current design considers the electrical driving capabilities for BLDC machines with three Hall sensors used for rotor position detection and speed measurement.

This board utilizes BSC007N04LS6 OptiMOS™ 6 40 V 0.7 mΩ power MOSFETs in 5x6 PQFN, SuperSO8 packages. A detachable heatsink can be mounted to the bottom side of the board to enable improved thermal management and increase power handling capability.

The demo board includes an on-board isolated debugger ready for direct connection to a PC via a USB type A port. The source code is implemented using the Infineon Eclipse-based IDE, DAVE™ (development platform for XMC™ microcontroller; www.infineon.com/DAVE). The control method implements a scalar speed control algorithm based on the BLDC motor using pulse-width modulation (PWM) and three position sensors. The block commutation scheme using Hall sensors is currently the most widely used method for the three-phase BLDC motor control in power tool applications. Block commutation of three-phase BLDC motors is an electronic commutation scheme also known as trapezoidal, six-step or 120-degree commutation. Each phase conducts for 120 electrical degrees during the positive and negative periods of a back-EMF cycle and remains off for the remainder of the cycle. This algorithm requires rotor position information for every 60 degrees, for which the three Hall sensors are used. The firmware is developed using the XMC1400 family (www.infineon.com/XMC).

With this kit, users can evaluate the 6EDL7141-based motor drive system using the control capabilities of the XMC1400 by means of the implemented control algorithm BLDC_SCALAR_HALL_XMC13 with customized features for power tool applications. The board includes a switch for changing the motor direction and a speed control. Configuration and control are also possible through the dedicated GUI,[1] which connects to the demo board through a USB cable interfacing with an on-board programmer/debugger.

The demo kit may also include a QBL4208-61-04-013 BLDC motor with three Hall sensors positioned at 120-degree relative angles, manufactured by Trinamic Motion Control GmbH, depending on the ordering option. This represents the majority case for motor applications with Hall sensors.

[1] Default parameters are shown as bold in section 8.2 "Register Map" of the 6EDL7141 datasheet [1].

Introduction

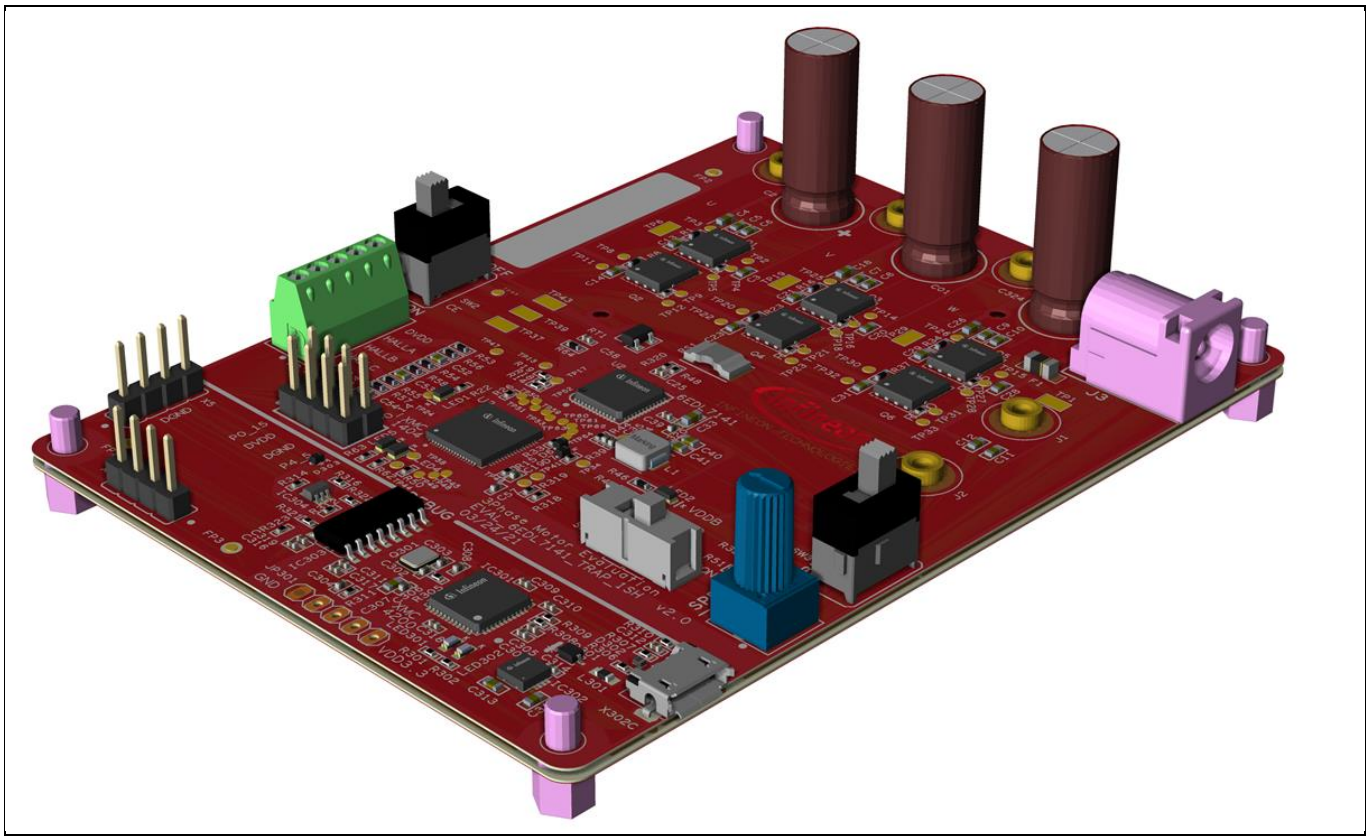

Figure 1 EVAL_6EDL7141_TRAP_1SH demo board

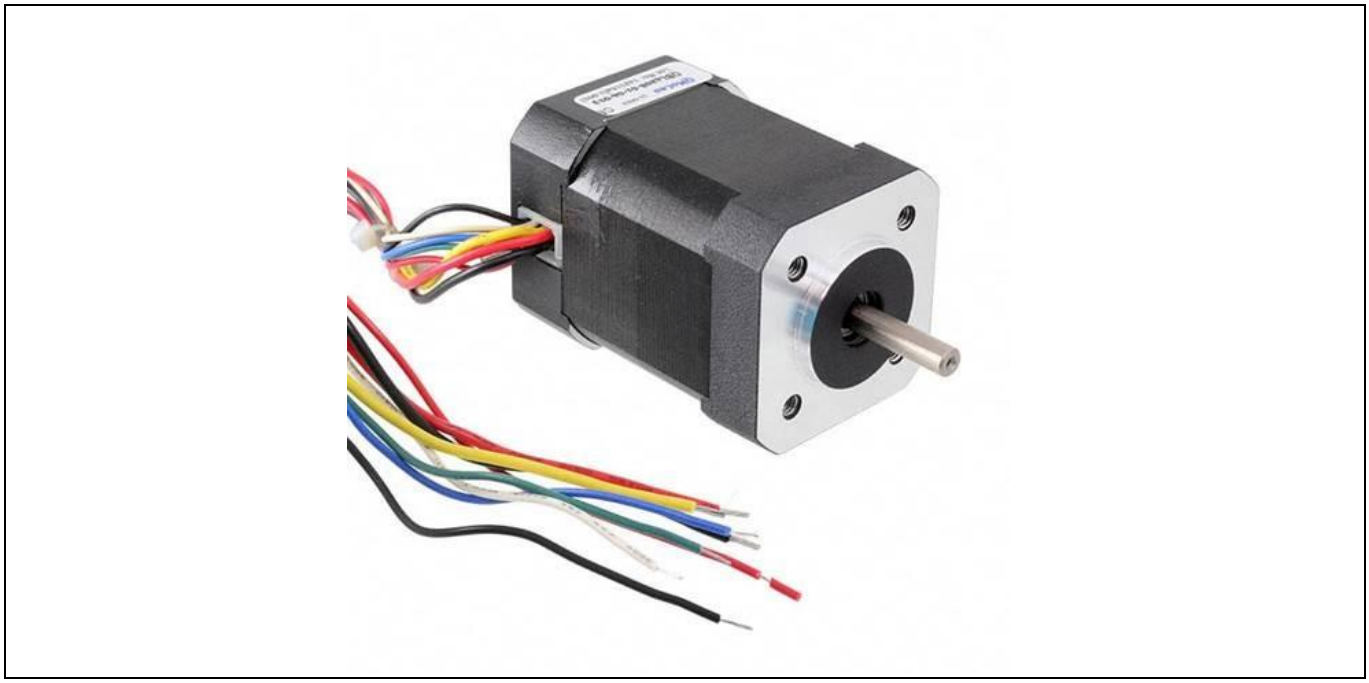

Figure 2 BLDC motor example

Introduction

The EVAL_6EDL7141_TRAP_1SH board system block diagram of the main system elements excluding the on-board debugger is shown below.

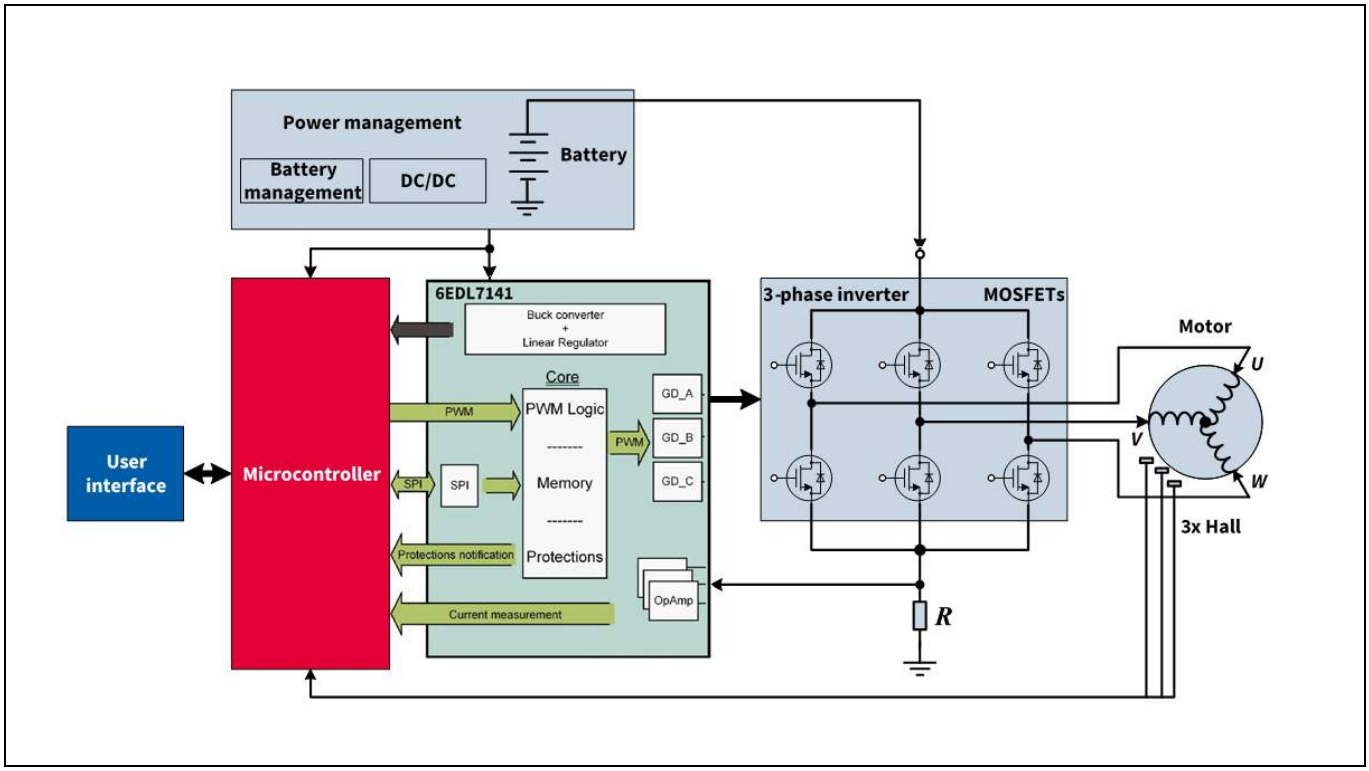

Figure 3 Simplified system block diagram

Rotary velocity plotted against torque measured with 24 V supply voltage for the example motor datasheet is shown below. The blue area represents the region where the motor may be safely used without overheating the stator coils.

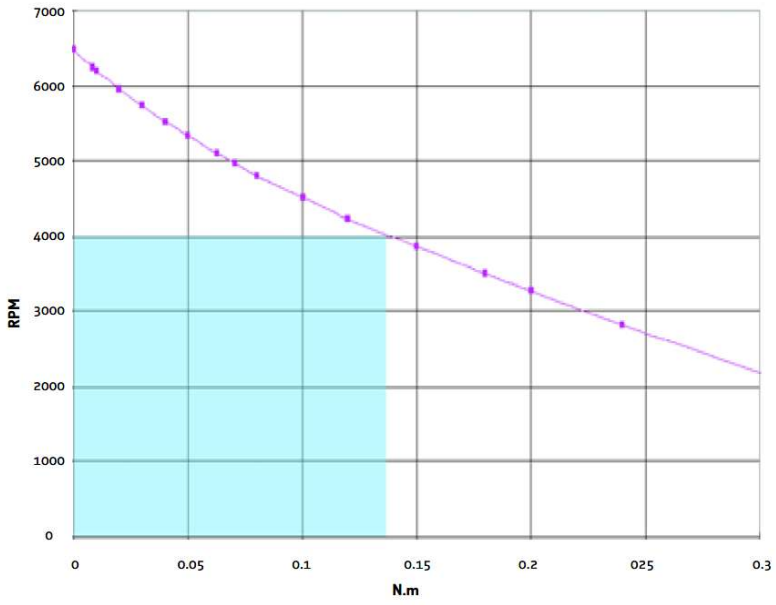

Figure 4 Rotary velocity vs. torque curve for example BLDC motor

1.3 6EDL7141 functional overview

The 6EDL7141 is a three-phase smart gate driver in a 48-pin VQFN package for brushless DC or permanent magnet synchronous motor drive systems. It is designed to operate in conjunction with a microcontroller such as an Infineon XMC1400 series. It consists of a configurable three-phase half-bridge gate driver able to operate in multiple PWM modes with an integrated DC-DC synchronous buck converter and low drop-out linear voltage regulator and also configurable precision current sense amplifiers. There are many configuration options, which can be set via an advanced microcontroller interface in conjunction with a PC-based GUI. Configuration settings can be made permanent by storing in the built-in one-time programmable memory.

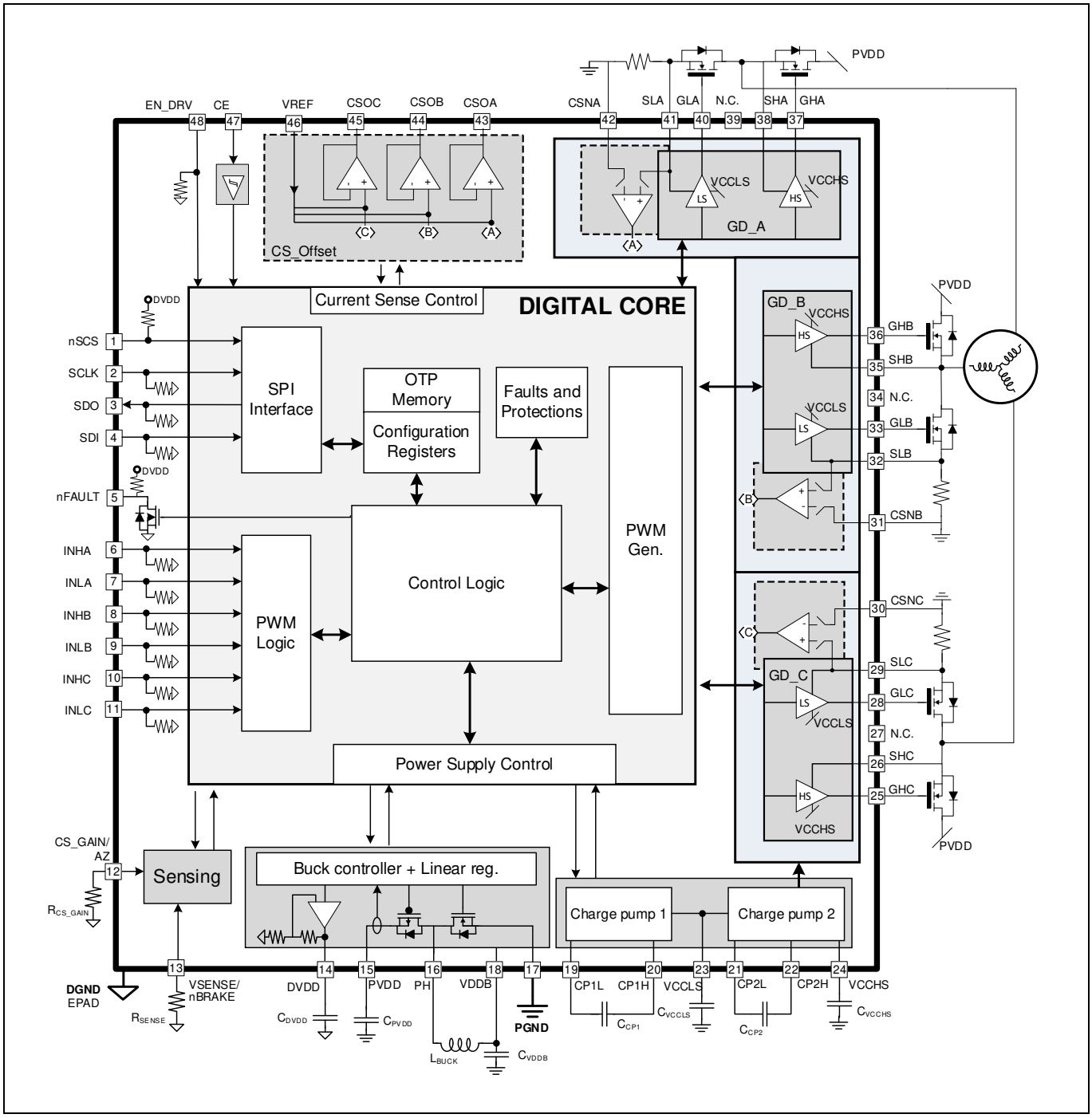

Figure 5 6EDL7141 internal block diagram

Introduction

The microcontroller communicates with the 6EDL7141 via an SPI to enable configuration. PWM signals from the microcontroller provide the gate drive control pulses, which can be decoded in several different ways. The 6EDL7141 provides gate drive pulses to the three-phase inverter low- and high-side MOSFETs. The gate drive output voltages (PVCC) can be selected to several different levels between 7 V and 15 V, and the switch-on and switch-off profiles can be optimized to minimize EMI and switch-off transients by configuration of gate drive current during several time intervals of the switching process. This also eliminates the need for resistor-diode gate drive networks. Protection signals and phase current measurements are available from the 6EDL7141 to connect to digital and analog microcontroller inputs.

The 6EDL7141 integrates three precision current sense amplifiers, which can be used to measure the current in the inverter via shunt resistors. Single-, double- or triple-shunt measurements are supported. Each current sense amplifier can be enabled individually. The gain and offset are configured internally and can be set via the user interface. An additional output buffer allows adding a variable offset voltage to the sense amplifier output, which can be set to four different values either by programming the internally generated level or by applying an external voltage at the VREF input pin so that negative current in current shunts can also be measured.

A positive overcurrent comparator detects an overcurrent condition on a motor winding for a positive shunt voltage. This comparator can be used to apply PWM cycle-by-cycle pulse truncation, terminating the gate drive to limit the maximum motor current. An additional negative overcurrent comparator is also used for detecting the overcurrent condition on motor winding for negative shunt currents. A built-in DAC is used for programming the thresholds of the overcurrent comparators.

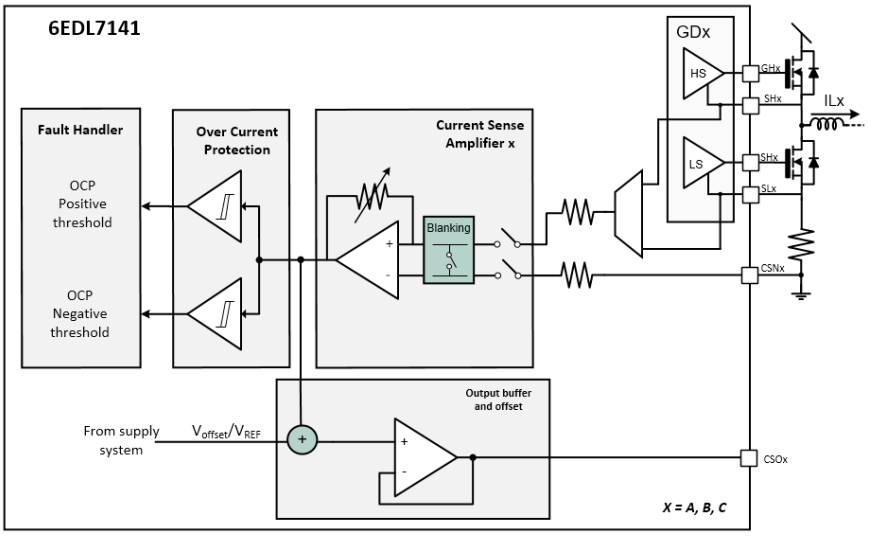

Figure 6 6EDL7141 current sense amplifiers and comparators

The 6EDL7141 also includes a complete power system infrastructure based on the synchronous buck regulator. This efficiently converts the battery voltage to an internal voltage, which is set to 6.5 V, 7 V or 8 V depending on the gate drive voltage setting, able to supply up to 300 mA. The only external components required are the inductor and capacitor. The buck regulator supplies the linear regulator, which can provide a noise-free 3.3 V or 5 V supply for the digital circuitry and microcontroller, set by the value of the resistor during start-up.

Integrated low-side and high-side charge pumps supplied from the buck regulator provide the gate driver supply voltages, which enable duty cycles up to 100 percent. Each charge pump uses an external switched capacitor (CP1 for the low-side and CP2 for the high-side) to transfer charge from the buck converter output to the gate driver bias supplies: VCCLS and VCCHS. VCCLS is referenced to the system zero-volt rail and VCCHS is referenced to the system positive supply rail. Unlike conventional half-bridge drivers, the 6EDL7141 includes an

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advanced high-side driver scheme that enables VCCHS to able to supply the switch-on voltage and current to the high-side gate drivers for all three phases without the need for separate floating supplies for each phase. The values of the switched capacitors and bias supply capacitors, CVCCLS and CVCCHS, need to be selected according to the datasheet instructions for the charge pumps to operate correctly. The charge pump clock frequency is selectable from at 195.3 kHz, 390.6 kHz, 781.3 kHz, or 1.56 MHz with optional frequency modulation to reduce EMI.

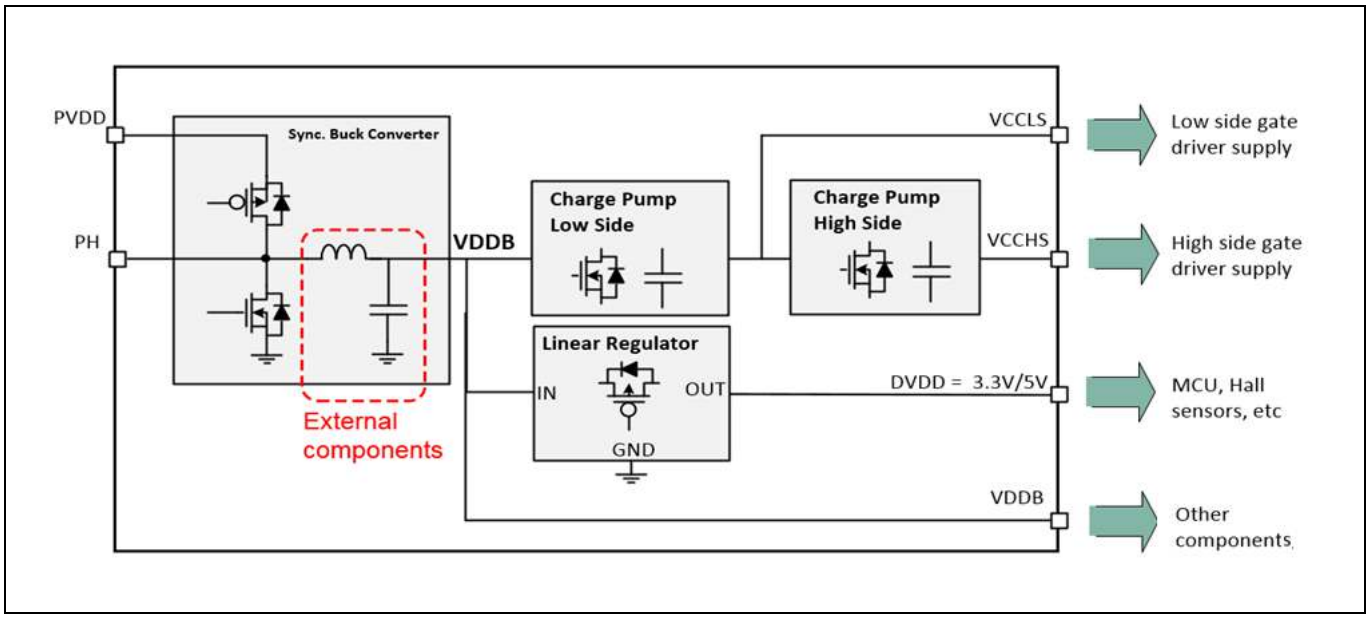

Figure 7 6EDL7141 integrated power supplies

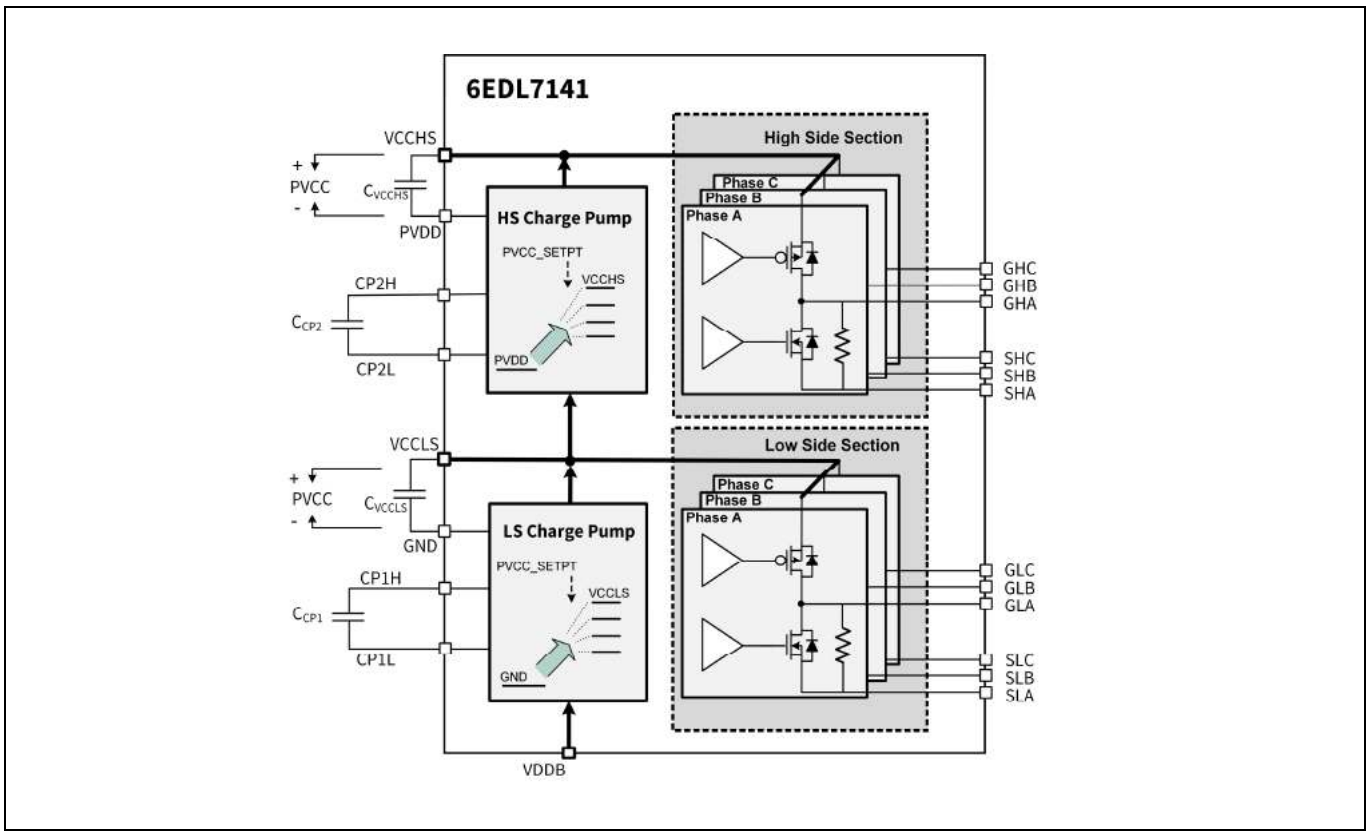

Figure 8 6EDL7141 integrated charge pumps and gate drivers

Introduction

The 6EDL7141 supports several PWM modes, which can be selected. These include:

- 6PWM
- 3PWM
- 1PWM and commutation pattern
- 1PWM with Hall sensor commutation
- 1PWM mode with Hall sensor commutation and alternating recirculation.

This allows the designer flexibility in terms of microcontroller selection to cover a variety of different applications. In one and three PWM modes the dead-time is configurable in the 6EDL7141.

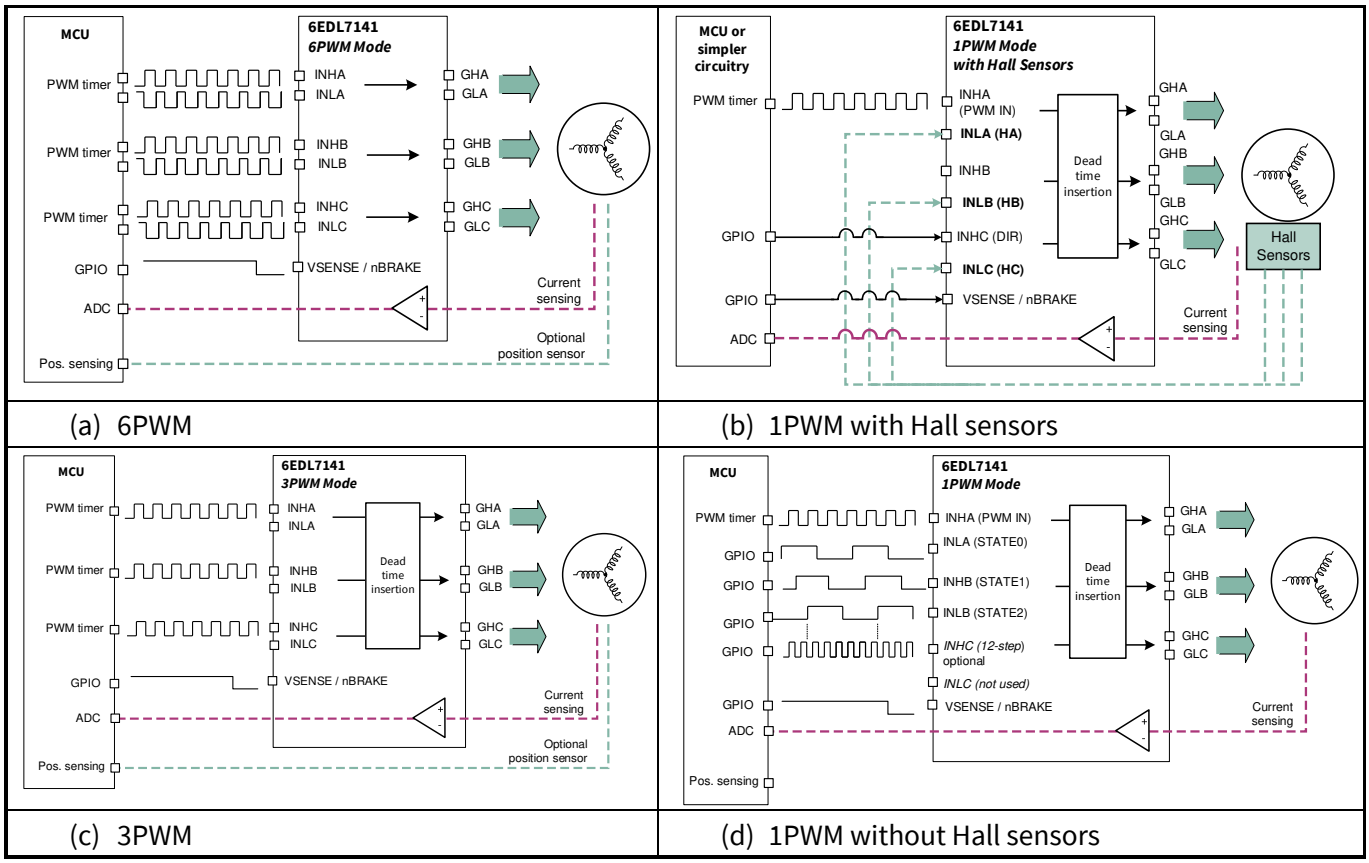

Figure 9 PWM switching modes supported by the 6EDL7141

The EVAL_6EDL7141_TRAP_1SH evaluation board operates using the 6PWM mode with the firmware supplied.

The 6EDL7141 also incorporates several protection functions, including:

- Overcurrent protection for the internal power supplies and inverter phases
- Undervoltage lock-out for the input bus voltage and digital supply voltage
- Overtemperature detection, warning, and shutdown
- A configurable watchdog timer
- Locked rotor detection based on Hall sensor inputs and memory fault detection.

2 Specifications

Input and output in normal operation:

- DC input voltage 12 V to 24 V, nominal 18 V
- Maximum input current 30 A
- Output voltage three-phase trapezoidal (six-stage) control
- Maximum output current per phase 25 A_{RMS}
- Maximum output continuous power 500 W

Control scheme:

- Trapezoidal/6-step/block commutation with Hall sensors
- Switching frequency 20 kHz
- Single current shunt

Protection features:

- Input fuse
- Input reverse polarity
- Output overcurrent
- Thermal shutdown

Maximum component temperature:

In an ambient temperature of 30°C, the maximum allowed component temperatures are as follows:

- Resistors less than 100°C
- Ceramic capacitors, film capacitors and electrolytic capacitors less than 100°C
- MOSFET transistors and diodes less than 100°C
- ICs less than 100°C

Dimensions of evaluation board:

Maximum width 3.0 inches/76.2 mm, maximum length 4.0 inches/101.6 mm.

Attention: ***The board should be tested only by qualified engineers and technicians.***

3 Schematics

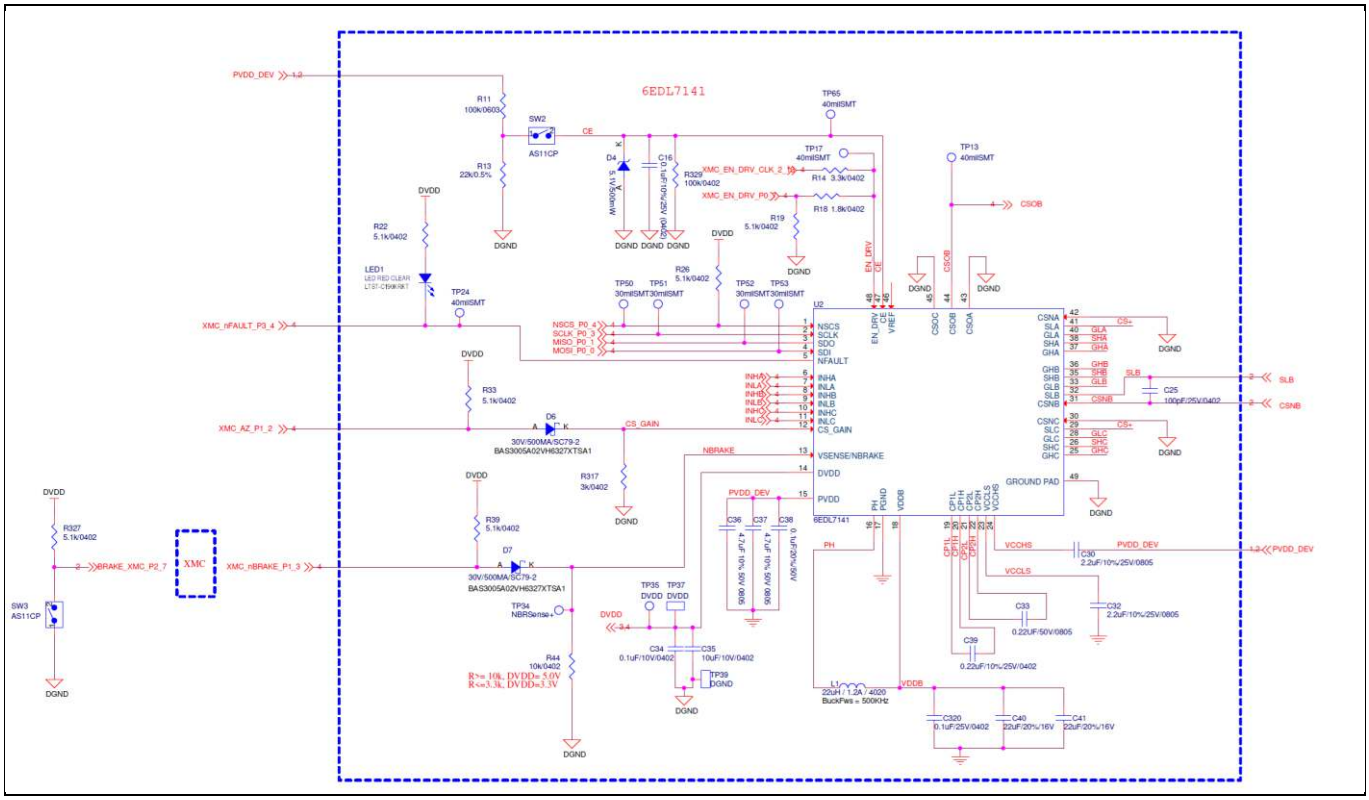

Figure 10 EVAL_6EDL7141_TRAP_1SH schematic – 6EDL7141 gate driver section

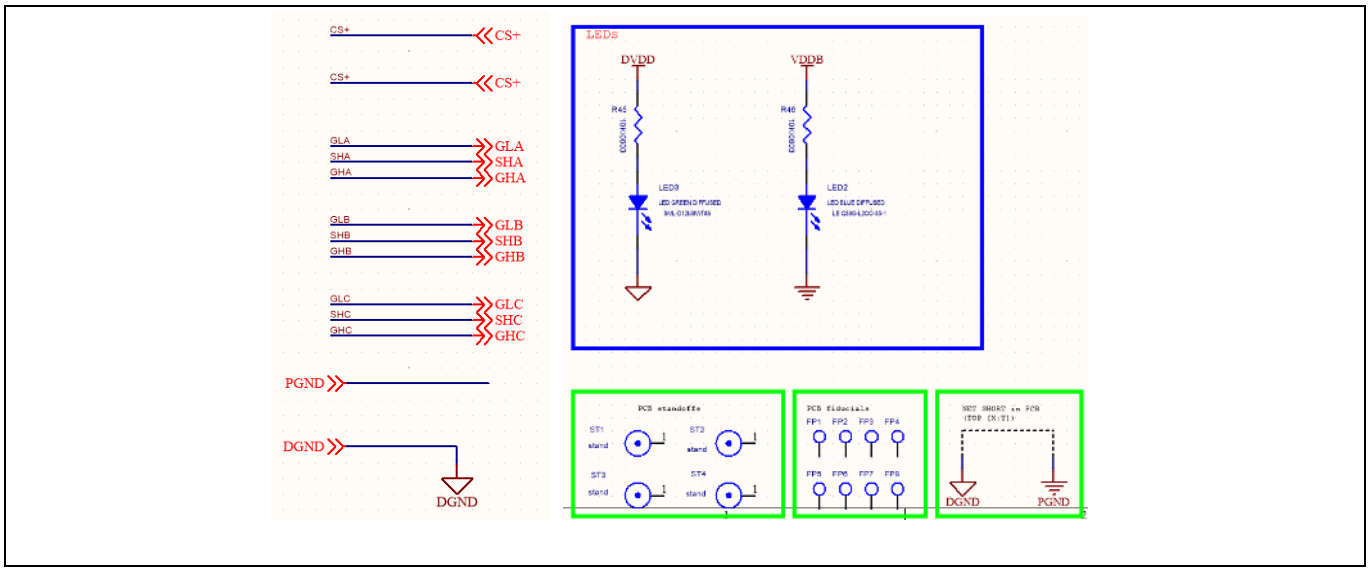

Figure 11 EVAL_6EDL7141_TRAP_1SH schematic – power LED indicators and connections

Schematics

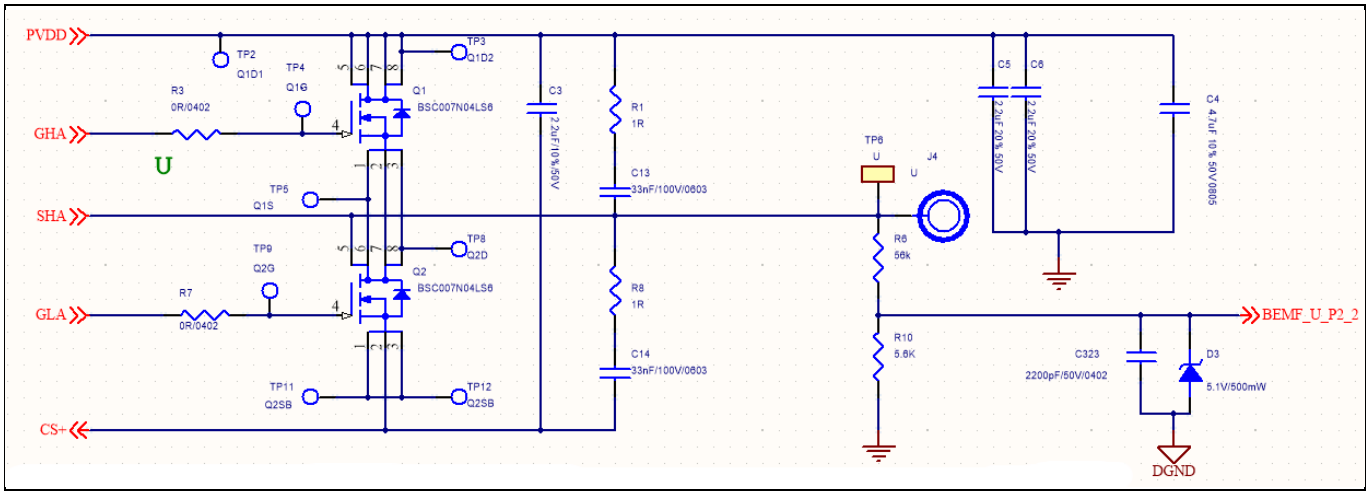

Figure 12 EVAL_6EDL7141_TRAP_1SH schematic – power stage, phase “U”

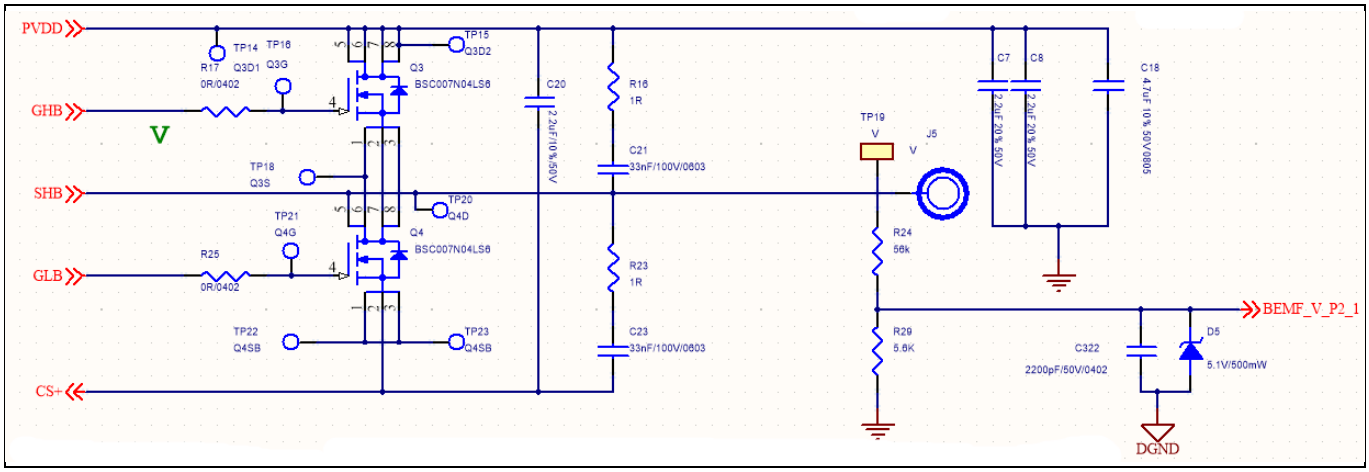

Figure 13 EVAL_6EDL7141_TRAP_1SH schematic – power stage, phase “V”

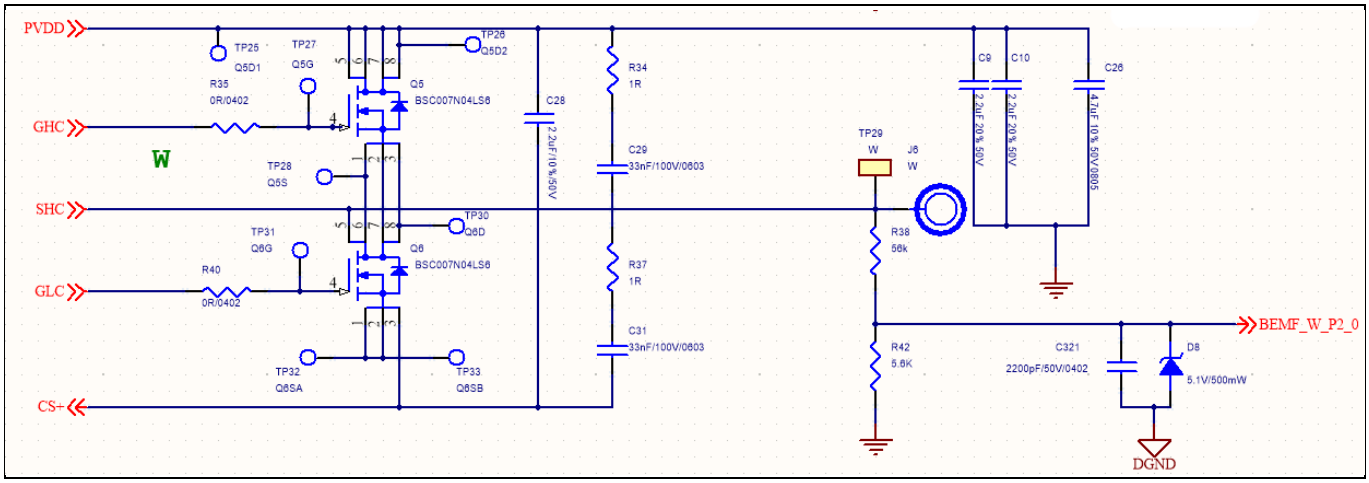

Figure 14 EVAL_6EDL7141_TRAP_1SH schematic – power stage, phase “W”

Schematics

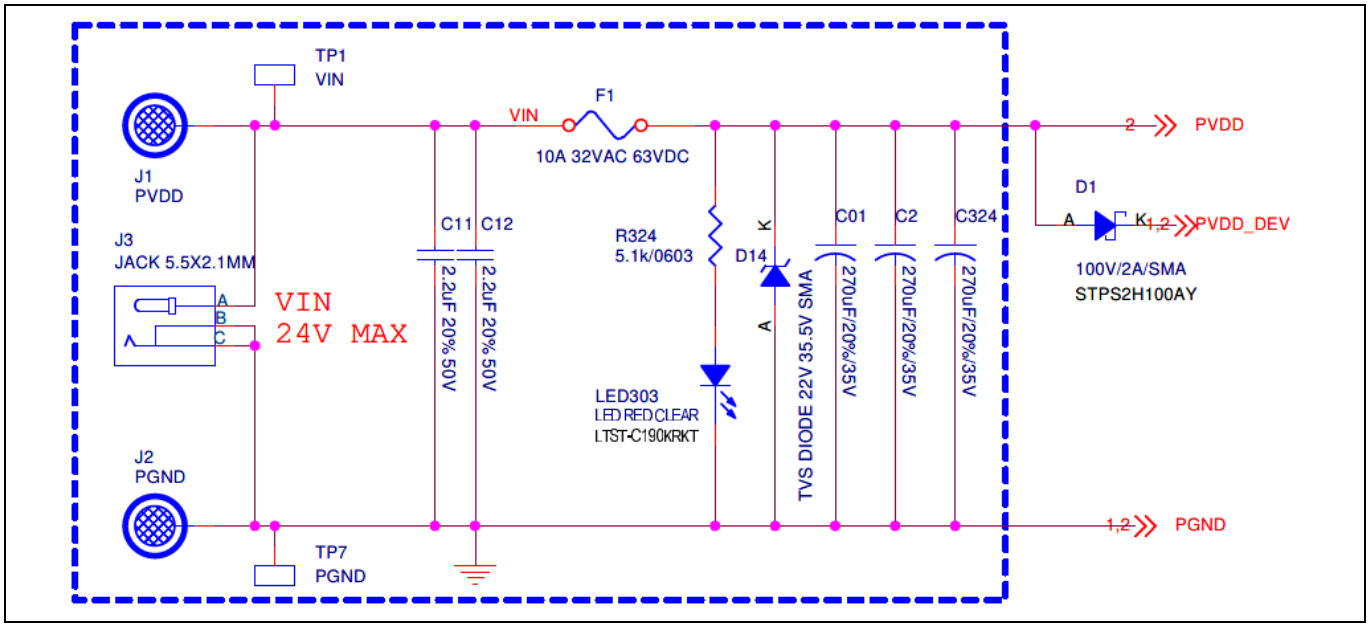

Figure 15 EVAL_6EDL7141_TRAP_1SH schematic – DC input

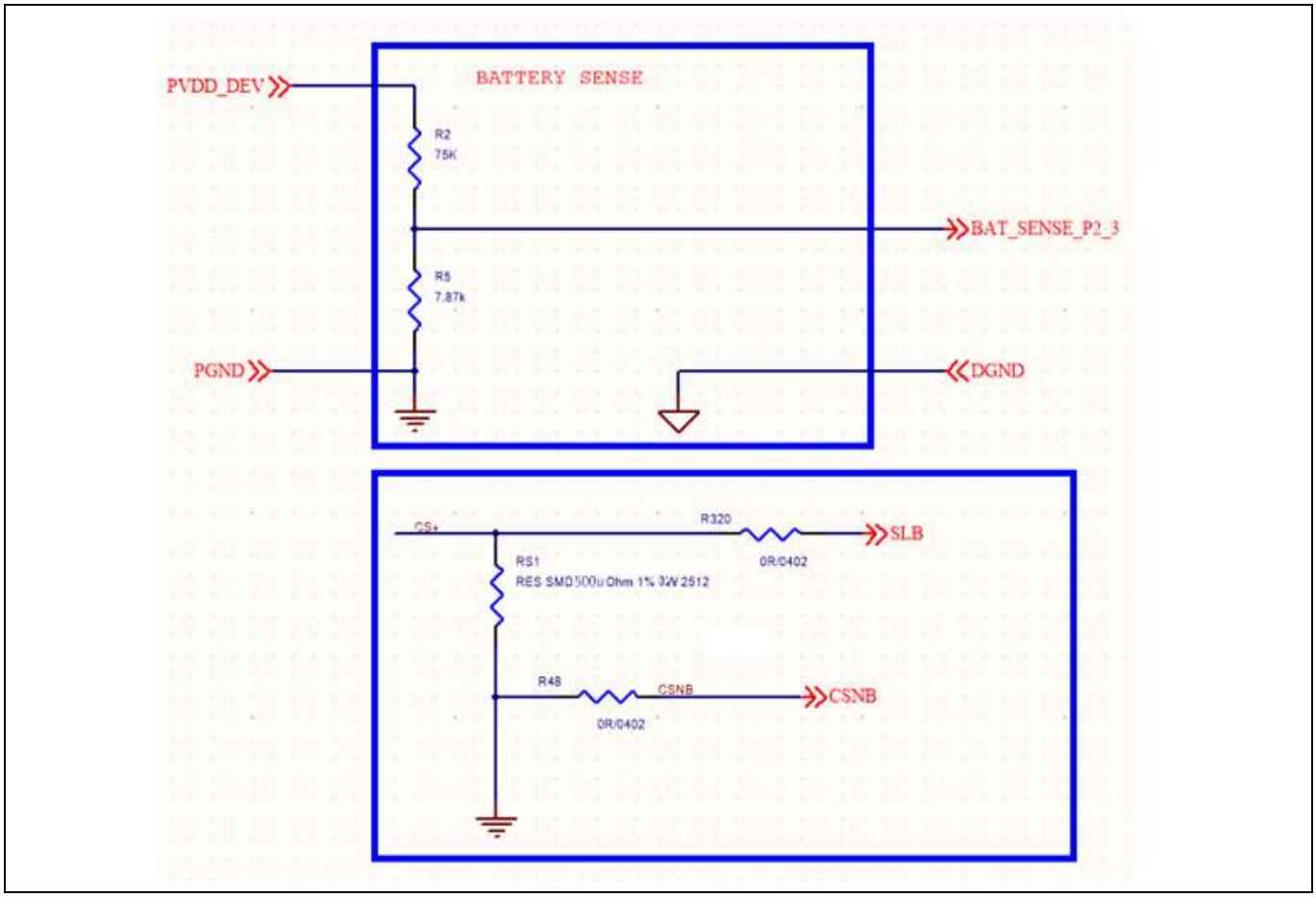

Figure 16 EVAL_6EDL7141_TRAP_1SH schematic – voltage and current sensing

Schematics

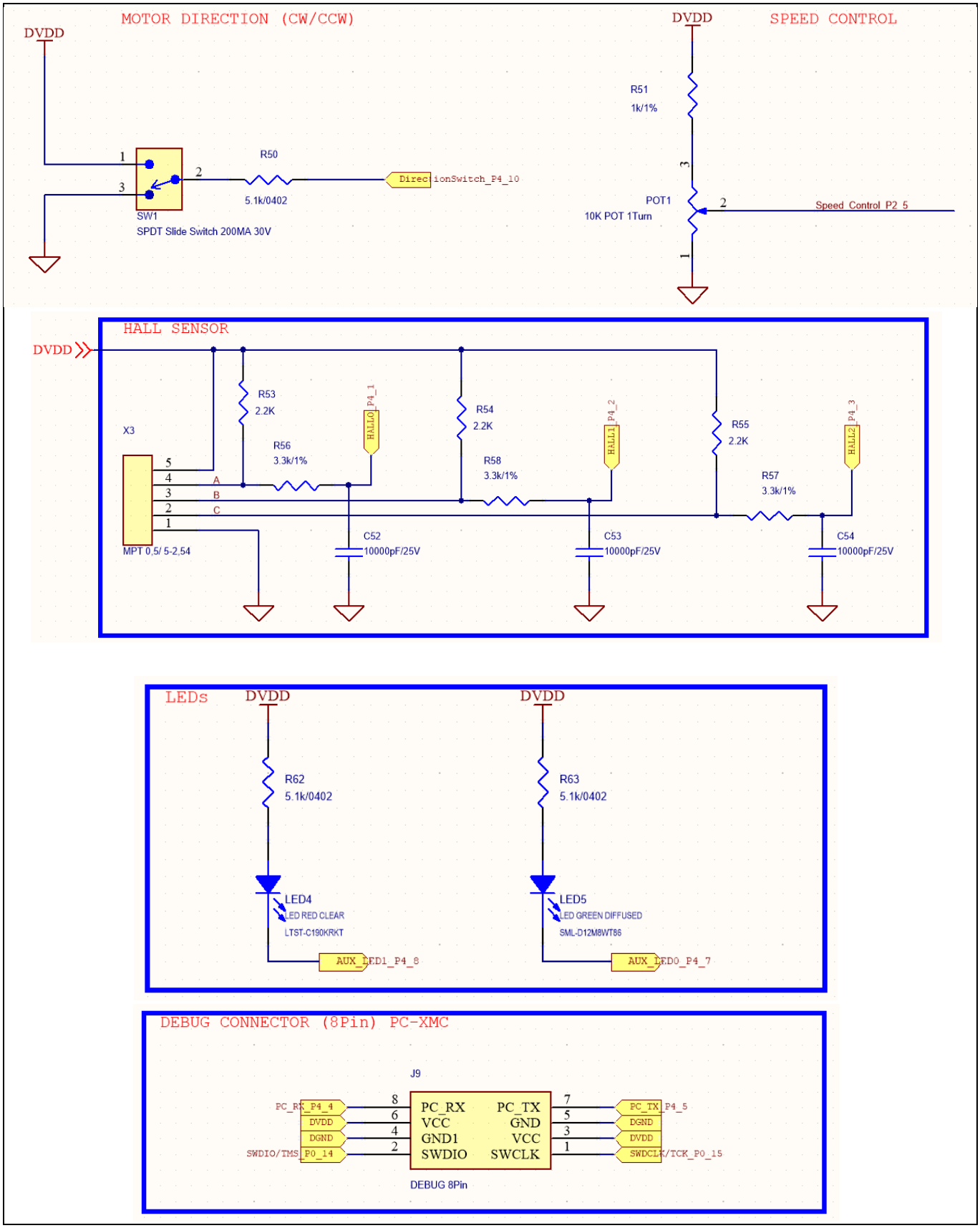

Figure 17 **EVAL_6EDL7141_TRAP_1SH schematic – direction switch, speed control, Hall sensor inputs, LED indicators and external debugger**

Schematics

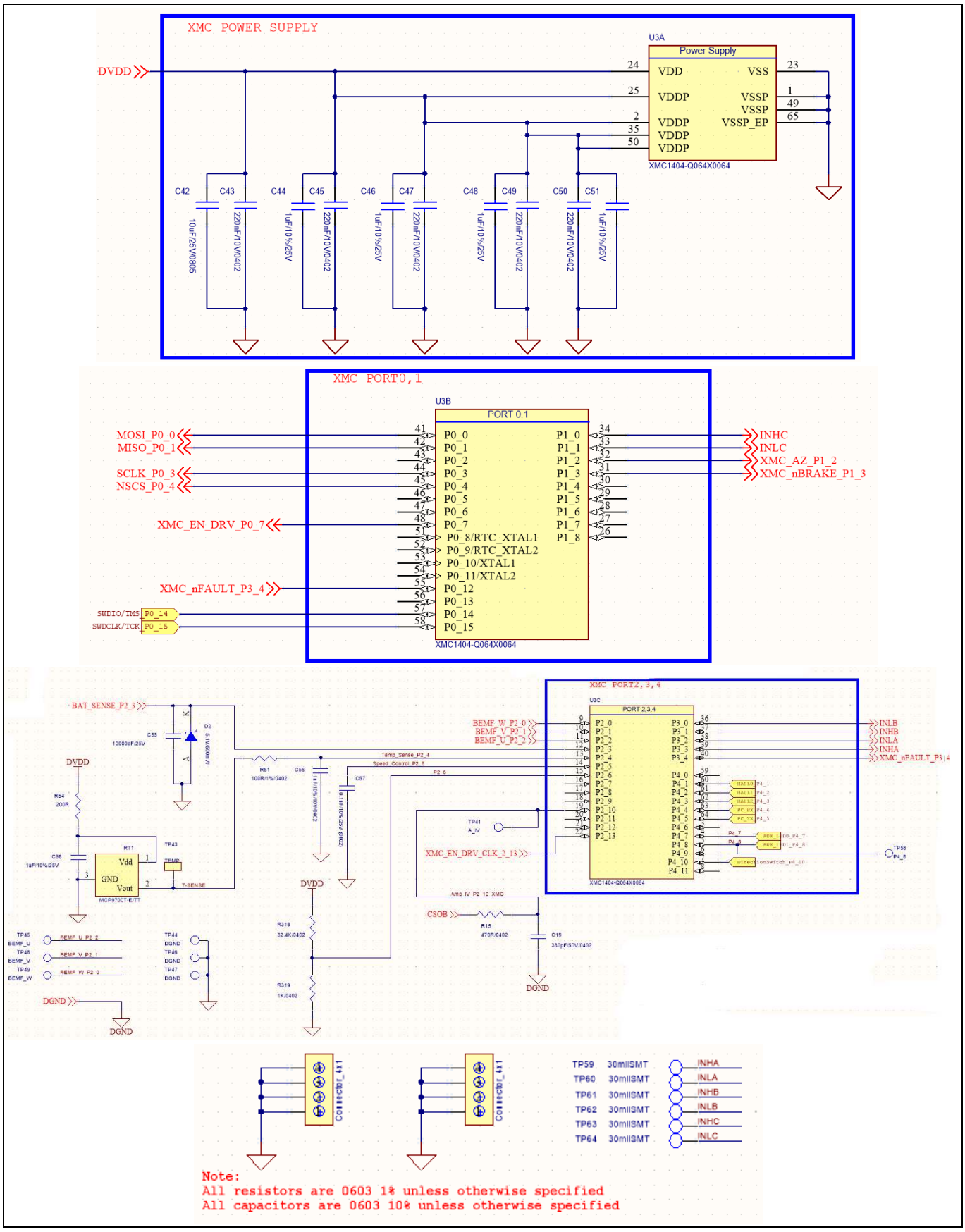

Figure 18 EVAL_6EDL7141_TRAP_1SH schematic – XMC1404 main controller power supply and connections

Schematics

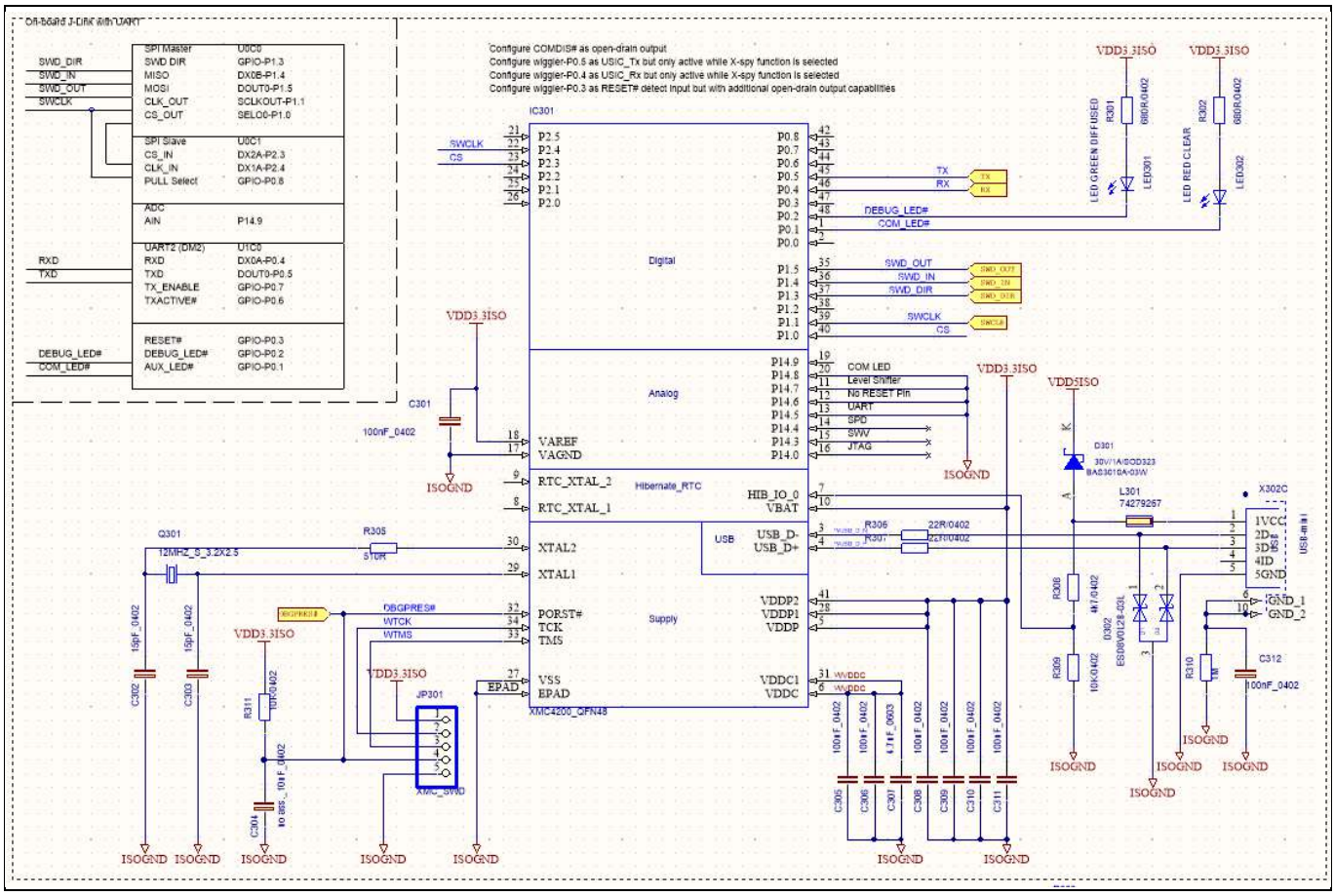

Figure 19 EVAL_6EDL7141_TRAP_1SH schematic – debugger controller section

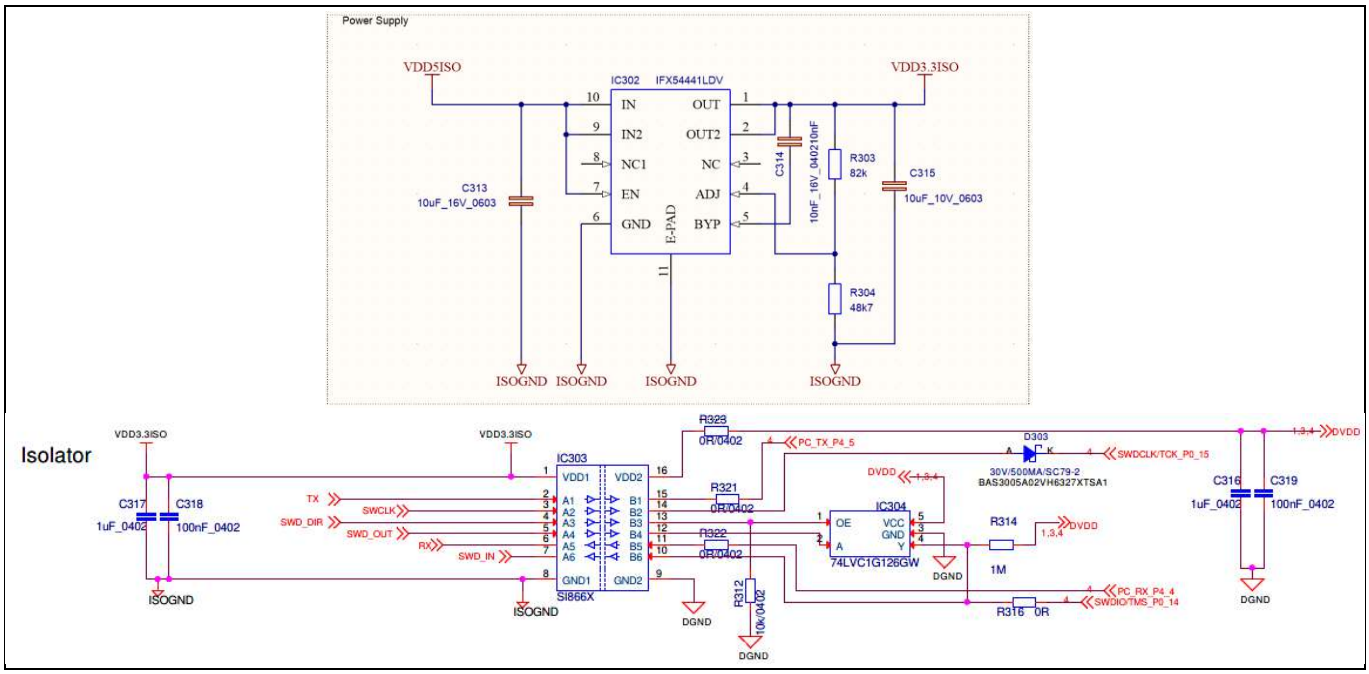

Figure 20 EVAL_6EDL7141_TRAP_1SH schematic – debugger power supply and isolators

4 Hardware functional description

The main hardware elements for block commutation with Hall sensors are the three-phase inverter power stage, the 6EDL7141 three-phase smart gate driver and the XMC1400 series 32-bit microcontroller with ARM® Cortex®-M0.

4.1 Three-phase inverter stage

The three-phase inverter switching devices are BSC007N04LS6 (OptiMOS™ 6 40 V 0.7 mΩ 5x6 PQFN) power MOSFETs optimized for battery-powered power tool applications. The demo board is able to support the following PWM schemes, which may be selected by firmware. In each case the PWM operates at a fixed frequency and the duty cycle is adjusted to control the average voltage applied to each stator winding. The winding inductances remove most of the PWM frequency component, leaving a small amount of ripple.

Table 1 Supported PWM schemes

Modulation scheme	Description
Low-side modulation	Modulation is applied to the low-side switches
High-side modulation	Modulation is applied to the high-side switches
High-side modulation with synchronous rectification	Modulation is applied to the high-side switches with a complementary pulse to the low-side switches.

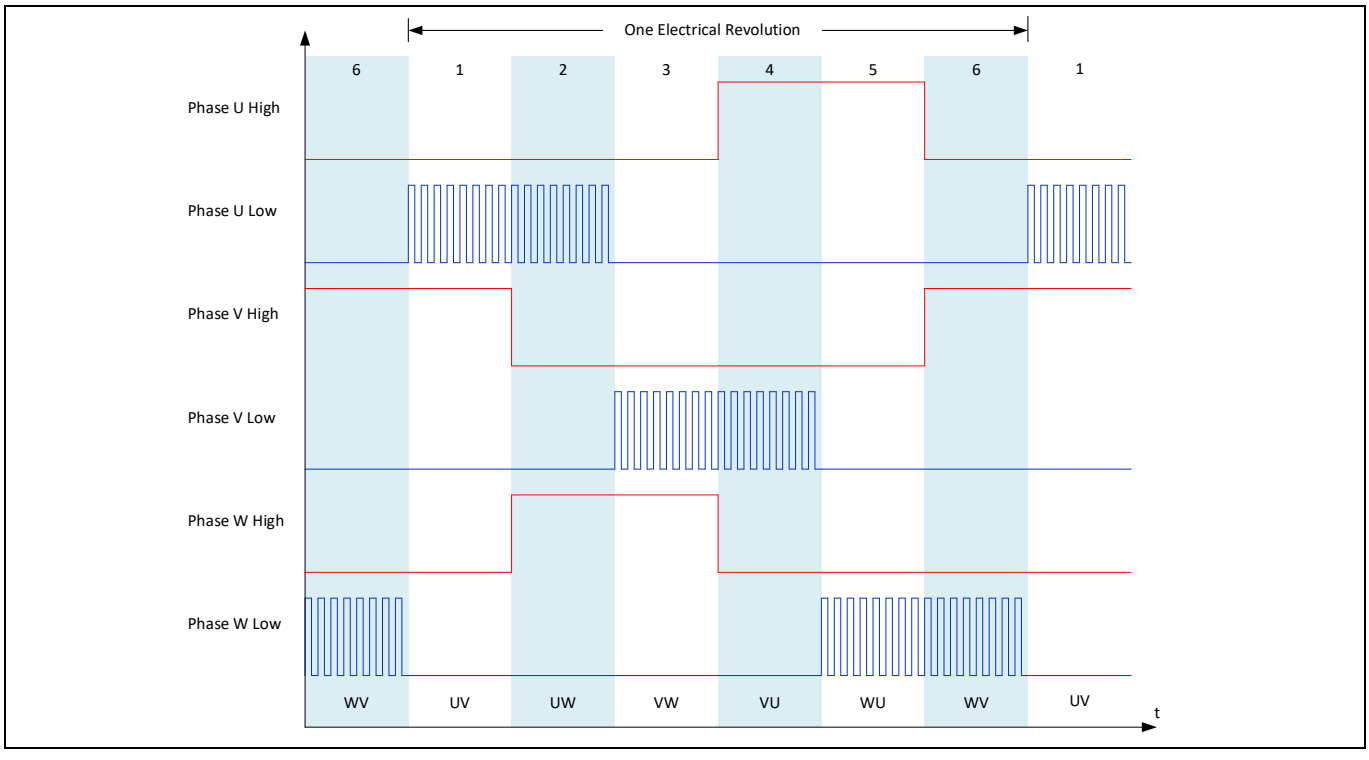

Figure 21 Low-side modulation

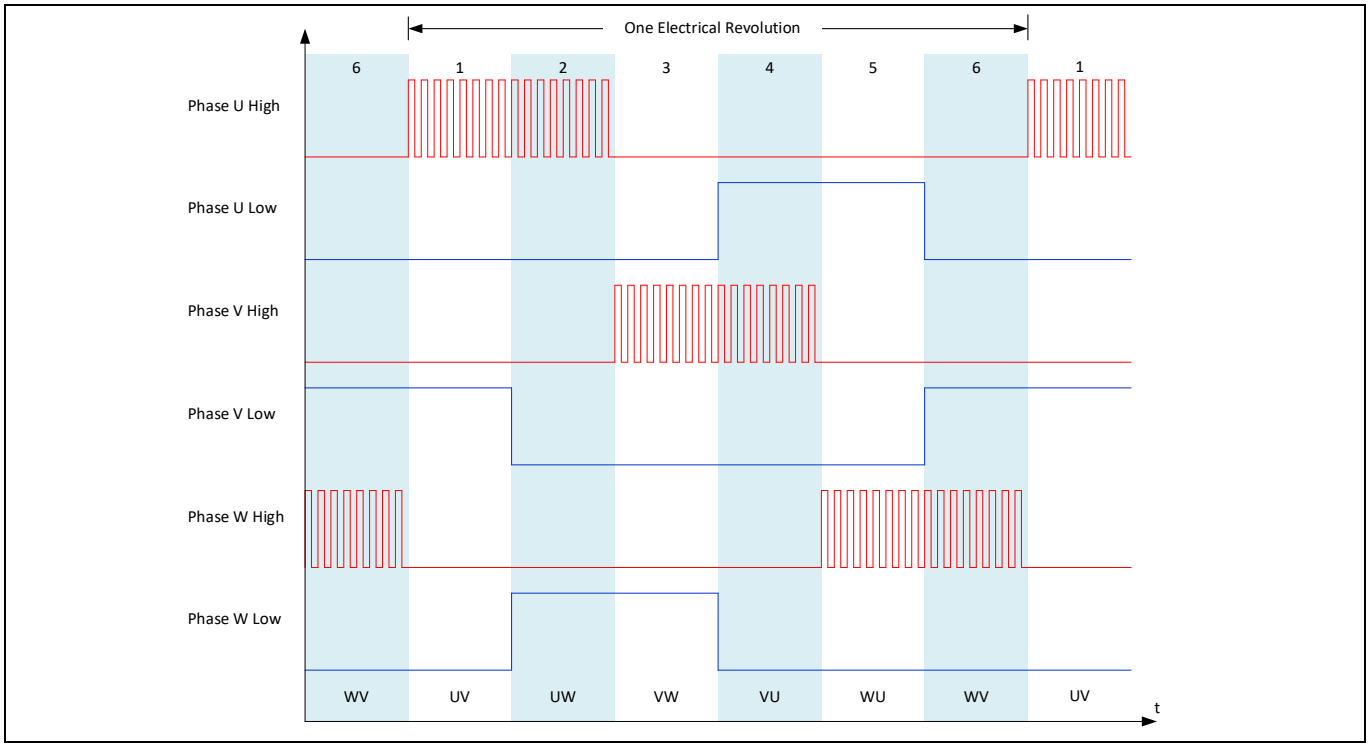

Figure 22 High-side modulation

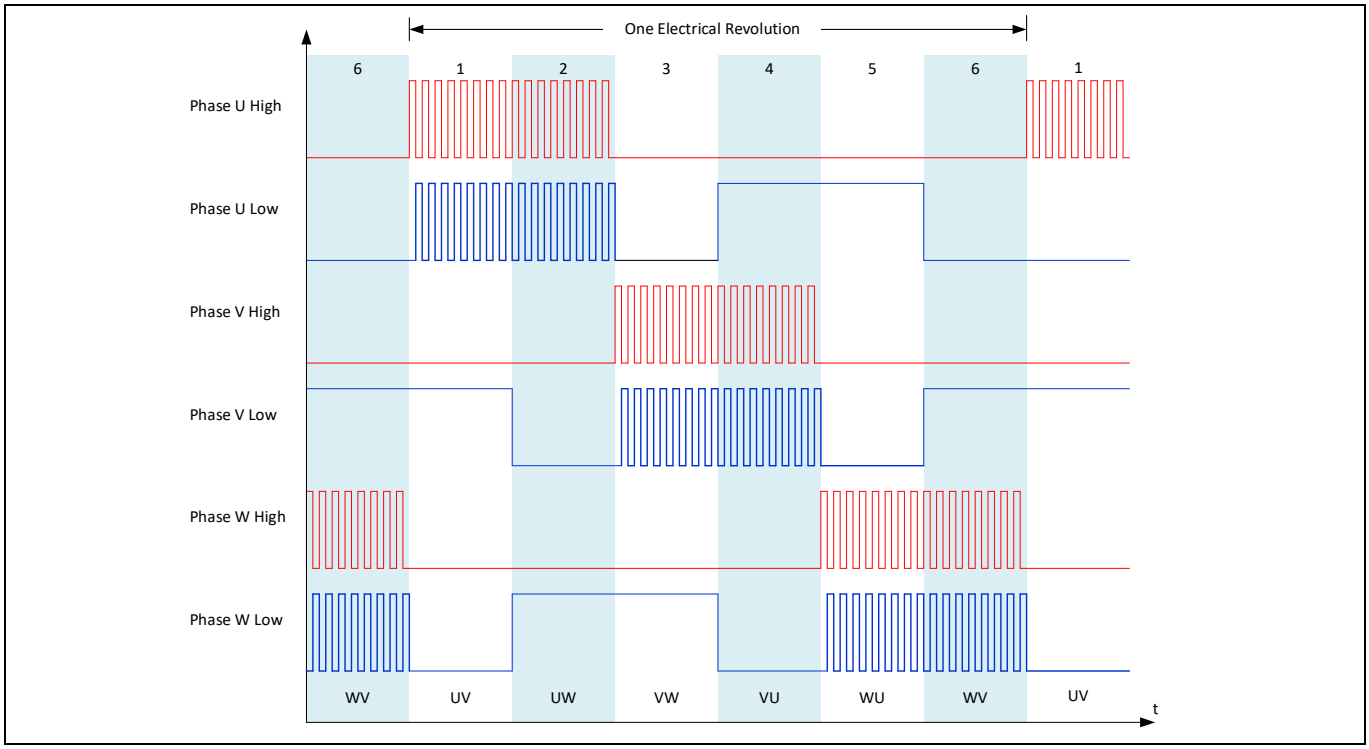

Figure 23 High-side modulation with synchronous rectification

During high-side modulation with synchronous rectification the switching dead-time is inserted between the rising and falling edges of the PWM signals to prevent the high-side and low-side MOSFETs of each inverter phase from being on at the same time during switching transitions (shoot-through condition). The body diode of each MOSFET conducts current when the MOSFET is off.

Hardware functional description

The 6EDL7141_BLDC_1SH demo board allows optional heatsinks to be attached under the board to extract heat from the MOSFETs, allowing higher power drive to the motor without overheating.

Typically block commutation with Hall sensors uses a single-shunt resistor (RS1 in this case) to sense the current of the DC-link. This is the combined current of each phase sense at the low-side.

4.2 6EDL7141 smart gate driver

Optimized gate drive pulses to the high- and low-side MOSFETs in each phase are provided by the 6EDL7141 smart gate driver (U2). Logic-level switching PWM pulses are supplied to the 6EDL7141 from the XMC1404 microcontroller (U3). The high- and low-side gate drivers allow operation over the full duty-cycle range up to 100 percent. The gate drive voltages can be set to different levels, including 7 V, 10 V, 12 V and 15 V. One benefit of the charge pumps is that voltage levels can be maintained even if the battery voltage drops to a lower level, allowing standard gate-level MOSFETs to be used.

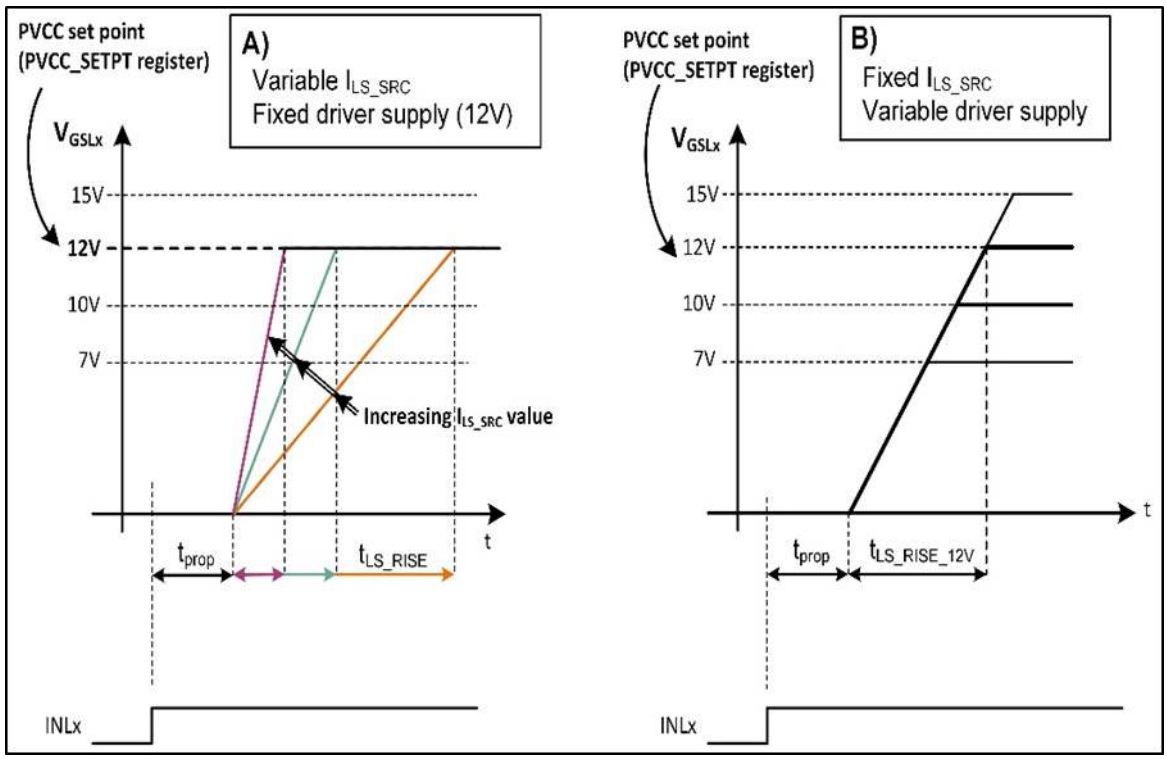

Figure 24 6EDL7141 gate drive control

Control of the drain-source rise and fall times is one of the most important parameters for optimizing drive systems, affecting critical factors such as switching losses, dead-time optimization and drain voltage ringing that can lead to possible MOSFET avalanching. Correct configuration of the gate drive also helps to minimize EMI emissions. The 6EDL7141 is capable of controlling the slew rate of the driving signal to control the rise and fall slew rates of the drain-to-source voltage by adjusting the gate drive sink and source currents during different time segments during the switch-on and switch-off processes. This permits the designer to eliminate diode resistor networks commonly used in gate drive circuits. In most cases, gate resistors can be removed altogether, reducing component count and at the same time simplifying and allowing further optimization of the circuit layout.

4.2.1 Configuration of the gate driver

4.2.1.1 Gate drive current and timing

Using the GUI tool, the designer can configure the gate driver current and timings with the following parameters via SPI accessible registers:

Table 2 Gate drive parameters[1]

Parameter	Description	Minimum	Maximum
I_{HS_SRC}	Source current value for switching on high-side MOSFETs	10 mA	1.5 A
I_{HS_SINK}	Sink current value for switching off high-side MOSFETs	10 mA	1.5 A
I_{LS_SRC}	Current value for switching on low-side MOSFETs	10 mA	1.5 A
I_{LS_SINK}	Current value for switching off low-side MOSFETs	10 mA	1.5 A
I_{PRE_SRC}	Pre-charge current value for switching on both high- and low-side	10 mA	1.5 A
I_{PRE_SNK}	Pre-charge current value for switching off both high- and low-side	10 mA	1.5 A
T_{DRIVE1}	Amount of time that I_{PRE_SRC} is applied. Shared configuration between high and low.	0 ns	2.59 µs
T_{DRIVE2}	Amount of time that I_{HS_SRC} and I_{LS_SRC} are applied. Shared configuration between high-side and low-side drivers.	0 ns	2.55 µs
T_{DRIVE3}	Amount of time that I_{PRE_SNK} is applied. Shared configuration between high- and low-side drivers.	0 ns	2.59 µs
T_{DRIVE4}	Amount of time that I_{HS_SINK} and I_{LS_SINK} and are applied. Shared configuration between high-side and low-side drivers.	0 ns	2.55 µs

The gate driver implementation is illustrated in **Figure 25**. The EVAL_6EDL_7141_TRAP_1SH evaluation board utilizes the 6PWM mode, in which the microcontroller inserts a specific dead-time between the INHx and INLx signals generated by its PWM modules. This driving scheme is also applicable to other PWM modes. Propagation delays are not shown for simplification of the diagram.
When the input signal from the microcontroller transitions from low to high, the gate driver switch-on sequence is triggered. The gate drive output first applies a constant current defined by the user-programmable value I_{PRE_SRC} for a time defined by T_{DRIVE1}, at the end of which the MOSFET gate voltage should have reached the threshold voltage $V_{GS(TH)}$. The next period of the gate switch-on sequence is defined by the parameter T_{DRIVE2}, which begins immediately after the completion of T_{DRIVE1}. The current applied during T_{DRIVE2} determines both dI_D/dt and dV_{DS}/dt of the MOSFETs, as it will supply the current to charge the Q_{SW} of the MOSFET being driven. In the three-phase motor drive configuration, each half-bridge operates in continuous mode with hard switch-on of the high-side. Hard switch-on of the low-side may also occur if the dead-time is not long enough for the snubber capacitor to charge due to the phase current. Once the T_{DRIVE2} period has elapsed, the gate driver applies full current (1.5 A) to ensure fastest full turn-on of the MOSFET by supplying the remaining charge required to raise V_{GS} to the programmed PVCC value ($Q_{OD} = Q_G - Q_{SW} - Q_{G(TH)}$).
A similar process takes place during the switch-off of the MOSFET, in which the parameters T_{DRIVE3} and T_{DRIVE4} determine the periods for which the programmed discharge currents are applied.

Note: When adjusting the slew rate to a desired value it is necessary to set the dead-time to a suitable value greater than the sum of T_{DRIVE1} and T_{DRIVE2} for the low to high transition and T_{DRIVE3} and T_{DRIVE4} for the high to low transition, or whichever is greater if both dead-times are equal.

[1] Available current and time delay values are listed in section 8 “Register Map” of the 6EDL7141 datasheet [1].

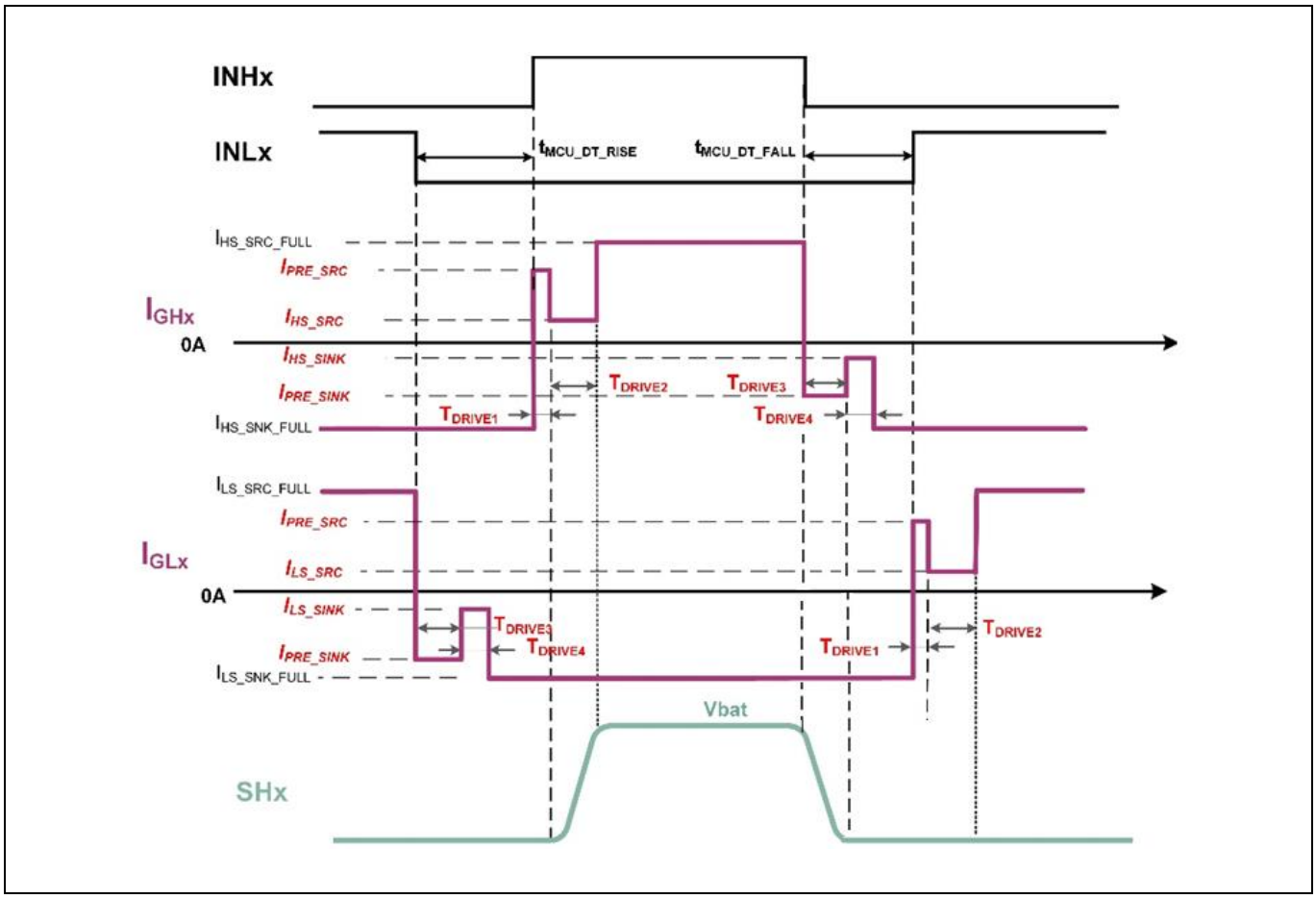

Figure 25 6EDL7141 slew rate control for half-bridge

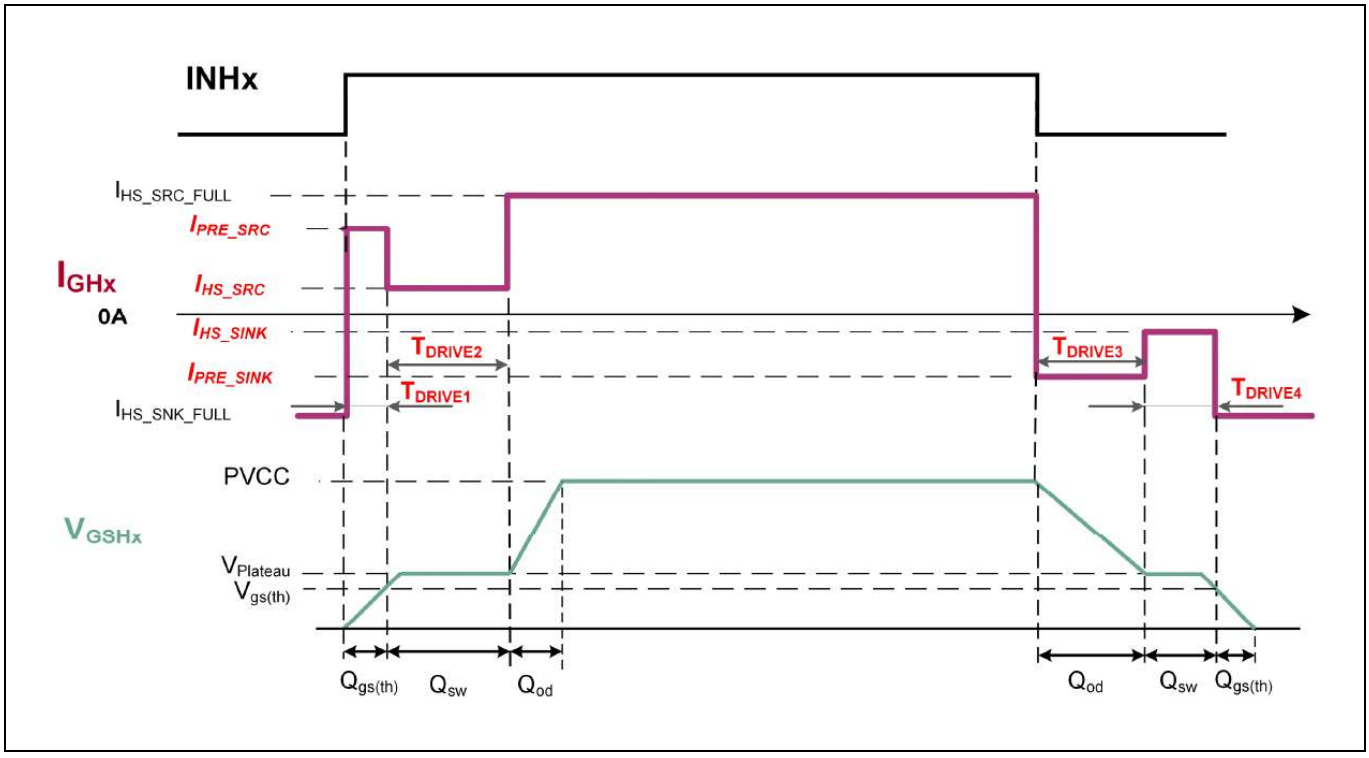

Figure 26 6EDL7141 gate drive profile

Figure 26 shows in detail the V_{GS} charging and discharging transitions for a high-side MOSFET in one of the inverter phases during a typical hard-switched transition. The different charging and discharging phases of the MOSFET switch-on and switch-off are illustrated above. Thanks to the flexible timing structure provided by the 6EDL7141 gate driver with its high $T_{DRIVE(X)}$ resolution and ability to set the current during each interval, the designer is able to configure and optimize the switch-on and switch-off operations without the need for any external gate drive components.

During hard-switching, the controlled gate drive currents enable adjustment of the slew rate dV_{DS}/dt, by controlling the gate drive current during the periods T_{DRIVE2} and T_{DRIVE4} during which the charge Q_{SW} is injected or extracted from the gate as V_{DS} transitions. Higher currents can be used for fast charging and discharging of $Q_{GS(TH)}$ and Q_{OD}, since neither dI_D/dt nor dV_{DS}/dt are affected during these periods.

The pre-charge current can be selected from seventeen available values. Sixteen are defined by $I_{PRE\_SRC/SNK}$ with an additional 1.5 A option, which is the maximum current capability of the gate driver. In cases where larger MOSFETs with relatively high gate charge are used, $Q_{G(TH)}$ during turn-on or Q_{OD} during turn-off may benefit from using the full gate driver capability. Full strength during the pre-charge may be selected via the GUI. In cases where $Q_{G(TH)}$ is too small to apply a larger current than the one used for slew rate control the user can set T_{DRIVE1} to value zero, which results in the gate driver going immediately to the beginning of the T_{DRIVE2} period with its corresponding gate current setting. This enables optimization for both large and small MOSFETs covering different technologies such as OptiMOS™ or StrongIRFET™. Similarly, T_{DRIVE2}, T_{DRIVE3} and/or T_{DRIVE4} can be set to zero, resulting in those intervals being skipped if required.

4.2.1.2 Gate drive voltage

As mentioned, motor drive systems utilize a range of different MOSFET sizes and technologies. Additionally, the MOSFETs may have standard or logic-level gate thresholds, where $V_{GS(TH)}$ for logic-level devices such as the BSC007N04LS6 used in the EVAL_6EDL7141_TRAP_1SH evaluation board is significantly lower than for standard-level parts. As a consequence, for a given gate-to-source voltage, a logic-level MOSFET would produce a lower $R_{DS(on)}$ than a normal-level MOSFET. Increasing the gate drive voltage reduces the $R_{DS(on)}$ of the MOSFET channel during conduction, and as a result the conduction losses of the system as shown in the figure below. However, increasing the driving voltage also increases the switching rise and fall times, leading to higher switching losses.

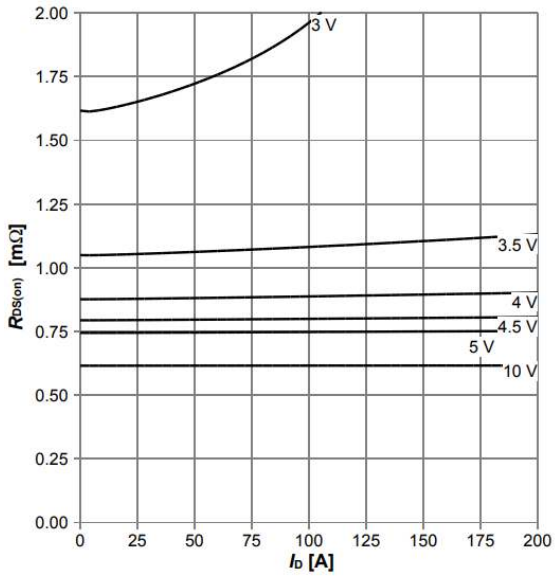

Figure 27 BSC007N04LS6 $R_{DS(on)}$ vs. V_{GS} characteristic

Hardware functional description

The 6EDL7141 offers the designer several driving voltage options to select from depending on the system requirements, allowing designers to adjust the MOSFET driving voltage (PVCC voltage) via SPI registers. The same-value PVCC applies to both high- and low-side charge pumps with four possible values: 7 V, 10 V, 12 V and 15 V. This is done by setting bit field PVCC_SETPT via the GUI, where the default value is 12 V. Gate drive outputs include undervoltage lockout (UVLO) protection.

MOSFETs in an inverter can be exposed to non-zero gate-source voltage levels when gate drivers are not activated. In some cases, such voltages can be high enough to pass the MOSFET gate turn-on threshold, partially switching on the device. If a high- and low-side MOSFET in an inverter phase were to switch on at the same time, the resulting high current could destroy the devices. In order to prevent this, it is common to add weak pull-down resistors between the gates and sources of each MOSFET. The 6EDL7141 avoids the need for these resistors by integrating the following functions into its gate driver outputs:

- Weak pull-down: A weak pull-down (RGS_PD_WEAK) is always connected between gate and source of each gate driver output. This ensures a weak pull-down during states where the gate driver is off, either because EN_RV is turned off or because the device is fully off (CE off). This mechanism is similar to the ones described above.
- Strong pull-down: During gate driver off periods, if the external gate-to-source voltage increases for any reason, a strong pull-down (RGD_PD_STRONG) is activated, ensuring a tight pull-down to prevent any partial turn-on.

4.2.1.3 Determining the values for EVAL_6EDL7141_TRAP_1SH

This system is designed for an 18 V battery with BSC007N04LS6 MOSFETs switching at 20 kHz with a dead-time of 500 ns. From **Figure 27** it can be seen that a gate drive V_{DR} of 10 V will be sufficient to produce the lowest $R_{DS(on)}$ specified in the datasheet. In this example, to minimize EMI without producing excessive switching losses, we design for a slew rate of 150 V/µs for both switch-on and switch-off. The designer may use different values providing sufficient dead-time is set to prevent shoot-through.

The following graph outlines the charging phases of the BSC007N04LS6 during the switch-on process, which are in reverse during switch-off.

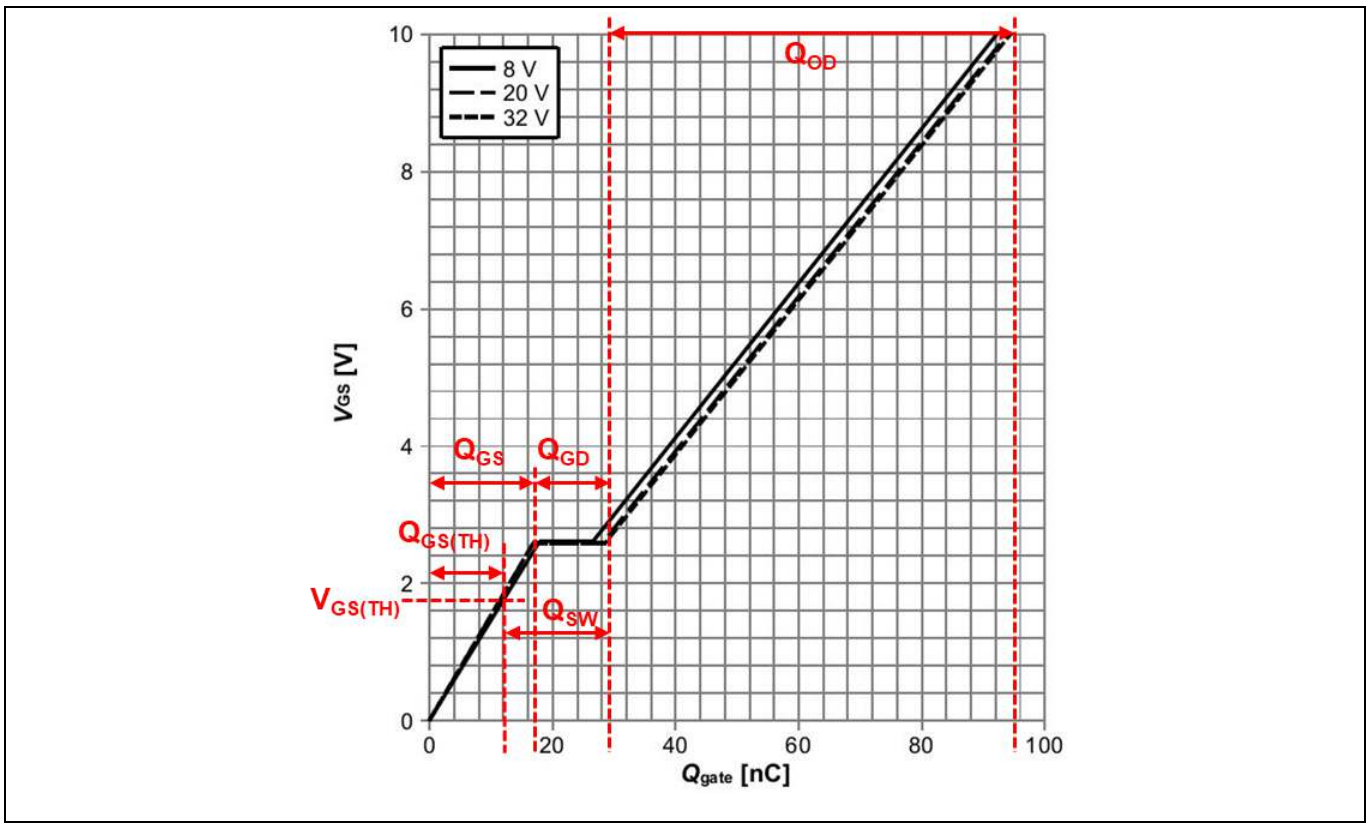

Figure 28 BSC007N04LS6 gate charge graph

It is important to consider that the V_{DS} transient produced at switch-off should be limited to a peak below the MOSFET BV_{DSS} rating in the worst-case condition of a stalled motor to prevent avalanching. The transient peak value is controlled by limiting the switch-off speed. The switch-off transient peak value is determined by:

$$V_{DS(PK)} = L_P \cdot \frac{di_D}{dt} \quad [1]$$

where L_P represents the inductance in the circuit carrying the drain current, which is composed of PCB trace and package inductances. dI_D/dt is determined by the selected gate current during T_{DRIVE4}.

4.2.1.3.1 Gate switch-on configuration procedure

1. Determine the gate drive voltage setting.

   It can be seen from **Figure 27** that the BSC007N04LS6 fully reaches lowest $R_{DS(on)}$ with 10 V gate drive voltage. Therefore, PVCC is set to 10 V.

2. Determine T_{DRIVE1} from a selected I_{PRE_SRC} value chosen based on the minimum available value of T_{DRIVE1}, which is 50 ns. Obtain $Q_{GS(TH)}$ from the graph or MOSFET datasheet. For the BSC007N04LS6 $Q_{GS(TH)}$ = 10.3 nC, considering the condition of V_{DS} = 20 V, which is close to the 18 V battery voltage.

   $$I_{PRE\_SRC} = \frac{Q_{GS(TH)}}{t_{DRIVE1}} \quad [2]$$

   $$I_{PRE\_SRC} = \frac{10.3\ nC}{50\ ns} = 206\ mA$$

   The value is rounded down to 200 mA so that during the T_{DRIVE1} period the gate will be charged almost to $V_{GS(TH)}$. To allow for tolerances it would be safer to further reduce this value to 175 mA.

3. Determine T_{DRIVE2} and I_{HS_SRC} or I_{LS_SRC} based on the desired slew rate – in this case, 150 V/µs.

   Obtain Q_{SW} from the graph or MOSFET datasheet. For the BSC007N04LS6 Q_{SW} = 18 nC.

   (Where $Q_{SW} = Q_{GS2} + Q_{GD}$, in this case Q_{GD} = 11.2 nC and $Q_{GS2} = Q_{GS} - Q_{G(TH)}$ = 17 nC – 10.3 nC = 6.7 nC.)

   T_{DRIVE2} can be calculated as follows:

   $$\frac{dV_{DS}}{dt} = \frac{V_{BAT}}{t_{DRIVE2}} \quad [3]$$

   $$t_{DRIVE2} = {V_{BAT}}\Big/{\left(\frac{dV_{DS}}{dt}\right)} = {18}/{150} = 120\ ns$$

   The result is then used to calculate the gate-source current required to complete the V_{GS} switching transition by reaching the end of the charge plateau.

   $$t_{DRIVE2} = \frac{Q_{SW}}{I_{HS,LS\_SRC}} \quad [4]$$

   $$I_{HS,LS\_SRC} = \frac{Q_{SW}}{t_{DRIVE2}} = \frac{18\ nC}{120\ ns} = 150\ mA$$

   In practice, it is necessary to ensure that the gate continues to be driven with I_{HS,LS_SRC} for the entire switching transition (dV_{DS}/dt) period; therefore t_{DRIVE2} is adjusted to 140 ns, giving a margin of at least 10 percent so that it will extend beyond the end of the transition.

4. During the final stage, Q_{OD} is charged, bringing V_{GS} from $V_{PLATEAU}$ to 10 V as quickly as possible.

   $$Q_{OD} = Q_G - Q_{SW} - Q_{G(TH)} \quad [5]$$

   For the BSC007N04LS6:

   $$Q_{OD} = 94\ nC - 18\ nC - 10.3\ nC = 65.7\ nC$$

5. The maximum gate drive source current of 1.5 A is applied during this period. The time required can be calculated by:

$$t_{OD} = \frac{Q_{OD}}{I_{GD\_SRC\_PEAK}} \quad [6]$$

$$t_{OD} = \frac{65.7\ nC}{1.5\ A} = 43.8\ ns$$

It should be noted that as V_{GS} charges to the full voltage the gate driver will no longer sustain 1.5 A source current, but the gate will remain pulled up.

4.2.1.3.2 Gate switch-off configuration procedure

1. During the first part of switch-off Q_{OD} is discharged to bring V_{GS} from 10 V to $V_{PLATEAU}$, which occurs during the period T_{DRIVE3} with the gate sink current I_{PRE_SINK}. Obtain Q_{OD} from the graph or MOSFET datasheet. This should happen quite rapidly.

   Choosing a T_{DRIVE3} value of 200 ns, I_{PRE_SINK} can be calculated as:

   $$I_{PRE\_SINK} = \frac{Q_{OD}}{T_{DRIVE3}} \quad [7]$$

   $$I_{PRE\_SINK} = \frac{65.7\ nC}{200\ ns} = 328.5\ mA$$

   This value is rounded down to the closest available value, giving 300 mA.

2. Determine T_{DRIVE4} and I_{HS_SINK} or I_{LS_SINK} based on the desired slew rate. In this case 150 V/µs.

   $$\frac{dV_{DS}}{dt} = \frac{V_{BAT}}{t_{DRIVE4}} \quad [8]$$

   $$t_{DRIVE4} = {V_{BAT}}\Big/{\left(\frac{dV_{DS}}{dt}\right)} = {18}/{150} = 120\ ns$$

   The result is then used to calculate the gate source current required to complete the V_{GS} switching transition by reaching the end of the gate threshold voltage $V_{GS(TH)}$.

   $$t_{DRIVE4} = \frac{Q_{SW}}{I_{HS,LS\_SINK}} \quad [9]$$

   $$I_{HS,LS\_SINK} = \frac{Q_{SW}}{t_{DRIVE4}} = \frac{18\ nC}{120\ ns} = 150\ mA$$

   As during switch-on, the period covering the switching transition (in this case T_{DRIVE4}) is extended to ensure that I_{HS,LS_SINK} will be applied until the transition is completed. Therefore, t_{DRIVE4} is again adjusted to 140 ns.

   Because in this example the same slew rate was selected for switch-off as for switch-on, $T_{DRIVE4} = T_{DRIVE2}$ and $I_{HS,LS\_SINK} = I_{HS,LS\_SRC}$. However designers might wish to select different switch-on and switch-off slew rates, in which case $T_{DRIVE4} \neq T_{DRIVE2}$ and $I_{HS,LS\_SINK} \neq I_{HS,LS\_SRC}$.

3. During the final stage, $Q_{G(TH)}$ is discharged, bringing V_{GS} from $V_{GS(TH)}$ to zero as rapidly as possible.

   For the BSC007N04LS6 $Q_{G(TH)}$ = 10.3 nC, therefore the remaining switch-off time is calculated from the maximum gate drive sink current of 1.5 A applied during this period.

The time required can be calculated by:

$$t_{TH} = \frac{Q_{G(TH)}}{I_{GD\_SINK\_PEAK}} \quad [10]$$

$$t_{TH} = \frac{10.3\ nC}{1.5\ A} = 6.87\ ns$$

As V_{GS} falls to zero the sink current will drop to zero, but the strong pull-down will remain while the MOSFET is off.

4.2.1.3.3 Setting the dead-time

1. Calculate the total switch-off time as follows:

$$T_{DRIVE(OFF)} = T_{DRIVE3} + T_{DRIVE4} + T_{TH} + t_{rr} \quad [11]$$

$$T_{DRIVE(OFF)} = 200\ ns + 140\ ns + 6.87ns\ +\ 36ns\ = 372.87\ ns$$

The MOSFET body diode recovery time t_{rr} should also be added. To avoid the possibility of shoot-through and/or avalanching of the MOSFETs due to part variations and also temperature variations, it is recommended to add at least 20 percent to the calculated value:

The dead-time T_{DT} should be set to be greater than $T_{DRIVE(OFF)}$ + 20 percent.

In the EVAL_6EDL7141_TRAP_1SH evaluation board the dead-time is set in the microcontroller, not in the 6EDL7141, since the system operates in 6PWM mode.

$$T_{DT} \geq T_{DRIVE(ON)} \times 1.2 \quad [12]$$

$$T_{DT} \geq 372.87\ ns \times 1.2\ = 446\ ns$$

The closest available value is 440 ns. The rising and falling dead-times (T_{DT+} and T_{DT-}) are both set to this or a higher value.

The designer should also be aware that if drain-to-source snubber networks are connected to each MOSFET to reduce EMI and switch-off transients (as they are in the EVAL_6EDL7141_TRAP_1SH) then hard-switching may occur in the low-side unless the dead-time is further increased to allow the snubber capacitors to charge. Furthermore, if the gate drive during switch-off produces a slower turn off then the switching transition (dV_{DS}/dt) will also be delayed, which may also produce hard-switching in the low-side unless the dead-time is increased. In this design the switching losses are acceptably low with hard-switching of both high- and low-sides.

Table 3 List of calculated gate drive parameters

Parameter	Description	Value
I_{HS_SRC}	Source current value for switching on high-side MOSFETs	150 mA
I_{HS_SINK}	Sink current value for switching off high-side MOSFETs	150 mA
I_{LS_SRC}	Current value for switching on low-side MOSFETs	150 mA
I_{LS_SINK}	Current value for switching off low-side MOSFETs	150 mA
I_{PRE_SRC}	Pre-charge current value for switching on both high- and low-side	175 mA
I_{PRE_SNK}	Pre-charge current value for switching off both high- and low-side	300 mA

T_{DRIVE1}	Amount of time that I_{PRE_SRC} is applied. Shared configuration between high and low.	50 ns
T_{DRIVE2}	Amount of time that I_{HS_SRC} and I_{LS_SRC} are applied. Shared configuration between high- and low-side drivers.	140 ns
T_{DRIVE3}	Amount of time that I_{PRE_SNK} is applied. Shared configuration between high- and low-side drivers.	200 ns
T_{DRIVE4}	Amount of time that I_{HS_SINK} and I_{LS_SINK} and are applied. Shared configuration between high-side and low-side drivers.	140 ns

4.2.1.3.4 Procedure for tuning the gate drive on the bench

1. Ensure that RC snubbers are fitted across the drain and source of each MOSFET Q1 to Q6.
2. *Do not use the 120 ns default values for the rising and falling dead-times!*
   Set a longer dead-time initially than the calculated value to ensure that shoot-through will not occur. Then reduce the dead-time to a suitable value once the T_{DRIVE} and gate drive current settings have been determined.
3. Create a project in the GUI for a BLDC single-shunt design and enter the values of: T_{DRIVE1}, T_{DRIVE2}, T_{DRIVE3}, T_{DRIVE4}, I_{PRE_SRC}, I_{PRE_SINK}, I_{HS,LS_SINK}, I_{HS,LS_SRC}, calculated using the procedure above.
4. Save the project.
5. Use the “write device” command to configure the 6EDL7141 with the values in the project.
6. Operate the board at nominal battery voltage and monitor the high- and low-side V_{GS} and V_{DS} waveforms using differential probes for the high-side.
7. Increase to maximum load[1] and check the V_{DS} transient peak values to ensure that avalanching is not taking place and that there is sufficient headroom between the peak voltage and the MOSFET BV_{DSS} rating.
8. Determine whether the slew rates are correct according to the target value. If not, adjust gate drive source and sink currents via the GUI as necessary to ensure correct switching transitions.
9. If carrying out EMI measurements, to reduce EMI the slew rate may be reduced. However, when doing this keep in mind that switching losses will be increased.
10. Set the dead-time values to the desired values. Ensure the dead-times are re-calculated and adjusted to accommodate the slower slew rates if the slew rates have been altered.
11. Save the project each time a value is changed.
12. When the final values have been decided, use the “burn OTP” function to permanently set these values in the 6EDL7141.

[1] If the load is a BLDC motor, increase the torque and speed to fully load the system.

4.2.2 Configuration of the buck and linear regulators

The VDDB output can be used to supply external components as long as the current limits of the buck converter, charge pumps and linear regulator are not exceeded. The voltage may be set to 6.5V, 7V or 8V, depending on the gate drive voltage selection. Intelligent overcurrent protections (OCPs) are also implemented for both the buck converter and the linear regulator to prevent any damage to the device if the VDDB output becomes overloaded. Additional overtemperature protections (OTS, OTW) are integrated to ensure that the device operates within correct thermal limits.
Two different switching frequencies, 500 kHz (default value) or 1 MHz, can be selected via the GUI. The buck inductor L1 value is 22 µH for 500 kHz switching and 10 µH for 1 MHz. The values for the buck output capacitors C40 and C41 is 22 µF with an additional 0.22 µF ceramic capacitor C320 added to reduce high-frequency noise. Both the synchronous buck converter and linear voltage regulator circuits are shown in the following figure:

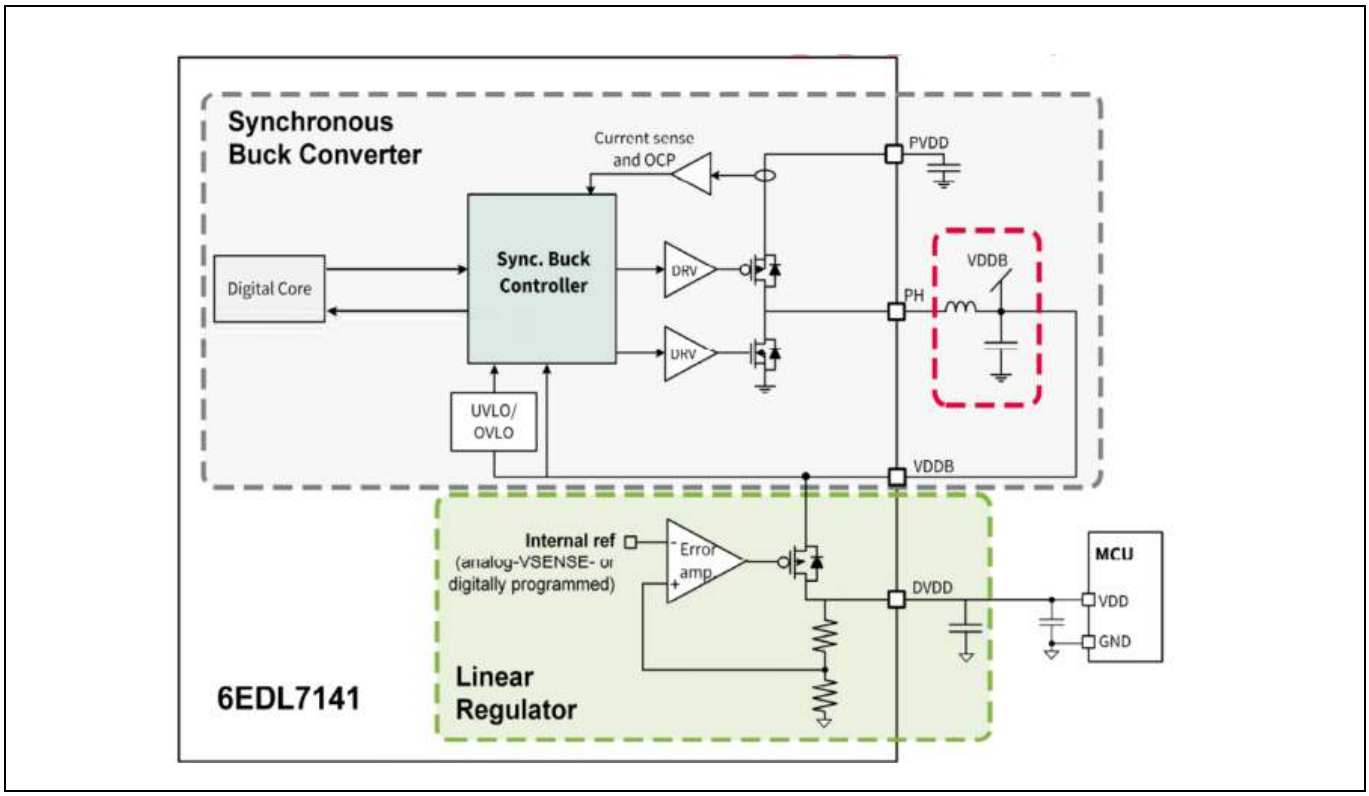

Figure 29 Detail of integrated synchronous buck converter and linear regulator

Hardware functional description

The following protections are implemented to ensure correct operation of the buck converter:

- output UVLO
- output overvoltage lockout (OVLO)
- OCP, cycle by cycle.

In a situation in which the current exceeds the OCP level, the buck converter controller terminates the high-side gate drive pulse until the start of the next PWM period. The low-side operates accordingly after insertion of the dead-time.
Once the OCP event takes place, a counter increments each consecutive period that the peak current is reached. After sixteen switching cycles, the buck OCP fault is triggered and the nFAULT pin is set low to signal the MCU. The buck converter will continue operation in current limitation to ensure the MCU remains powered. If the OCP is not triggered for three consecutive PWM periods, the counter resets.

The integrated linear regulator output DVDD can be set to either 3.3 V or 5 V by means of an external resistor R44, which is set to 10 kΩ on this evaluation board to set DVDD to 5 V. It is possible to override this hardware setting through the GUI, which can also read back the value set by the hardware. The linear regulator can also be used to provide an offset to the current sense amplifiers to allow negative current measurements.

DVDD OCP can be configured between four different levels – 50 mA, 150 mA, 300 mA or 450 mA, with 450 mA being the default value. If the OCP level is reached a fault is reported through the nFAULT pin. The DVDD OCP works in two different stages:

1. Pre warning mode at 66 percent of selected OCP level:
   The nFAULT pin is pulled down to signal the controller that an OCP warning has occurred. If the current level reduces before reaching the 100 percent level, the operation will continue normally, releasing the nFAULT pin. The pre-warning allows some extra time for the microcontroller to make a decision on how to react to the possible OCP event.

2. Current limiting mode at 100 percent of selected OCP level:
   If current increases beyond the configured OCP level, the DVDD regulator limits its output current. This causes the DVDD voltage to drop, eventually resulting in a DVDD UVLO fault if the UVLO threshold is crossed. This protects DVDD against a short-circuit condition.
   Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device should be operated only under recommended operating conditions as specified in the datasheet [1].

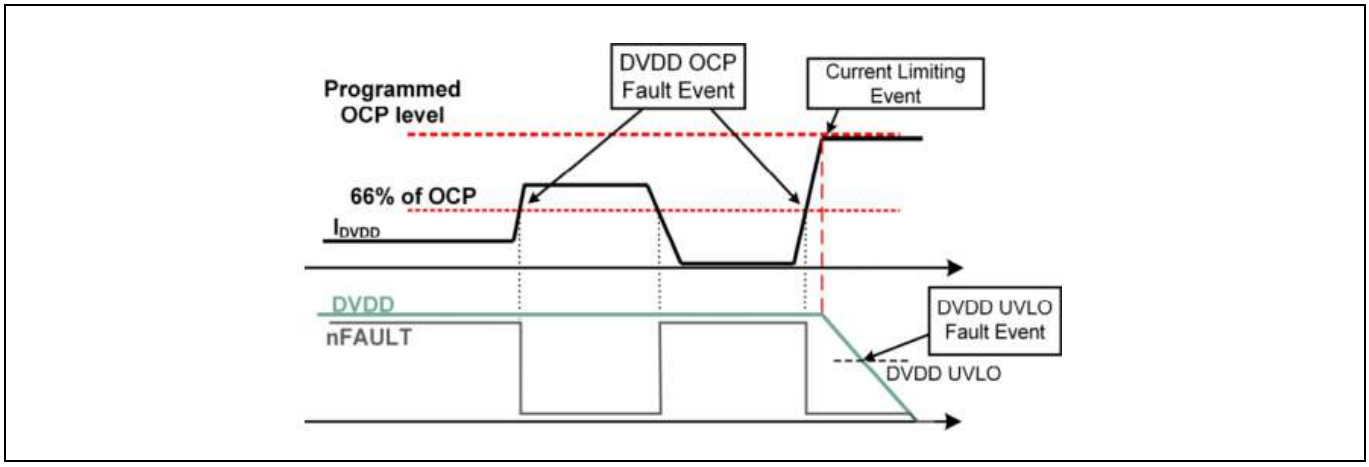

Figure 30 DVDD OCP behavior including pre-warning and current limiting modes

4.2.3 Configuration of the charge pumps

The high- and low-side gate driver charge pumps are based on switched capacitor circuits that operate at a determined switching frequency. Selection from one of four frequencies, 781.3 kHz, 390.6 kHz, 195.3 kHz, and 1.56 MHz, allows flexibility for EMC optimization, with 781.3 kHz being the default setting. Another useful feature in reducing the EMI impact of the charge pump is the spread spectrum feature, which can also be enabled and disabled via the GUI. This function is enabled by default to provide a frequency variation into the charge pump clock signal in order to distribute emissions over a wider frequency range, thereby reducing peaks.

The selection of charge pump flying capacitors C33 and C39 are set at 0.22 µF and the tank capacitors C30 and C32 are set to 2.2 µF. The 6EDL7141 provides pre-charging of the charge pump output capacitors (C30 and C32) to a voltage just below the buck converter output voltage (VDDB) before the EN_DRV pin is activated. In this way, the charge pump start-up time and therefore the system start-up time are reduced. In this case, when EN_DRV is activated by the microcontroller to enable the gate driver stage, the charge pumps need only to ramp up the voltage from the existing pre-charge voltage to the selected target value. Pre-charge is disabled by default and can be enabled via the GUI.

The start-up time for the charge pumps, defined as the time that the gate drive supply voltages require to get to the target programmed voltage, depends on several factors:

- Target voltage: the higher it is, the longer the start-up time for the gate drivers.
- Charge pump clock frequency: higher clock frequency results in faster start-up time.
- Charge pump tank capacitor values: a smaller value results in faster ramp-up time but higher ripple.
- Charge pump flying capacitors: smaller capacitors lead to slower start-up time.

4.2.4 Configuration of the current sense amplifiers

The device integrates three current sense amplifiers that can be used to measure the current in the inverter via shunt resistors. Single-, double- or triple-shunt measurements are supported, as shown below.
Each current sense amplifier can be enabled individually. Gain and offset are generated internally and are programmable.

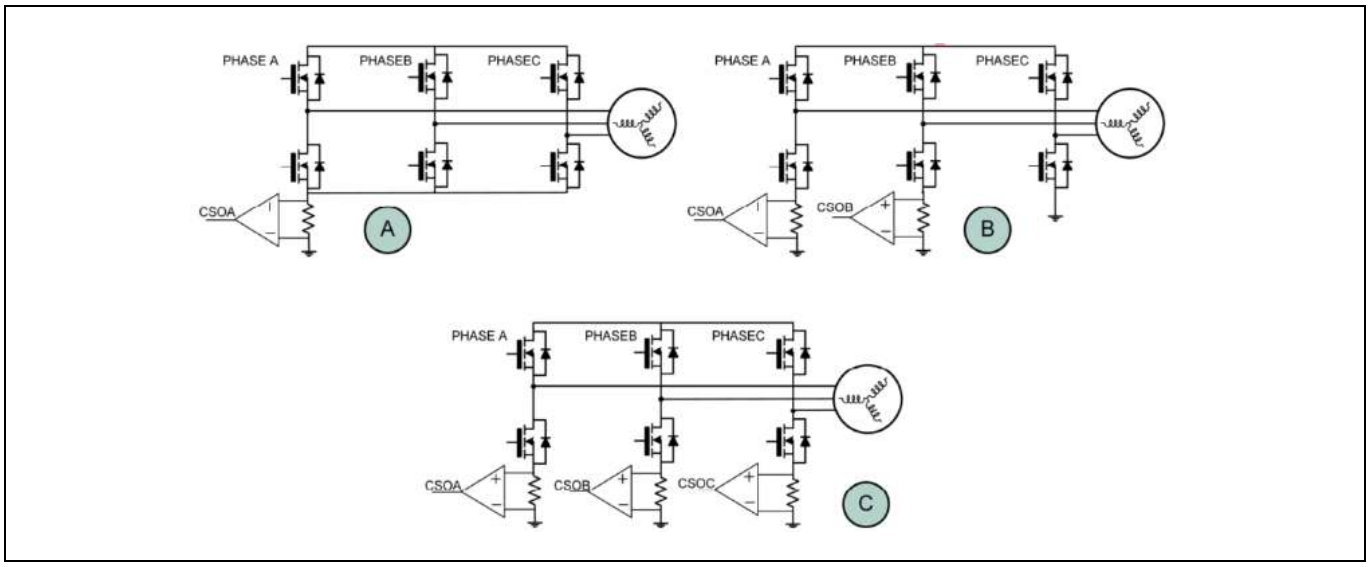

Figure 31 Single- (A), dual- (B) and triple- (C) shunt current sensing configurations

Hardware functional description

The current sense amplifier block contains the following sub-blocks, explained in detail in this section:

- Current sense amplifier: Connected to external shunt resistor or internally to an SHx pin for $R_{DS(on)}$ sensing. This module amplifies the shunt voltage or $V_{DS(on)}$ voltage to a level suitable for a microcontroller ADC input. It includes leading-edge blanking of the signal synchronized to the gate drive, which is active during periods to eliminate noise.
- Output buffer: Allows adding a variable offset voltage to the sense amplifier output. The offset amount can be set to one of four different values, either by programming the internally generated level or by applying an external voltage at the VREF input pin. With this implementation, negative shunt currents can also be measured.
- Positive overcurrent comparator: Used for detecting the overcurrent conditions on motor windings for positive shunt voltage. This comparator causes the gate drive pulse to be terminated, thus limiting the motor current.
- Negative overcurrent comparator: Used for detecting the overcurrent condition on motor windings for negative shunt currents.
- OCP DAC: Used for programming the overcurrent comparator thresholds. One sets the positive level and a second sets the negative level, which are shared among the different OCP comparators.

The current sense amplifier architecture includes an “auto-zero” function. This takes place during 6EDL7141 start-up and operation to maintain accuracy of measurements during the lifetime of the device. If no GHx rising edge happens for a given time (tAUTO_ZERO_CYCLE), i.e., if the low-side is fully turned on for a long period in a six-step commutation, then an internal watchdog timer triggers an auto-zero compensation. Auto-zero is continuous during the standby state. The auto-zero feature can be disabled via the GUI. In addition, the 6EDL7141 includes a current sense amplifier user calibration mode that can be used to measure and compensate for offset at a time when the shunt current is known to be zero, i.e., when all of the gate drives are low.

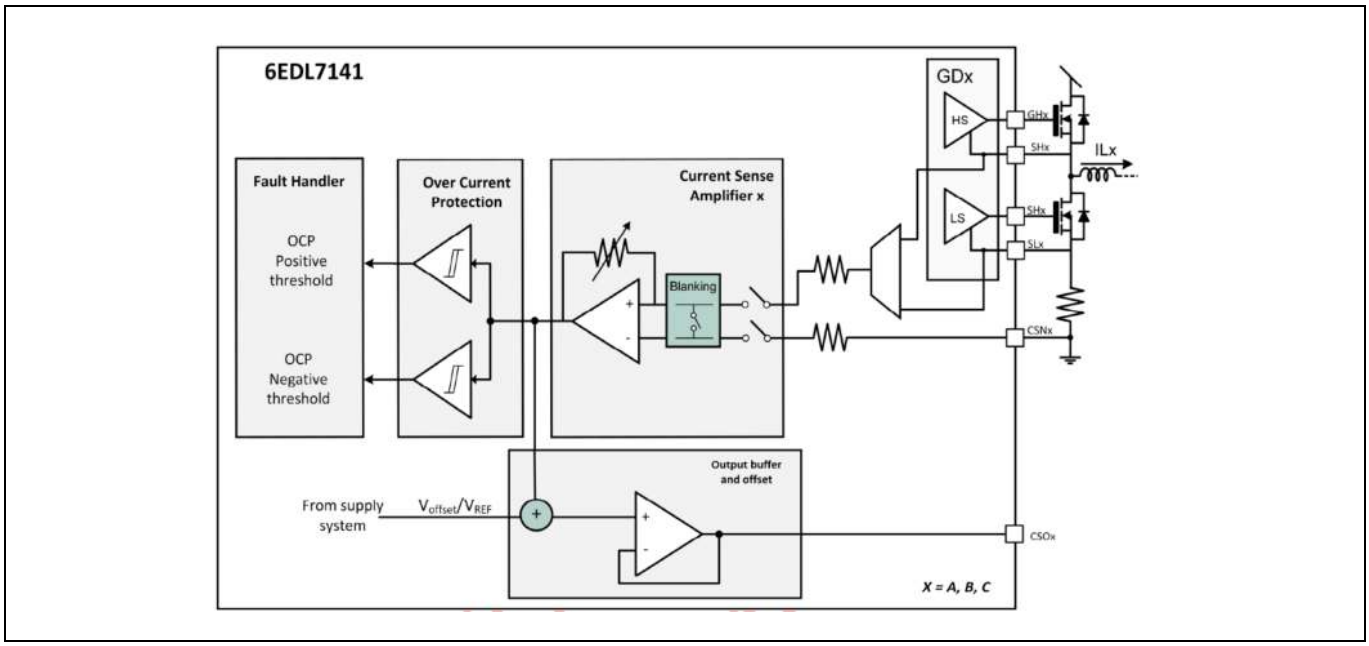

Figure 32 Current sense amplifier simplified block diagram

The current sense amplifiers in 6EDL7141 can be configured for $R_{DS(on)}$ sensing to avoid the use of shunt resistors; however, this function is not used in the EVAL_6EDL7141_TRAP_1SH board, which uses a single 500 µΩ shunt resistor RS1. In this implementation only a single current sense amplifier is required.

Hardware functional description

The current sense amplifiers have a default voltage gain of 4. This can be changed via the GUI to any of the following values: 8, 12, 14, 20, 24, 32 or 64. Alternatively, the gain can be selected by connecting an external resistor from pin CS_GAIN to ground. In order to enable analog programming of the current sense amplifier via an external resistor, the user must ensure that bit field CS_GAIN_ANA is set accordingly. The value of RGAIN is read during the start-up sequence of the 6EDL7141. Table 15 in the datasheet [1] provides the resistor values and register settings for gain selection in both analog and digital modes.

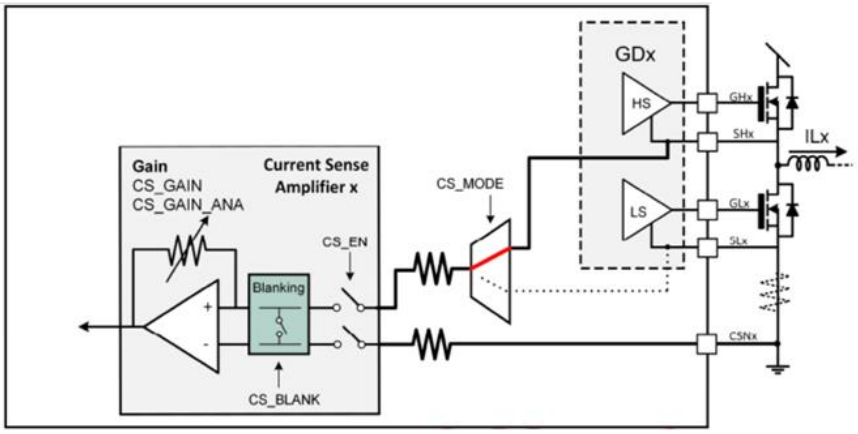

Figure 33 System diagram of a low-side $R_{DS(on)}$ current sensing configuration (not used here)

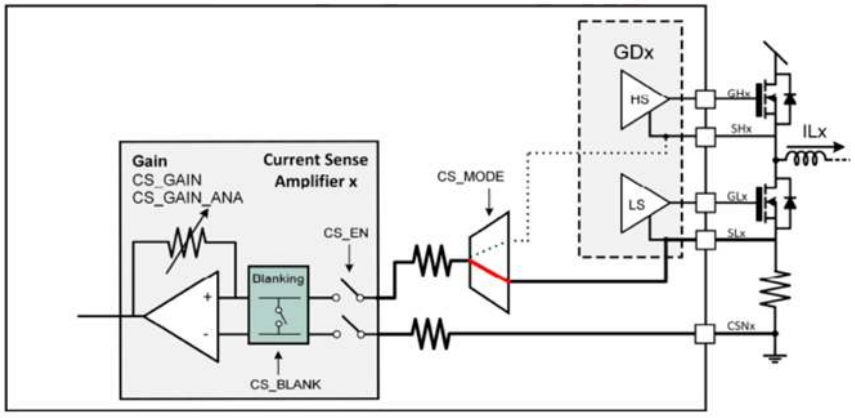

Figure 34 System diagram of an external shunt current sensing configuration

In many motor drive inverters such as this evaluation board, the current is sensed via shunt resistors. In this case, the voltage across the shunt needs to be amplified only when the low-side MOSFET is switched on. In other cases, it might be useful to monitor the signal continuously. The 6EDL7141 supports four different modes of operation of the current sense amplifiers regarding when the output is connected to the amplifier, which can be selected through the GUI.

Hardware functional description

These four modes are:

- Always OFF: current sense amplifier output disabled. This is achieved by disabling the amplifier in register CSAMP_CFG via bit field CS_EN.
- GL ON (default mode): in this mode, the CSOx pin is connected to the amplifier only when the corresponding GLx signal is active. In single-shunt mode CSOx is connected according to the ORing of all two or three GLx signals. If two or three amplifiers are enabled, then the signals for enabling CSOx come from the corresponding GLx signal. This mode is mandatory if $R_{DS(on)}$ sensing is selected to avoid overvoltage damage to the internal circuitry.
- GH OFF: similarly to GL ON, this mode exposes the output to GL ON period but extends the sensing period to the dead-times, both rising and falling.
- Always ON: this mode connects the activated amplifier CSOx signals continuously to the amplifier independently of PWM signals.

The programmable leading edge blanking function can be configured in the current sense amplifiers. Since both phase node voltage SHx and SLx pins (CSNy) are subject to ringing due to the switching activity, the blanking module disconnects the inputs for a configurable time (CS_BLANK). The default blanking time is zero, and values between 50 ns and 8 µs can be selected via the GUI. The 6EDL7141 internal linear voltage regulator (DVDD) can be used for offset generation for current sense amplifiers. The default value is 1/2DVDD; values of: 5/12, 1/3 and 1/4DVDD are also available.

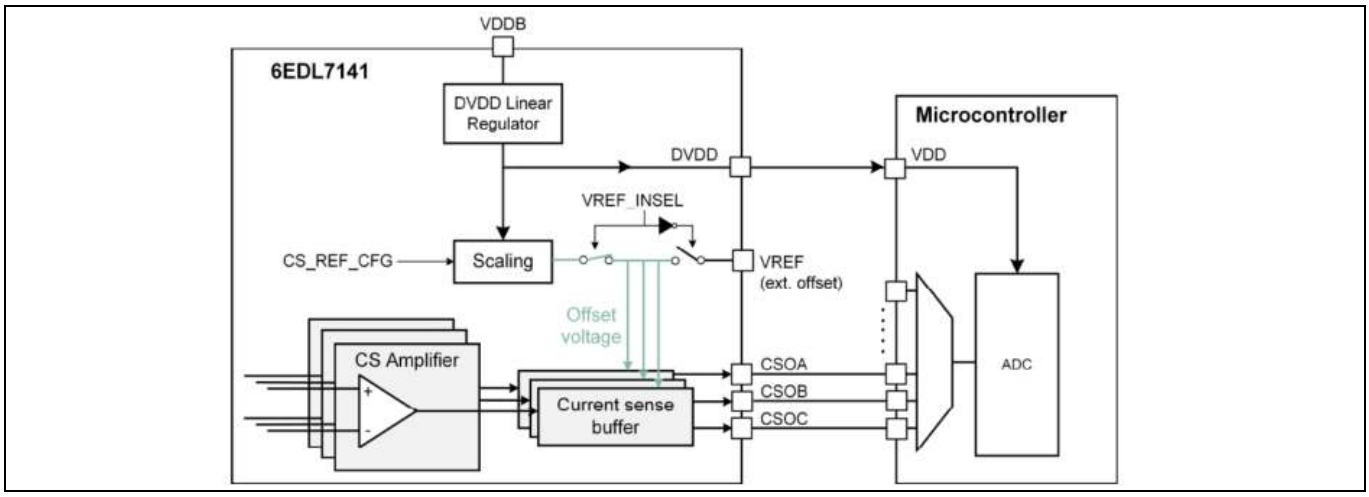

Figure 35 Current sense amplifier offset generation block diagram

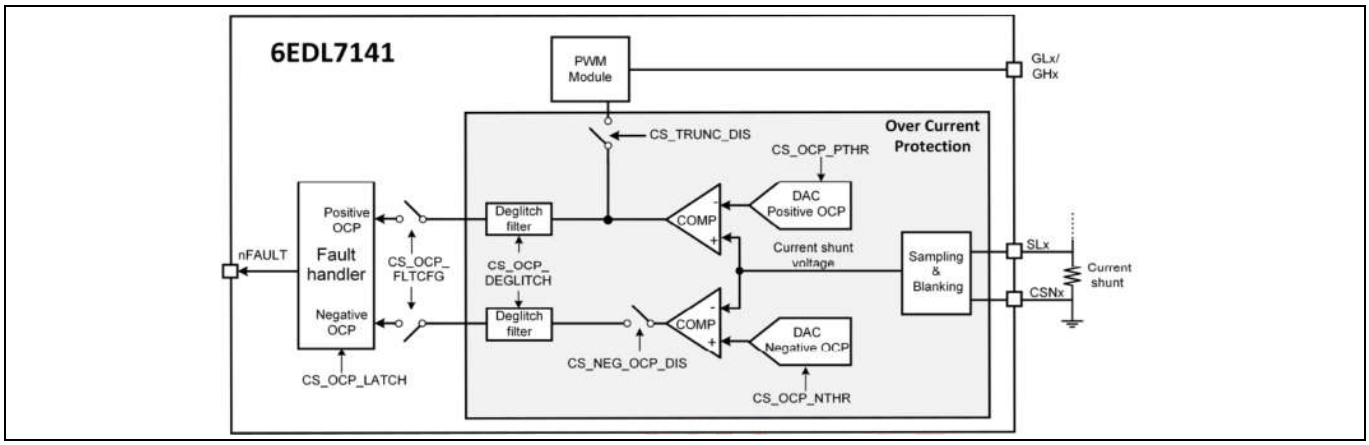

Figure 36 Current sense amplifier architecture

Hardware functional description

How the 6EDL7141 reacts to an OCP event is programmable via the GUI. The following scenarios can be useful for different applications:

- Apply PWM truncation immediately after OCP event and report on nFAULT pin after OCP event – deglitching is disabled if truncation is enabled.
- Disable reporting but keep truncation of PWM.
- Trigger a configurable brake action upon OCP event. If truncation is not desired, a brake event can be configured using one of the available braking modes.
- Disable OCP protection, both nFAULT reporting and truncation of PWM. In this case, OCP is ignored.

It is also possible to select whether the OCP fault is latched or not via the GUI. In a latch configuration, the nFAULT pin is held low until the fault is cleared via an SPI command or after a power cycle. If the OCP fault is configured as non-latched, the nFAULT pin remains low while the fault is being detected but will pull up again when the OCP condition is no longer present. Configuration allows the user to set a target number of consecutive events (PWM cycles) required to activate the nFAULT fault signaling.

If a positive OCP event occurs, the high-side PWM is truncated. The result is that the high-side MOSFETs are all switched off and the current flowing in the motor windings therefore recirculates through the low-side MOSFET body diodes.

4.3 XMC1404-VQFN64-200kB microcontroller

The microcontroller interacts with the system through the following inputs and outputs:

Table 4 Microcontroller inputs and outputs

Port	Configuration	Description
P0.7	Digital input	Enable
P2.7	Digital input	Braking switch
P4.1	Digital input	Hall sensor input – phase A
P4.2	Digital input	Hall sensor input – phase B
P4.3	Digital input	Hall sensor input – phase C
P4.10	Digital input	Motor direction
P2.3	Analog input	Battery voltage sense
P2.10	Analog input	Shunt current sense through amplifier
P2.5	Analog input	Potentiometer voltage sense
P2.2	Analog input	Back EMF sense – phase U
P2.1	Analog input	Back EMF sense – phase V
P2.0	Analog input	Back EMF sense – phase W
P2.4	Analog input	Temperature sensing
P3.2	PWM output	Low-side gate pulse – phase U (INLA)
P3.3	PWM output	High-side gate pulse – phase U (INHA)
P3.0	PWM output	Low-side gate pulse – phase V (INLB)
P3.1	PWM output	High-side gate pulse – phase V (INHB)
P1.1	PWM output	Low-side gate pulse – phase W (INLC)
P1.0	PWM output	High-side gate pulse – phase W (INHC)
P1.3	Digital output	Brake command
P1.2	Digital output	Auto zero command
P0.12	Digital output	Fault indicator
P3.4	Digital output	Fault indicator (nFAULT) (LED1)
P4.7	Digital output	LED indicator (LED5)
P4.8	Digital output	LED indicator (LED4)
P4.4	Debug	PC_RX
P4.5	Debug	PC_TX
P0.14	Debug	SWDIO/TMS
P0.15	Debug	SWDCLK/TCK

4.4 Board connections and controls

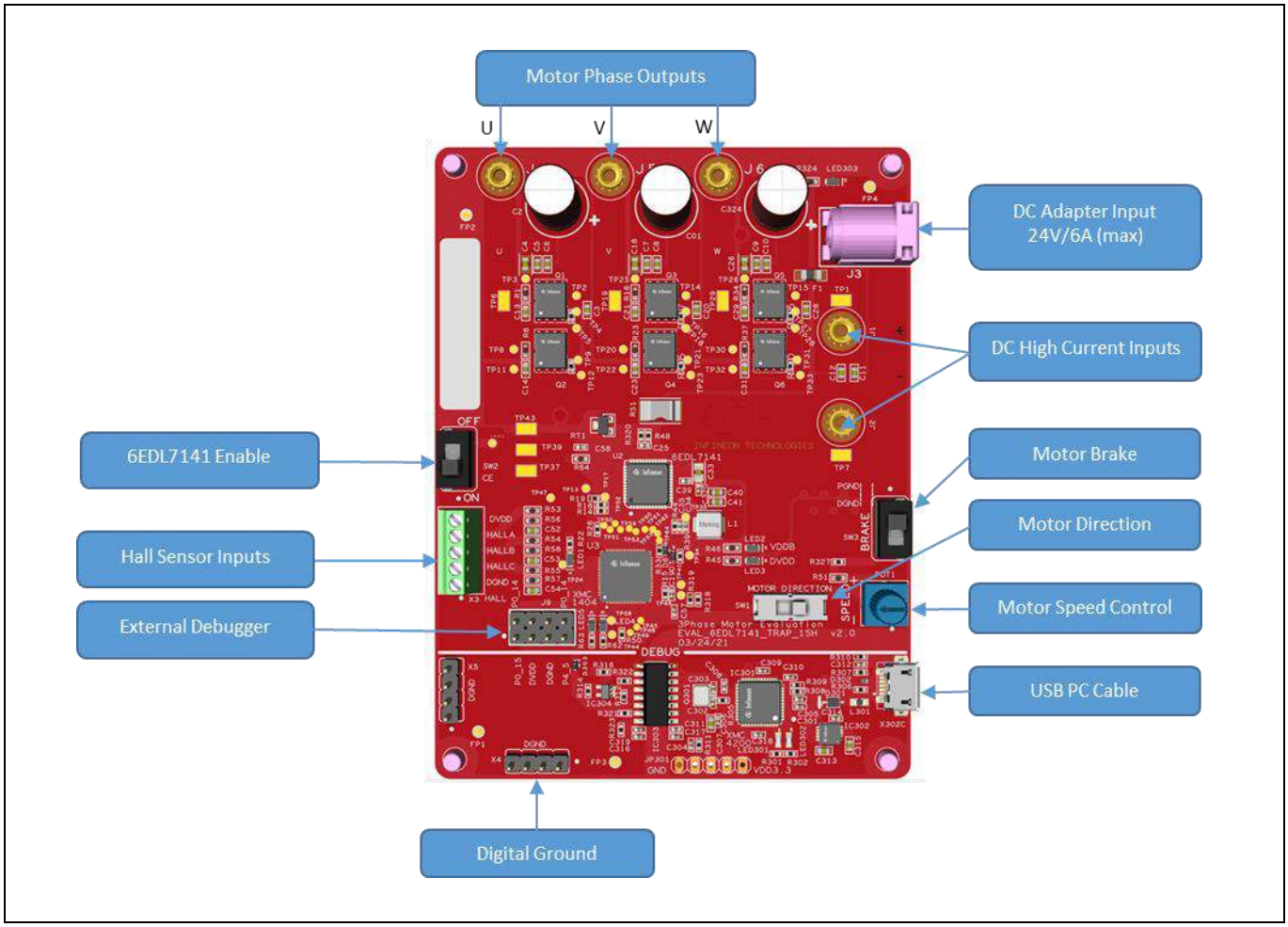

Figure 37 EVAL_6EDL7141_TRAP_1SH external connections and controls

4.5 On-board programmer/debugger

The EVAL_6EDL7141_TRAP_1SH board includes an on-board debugger, which is located below the yellow line shown on the top-side component legend. This is connected to a PC through a USB cable to enable control, programming and debugging via a dedicated GUI or firmware development tool such as DAVE™.

4.6 External programmer/debugger

If for any reason the user wishes to use an external debugger such as the XMC™ Link, this can be connected via the 4 x 2-way header indicated.

5 Control and firmware

5.1 Trapezoidal control also known as six-step or block commutation

In contrast to common synchronous machines, which are driven with sine wave voltages, BLDC motors are most commonly driven with a block-shaped voltage resulting in a trapezoidal-shaped current. Trapezoidal control is also known as block commutation or six-step control because there are six commutation intervals for each revolution, which are 60 degrees apart. This is the simplest BLDC motor control algorithm. Although performance is acceptable for power tools, block commutation is known to create a torque ripple with six times the frequency of the electrical rotary frequency of the three-phase motor. This leads to vibrations and acoustic noise due to the discrete switching between the phases such that the stator and rotor fields are not always perpendicular to each other. This generates high torque ripple, resulting in some inevitable vibration and noise.

In three-phase machines during each commutation step a current path is formed between a pair of windings, leaving the third winding disconnected. The Hall sensor outputs are either high or low depending on which pole of the rotor permanent magnet they are in proximity with, in the current position. During rotation, when one of the rotor north–south pole interfaces passes a Hall sensor, its output toggles and the controller then switches the DC voltage to the next phase (shown below as “A”, “B” or “C”). The XMC1400 series microcontroller has sufficient processing power to execute this control algorithm. As shown below, the voltage has a rectangular shape, which results in a trapezoidal current and back-EMF shape in the machine.

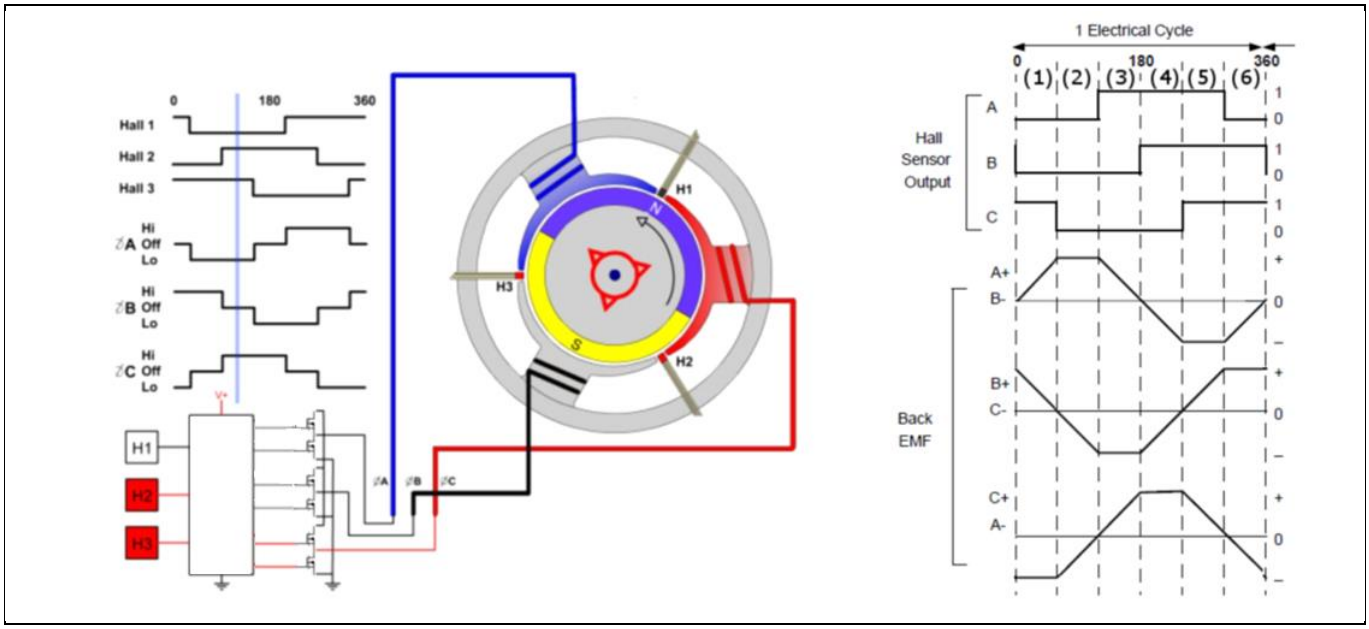

Figure 38 Control of a BLDC motor with Hall sensors

During each commutation step one of the windings is energized with current entering into it, the second winding has current exiting it, and the third is in a non-energized open-circuit condition. The torque is produced because of the interaction between the magnetic field generated by the stator coils and the permanent magnets. Ideally, the peak torque occurs when these two fields are at 90 degrees to each other and falls off as the fields move together.

Control and firmware

The block diagram of a typical BLDC trapezoidal control block commutation system with Hall sensors is shown below:

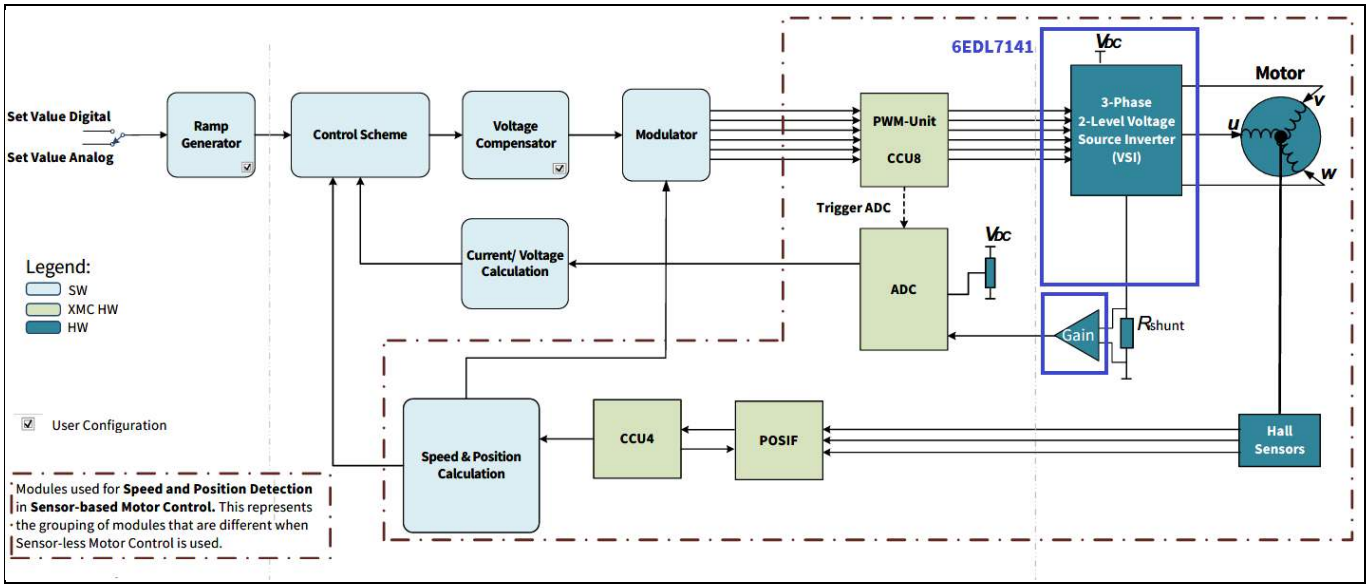

Figure 39 Block diagram of trapezoidal/block commutation algorithm

The switching patterns are shown in the diagram below. In the EVAL6EDL7141_BLDC_1SH implementation the 6PWM mode is used, where all of the high- and low-side gate drive pulses are generated by the microcontroller, which also senses the Hall sensor outputs. The firmware is based on the BLDC_SCALAR_HALL_XMC13 platform developed by Infineon.

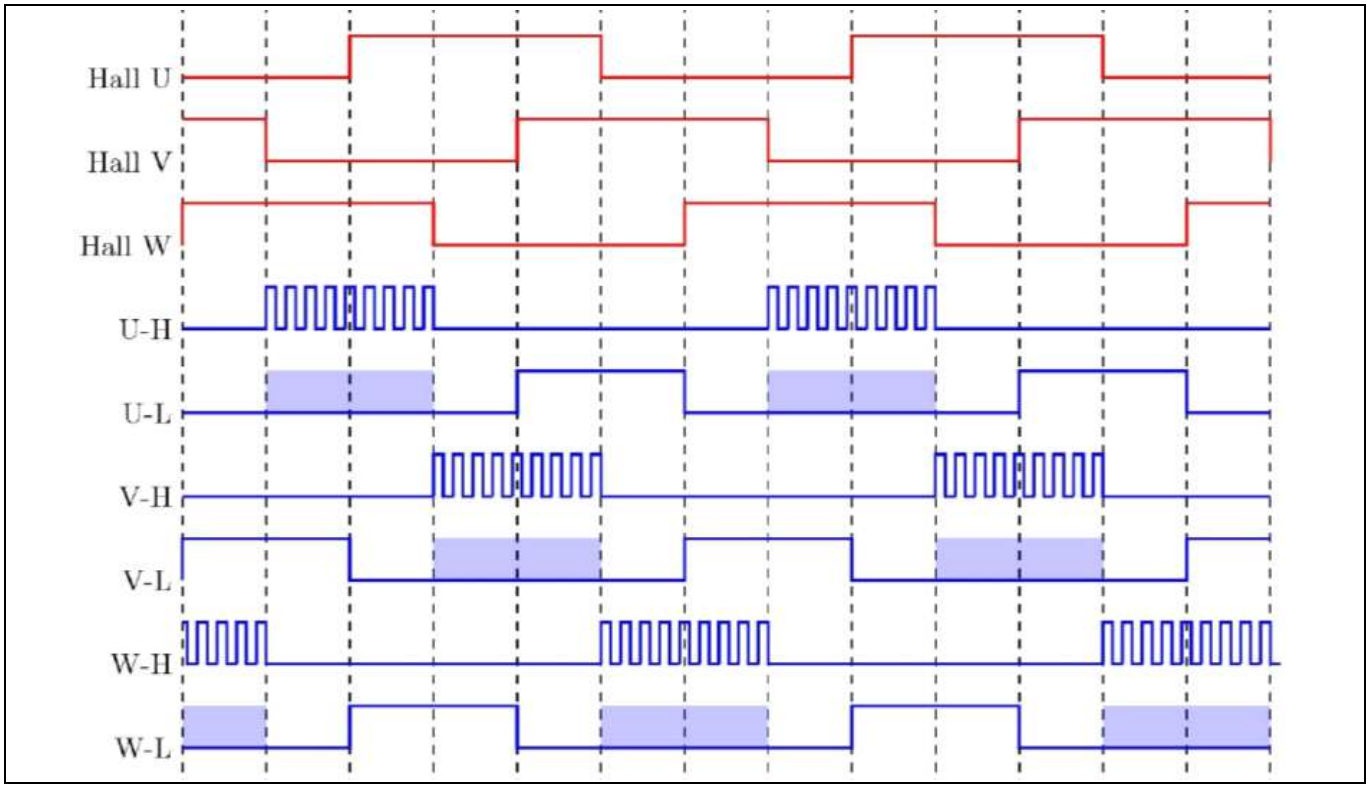

Figure 40 Switching patterns for trapezoidal/block commutation

5.2 P-I control

As illustrated in the block diagram above, a closed-loop control system is used to regulate the motor voltage, current or speed. Speed control is the default control method set by the GUI and selected in the pre-installed firmware. A command value is applied to the system through the potentiometer on the board or from the GUI in test bench mode via the slider control. The firmware implements a proportional-integral (P-I) control loop as shown:

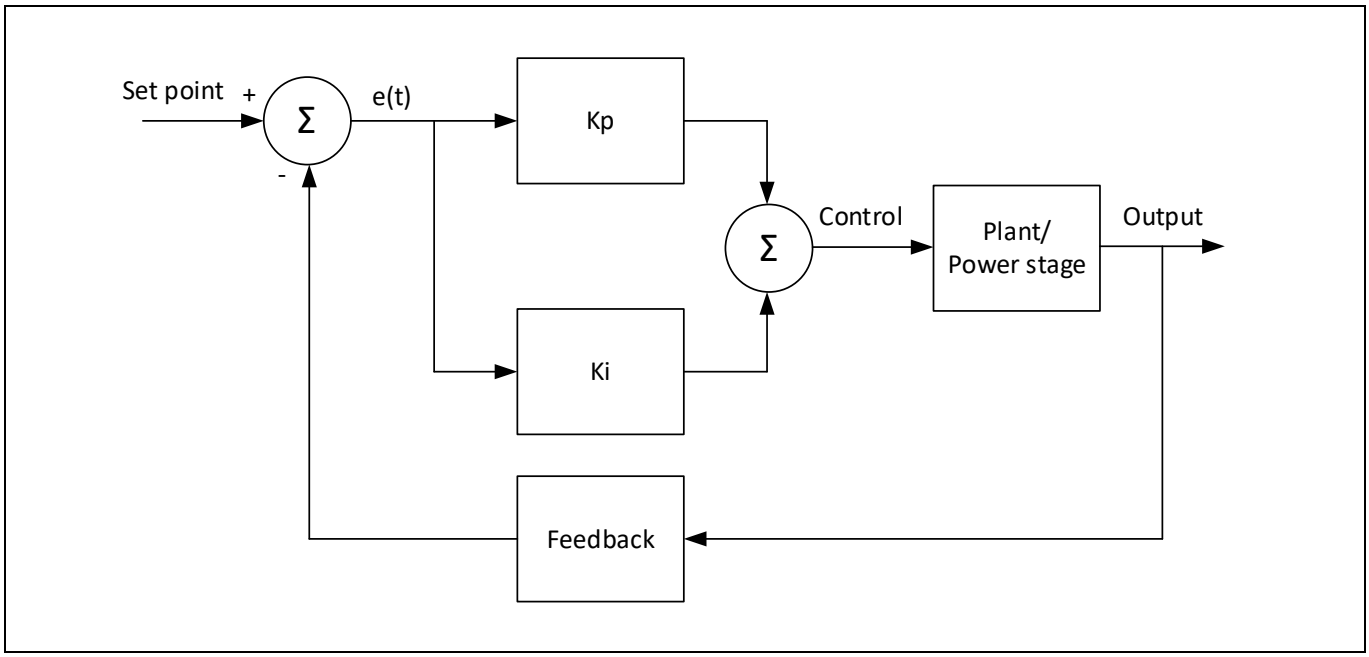

Figure 41 P-I control block diagram

The gain factors, K_P and K_I, can be selected via the GUI firmware options (XMC1400 -> Control loop) along with other parameters described in the next section. The firmware can then be programmed into the target board's microcontroller with the GUI Flash firmware option.

The P-I controller is a widely used feedback control mechanism, which continuously calculates an error value e(t) that is the difference between the setpoint of the measured output quantity (in this case speed in RPM) and the actual measured value. In this case the speed is derived by the firmware from the Hall sensor input signals. The error value is fed to the proportional calculator where it is multiplied by K_P and to the integral calculator where it is integrated with respect to time and the result multiplied by K_I. These two results are then summed together to provide a control value, which is applied to the power stage to provide a correction that will adjust the output to match the setpoint. The goal is to optimize the values of K_P and K_I for the specific system (inverter and motor) to achieve minimal delay and overshoot when changes are made to the commanded speed.

6 Graphical user interface

The 6EDLMC GUI downloads control firmware and configuration settings for the 6EDL7141 on motor control boards operating with trapezoidal or field-oriented control with one or three shunts. Once the parameters for a particular project have been selected, the configuration can be saved. The opening screen is as follows:

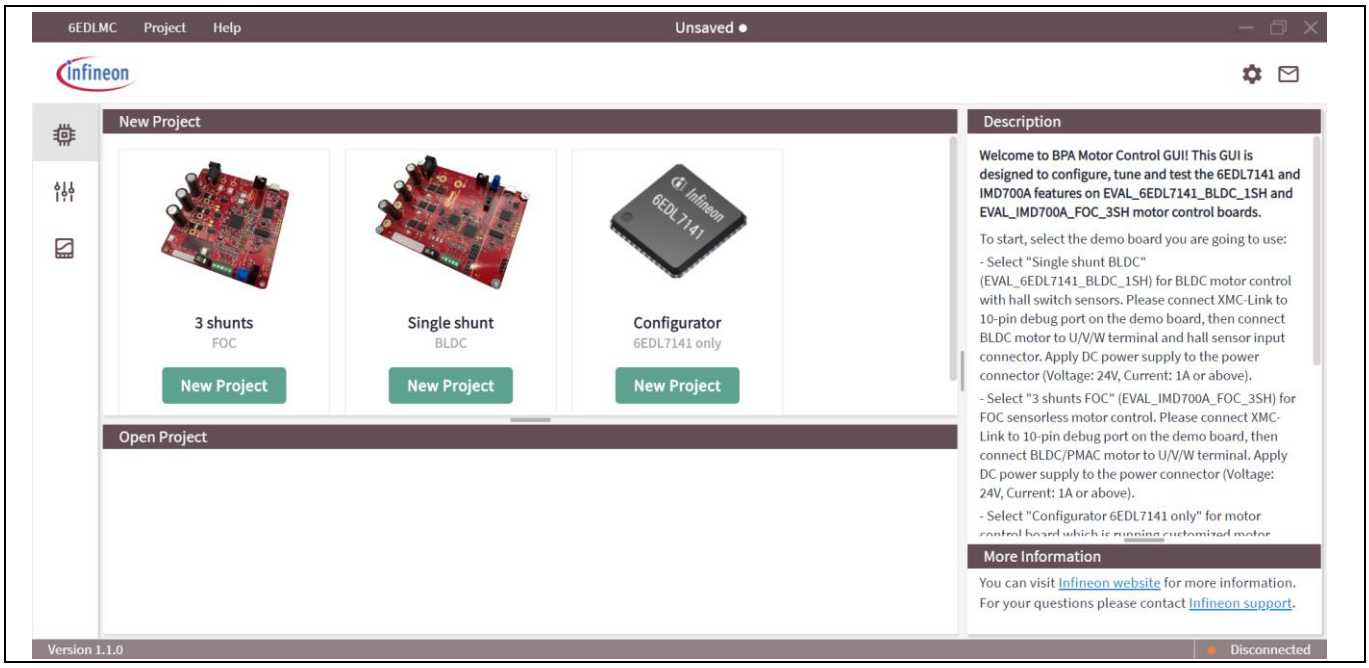

Figure 42 6EDLMC GUI opening screen

To start a new project first select the required configuration from the three available options. The EVAL_6EDL7141_TRAP_1SH evaluation board is a single-shunt design for BLDC, which when selected brings the GUI to the next screen. The next step is to expand the dropdown menu from the “XMC1400” option in the “Parameter Controls” panel.

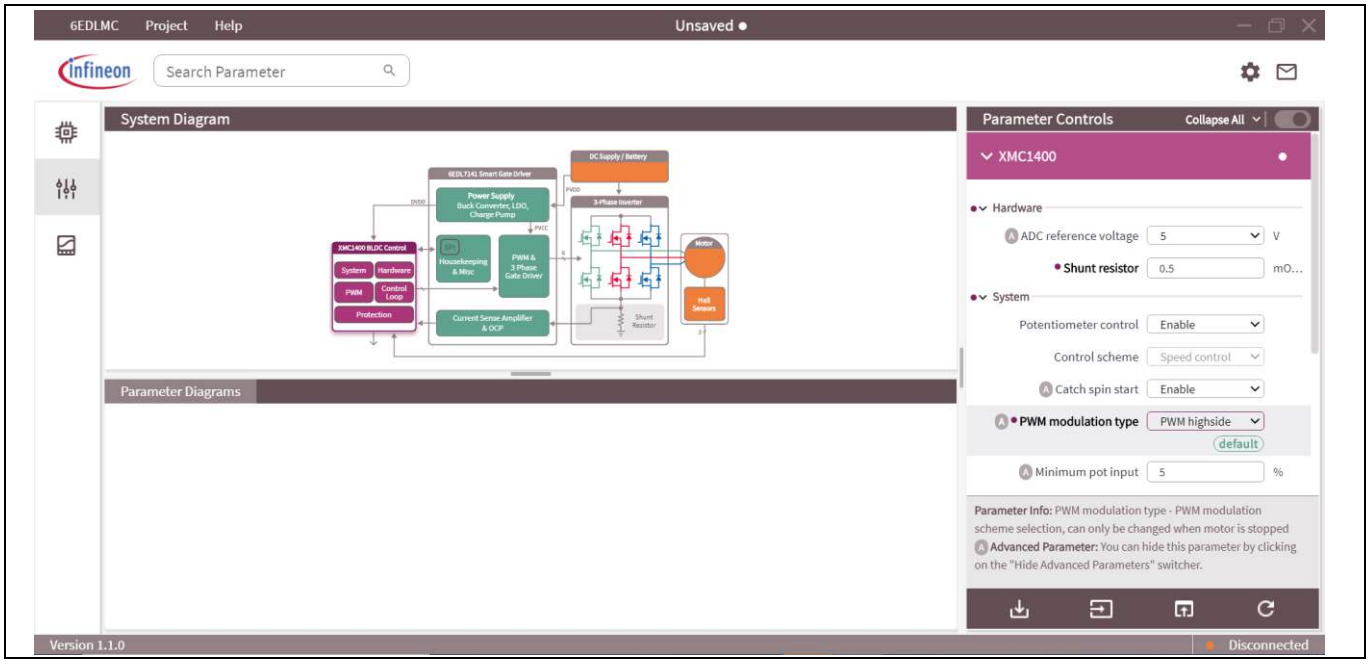

Figure 43 Trapezoidal control with single-shunt firmware configuration menu

6.1 Downloading the firmware from the GUI

In order to support transfer of 6EDL7141 parameters from the GUI, the firmware must include the functions that support this. The EVAL_6EDL71741_TRAP_1SH board is pre-installed with the correct firmware and parameters.

The GUI includes a suite of firmware options that can be downloaded to any compatible motor drive board, which uses the XMC1400 microcontroller with the 6EDL7141 or the integrated IMD700/1 A. In the figure above, on the right-hand side the XMC1400 is expanded to show the firmware options available. The figure below displays some of the firmware options that are available such as the PWM frequency and dead-time.[1]

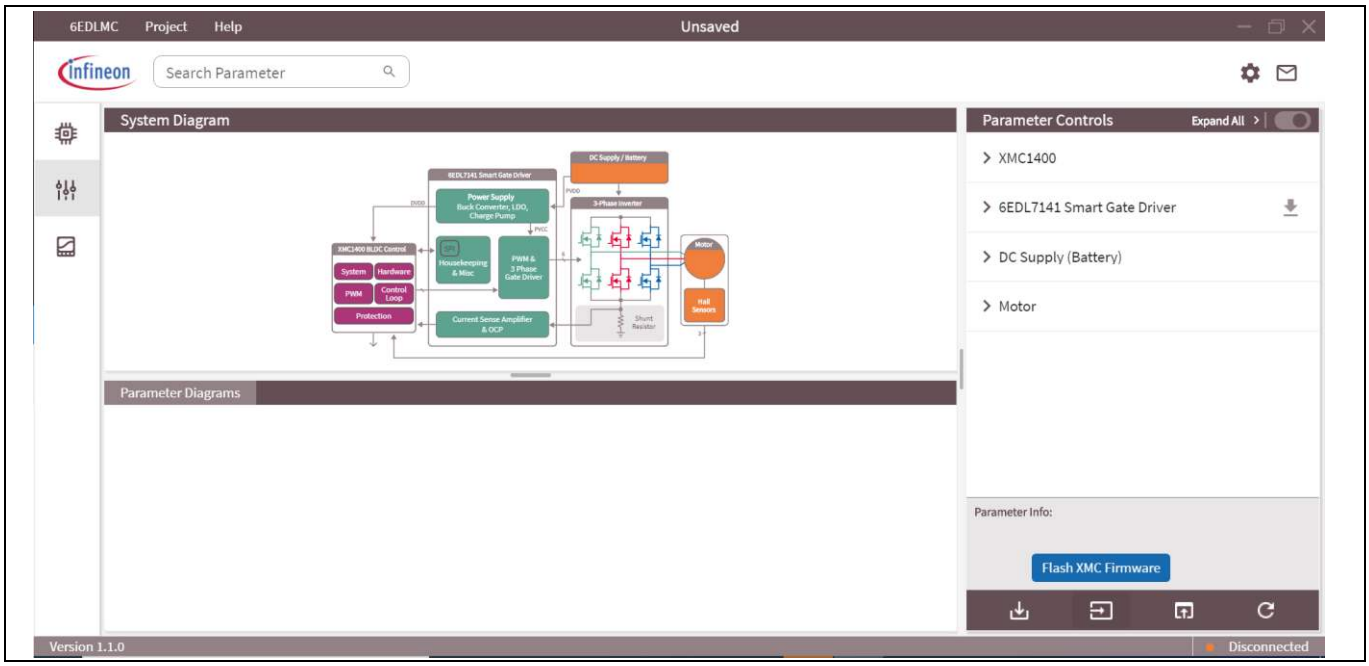

Figure 44 Firmware options and download

There are various important firmware parameters to be selected before downloading, which are listed in the table below. When the firmware parameters have been selected in the GUI, the firmware may be downloaded to the board via the USB cable by clicking the “Flash Firmware” button as shown above. A message will appear to inform the user that the firmware was successfully programmed onto the microcontroller.

Table 5 List of firmware parameters

Parameter	Description	Value	Unit
ADC reference voltage	V_{ADC} reference voltage, same as DVDD	5	V
Shunt resistor	BOM RS1	0.5	mΩ
Potentiometer control	Enable hardware potentiometer	Enable	
Control scheme	Select command parameter	Speed control	
Catch spin start	Catch start a rotating motor	Enable	
PWM modulation type	Select PWM modulation scheme Refer to section 4.1	High-side sync	
Minimum pot. input	Minimum potentiometer input level	5	%
Stall detection time	Delay on stall detection response	1.2	Seconds

[1] In 6PWM mode the dead-time is set by the microcontroller or 6EDL7141, whichever is greater. In other modes it is set by the 6EDL7141.

Graphical user interface

Stall min. amplitude	When amplitude of setpoint is below this value, stall detection is disabled	10%	%
Stall	Enable/disable stall detection	Enable	
Overvoltage threshold	DC-link overvoltage threshold	30	V
DC-link overvoltage	Enable/disable overvoltage protection	Enable	
Undervoltage threshold	DC-link undervoltage threshold	16	V
DC-link undervoltage	Enable/disable undervoltage protection	Enable	
TRAP	Enable/disable overcurrent protection	Enable	
Wrong Hall	Enable/disable incorrect Hall sensor connection detection and shutdown	Enable	
Hall learning	Enable/disable Hall sensor learning	Enable	
SPI timeout error	Enable/disable SPI timeout error	Enable	
PWM frequency	PWM switching frequency	20	kHz
Dead-time rising	PWM dead-time for rising edge	0.44	µs
Dead-time falling	PWM dead-time for falling edge	0.44	µs
DC bus compensation	Enable/disable DC bus compensation	Disable	
Current sense delay	Current sense ADC trigger delay from center of PWM on-time	0.75	µs
Maximum duty cycle	Maximum PWM output duty cycle	100	%
Demag blanking time	Demagnetization blanking time for skipping DC-link current measure after PWM commutation	100	µs
Phase advance speed	Phase advance starting speed, advance angle increase linearly above this speed	1000	RPM
Phase advance angle	Maximum phase advance angle (at maximum speed), set 0 to disable phase advance	30	Degrees
Ramp-up time	Ramp-up time from zero to maximum speed	0.5	Seconds
Ramp-down time	Ramp-down time from maximum speed to zero	0.5	Seconds
Ramp-down hold voltage	Maximum DC-link voltage that allows ramp-down, ramp-down will be hold if DC-link voltage above the threshold	28	V
Speed control rate	Speed control execution rate in number of PWM cycles	1	
Speed K_P	P-I control parameter: proportional	200	
Speed K_I	P-I control parameter: integral	10	
Speed P-I limit	Speed P-I regulator voltage output limit	100	%

6.2 Configuring the 6EDL7141 parameters

The PWM configuration and gate driver parameters can be selected by expanding the “PWM and Three Phase Gate Driver” menu and selecting each parameter from the options available.

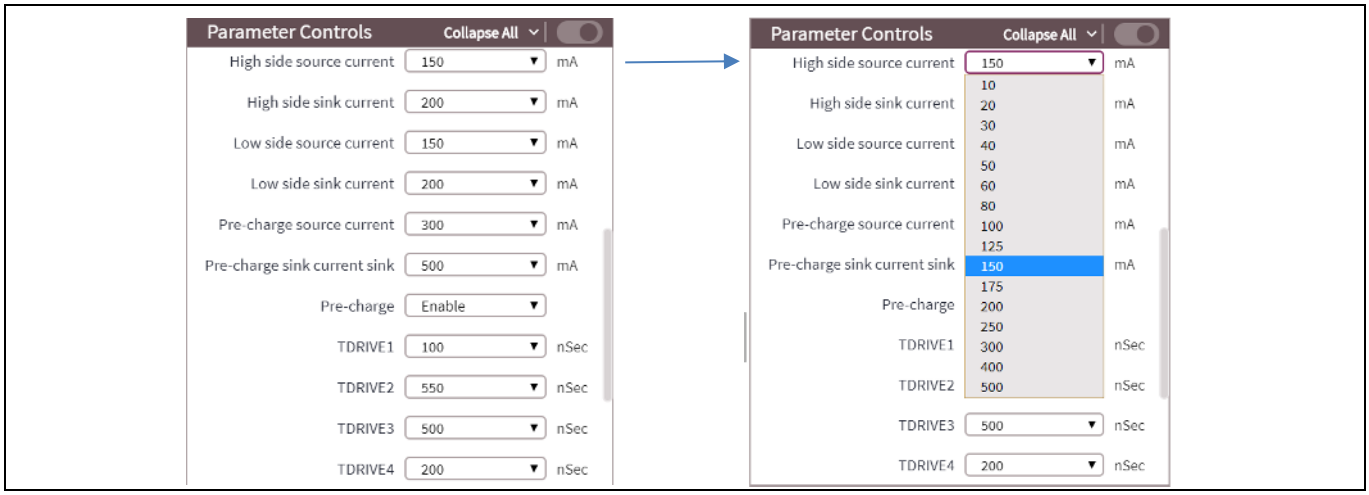

Figure 45 Selecting the gate drive parameters

The GUI enables configuration of all of the 6EDL7141 selectable parameters, including the on-board power supply and charge pump settings and the current sense amplifiers and overcurrent protection thresholds as discussed in previous sections.

Once all of the firmware options and 6EDL7141 parameters have been selected for a design, the project should be saved via the “Project” menu at the top of the screen. The project file has a .6EDL extension.

The target board containing the 6EDL7141 can be connected to the PC via an XMC™ Link debugger; however, this is not necessary for the EVAL_6EDL7141_TRAP_1SH evaluation board, which has its own on-board debugger and can be connected directly to a USB port on the PC. The 6EDL7141 can be programmed with the selected values using the following options:

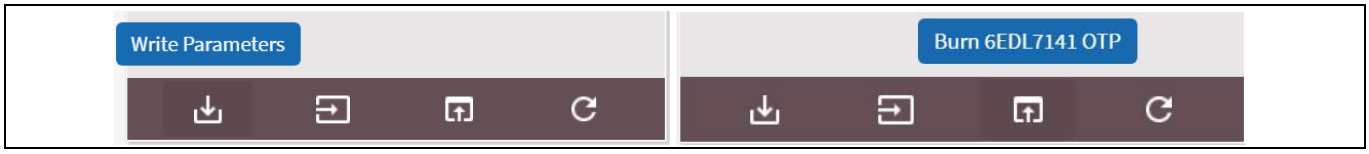

Figure 46 Transferring the settings to the 6EDL7141

The “Write Parameters” option transfers the configuration to volatile memory, which will remain only while the 6EDL7141 is powered. This option should be used during bench testing and optimization until the designer is completely satisfied that all of the correct values have been selected. If values are changed during bench evaluation, the project should be saved again. When the designer is sure that the final values have been obtained, the “Burn 6EDL7141 OTP” option may be used to permanently set the configuration in the one-time programmable (OTP) memory.

Graphical user interface

Table 6 List of additional 6EDL7141 parameters

Parameter	Value	Unit
Power supply		
PVCC setpoint	12	V
Charge pump clock frequency	781.25	kHz
Charge pump spread spectrum	Enable	
Charge pump pre-charge	Disable	
Buck converter frequency	500	kHz
DVDD setpoint	V_SENSE pin	
DVDD soft-start time	100	µs
DVDD turn-on delay	200	µs
DVDD OCP threshold	450	mV
PWM and three-phase gate driver[1]		
PWM mode	6 PWM	
PWM freewheeling mode	Active FW	
Brake configuration	Low-side	
Alternate recirculation	Disable	
Pre-charge	Enable	
Current sense and OCP		
Amplifier A	Disable	
Amplifier B	Enable	
Amplifier C	Disable	
Amplifier gain	8x	
Amplifier gain analog select	Disable	
Amplifier mode	Shunt resistor	
Internal offset selection	¼ DVDD	
Use external offset	Disable	
Amplifier timing mode	GLx high	
Amplifier blanking time	1000	ns
Amplifier auto zero	Internal trigger	
OCP positive threshold	300	mV
OCP negative threshold	-300	mV
PWM truncation	Enable	
OCP deglitch time	8	µs
OCP fault trigger	8 events	
OCP fault latching	Disable	
Brake on OCP	Enable	
Negative OCP	Enable	

[1] Refer to Table 3 for parameters not listed here

Graphical user interface

Housekeeping		
Hall sensor deglitch time	640	ns
Overtemperature shutdown	Enable	
ADC measurement filter	8	
APC PVDD measurement filter	32	
Watchdog (WD) timer	Disable	
WD input selection	EN_DRV	
WD fault report	Status reg. only	
WD period time	100	µs
Buck converter WD	Enable	
Rotor lock detection time	1	s
Rotor lock detection	Disable	
WD fault latching	Disable	
Brake on WD timer overflow	Disable	
WD DVDD restart delay	0.5	ms
WD DVDD restart attempts	0	
User ID	0	

6.3 Using the GUI to control the board

The GUI is also able to operate and monitor a 6EDL7141-based motor drive inverter such as the EVAL_6EDL7141_TRAP_1SH through its test bench screen, which is shown in the figure below:

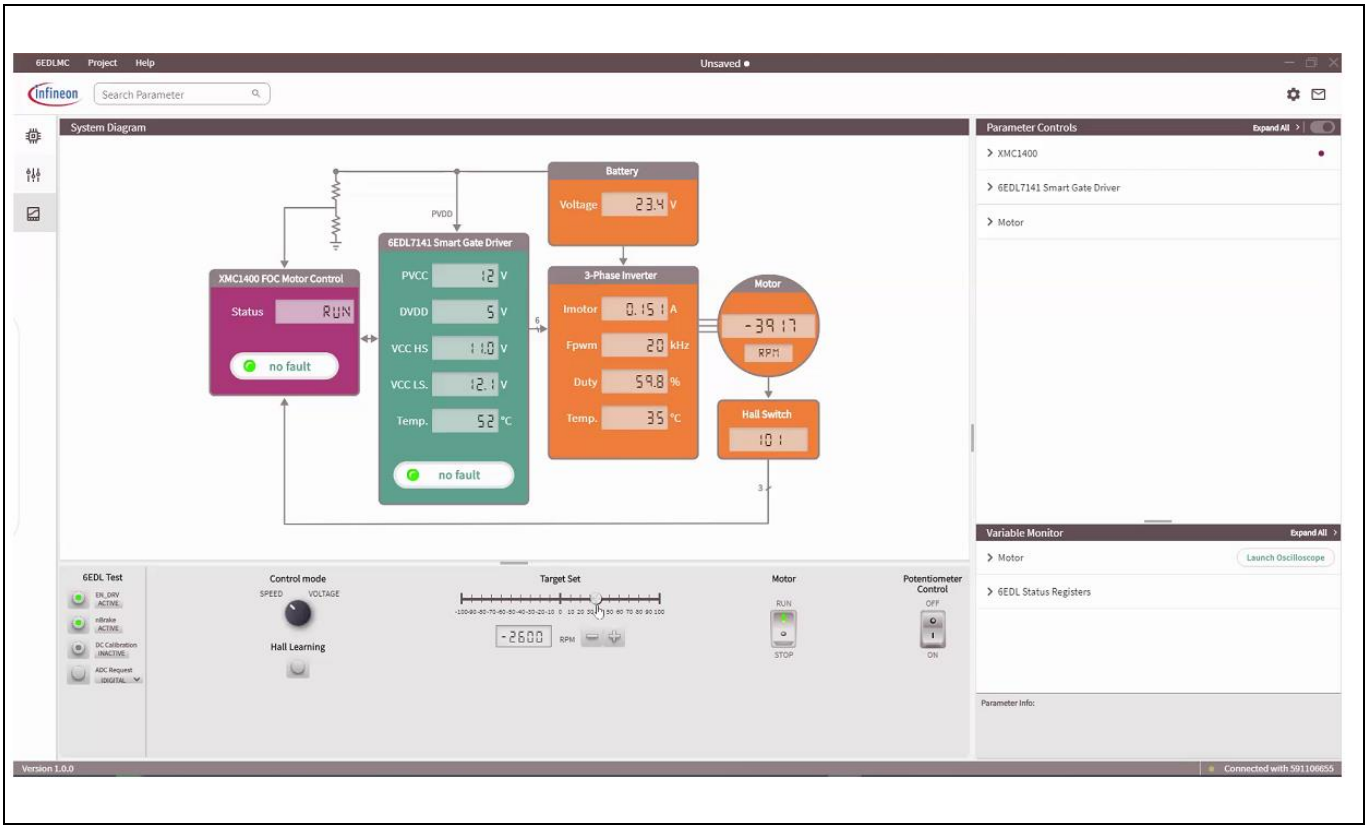

Figure 47 GUI test bench screen

The test bench screen provides a real-time display of the system parameters such as the power supply, internal regulator, and charge pump voltages as well as the battery input voltage. It also indicates the rotor revolutions per minute (RPM), the motor current, the PWM switching frequency and duty cycle, and also the 6EDL7141's temperature from its integrated sensor. Fault status is also indicated.

In addition to monitoring, the motor direction and speed can also be commanded from this GUI screen using the "Target Set" slider control in the lower area of the screen. The motor can be started or stopped via the motor switch and the board-mounted speed control potentiometer can also be enabled and disabled. In order to control the speed through the GUI, the potentiometer control switch on the right must be in the off position.

7 Bill of materials

Reference	Qty	Value/Rating	Manufacturer	Part number
C01, C2, C324	3	270 µF/35 V/20%	United Chemi-Con	EKZE350ELL271MH20D
C3, C20, C28	3	2.2 µF/50 V/0603	Murata	GRM188R61H225KE11D
C4, C18, C26, C36, C37	5	4.7 µF/50 V/0805	Murata	GRM21BR61H475KE51L
C5, C6, C7, C8, C9, C10, C11, C12	8	2.2 µF/50 V/0603	Murata	GRM188R61H225ME11D
C13, C14, C21, C23, C29, C31	6	33 nF/100 V/0603	TDK	CGA3E3X8R2A333K080AB
C16, C57	2	0.1 µF/25 V/0402	Samsung	CL05A104KA5NNNC
C19	1	330 pF/50 V/0402	Murata	GCM155R71H331KA37D
C25	1	100 pF/25 V/0402	KEMET	C0402C101J3GACTU
C30, C32	2	2.2 µF/25 V/0805	Samsung	CL21A225KAFNNNG
C33	1	0.22 µF/50 V/0805	KEMET	C0805C224K5RACAUTO
C34	1	0.1 µF/10 V/0402	Samsung	CL05A104KP5NNNC
C35	1	10 µF/10 V/0402	Samsung	CL05A106MP5NUNC
C38	1	0.1 µF/50 V/0603	Yageo	CC0603KRX7R0BB104
C39	1	0.22 µF/25 V/0402	Murata	GRT155R61E224ME01D
C40, C41	2	22 µF/20%/16 V	Samsung	CL10A226MO7JZNC
C42	1	10 µF/25 V/0805	Samsung	CL21A106KAFN3NE
C43, C45, C47, C49, C50	5	220 nF/10 V/0402	TDK	GRM155R61A224KE19J
C44, C46, C48, C51, C58	5	1 µF/10%/25 V	Samsung	CL10A105KA8NNNC
C52, C53, C54, C55	4	10000 pF/25 V/0603	AVX	06033D103KAT2A
C56	1	1 µF/10%/10 V/0402	Murata	GRM155C81A105KA12D
C301, C305, C306, C308, C309, C310, C311, C312, C318, C319, C320	11	100 nF/25 V/0402	Vishay Vitramon	VJ0402Y104KXXCW1BC
C302, C303	2	15 pF/25 V/0402	Walsin Technology	0402N150J250CT
C304	1	10 nF/25 V/0402	KEMET	C0402C103J3RACAUTO
C307	1	4.7 µF/25 V/0603	Taiyo Yuden	TMK107BBJ475MA-T

Bill of materials

C313, C315	2	10 µF/16 V/0603	TDK	GRM188R61E106MA73J
C314	1	10 nF/16 V/0402	KEMET	C0402C103J3RACAUTO
C316, C317	2	1 µF/6.3 V/0402	Taiyo Yuden	JMK105BJ105KV-F
C321, C322, C323	3	2200 pF/50 V/0402	TDK Corporation	C1005X5R1H222K050BA
D1	1	100 V/2 A/SMA	ST Microelectronics	STPS2H100AY
D2, D3, D4, D5, D8	5	5.1 V/500 mW	ON Semi	MM5Z5V1T1G
D6, D7	2	30 V/500 mA/SC79-2	Infineon	BAS3005A02VH6327XTSA1
D14	1	TVS diode/22 V/35.5 V/SMA	Diodes	SMAJ22A-FDICT-ND
D301	1	30 V/1 A/SOD323	Infineon	BAS3010A-03W
D302	1	TVS diode/5.3 V/TSLP-3	Infineon	ESD5V3U2U-03LRH E6327
F1	1	10 A/32 V AC/63 V DC	Littelfuse	0458010.DR
HS1	1	Heatsink 40 x 20 x 12 mm	Alpha Novatech	LPD4020-10B
IC301	1	XMC4200_QFN48	Infineon	XMC4200Q48K256BAXUMA1
IC302	1	IFX54441LDV	Infineon	IFX54441LDVXUMA1
IC303	1	SI866X	Silicon Labs	634-SI8662BB-B-IS1
IC304	1	74LVC1G126GW	Nexperia	74LVC1G126GW,125
J1, J2, J4, J5, J6	5	Banana Jack	Keystone Electronics	476-4
J3	1	Jack 5.5 x 2.1 mm	Tensility International Corp	54-00129
J9	1	Conn. header vert./8POS/2.54 mm	Adam Tech	PH2-08-UA
LED1, LED4, LED302	3	LED red clear	Osram	LS Q976-NR-1
LED2	1	LED blue diffused	Osram	LB Q39G-L2OO-35-1
LED3, LED5, LED301	3	LED green diffused	Rohm	SML-D12M8WT86
L1	1	22 µH/1.2 A/4020	Bourns	SRP4020TA-220M
L301	1	Ferrite bead/60 Ω/0603 1LN	Würth Elektronik	74279267
POT1	1	10k pot. 1-turn	Bourns	3362P-1-103TLF
Q1, Q2, Q3, Q4, Q5, Q6	6	40 V, 0.7 mΩ, SuperSO8 5x6 package	Infineon	BSC007N04LS6

Bill of materials

Q301	1	Crystal/12.0000 MHz/8 pF/SMD	Kyocera	CX3225GA12000D0PTVCC
RS1	1	500 µΩ/3 W/2512/1%	TE Connectivity	TLR3A30ER0005FTDG
RT1	1	Low-power linear active thermistor ICs	Microchip	MCP9700T-E/TT
R1, R8, R16, R23, R34, R37	6	1 Ω/0.1 W/0603/1%	Yageo	RC0603FR-071RL
R2	1	75k/0.1 W/0603/1%	Panasonic	ERJ-3EKF7502V
R3, R7, R17, R25, R35, R40, R48, R320, R321, R322, R323	11	0 R/0.1 W/0402	Panasonic	ERJ-2GE0R00X
R5	1	7.87k/0.1 W/0603/1%	Yageo	RC0603FR-077K87L
R6, R24, R38	3	56k/0.1 W/0603/1%	Yageo	RC0603FR-0756KL
R10, R29, R42	3	5.6k/0.1 W/0603/1%	Panasonic	ERJ-3EKF1651V
R11	1	100k/0.1 W/0603/1%	Yageo	RC0603FR-07100KL
R13	1	22k/0.1 W/0603/1%	Yageo	RC0603FR-0722KL
R14	1	3.3k/0.1 W/0402/1%	KOA Speer Electronics	RK73B1ETTP332J
R15	1	470 R/0.1 W/0402/1%	Panasonic	ERJ-2RKF4700X
R18	1	1.8k/0.063 W/0402/0.1%	Panasonic	ERA-2AEB182X
R19, R22, R26, R33, R39, R50, R62, R63	8	5.1k/0.1 W/0402/5%	Panasonic	ERJ-2GEJ512X
R44, R312, R309, R311	4	10k/0.063 W/0402/5%	Yageo	RC0402JR-0710KL
R45, R46	2	10k/0.1 W/0603/5%	Yageo	RC0603JR-0710KL
R51	1	1k/0.1 W/0603/1%	Yageo	RC0603FR-071KL
R53, R54, R55	3	2.2k/0.1 W/0603/1%	Yageo	RC0603FR-072K2L
R56, R57, R58	3	3.3k/0.1 W/0603/1%	Yageo	RT0603FRE073K3L
R61	1	100 R/0.063 W/1%/0402	Yageo	RC0402FR-07100RL
R64	1	200 R/0.1 W/0603/1%	Yageo	AC0603FR-07200RL
R301, R302	2	680 R/0.063 W/0402/1%	Vishay Dale	CRCW0402680RFKEDC
R303	1	82k/0.1 W/0603/1%	Panasonic	ERJ-3EKF8202V
R304	1	48.7k/0.1 W/0603/1%	Yageo	RC0603FR-0748K7L

Bill of materials

R305	1	510 R/0.1 W/0402/1%	Panasonic	ERJ-U02F5100X
R306, R307	2	22 R/0.1 W/0402/5%	Panasonic	ERJ-2GEJ220X
R308	1	4k7/0.1 W/0402/1%	Panasonic	ERJ-2RKF4701X
R310, R314	2	1 M/0.1 W/0402/1%	Yageo	RC0402FR-071ML
R315, R316	2	0 R/0.1 W/0603	KOA Speer Electronics	RK73Z1HTTC
R317	1	3k/0.063 W/0402/1%	Yageo	RC0402FR-073KL
R318	1	32.4k/0.063 W/0402/1%	Bourns	CR0402-FX-3242GLFCT-ND
R319	1	1k/0.063 W/0402/1%	Yageo	RT0402FRE071KL
ST1, ST2, ST3, ST4	4	Hex Standoff Threaded #4-40 Aluminum 0.250" (6.35mm) 1/4" -	Keystone Electronics	8714
SW1	1	Slide switch SPDT/200 MA/30 V	E-Switch	EG1218
SW2	1	Slide switch SPST/0.4 VA/28 V	NKK Switches	AS11CP
U2	1	Three-phase smart gate driver	Infineon	6EDL7141
U3	1	32-bit microcontrollers with ARM® Cortex®-M0	Infineon	XMC1404-Q064X0200 AA
X3	1	Conn. term. block/2.54 mm/5POS	Phoenix Contact	MPT 0,5/ 5-2,54 - 1725685
X4, X5	2	Header/4 x 1/TH/0.025 sq/100 mil/SP	Molex, Amp	PH1-04-UA
X302C	1	Conn. receptor/USB2.0/MICRO AB/SMD RA	Würth Elektronik	629105150921

8 Motor specifications

The motor used for obtaining the results presented here is a QBL4208-61-04-013 BLDC motor with three Hall sensors positioned at 120-degree relative angles, manufactured by Trinamic Motion Control GmbH. The specifications are as follows:

- Hall effect angle: 120-degree electric angle
- Shaft run-out: 0.025 mm
- Insulation class: B
- Radial play: 0.02 mm, 450 G load
- Max. radial force: 28 N (10 mm from flange)
- Max. axial force: 10 N
- Dielectric strength: 500 V DC for 1 minute
- Insulation resistance: 100 MΩ min. 500 V DC
- Recommended ambient temp.: -20°C to +40°C
- Bearing: Brushless motors fitted with ball bearings

Table 7 QBL4208 motor technical data

Specifications	Unit	QBL 4208			
		-41-04-006	-61-04-013	-81-04-019	-100-04-025
No. of poles		8	8	8	8
No. of phases		3	3	3	3
Rated voltage	V	24	24	24	24
Rated phase current	A	1.79	3.47	5.14	6.95
Rated speed	RPM	4000	4000	4000	4000
Rated torque	Nm	0.0625	0.125	0.185	0.25
Maximum peak torque	Nm	0.19	0.38	0.56	0.75
Torque constant	Nm/A	0.035	0.036	0.036	0.036
Line to line resistance	Ω	1.8	0.72	0.55	0.28
Line to line inductance	mH	2.6	1.2	0.8	0.54
Maximum peak current	A	5.4	10.6	15.5	20
Length (L_{MAX})	mm	41	61	81	100
Rotor inertia	$kgm^2 \times 10^{-6}$	24	48	72	96
Mass	kg	0.3	0.45	0.65	0.8

Motor specifications

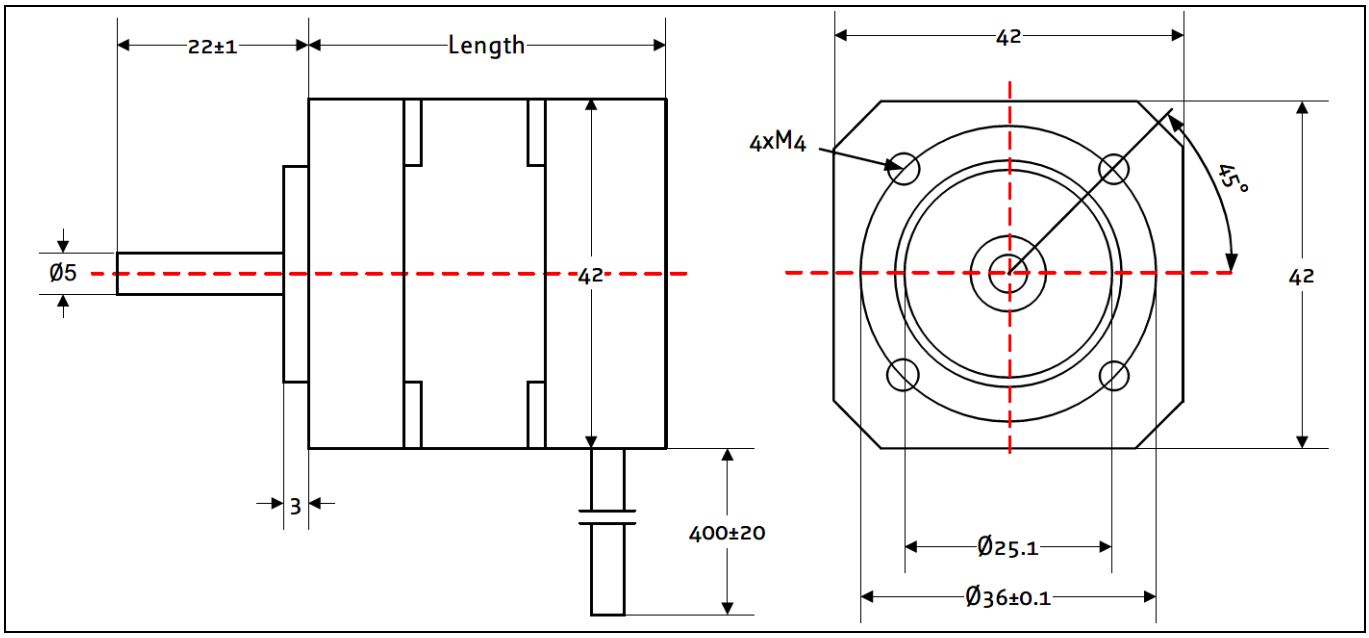

Figure 48 QBL4208-61-04-013 motor dimensions

9 PCB layout

The EVAL_6EDL7141_TRAP_1SH evaluation board utilizes a six-layer PCB with 2 oz. copper on the top and bottom layers and 1 oz. copper on the internal layers. Components are mounted on the top and bottom sides. The width is 3.0 inches/76.2 mm, and the length is 4.0 inches/101.6 mm.

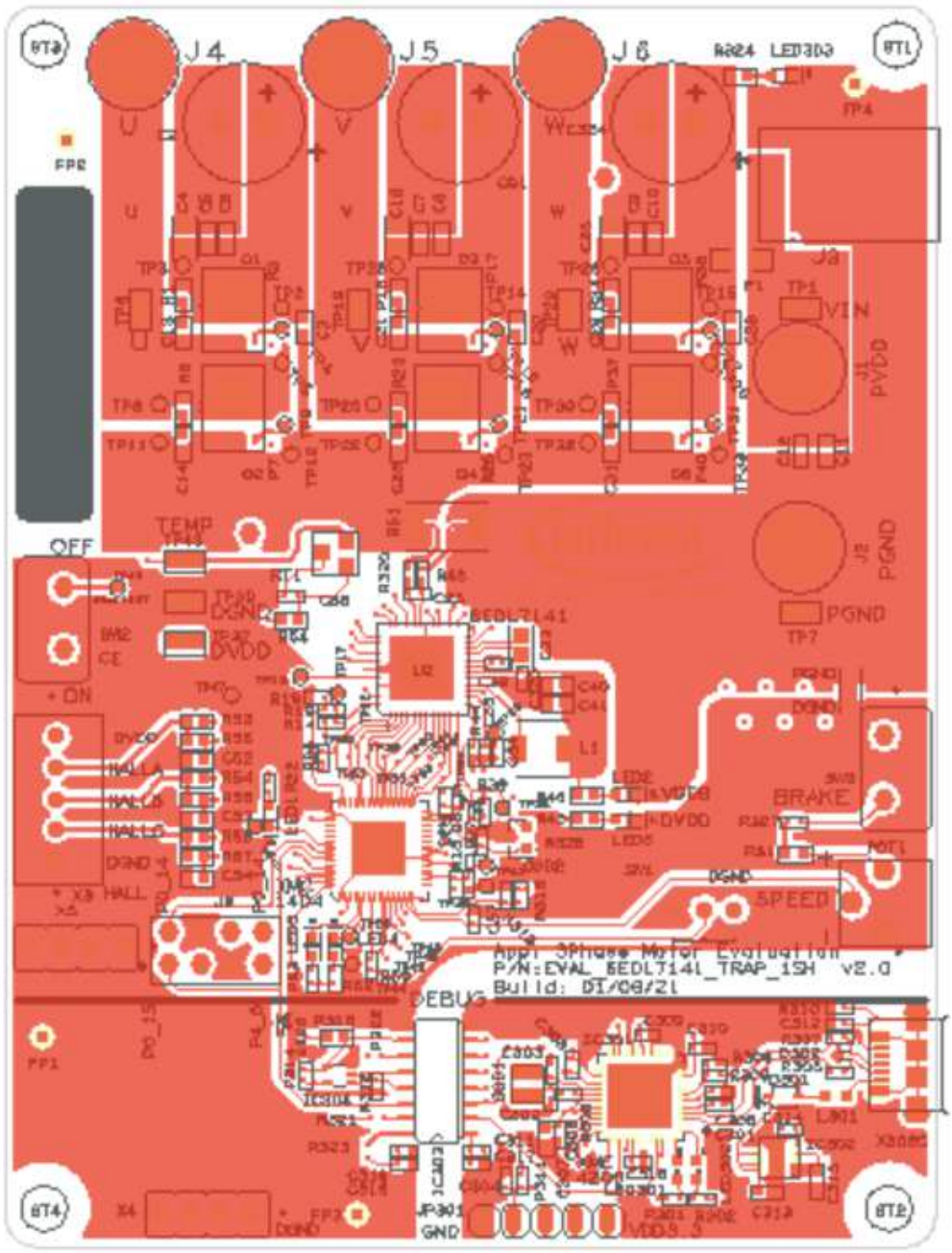

Figure 49 EVAL_6EDL7141_TRAP_1SH PCB top layer with silkscreen

PCB layout

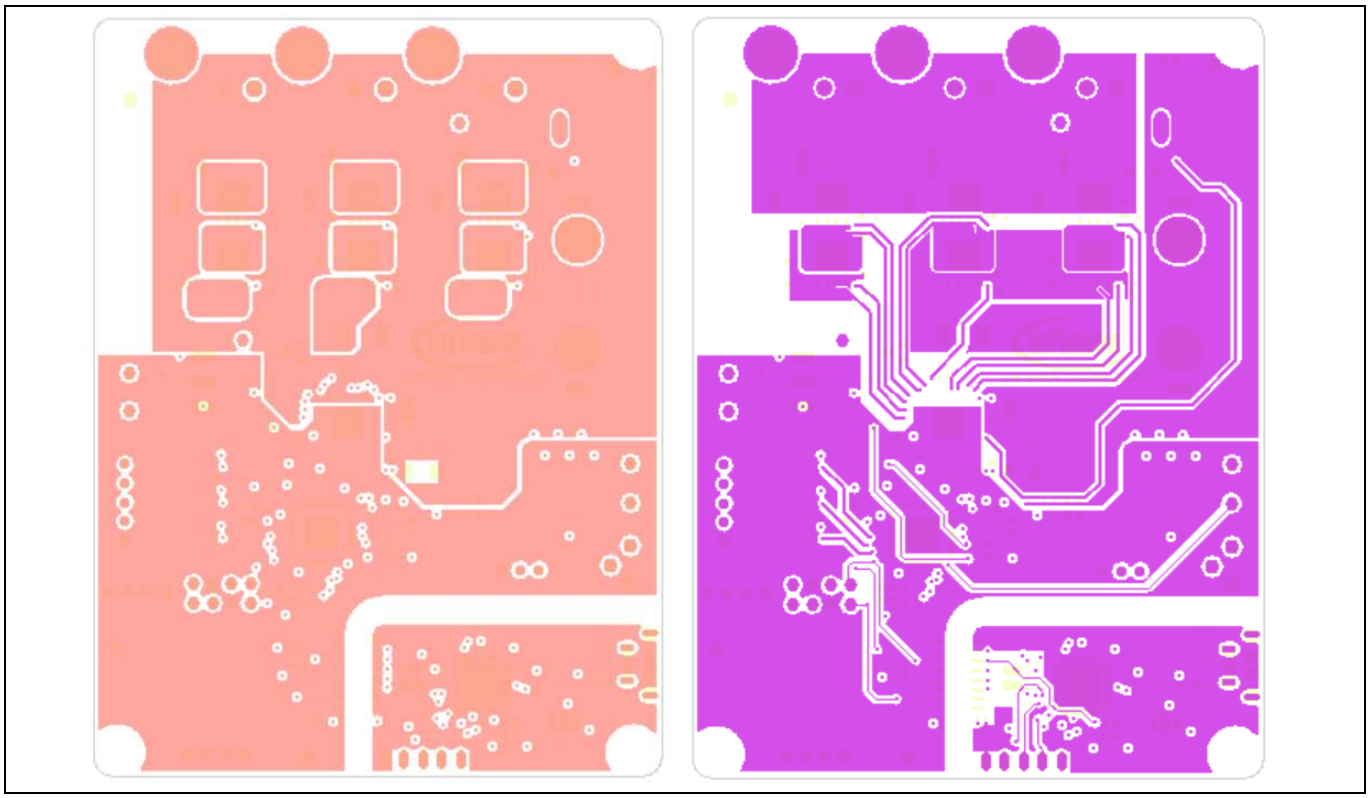

Figure 50 EVAL_6EDL7141_TRAP_1SH PCB internal layers 1 (left) GND and 2 (right)

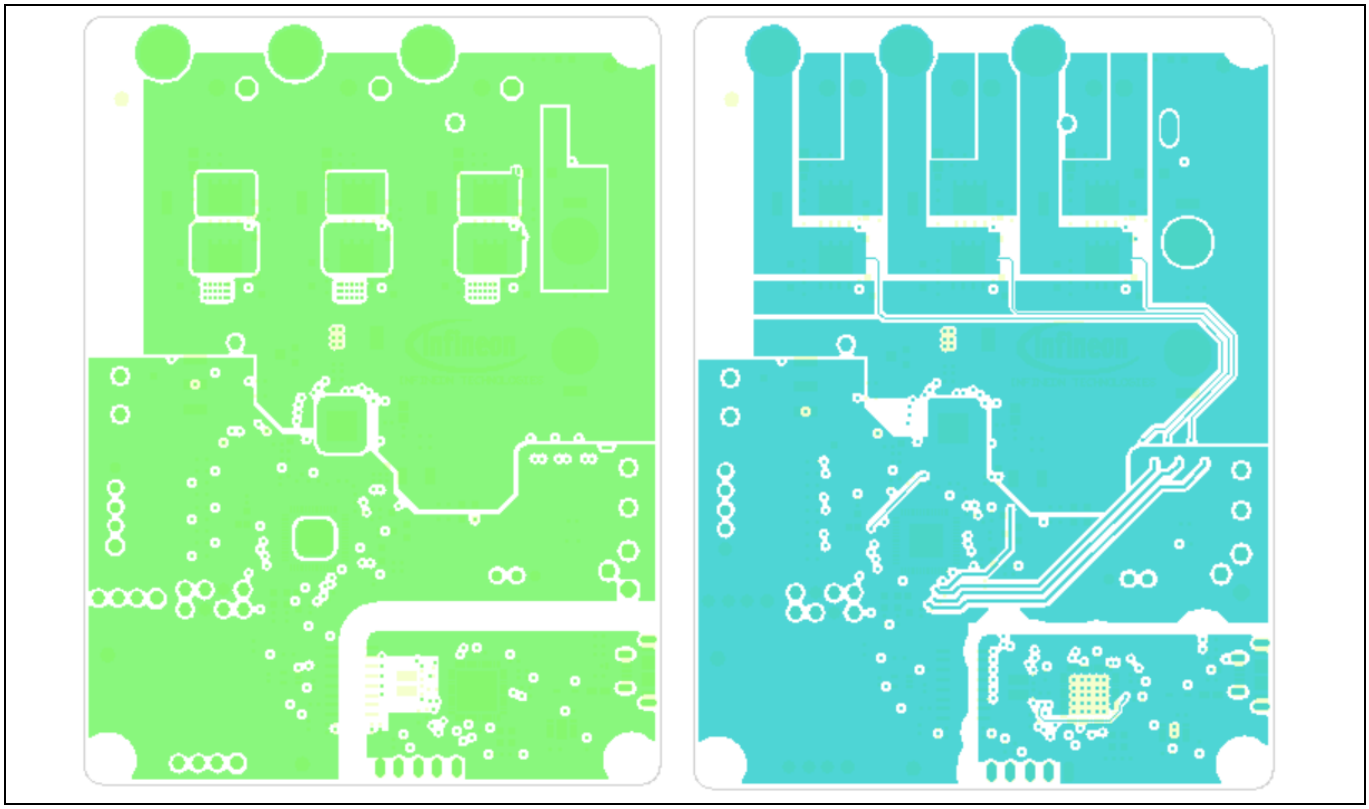

Figure 51 EVAL_6EDL7141_TRAP_1SH PCB internal layers 3 (left) DVDD and 4 (right)

PCB layout

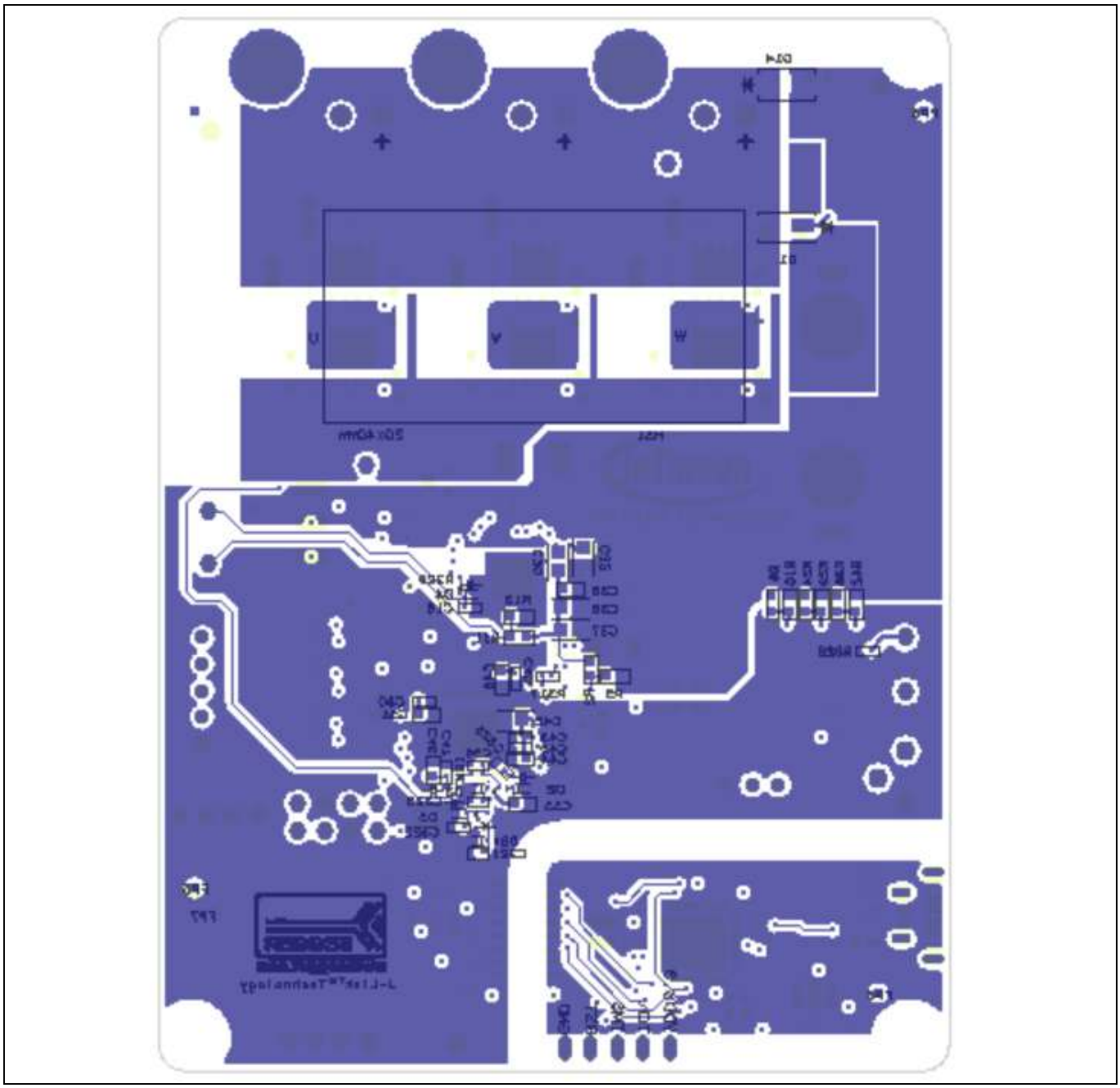

Figure 52 EVAL_6EDL7141_TRAP_1SH PCB bottom layer with silkscreen

The PCB layout is optimized to minimize radiated EMI. This is done by keeping the loops carrying the switching currents as small as possible. The high-frequency switching current loops are illustrated in the figure below. It should be noted that during the switching transition, the high-side gate drive loop current returns to the main ground rather than back to the gate driver as in a conventional high-side driver. Since this is the case, the high-side gate drive loop should also be kept as tight as possible. The top layer connects the DC bus to the top-side MOSFET drains; the first internal layer returns the MOSFET current via the current sense shunt. The switching loop for each phase begins and ends at the electrolytic capacitor and high-frequency decoupling capacitors. The return traces on the first internal layer pass underneath the power traces, thus creating very tight high-frequency switching loops.

PCB layout

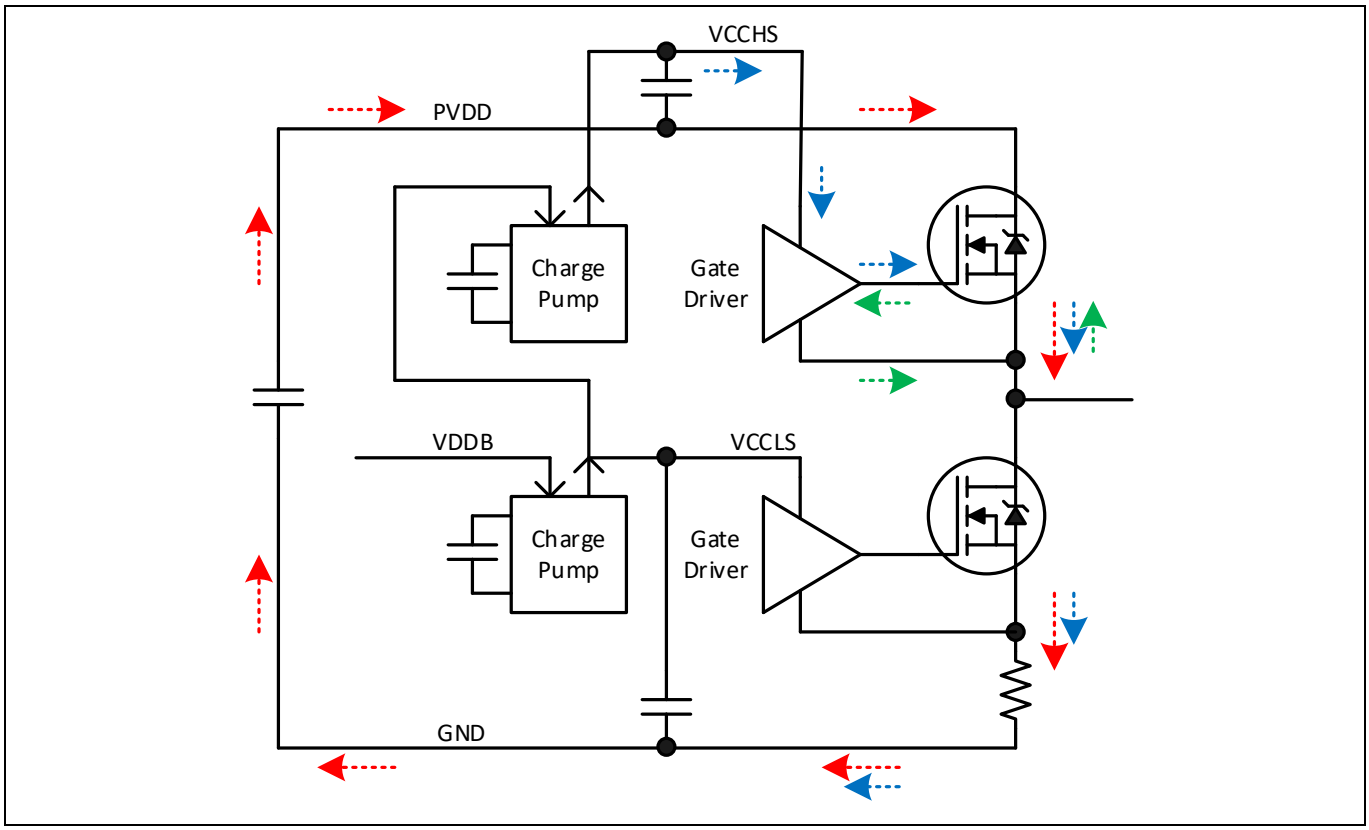

Figure 53 **High-frequency current loop for one phase**
Red: main HF switching loop; Blue: high-side gate drive switch on current loop; Green: high-side gate drive switch-off current loop

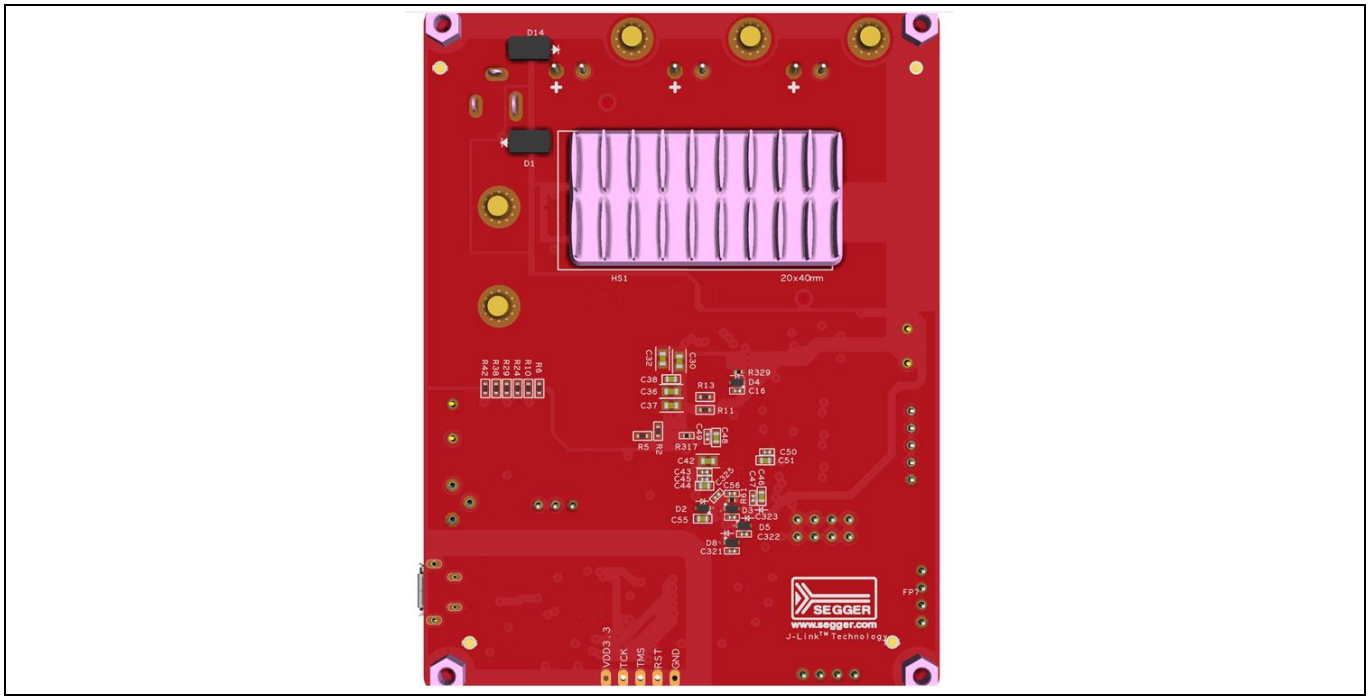

Figure 54 **Board underside with optional heatsink attached**

10 Test results

10.1 Operating waveforms

The following waveforms were captured with the EVAL_6EDL7141_TRAP_1SH board driving a motor at 1500 RPM with an input power of 300 W at 18 V input.

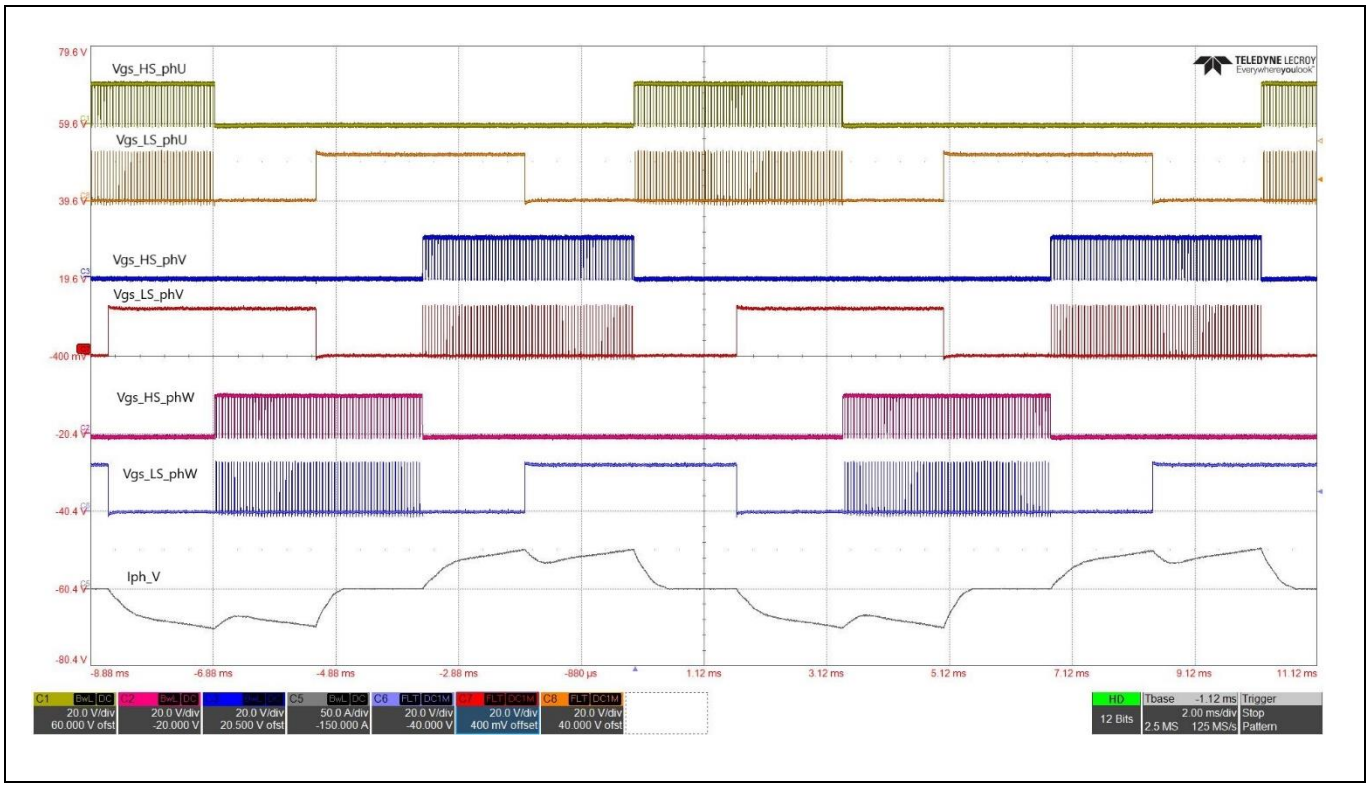

Figure 55 High- and low-side gate drive pulses (2 ms/div) $V_{GS\_HS\_phU}$ (yellow), $V_{GS\_LS\_phU}$ (orange), $V_{GS\_HS\_phV}$ (blue), $V_{GS\_LS\_phV}$ (red), $V_{GS\_HS\_phW}$ (pink), $V_{GS\_LS\_phW}$ (purple), I_{PHASE_phV} (gray)

The waveforms above show the high-side PWM with synchronous rectification of the low-side in accordance with **Figure 23**, though the direction of motor spin is opposite and therefore the waveforms for phases V and W are swapped. The phase current waveform displays the classic trapezoidal/six-step profile.

Test results

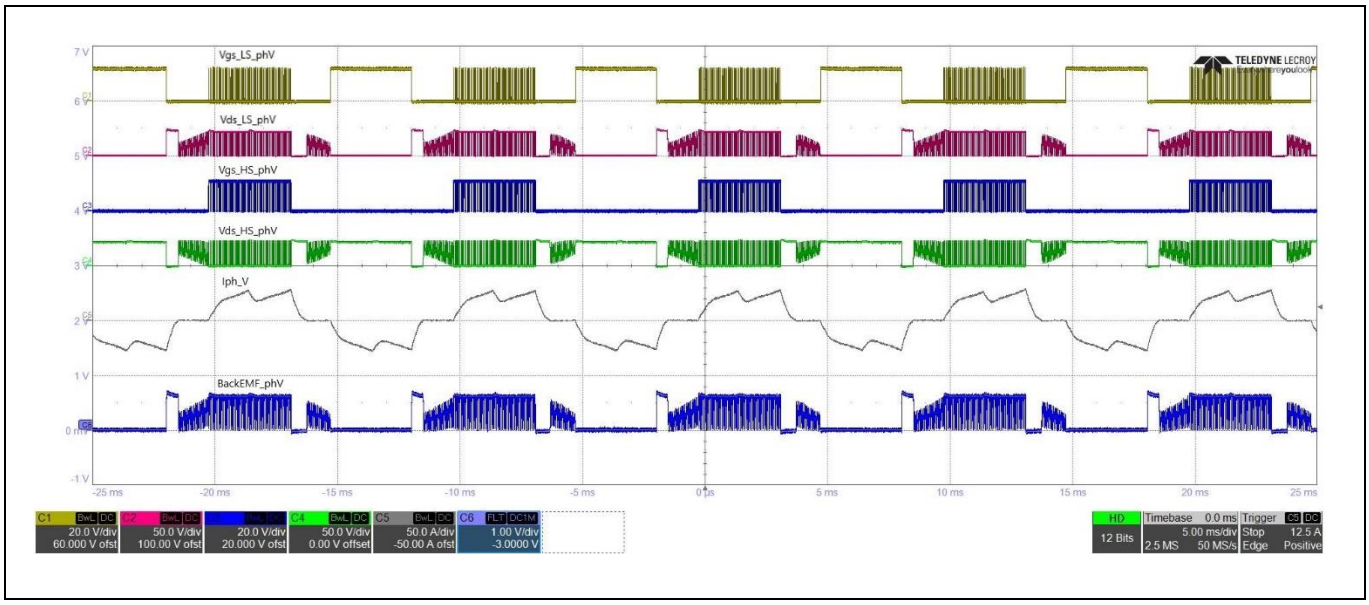

Figure 56 Phase “V” waveforms (5 ms/div)
V_{GS_LS} (yellow), V_{DS_LS} (red), V_{GS_HS} (blue), V_{DS_HS} (green), I_{PHASE} (gray), back EMF (blue)

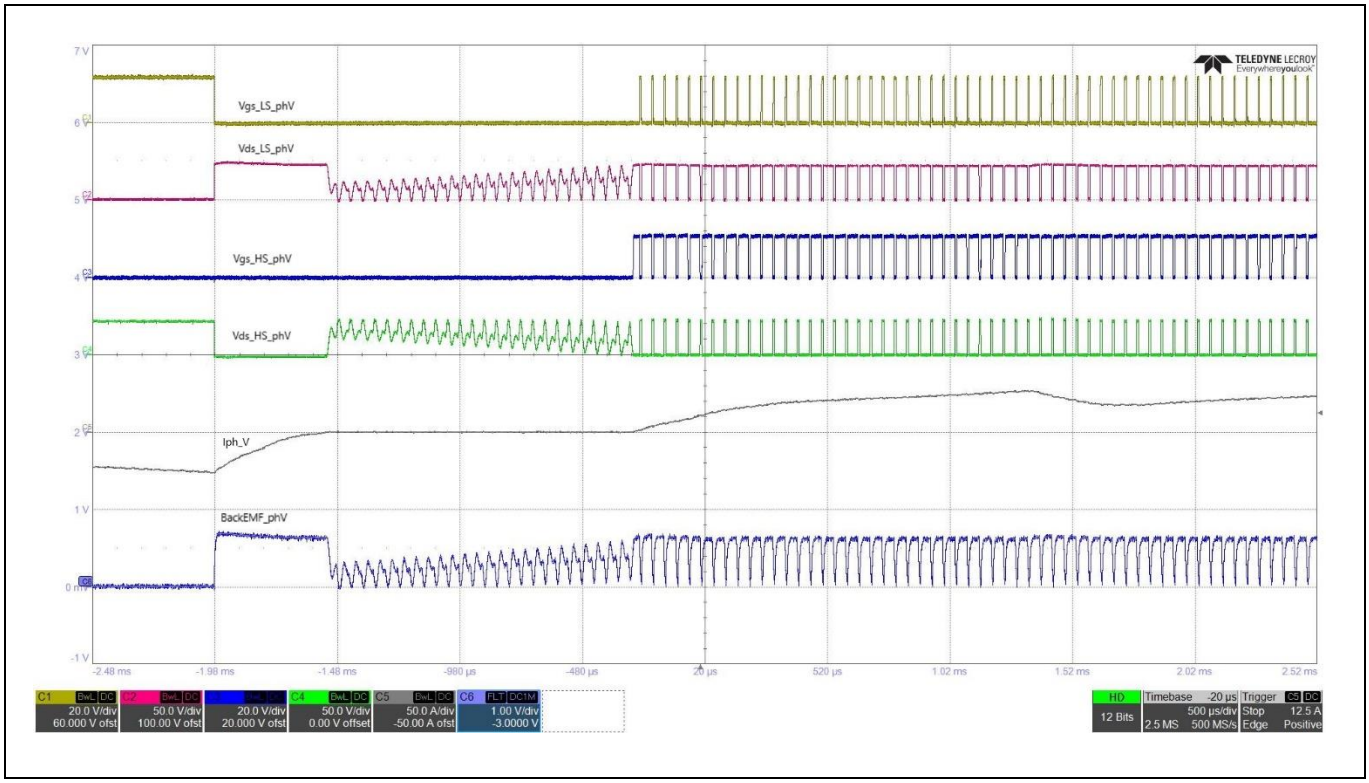

Figure 57 Phase “V” waveforms (500 µs/div)
V_{GS_LS} (yellow), V_{DS_LS} (red), V_{GS_HS} (blue), V_{DS_HS} (green), I_{PHASE} (gray), back EMF (blue)

Test results

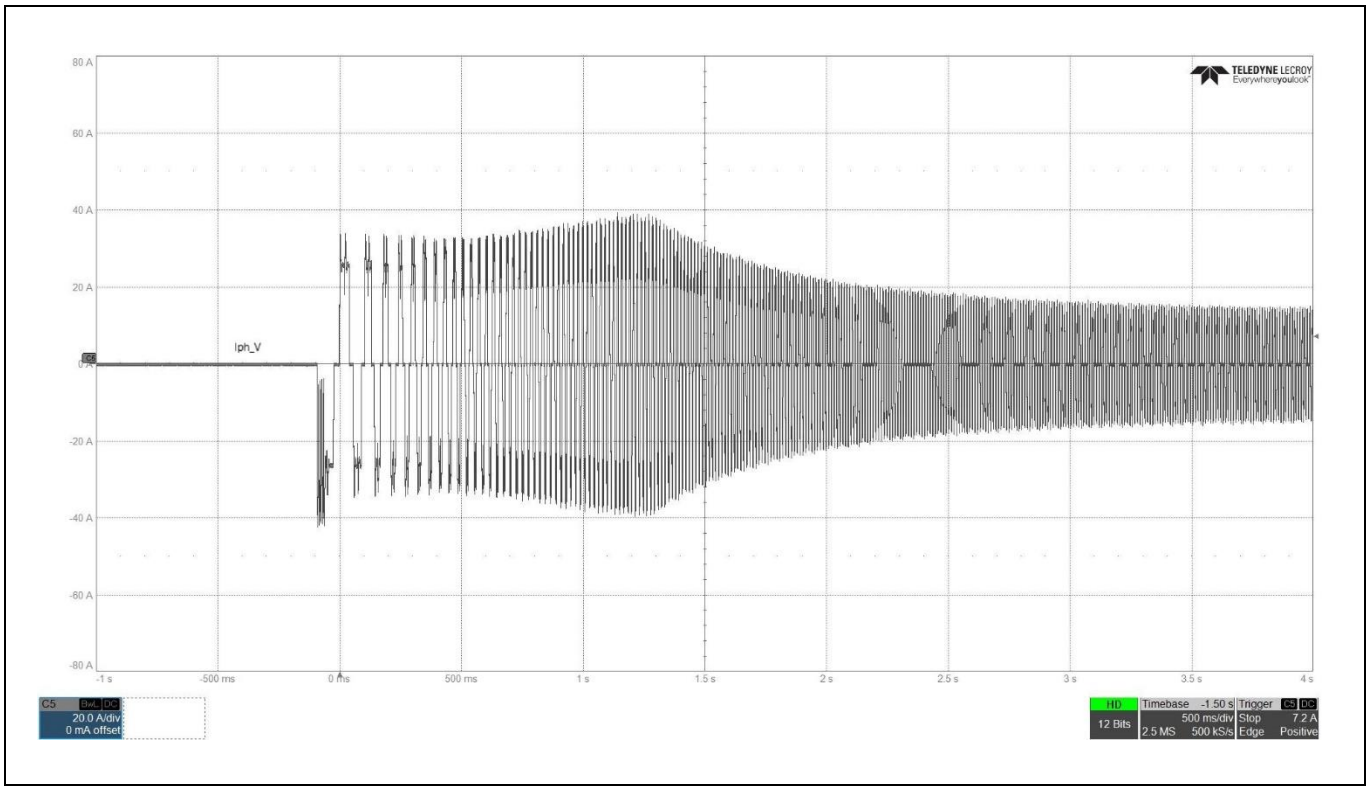

Figure 58 **Phase “V” start current (500 ms/div)**
I_{PHASE} (gray)

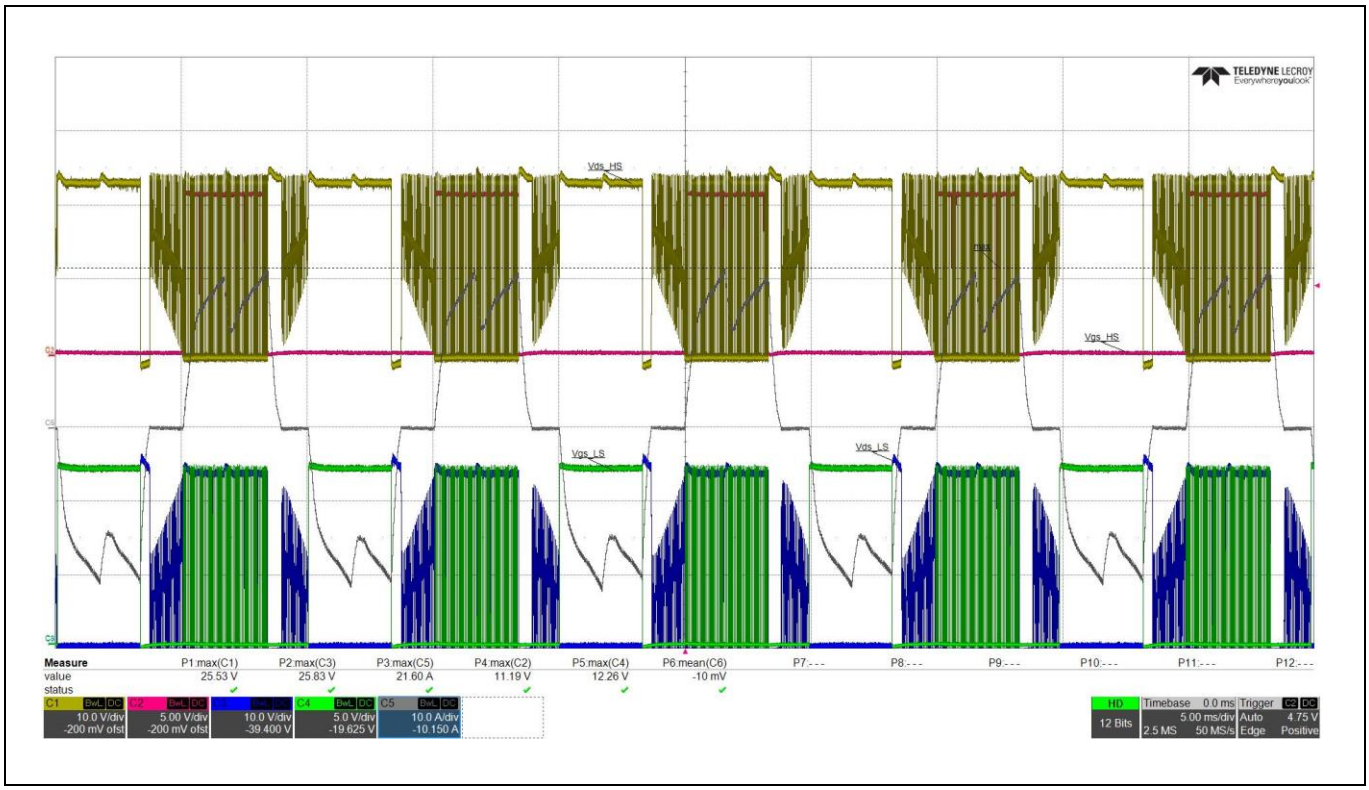

Figure 59 **Phase “V” waveforms for 24 V input at 300 W (5 ms/div)**
V_{GS_LS} (green), V_{DS_LS} (blue), V_{GS_HS} (red), V_{DS_HS} (yellow), I_{PHASE} (gray)

Test results

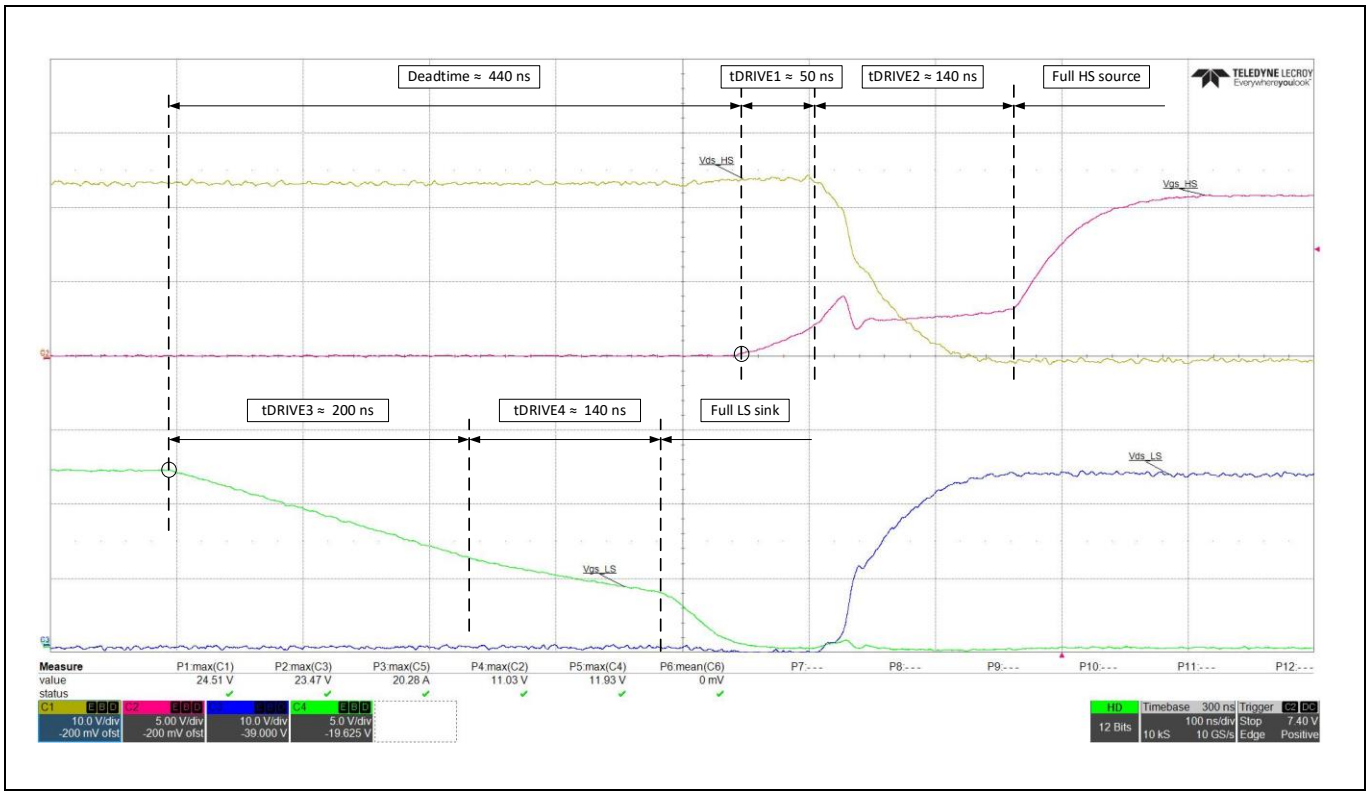

Figure 60 **Phase "V" node positive transition for 24 V input at 300 W (100 ns/div)**
V_{GS_LS} (green), V_{DS_LS} (blue), V_{GS_HS} (red), V_{DS_HS} (yellow)

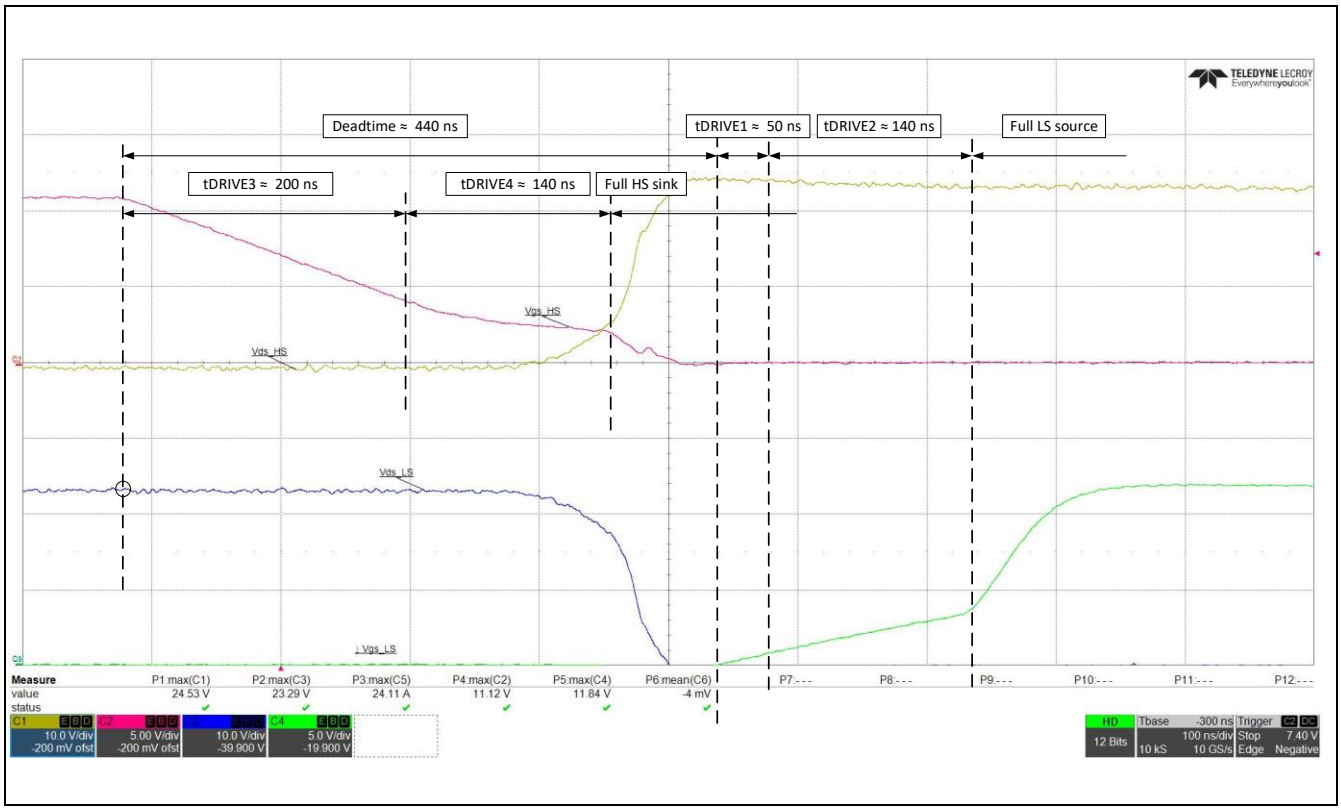

Figure 61 **Phase "V" node negative transition for 24 V input at 300 W (100 ns/div)**
V_{GS_LS} (green), V_{DS_LS} (blue), V_{GS_HS} (red), V_{DS_HS} (yellow)

Test results

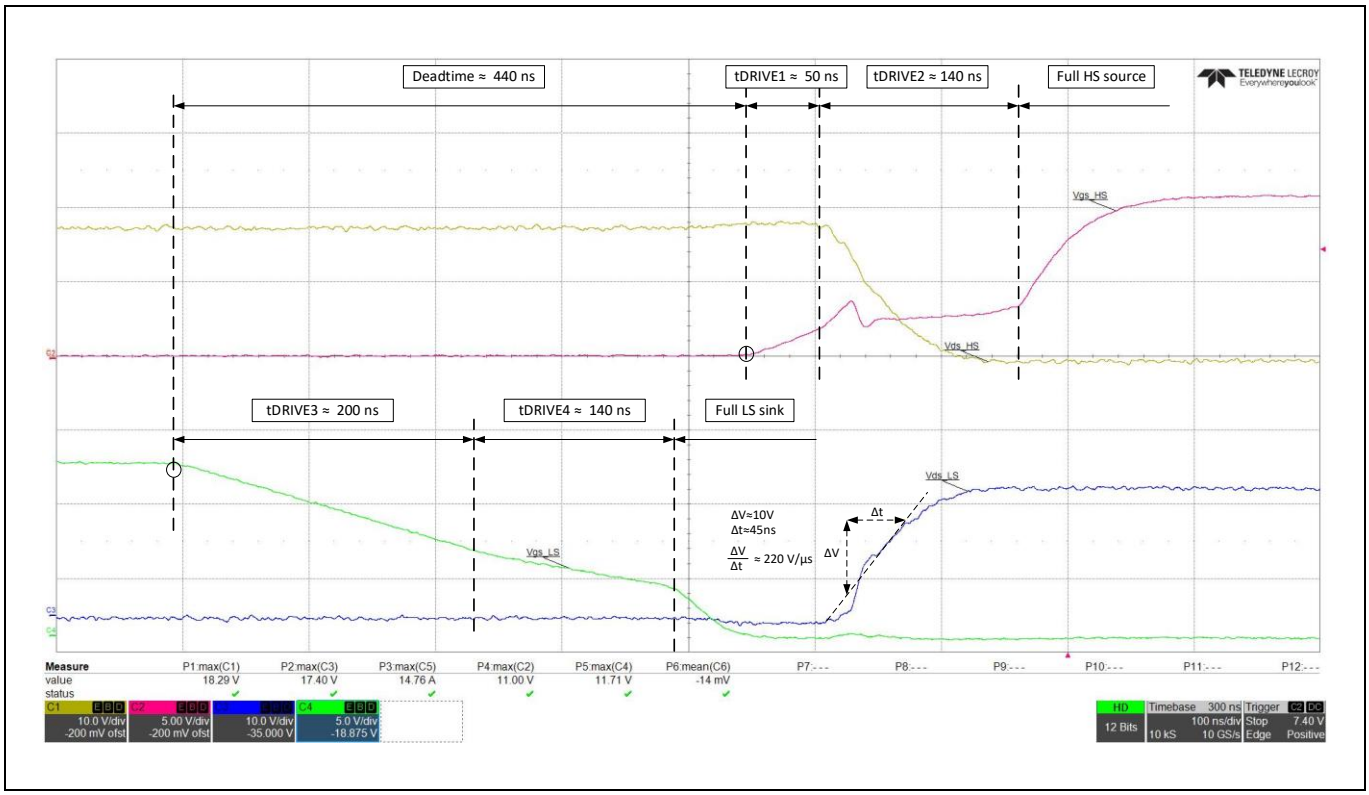

Figure 62 Phase "V" node positive transition for 18 V input at 300 W (100 ns/div) V_{GS_LS} (green), V_{DS_LS} (blue), V_{GS_HS} (red), V_{DS_HS} (yellow)

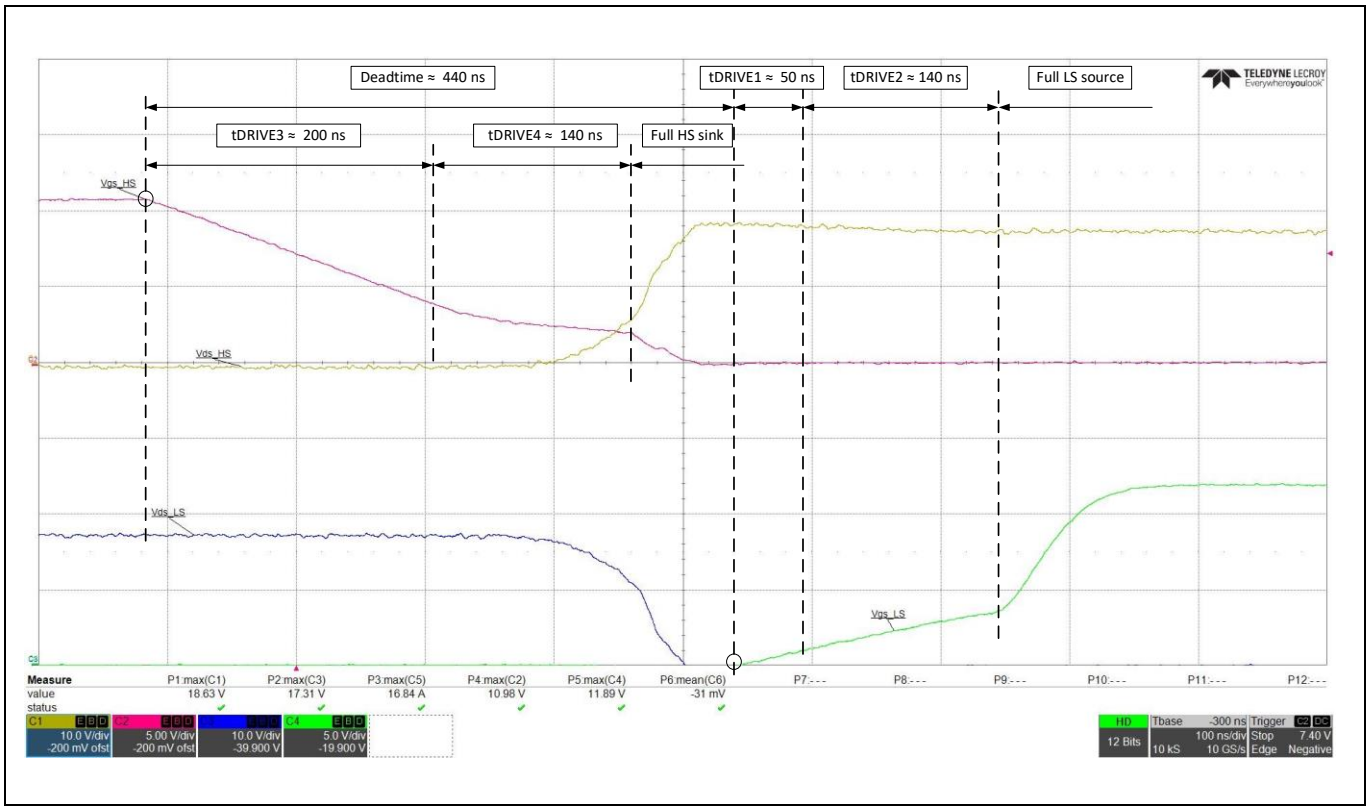

Figure 63 Phase "V" node negative transition for 18 V input at 300 W (100 ns/div) V_{GS_LS} (green), V_{DS_LS} (blue), V_{GS_HS} (red), V_{DS_HS} (yellow)

10.1 Power measurements

		Element 3	Element 4	Element 5	Element 6
Urms	[V]	18.021	7.319	7.287	7.314
Irms	[A]	17.886	15.522	15.670	15.499
P	[W]	0.3041 k	0.0908 k	0.0911 k	0.0913 k

Figure 64 Input and output measurements at nominal input voltage 18 V and 300 W input power

In the above results element 3 represents the DC input to the inverter. Elements 4, 5 and 6 are connected to the output phases U, V and W, respectively.

The total output power is equal to 90.8 W + 91.1 W + 91.3 W = 273.2 W for an input power of 304.1 W.

This gives an efficiency of 273.2/304.1 = 89.8 percent with losses of 30.9 W.

However, some of the losses can be attributed to the input and output cables so the true inverter efficiency is higher than this value. This is evidenced by the very moderate component temperature rise measurements in the following section.

		Element 3	Element 4	Element 5	Element 6
Urms	[V]	24.018	9.689	9.607	9.817
Irms	[A]	24.669	22.218	22.319	22.134
P	[W]	0.5553 k	0.1637 k	0.1602 k	0.1657 k

Figure 65 Input and output measurements at nominal input voltage 24 V and 500 W input power

The total output power is equal to 163.7 W + 160.2 W + 165.7 W = 489.6 W for an input power of 555.3 W.

This gives an efficiency of 489.6/555.3 = 88.2 percent with losses of 65.7 W.

Again, a proportion of the losses can be attributed to the input and output cables, so the actual inverter efficiency is higher. Component temperature rise measurements in the following section also indicate this to be the case.

10.2 Thermal measurements

Thermal images were taken after 15 minutes of operation to allow the component temperatures to rise and reach steady-state. No heatsinking or forced air-cooling was used.

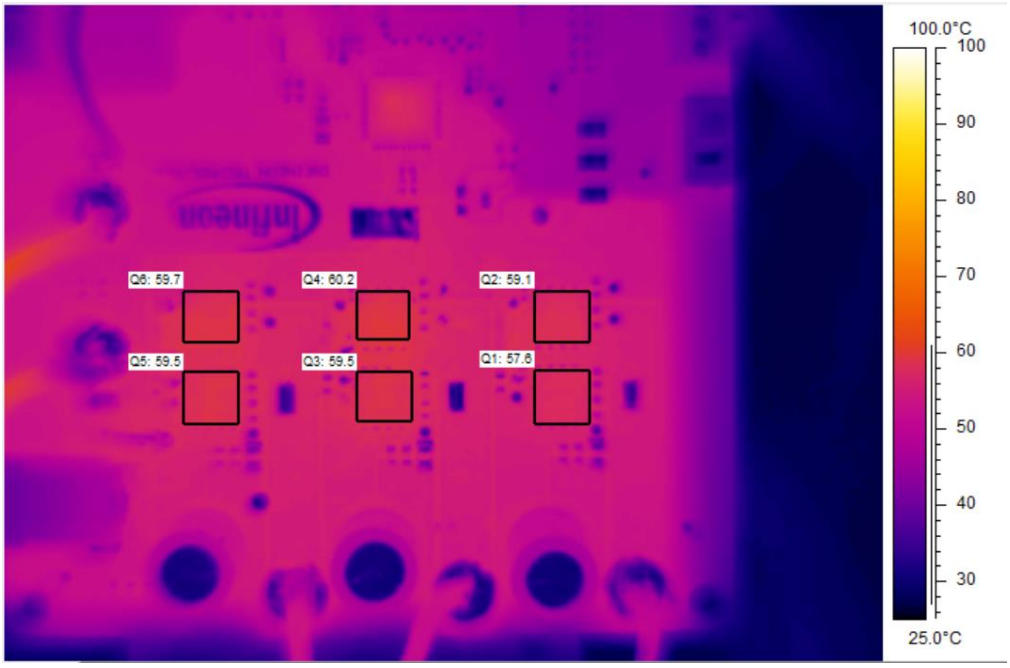

Figure 66 Thermal measurements at 18 V input and 300 W load

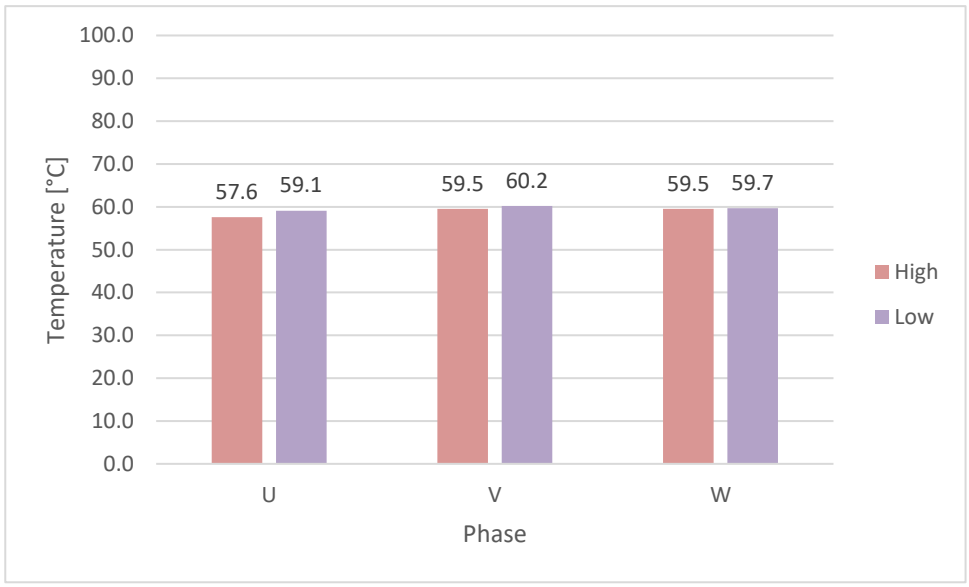

Figure 67 Thermal measurement summary at 18 V input and 300 W load

Test results

The temperature rise at 18 V input and 300 W input power is only 35°C. The voltage was increased to 24 V and the load increased to raise the input power to 500 W, with the following results:

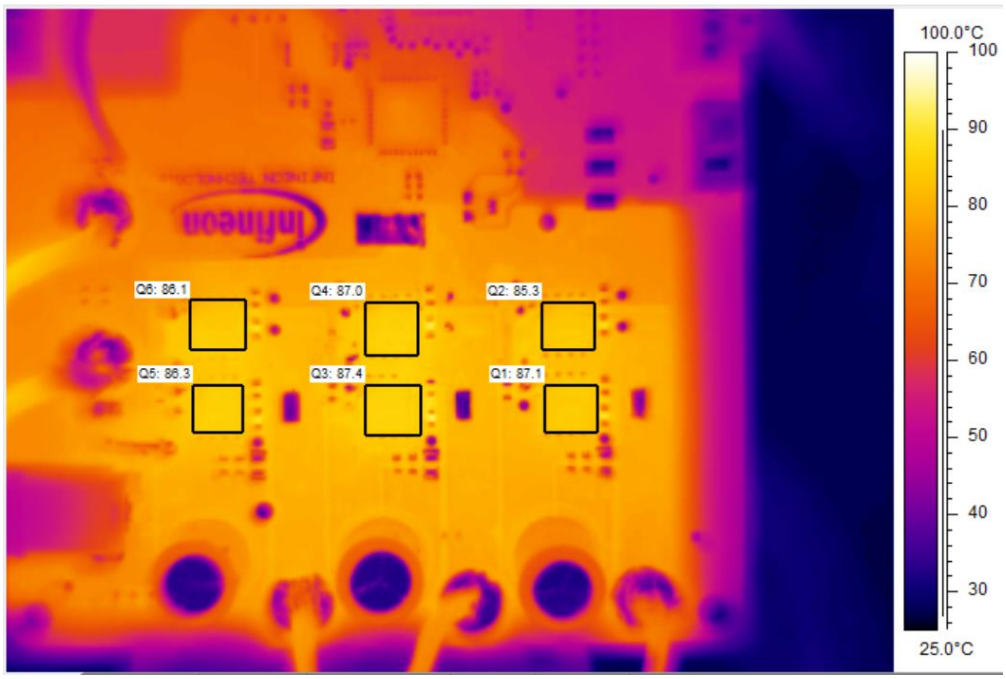

Figure 68 Thermal measurements at 24 V input and 500 W load

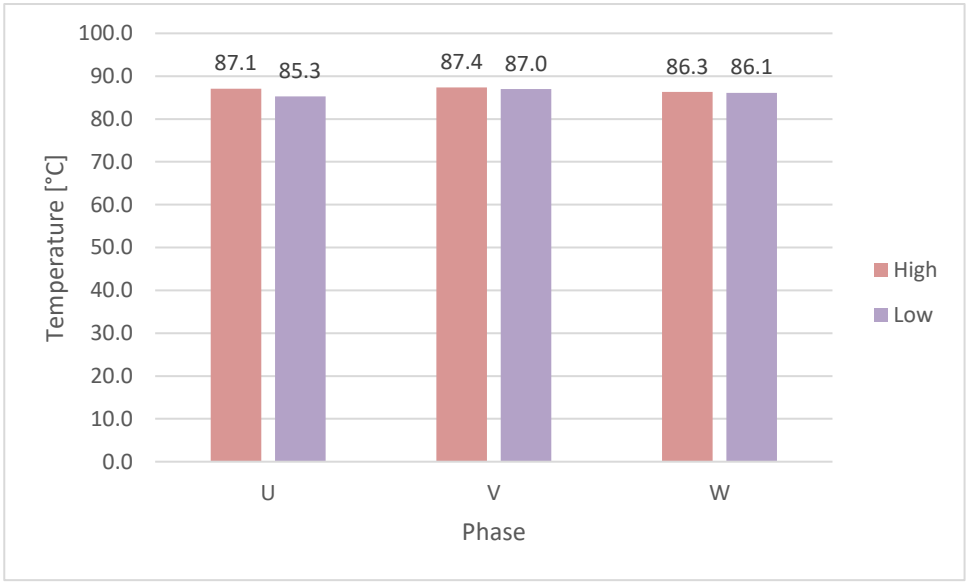

Figure 69 Thermal measurement summary at 18 V input and 300 W load

It can be seen that the temperature rise is less than 65°C and in both cases the difference in case temperatures between all of the inverter MOSFETs is negligible.

11 Conclusion

The EVAL_6EDL71141_TRAP_1SH evaluation board meets specifications, and the features and versatility of the 6EDL7141 have been demonstrated. The principle of operation, design of the circuitry, control scheme and PCB layout have all been discussed. The motor speed, direction and braking may be controlled locally with switches and a potentiometer located on the board or may be controlled by the GUI tool. The extensive capabilities of the GUI tool have been explained. The calculation method for the gate drive parameters has been shown and the results verified in the test waveforms. The ability to install customized firmware and configuration parameters to the system greatly simplifies the design process, eliminates unnecessary components and is thereby able to simplify product development and reduce time to market.

It is noted that due to the non-linearity of the hard-switched dVds/dt waveform that occurs at high-side, switch-on initiates the positive transition of the phase node. The measured slew rate of 220 V/µs is higher than the target value of 150 V/µs. A moderately high margin of error is to be expected in this calculation not only due to non-linearity but also due to expected tolerances in the gate charge and gate drive current values. Allowing for this, the benefits of the 6EDL7141 configurable gate drive outputs are clearly seen and the switching performance has been shown without the need for any gate drive resistors or diodes. In this design example a fairly slow slew rate (dVds/dt) was chosen to minimize EMI and V_{DS} switch-off transients. The test waveforms do not show any switch-off transients and therefore the slew rate could be further increased without risking MOSFET avalanche during switch-off. The drain-source snubber networks could also be removed to further reduce switching losses and improve efficiency.

The low-side switch-on is negligible; this occurs after the phase node voltage has already transitioned, as at high-side switch-off the phase current commutates to the low-side MOSFET body diode.

Thermal measurements show that the three-phase inverter BSC007B04LS6 best-in-class OptiMOS™ 6 switches in 5x6 PQFN SuperSO8 (TDSON-8 FL) packages offer excellent performance without the need to attach a heatsink up to 500 W of input power. By attaching a heatsink to the underside of the board the power handling ability of this driver could be further increased.

12 References

[1] Infineon Technologies, **6EDL7141 datasheet**

[2] Infineon Technologies, Sensored trapezoidal control firmware design in EVAL_6EDL7141_TRAP_1SH

[3] Infineon Motor Handbook, Version: 2.1, Release date: December 3, 2019
Institute for Power Electronics and Electrical Drives, RWTH Aachen University:
Fang Qi, Daniel Scharfenstein, Claude Weiss
Infineon Technologies AG: Dr. Clemens Müller, Dr. Ulrich Schwarzer

[4] Infineon Technologies, Application Note AN_1911_PL88_2001_203254, **Block commutation vs. FOC in power tool motor control**, V 1.0, November 2019

[5] Infineon Technologies, Application Note AP32359, **BLDC motor control software using XMC™**, V 1.0, January 2017

[6] Infineon Technologies, Application Note ER_201612_PL16_04, **ME/MF Direct™ FET Kit, DEMO-PTOOL-300W-M**, V 1.0, December 2016

[7] Faulhaber, Application Note 136, Block commutation with digital Hall sensors, Dr. Fritz Faulhaber & Co.

[8] Infineon Technologies, Application Note AP32359, BLDC motor control software using XMC™, V 1.0, January 2017

[9] Infineon Technologies, Application Note AP32370, **PMSM FOC motor control software using XMC™**, V 1.5, December 2018

[10] Infineon Technologies, White Paper, Power Loss and Optimized MOSFET Selection in BLDC Motor Inverter Designs – Understanding MOSFET power losses in block (trapezoidal) commutation, April 2016

[11] Infineon Technologies and RWTH Aachen University, Motor Handbook, Version 2.1, March 2019

[12] Wei-Feng Zhang and Yue-Hui Yu, Comparison of Three SVPWM Strategies, Journal of Electronic Science and Technology of China, Vol. 5, No. 3, September 2007

Revision history

Document version	Date of release	Description of changes
V 1.0	June 11, 2021	First release
V 1.1	November 15, 2021	Updated: Figure 1, Table 4, Figure 37 and added figure 54. Text updated section 4.2.1.3. Added firmware documentation reference [2].

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