5 Channel ACPI Regulator with Step-Down DC/DC Controller

General Description

The RT9643 is a combo regulator which is compliant to ACPI specification for desktop/motherboard power management and system application. The part features one switch regulator for DDR memory VDDQ power; three linear regulators including 1.5Amp peak sourcing/sinking capability regulator for DDR VTT, a 1.2V ultra-low-dropout linear controller for chipset miscellaneous power, a 3.3VSB power with 1.25Amp peak current capability; and 2 dual power control including 5VDL, and 3.3VDL control for S3 and S5 system power. The part totally feature 5 sets power which are compliant to ACPI specification into a single small footprint package VQFN-24L 5x5.

The part is generally operated to conform to ACPI specification, in S3 state, there are only VDDQ and 3.3VSB regulators remain on while the VTT and ULDO regulators are off. In the transition from S3 to S0, an external SS capacitor is attached for linear regulators to control its slew rates respectively to avoid inrush current induced. Moreover, the PGOOD signal raises high in S0 stage while all 3 regulators go stable. In the stage of S5 (EN = 0), there only 3.3VSB LDO remain on, while the other regulators are powered down. The VDDQ PWM regulator is a voltage mode implementation with external compensation to provide high load transient response. The VTT is regulated to follow 1/2 of VDDQ and is capable of sourcing or sinking 1.5A peak currents.

Ordering Information

RT9643 □□

- Package Type
  QV : VQFN-24L 5x5 (V-Type)
- Operating Temperature Range
  P : Pb Free with Commercial Standard
  G : Green (Halogen Free with Commercial Standard)

Note :

Richtek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

Features

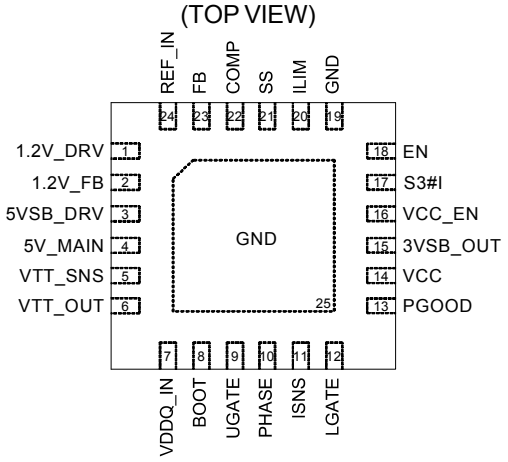
- **Integrated 5 Channels Power Regulator**
  - **DC/DC Buck PWM Regulator for V_{DDQ} (2.5V or 1.8V)**
  - **Linear Regulator Supports 1.5Amp Peak Sinking/ Sourcing Capability for VTT**
  - **1.2V Ultra-Low-Dropout Linear Controller for GMCH VTT Power**
  - **3.3VSB Linear Regulator Supports 1.25A Capability**
  - **5VDL Switch Control**
  - **3VDL Switch Control**
- **Conform to ACPI Specification**
  - **Support Power Management at S0, S3, and S5 State**
- **300kHz Fixed Frequency Switching**
- **$R_{DS(ON)}$ Current Sensing or Optional Current Sense Resistor for Precision Over-Current Detect**
- **Embedded Synchronous Boot-Strapped Diode**
- **Power Good Signal Indication for All Voltages**
- **Thermal Shutdown**
- **24-Lead VQFN Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- DDR VDDQ and VTT Voltage Generator with ACPI Support
- Desktop System Power
- Servers System Power

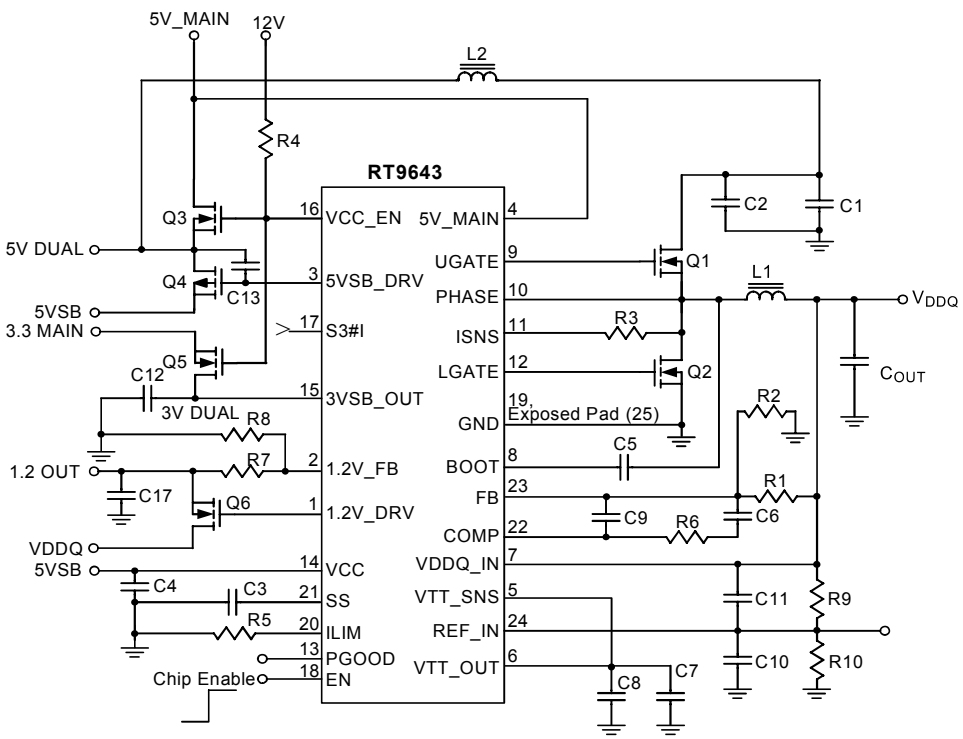
Pin Configurations

(TOP VIEW)



VQFN-24L 5x5

Typical Application Circuit



Operation

The RT9643 provides 5 functions:

1. A general purpose PWM regulator, used to generate VDDQ power for DDR memory.

2. A source-sink linear VTT regulator capable of sinking and sourcing 1.5A peak(minimum).

3. An adjustable Low Drop Out controller which, in conjunction with an external N-Channel power MOSFET, provides a programmable low voltage output. It normally provides 1.2V for GTL FSB termination voltage.

4. Generating a 5V DUAL voltage using an external N-channel to supply power from 5V MAIN in S0, and an external P-Channel to provide power from 5V Standby (5VSB) in S3.

5.An internal LDO which regulates "3V DUAL" in S3 mode from VCC(VSB). In S3, this regulator is capable of 1.25A peak currents with current limit protection (2A typ.).

100kΩ pull up resistor to V_{OUT} to obtain an output voltage. When the output voltage arrive 90% of normal value the power good will output voltage with 3ms delay time.

When the output voltage falling arrive 75% of normal value the power good will turn off with less than 1ms delay time. But, there are two exceptions. One is the enable pull low the power good will turn off quickly. The second is the V_{CC} falling arrive POR value (4V typ.) the power good also will turn off quickly.

Table 1. While S5àS0àS3

State	S3#I	EN(S5#)	VCC_EN	5VSB_DRV	VDDQ	VTT_OUT	1.2 OUT	3V Dual	5V Dual
S5	X	L	L	L	OFF	OFF	OFF	ON	OFF
S3	L	H	L	L	ON	OFF	OFF	ON	+5VSB
S0	H	H	H	H	ON	ON	ON	OFF	+5VMAIN

Start up Sequencing

The VCC pin provides power to all logic and analog control functions of the regulator including : After VCC is above UVLO, the start-up sequence begins as shown in Figure 1.

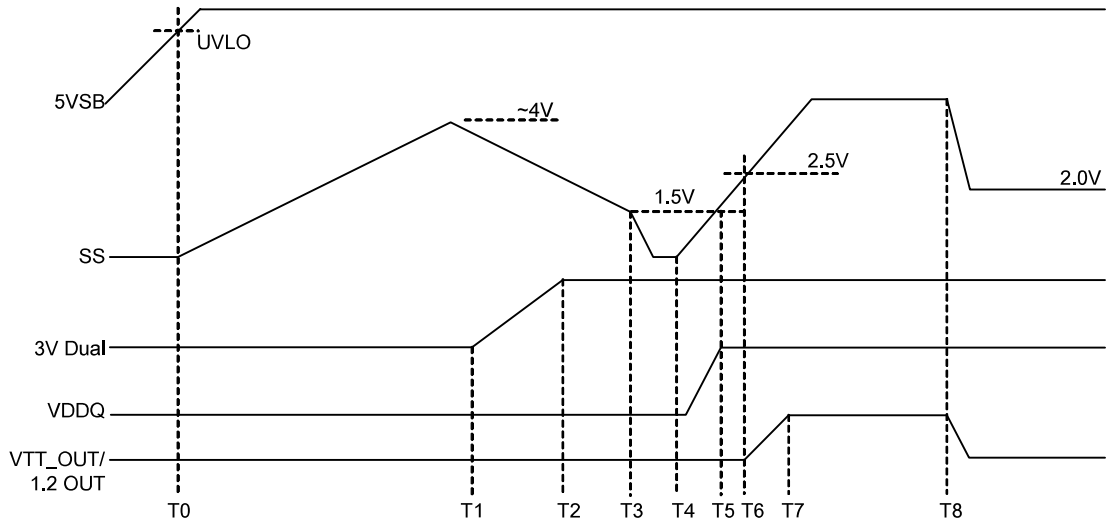


Figure 1

T0 to T3 : After initial power-up, the IC will ignore all logic inputs for a time period (T3-T0) of about :

$$T3 - T0 = \frac{6.5 \times C_{SS}}{5\mu}$$

The 3V Dual LDO is in regulation. The 3.3V LDO′s slew rate is limited by the discharge slope of C_{SS}. If 3V MAIN has come up prior to this time, the 3V DUAL node will already be pre-charged through the body diode of Q5 (see Figure 1).

T3 to T4 : The IC waits about 100μs before initiating soft-start on VDDQ to allow C_{SS} time to fully discharged. The IC is in "SLEEP" or S5 state when EN is low. In S5 only the 3.3V LDO is on. If the IC is in S5 at T4, C_{SS} will be held to 0V.

T4 to T5 : While First time to enter S0, The IC will start VDDQ only if 5V_MAIN is above its UVLO threshold (5V_MAIN o.k.) and S3#I is high.

T5 to T7 : After VDDQ is stabilized (when C_{SS} is above about 1.5V) which will allow the 1.2V LDO and the VTT LDO to soft start. To ensure that the VDDQ output is not subjected to large transient currents during transition, the VTT and 1.2V LDO slew rates are limited by the slew rate of the C_{SS} until the LDO is in regulation. In addition, the VTT regulator is current limited.

T8 (S0 to S3) : Dropping the S3#I signal. When this occurs, VCC_EN goes low, and the 3.3V LDO turns on. The 1.2V LDO and the VTT LDO are turned off, and C_{SS} is discharged to 2V. 5VSB_DRV pulls low to turn on the P-Channel 5V DUAL switch.

S3 to S0 : The system signals this transition by raising the S3#I signal. S0 mode is not entered until 5V_MAIN o.k..

Then the following occurs :

VCC_EN releases and pull high by external resistor.

5VSB_DRV pulls high to turn off the P-Channel switch.

The 3.3V LDO turns off.

The 1.2V LDO and the VTT LDO are turned on and C_{SS} is allowed to charge up

In most systems, the ATX power supply is enabled when S3#I goes to high. At that point, 5V_MAIN and 3.3 MAIN will start to rise. The RT9643 waits until 5V_MAIN is above 4.5V to turn on Q3 and Q5. This can cause about a 10% "bump" in both 5V DUAL and 3.3V DUAL when Q3 and Q5 turn on, since at that point, 5V_MAIN and 3.3 MAIN are at 90% of their regulation value.

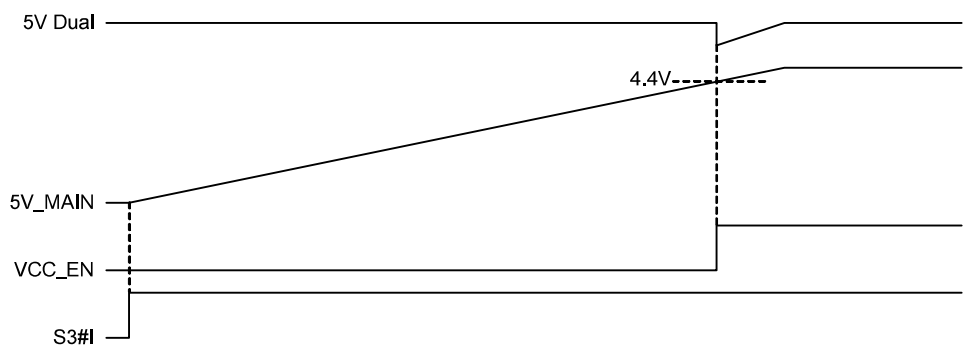


Figure 2. S3 to S0 Transition (5V DUAL)

To eliminate the "bump" add delay to the 5V_MAIN pin as shown below. The 5V_MAIN pin on the RT9643 does not supply power to the IC, it is only used to monitor the voltage level of the 5V_MAIN supply.

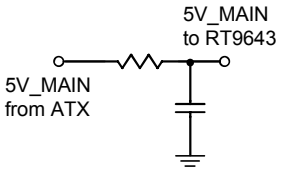


Figure 3. Adding Delay to 5V_MAIN

Another method to eliminate the potential for this "bump" is to use the PWR_OK to drive the 5V_MAIN pin. Some systems cannot tolerate the long delay for PWR_OK (>100ms) to assert, hence the solution in figure C may be preferable.

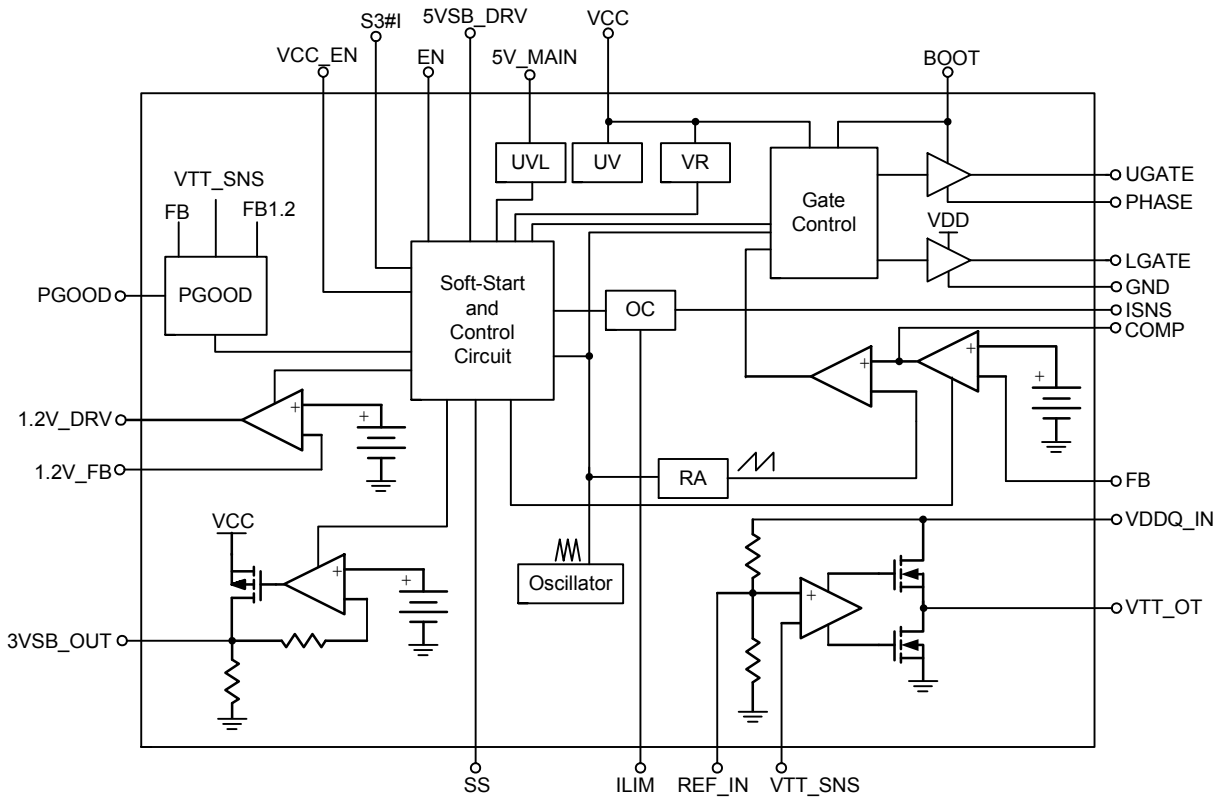
S5 to S3 : During S5 to S3 transition, the IC will pull 5VSB_DRV low with 500nA current sink to limit inrush in Q4 if 5V MAIN is below its UVLO threshold. At that time, 5V Dual is charged. The limited gate drive controls the inrush current through Q4 as it charges C1 (Capacitance on 5V Dual). Depending on the CGD of Q4, the current available from 5VSB, and the size of C1, C13 may be omitted.

$$I_{Q4(INRUSH)} = \frac{C1 \times 5 \times 10^{-7}}{C13 + C_{GD(Q4)}}$$

Table 3. B.O.M of the Application Circuit

Component Description	Qty	Ref	Vendor
See notes below		Cout	
See notes below		C1,C12,C17	
Capacitor 1uF, 10%, 16VDC, X7R, 0603	2	C2,C4	TDK
Capacitor 10nF, 10%, 50VDC, X7R, 0603	1	C3	TDK
Capacitor 10nF, 10%, 16V, X7R, 0603	1	C6	WALSIN
Capacitor 220pF, 10%, 50VDC, NPO, 0603	1	C9	WALSIN
Capacitor 10nF, 10%, 50VDC, X7R, 0603	2	C10, C11	TDK
Capacitor 220nF,10%, 10VDC, X7R, 0603	1	C5	WALSIN
Capacitor 100nF, 10%, 25VDC, X7R, 0603	1	C8	WALSIN
Inductor 1.8uH, 3.24m?16 Amps	1	L1	Inter-Technical
Inductor 0.39uH, 2.8m, 15 Amps	1	L2	Inter-Technical
MOSFET N-CH, 8.8m, 30V, 50A, D-PAK, FSID: FDD6296	1	Q1	Fairchild
MOSFET N-CH, 6m, 30V, 75A, D-PAK, FSID: FDD6606	1	Q2	Fairchild
MOSFET N-CH, 32m, 20V, 21A, D-PAK, FSID: FDD6530A	3	Q3,Q5,Q6	Fairchild
MOSFET P-CH, 35m, -20V, -5.5A, SSOT-6, FSID : DC602P	1	Q4	Fairchild
Resistor 1.82k, 1%, 0805	4	R1,R2,R9,R10	Yageo
Resistor 56k, 1%, 0805	1	R5	Any
Resistor 11.8k, 1%, 0805	1	R6	Any
Resistor 3.01k, 1%, 0603	1	R7	Any
Resistor 9.09k, 1%, 0603	1	R8	Any
Resistor 10k, 1%, 0805	1	R4	Any
Resistor 1k, 1%, 0805	1	R3	Any
RT9643	1	U1	RichTek

Function Block Diagram



Functional Pin Description

1.2V_DRV (Pin1)

Gate drive for 1.2V linear controller. The pin will be turned off (low) in S3 and S5 state.

1.2V_FB (Pin2)

Feedback for the 1.2V linear controller. The pin is applied for 1.2V LDO output regulation sense. The voltage can be disabled by pulling the pin higher than 0.9V.

5VSB_DRV (Pin3)

5VSB Control Switch. The pin is applied to drive an external P-Channel MOSFET to switch 5VDL power to 5VSB in S3 stage. The pin goes high in S0 and S5.

5V_Main (Pin4)

5V main power. When this pin is below 4.5V, transition from S3 to S0 is inhibited.

VTT_SNS (Pin5)

Remote sense for VTT. The pin is applied to remote sense the output voltage of VTT.

VTT_OUT (Pin6)

Output of VTT. Regulator power VTT output.

VDDQ_IN (Pin7)

Input of external VDDQ. Input power of VTT, the VTT is implemented to tracking 1/2 VDDQ.

BOOT (Pin8)

PWM Boot. The pin is applied for VDDQ PWM boot-strapped power for the embedded driver power.

UGATE (Pin9)

High-Side Drive. High-side MOSFET driver output of VDDQ PWM. Connect to gate of high-side MOSFET.

PHASE (Pin10)

Phase node of VDDQ PWM. The pin is applied to sense phase node of VDDQ PWM for gates switch control.

ISNS (Pin11)

Current Sense input. Monitors the voltage drop across the low-side MOSFET or external sense resistor for over current control.

LGATE (Pin12)

Low-Side Drive. The low-side MOSFET driver output. Connect to gate of low-side MOSFET.

PGOOD (Pin13)

Power Good Indication Signal. An open-drain output signal that will pull LOW if FB is outside of a ±10% range of the 0.9V reference and the LDO outputs are > 80% or < 110% of its reference. PGOOD goes low when S3 is high. The power good signal from the PWM regulator enables the VTT regulator and the LDO controller.

VCC (Pin14)

IC VCC. 5VSB is generally applied for bias power for IC logics and gate driver control. The IC stays at standby until this pin is higher than 4.35V.

3VSB_OUT (Pin15)

3.3VSB LDO Output. Internal linear regulator and is capable to drive up to 1.25Amp peak current. The power is Turned off in S0 state, and on in S5 or S3 stage.

VCC_EN (Pin16)

VCC enable signal for dual power. The pin is applied to control VCC power on for 3.3VDL and 5VDL, the signal is an open drain output which pulls the gate of an two N-Channel blocking MOSFETs low in S5 and S3. This pin goes high (open) in S0.

S3#I (Pin17)

S3 Input. When LOW, the VTT and 1.2V LDO regulators are turned off and 3.3VSB regulator is turned on the. PGOOD is set to low when S3#I is LOW.

EN (Pin18)

Chip ENABLE. Typically tied to S5#. When this pin is low, the IC is operated in standby mode, all regulators are off and VCC_EN is low.

GND [Pin19, Exposed Pad (25)]

IC GROUND. The ground power for whole chip. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

ILIM (Pin20)

Current Limit setting pin. A external resistor is attached to set the current limit value.

SS (Pin21)

Soft Start. A external capacitor is attached to control the slew rate of the converter during initialization as well as sets the initial slew rate of the LDO controllers when transitioning from S3 to S0. This pin is charged/discharged with a internal 5uA current source during initialization, and charged with 50uA during PWM soft-start.

COMP (Pin22)

Compensation pin of VDDQ PWM. Output of the PWM error amplifier. Connect compensation network between this pin and FB.

FB (Pin23)

VDDQ PWM Feedback. The output feedback of VDDQ PWM. The pin is applied for voltage regulation, PGOOD, under-voltage, and over-voltage protection and monitoring.

REF_IN (Pin24)

VTT voltage setting. The VTT regulator tracks the voltage set the pin, typically, it should be 1/2VDDQ

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{CC} ---------- 6.5V
- PHASE Voltage ---------- GND – 5V to 24V
- UGATE Voltage ---------- V_{PHASE} – 0.3V to V_{BOOT} + 0.3V
- LGATE Voltage ---------- GND – 0.3V to V_{CC} + 0.3V
- BOOT to GND ---------- 24V
- VCC_EN to GND ---------- 24V
- BOOT to PHASE ---------- 6.5V
- BOOT to UGATE ---------- 6.5V
- UGATE to PHASE ---------- 6.5V
- Input, Output or I/O Voltage ---------- GND – 0.3V to V_{CC} + 0.3V
- Storage Temperature Range ---------- –65°C to 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature Range ---------- –20°C to 125°C
- Power Dissipation, PD @ T_A = 25°C
  VQFN-24L 5x5 ---------- 1.923W
- Package Thermal Resistance (Note 4)
  VQFN-24L 5x5, θ_{JA} ---------- 52°C/W
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Supply Voltage, V_{CC} ---------- 5V ± 10%
- Ambient Temperature Range ---------- –10°C to 85°C

Electrical Characteristics

(Recommended Operating Conditions, unless otherwise specification)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Converter & POR						
VCC Current	I_{VCC}	LGATE, UGATE open, FB > 0.9, I(VTT) = 0, EN = 1, S3#I = 1	--	6	24	mA
		EN = 1, S3#I=LOW, I(3.3)< 10mA	--	6	24	mA
		EN = 0, I(3.3) = 0	--	2	4	mA
VCC UVLO Threshold		Rising V_{CC}	4.0	4.2	4.4	V
		Falling	3.9	4.05	4.2	V
		Hysteresis	--	150	--	mV
5V_MainUVLO Threshold		Rising	4.3	4.4	4.6	V
		Falling	3.9	4.1	4.2	V
		Hysteresis	--	300	--	mV

To be continued

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Oscillator						
Frequency	F_{OSC}		250	300	350	kHz
Ramp Amplitude pk-pk			--	1.8	--	V
Ramp offset			--	0.5	--	V
Reference and Soft Start						
Internal Reference voltage			0.891	0.900	0.909	V
Soft Start Current		Initial ramp after power-up	--	5	--	μA
		During PWM/LOD soft start	--	48	--	μA
SS discharge on resistance		EN = 0	--	280	--	Ω
PWM Converter						
Load Regulation		I_{OUT} from 0 to 16A	-2	--	+2	%
FB Bias Current			0.75	1	1.25	μA
Under Voltage shutdown		2us noise filter	65	75	80	%
Isns over-current threshold		RILIM	145	170	195	μA
Over voltage threshold			110	115	120	%
PWM Output Driver						
UGATE Output Resistance		Sourcing	--	1.8	3	Ω
		Sinking	--	1.8	3	Ω
LGATE Output Resistance		Sourcing	-	1.8	3	Ω
		Sinking	--	1.2	2	Ω
PGOOD (Power good Output) and control pins, VDDQ output						
Lower threshold		2us noise filter	86	--	92	%
Upper threshold		2us noise filter	108	--	115	%
PGOOD Output Low		I_{PGOOD}	--	--	0.5	V
Leakage Current		Pull up to 5V	--	--	1	μA
VTT Regulator						
VDDQ IN Current		S0 mode, I_{VTT} = 0	--	35	70	mA
V_{REF} IN to VTT Differential Output Voltage		I_{VTT} = 0, T_A = 25°C	-20	--	20	mV
		I_{VTT} = ±1.25A (pulsed)	-40	--	40	mV
Internal Divider Gain		EN=0	0.493	0.498	0.503	V/V
VTT Current Limit		Pulse(300ms $_{MAX}$), T_A = 25°C	±1.5	±3	±4	A
VTT Leakage Current		S3#I = Low	–20	--	20	μA
VTT SNS input resistance		VTT = 0.9V	--	110	--	kΩ
VTT PGOOD		Measured at VTT SNS	80	--	110	%
Drop-Out Voltage		ITT = ±1.5A	-0.8	--	0.8	V

To be continued

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
1.2V LDO						
Regulation		I(1.2) from 0 to 5A	1.17	1.2	1.23	V
Drop-Out Voltage		I(1.2) ≦ 5A, $R_{DS(ON)}$ < 50mΩ	--	--	0.3	V
External Gate Drive		V_{CC} = 4.75V	--	--	4.5	V
Gate Drive Source Current			--	1.2	--	mA
Gate Drive Sink Current			--	1.2	--	mA
FB 1.2V PGOOD Threshold			--	--	0.8	V
3.3V LDO						
Regulation		I(3.3) from 0 to 1.25A, V_{CC} > 4.75V	3.2	3.3	3.4	V
Drop-Out Voltage		I(3.3) ≦ 1.25A	--	--	1.5	V
Control Function						
S3#I, EN input threshold			1	1.25	1.55	V
S3#I, EN input Current			-1	--	1	μA
Over-Temperature Shutdown			--	150	--	°C
Over-Temperature Hysteresis			--	25	--	°C
V_{CC_EN} Output Low $R_{DS(ON)}$			--	170	300	Ω
VCC_EN Output High Leakage		V_{VCC_EN} = 12V	--	4	10	μA
5VSB_DRV Output Low resistance		5V_MAIN OK	--	125	200	Ω
5VSB_DRV Sink Current		5V_MAIN < UVLO	--	500	--	nA
5VSB_DRVOutput High			--	820	1200	Ω

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution is highly recommended.

Note 3. The operating conditions beyond the recommended range is not guaranteed.

Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board (single-layer, 1S) of JEDEC 51-3 thermal measurement standard.

Application Information

PWM Regulator

The RT9643 combines a single-phase synchronous buck PWM controller designed to drive two N-Channel MOSFETs. It provides a highly accurate, programmable output voltage precisely regulated to low voltage requirement with an internal 0.9V reference.

Setting the output voltage

The output voltage of the PWM regulator can be set in the range of 0.9V to 90% of its power input by an external resistor divider.

The internal reference is 0.9V. The output is divided down by an external voltage divider to the FB pin (for example, R1 and R2 in Typical Application Circuit). There is also a 1μA precision (±5%) current sourced out of FB to ensure that if the pin is open, VDDQ will remain low. The output voltage therefore is :

$$\frac{0.9V}{R2} = \frac{V_{OUT} - 0.9V}{R1} + 1\mu A$$

To minimize noise pickup on this node, keep the resistor to GND (R2) below 2k. We selected R2 at 1.82k and solved for R1.

$$R1 = \frac{R2 \times (V_{OUT} - 0.9)}{0.9 - 1\mu A \times R2} = 1.816k \approx 1.82k$$

The synchronous buck converter is optimized for 5V operation.

Oscillator

The internal oscillator frequency is 300kHz. The internal PWM ramp is reset on the rising clock edge.

PWM Soft Start

When the PWM regulator is enabled the circuit will wait until the VDDQ_IN pin is below 100mV to ensure that the soft-start cycle does not begin with a large residual voltage on the PWM regulator output.

When the PWM regulator is disabled, 50Ω is turned on from VDDQ_IN to PGND to discharge the output.

The voltage at the positive input of the error amplifier is limited to V_{CSS} which is charged with a 50μA current source. The output voltage starts to go up when V_{CSS} is larger than 0.4V. To prevent large duty cycles and high currents during the beginning of the PWM soft-start, Once C_{SS} has charged to 1.3V, the output voltage will be in regulation.

The time it takes SS to reach 1.3V is : $T_{1.3} = \frac{1.3 \times C_{SS}}{50}$

where T1.3 is in ms if C_{SS} is in nF.

The PWM regulator′s latched faults are enabled until C_{SS} charges up to 1.5V. When C_{SS} reaches 2.5V, the VTT and 1.2V LDO will begin their soft-start ramps. After the VTT and 1.2V LDO regulators are in regulation, PGOOD is then allowed to go HIGH (open). UVLO on V_{CC} will discharge SS and reset the IC.

Current Sensing Section

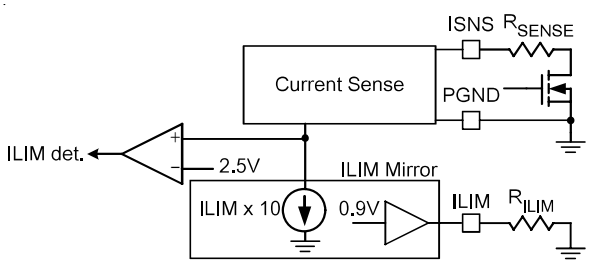


Figure 4. Current Sense & Limit

The following discussion refers to Figure 4.

The current through R_{SENSE} resistor (ISNS) is sensed shortly after low side MOSFET is turned on.

Setting the Current Limit

An ISNS is compared to the current established when a 0.9 V internal reference drives the ILIM pin. R_{ILIM}, the $R_{DS(ON)}$ of Q2, and R_{SENSE} determine the current limit :

$$R_{ILIM} = \frac{10 \times 0.9}{I_{LIMIT}} \times \frac{R_{SENSE}}{R_{DS(ON)}}$$

Where I_{LIMIT} is the peak inductor current. Since the tolerance on the current limit is largely dependent on the ratio of the external resistors it is fairly accurate if the voltage drop on the Switching Node side of R_{SENSE} is an accurate representation of the load current.

When using the MOSFET as the sensing element, the variation of $R_{DS(ON)}$ causes proportional variation in the ISNS. This value not only varies from device to device, but also has a typical junction temperature coefficient of about 0.4%/°C (consult the MOSFET datasheet for actual values), so the actual current limit set point will decrease proportional to increasing MOSFET die temperature. A factor of 1.6 in the current limit set point should compensate for all MOSFET $R_{DS(ON)}$ variations, assuming the MOSFET's heat sinking will keep its operating die temperature below 125°C.

Current limit (I_{LIMIT}) should be set sufficiently high as to allow inductor current to rise in response to an output load transient. Typically, a factor of 1.3 is sufficient. In addition, since I_{LIMIT} is a peak current cut-off value, we will need to multiply $I_{LOAD(MAX)}$ by the inductor ripple current (20% is chosen).

$I_{LIMIT} > I_{LOAD(MAX)} \times 1.6 \times 1.3 \times 1.2$

Gate Driver Section

The adaptive gate control logic translates the internal PWM control signal into the MOSFET gate drive signals providing necessary amplification, level shifting and shoot-through protection. Also, it has functions that help optimize the IC performance over a wide range of operating conditions. Since MOSFET switching time can vary dramatically from type to type and with the input voltage, the gate control logic provides adaptive dead time by monitoring the gate to source voltages of both upper and lower MOSFETs. The lower MOSFET drive is not turned on until the PHASE has decreased to less than approximately one VT (~0.6volt). Similarly, the upper MOSFET is not turned on until the gate-to-source voltage of the lower MOSFET has decreased to less than approximately one VT (~0.6 volt). This allows a wide variety of upper and lower MOSFETs to be used without a concern for simultaneous conduction, or shoot-through.

There must be a low-resistance, low-inductance path between the driver pin and the MOSFET gate for the adaptive dead-time circuit to work properly. Any delay along that path will subtract from the delay generated by the adaptive dead-time circuit and shoot-through may occur.

Frequency Loop Compensation

The loop is compensated using a feedback network around the error amplifier, which is a voltage output OP Amp. Figure 5 shows a complete type3 compensation network. A type2 compensation configuration eliminates R3 and C3 and is shown in typical application circuit. Type2 compensation can be used for most applications. For critical applications that require wide loop-bandwidth, and use very low ESR output capacitors, type3 compensation may be required.

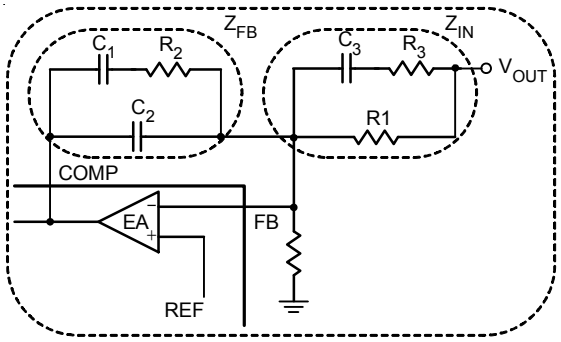


Figure 5. Compensation Network

PGOOD Signal

PGOOD monitors the status of the PWM output as well as the VTT and 1.2V LDO regulators. PGOOD remains low unless all of the conditions below are met :

1. S3#I is HIGH
2. SS is above 4V
3. Fault latch is cleared
4. FB is between 90% and 110% of V_{REF}
5. VTT and 1.2V LDO regulators are in regulation

Protection

The converter output is monitored and protected against extreme overload, short circuit, over-voltage and under-voltage conditions.

An internal "Fault Latch" is set for any fault intended to shut down the IC. When the "Fault Latch" is set, the IC will discharge VDDQ_IN by driving L_{GATE} high until VDDQ_IN < 0.5V. L_{GATE} will then go low until VDDQ_IN > 0.8V. This behavior will discharge the output without causing undershoot (negative output voltage).

To discharge the output capacitors, a 50Ω load resistor is switched in from VDDQ_IN to PGND whenever the IC is in fault condition, or when EN is low. After a latched fault, operation can be restored by recycling power or by toggling the EN pin.

Under-Voltage Shutdown

If FB stays below the under-voltage threshold for 2μs, the "Fault latch" is set. This fault is prevented from setting the fault latch during PWM soft-start (SS < 1.5V).

Over-Current Sensing

If the circuit's current limit signal ("I_{LIM} det" as shown in Figure 4) is high at the beginning of a clock cycle, a pulse skipping circuit is activated and UGATE is inhibited. The circuit continues to pulse skip in this manner for the next 8 clock cycles. If at any time from the 9th to the 16th clock cycle, the "I_{LIM} det" is again reached, the fault latch is set. If "I_{LIM} det" does not occur between cycle 9 and 16, normal operation is restored and the over-current circuit resets itself. This fault is prevented from setting the fault latch during soft-start (SS < 1.5V).

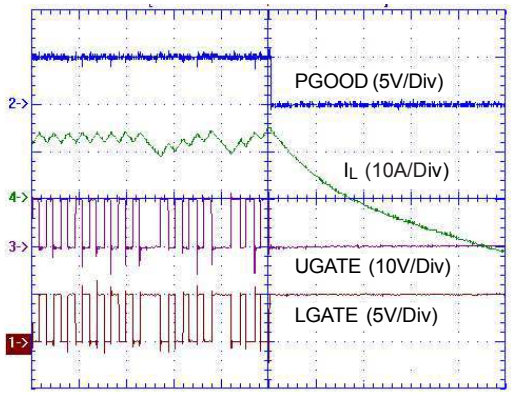


Figure 6. Over Current Protection Waveform

OVP / HS Fault / FB short to GND detection:

A **HS Fault** is detected when there is more than 0.5V from PHASE to PGND 350ns after L_{GATE} reaches 4V (same time as the current sampling time).

OVP Fault Detection occurs if FB > 115% VREF for 16 clock cycles. During soft-start, the output voltage could potentially "run away" if either the FB pin is shorted to GND or R1 is open. This fault will be detected if the following condition persists for more than 14μs during soft-start.

1. VDDQ_IN (PWM output voltage) > 1V and

2. FB < 100mV

Any of these 3 faults will set the fault latch. These 3 faults can set the fault latch during the SS time (SS < 1.5V).

To ensure that FB pin open will not cause a destructive condition, a 1μA current source ensures that the FB pin will be high if open. This will cause the regulator to keep the output low, and eventually result in an Under-voltage fault shutdown (after PWM SS complete).

Over-Temperature Protection

RT9643 incorporates an internal over temperature circuit designed to protect the device during overload conditions. If the junction temperature reaches a nominal temperature of 150°C, the over temperature circuit will shut the chip. Normal operation is restored at when the die temperature falls below 125°C with internal Power On Reset asserted, resulting in a full soft-start cycle. To accomplish this, the over temperature comparator should discharge the SS pin.

VTT Regulator

The VTT regulator is a simple and high-speed linear regulator designed to generate termination voltage in double data rate (DDR) memory system. The regulator is capable of actively sinking or sourcing up to 1.25A while regulating an output voltage to within 40mV. The output termination voltage can be tightly regulated to track 1/2VDDQ_IN by two internal voltage divider resistors (50k for each resistor) or two external voltage divider resistors from the output of the PWM regulator.

The VTT regulator also incorporates a high-speed differential amplifier to provide ultra-fast response in line/load transient. Other features include extremely low initial offset voltage, excellent load regulation, current limiting in bi-directions.

The VTT regulator is enabled when S3#I is HIGH and the PWM regulator's internal PGOOD signal is true. The VTT regulator also includes its own PGOOD signal which is high when VTT_SNS > 90% of REF_IN.

LDO Controller

The LDO controller combined with an external N-Channel MOSFET pass element is used to provide 1.2V for the

Front-side bus GTL termination. The driving voltage on the gate drive pin can be pull up to within 0.5V of VCC. Use low Vth MOSFET to assure RDS(ON) is small enough for full load operation. The soft start for the LDO is accomplished by clamping the input voltage to a smooth up-going ramp. The final input reference voltage after soft start is 0.9V.

Component Selection

Components should be appropriately selected to ensure stable operation, fast transient response, high efficiency, minimum BOM cost and maximum reliability.

Output Inductor Selection

The selection of output inductor is based on the considerations of efficiency, output power and operating frequency. For a synchronous buck converter, the ripple current of inductor (ΔI_L) can be calculated as follows :

$$\Delta I_L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times f_{OSC} \times L}$$

Generally, an inductor that limits the ripple current between 20% and 50% of output current is appropriate. Make sure that the output inductor could handle the maximum output current and would not saturate over the operation temperature range.

Output Capacitor Selection

The output capacitors determine the output ripple voltage (ΔV_{OUT}) and the initial voltage drop after a high slew-rate load transient. The selection of output capacitor depends on the output ripple requirement. The output ripple voltage is described as follows :

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{1}{8} \times \frac{V_{OUT}}{f_{OSC}^2 \times L \times C_{OUT}} (1 - D)$$

For electrolytic capacitor application, typically 90~95% of the output voltage ripple is contributed by the ESR of output capacitors. Paralleling lower ESR ceramic capacitor with the bulk capacitors could dramatically reduce the equivalent ESR and consequently the ripple voltage.

Input Capacitor Selection

Use mixed types of input bypass capacitors to control the input voltage ripple and switching voltage spike across the MOSFETs. The buck converter draws pulsewise current from the input capacitor during the on time of upper MOSFET. The RMS value of ripple current flowing through the input capacitor is described as :

$$I_{IN(RMS)} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The input bulk capacitor must be cable of handling this ripple current. Sometime, for higher efficiency the low ESR capacitor is necessarily. Appropriate high frequency ceramic capacitors physically near the MOSFETs effectively reduce the switching voltage spikes.

MOSFET Selection

The selection of MOSFETs is based upon the considerations of $R_{DS(ON)}$, gate driving requirements, and thermal management requirements. The power loss of upper MOSFET consists of conduction loss and switching loss and is expressed as :

$$P_{UPPER} = P_{COND\_UPPER} + P_{SW\_UPPER}$$
$$= I_{OUT} \times R_{DS(ON)} \times D + \frac{1}{2} I_{OUT} \times V_{IN} \times (T_{RISE} + T_{FALL}) \times f_{OSC}$$

where T_{RISE} and T_{FALL} are rising and falling time of V_{DS} of upper MOSFET respectively. $R_{DS(ON)}$ and Q_G should be simultaneously considered to minimize power loss of upper MOSFET.

The power loss of lower MOSFET consists of conduction loss, reverse recovery loss of body diode, and conduction loss of body diode and is express as :

$$P_{LOWER} = P_{COND\_LOWER} + P_{RR} + P_{DIODE}$$
$$= I_{OUT} \times R_{DS(ON)} \times (1 - D) + Q_{RR} \times V_{IN} \times f_{OSC}$$
$$+ \frac{1}{2} \times I_{OUT} \times V_F \times T_{DIODE} \times f_{OSC}$$

where T_{DIODE} is the conducting time of lower body diode.

Special control scheme is adopted to minimize body diode conducting time. As a result, the $R_{DS(ON)}$ loss dominates the power loss of lower MOSFET. Use MOSFET with adequate $R_{DS(ON)}$ to minimize power loss and satisfy thermal requirements.

Bypass Capacitor Notes

Input capacitor C1 is typically chosen based on the ripple current requirements. COUT is typically selected based on both current ripple rating and ESR requirement. C17

and C12 selection will be largely determined by ESR and load transient response requirements.

PWM Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency and radiate noise, that results in over-voltage stress on devices. Careful component placement layout and printed circuit design can minimize the voltage spikes induced in the converter. Consider, as an example, the turn-off transition of the upper MOSFET prior to turn-off, the upper MOSFET was carrying the full load current. During turn-off, current stops flowing in the upper MOSFET and is picked up by the low side MOSFET or schottky diode. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selections, layout of the critical components, and use shorter and wider PCB traces help in minimizing the magnitude of voltage spikes.

There are two sets of critical components in a DC-DC converter using the RT9643. The switching power components are most critical because they switch large amounts of energy, and as such, they tend to generate equally large amounts of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bypass current.

The power components and the PWM controller should be placed firstly. Place the input capacitors, especially the high-frequency ceramic decoupling capacitors, close to the power switches. Place the output inductor and output capacitors between the MOSFETs and the load. Also locate the PWM controller near by MOSFETs.

A multi-layer printed circuit board is recommended.

Figure 9 shows the connections of the critical components in the converter. Note that the capacitors C_{IN} and C_{OUT} each of them represents numerous physical capacitors. Use a dedicated grounding plane and use vias to ground all critical components to this layer. Apply another solid layer as a power plane and cut this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the PHASE node, but it is not necessary to oversize this particular island. Since the PHASE node is subjected to very high dV/dt voltages, the stray capacitance formed between these island and the surrounding circuitry will tend to couple switching noise. Use the remaining printed circuit layers for small signal routing. The PCB traces between the PWM controller and the gate of MOSFET and also the traces connecting source of MOSFETs should be sized to carry 2A peak currents.

Below PCB gerber files are our test board for your reference :

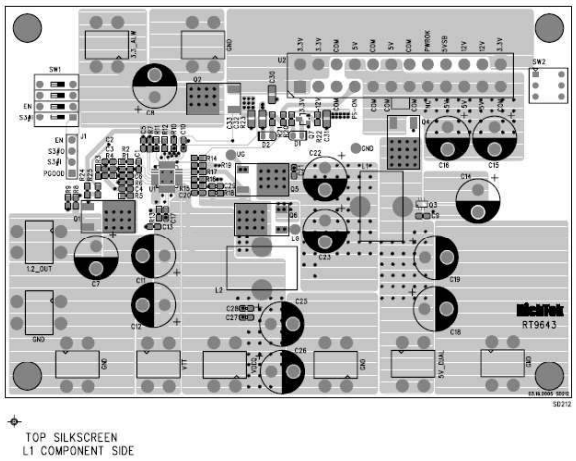


Figure 7. Component Side

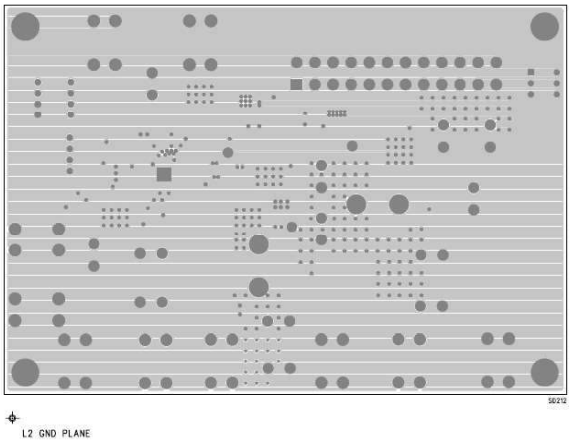


Figure 8. GND

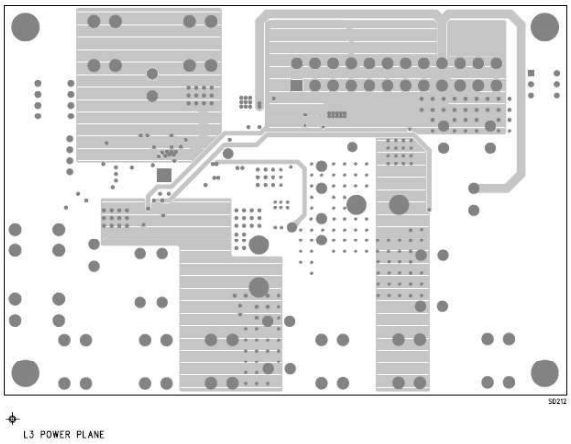


Figure 9. Power

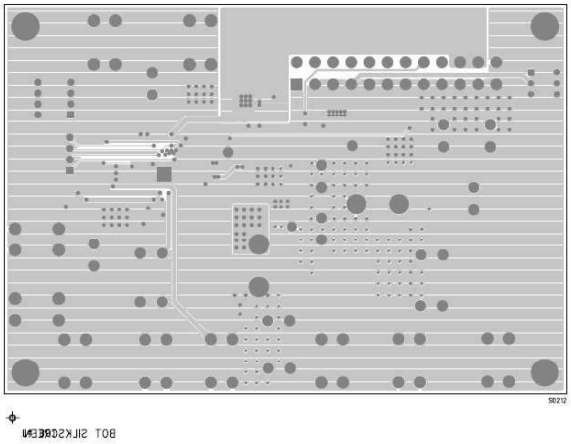
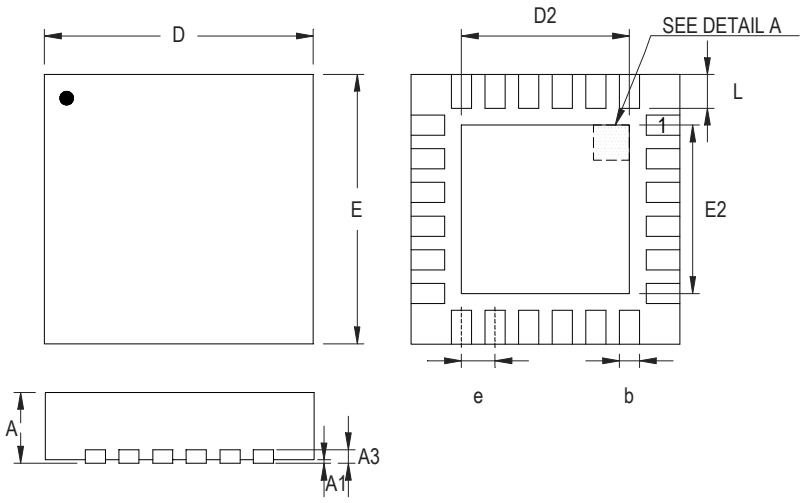
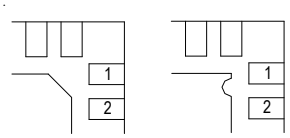


Figure 10. Bottom

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.250	0.350	0.010	0.014
D	4.950	5.050	0.195	0.199
D2	3.100	3.400	0.122	0.134
E	4.950	5.050	0.195	0.199
E2	3.100	3.400	0.122	0.134
e	0.650		0.026	
L	0.350	0.450	0.014	0.018

V-Type 24L QFN 5x5 Package

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