SiT2044B

1 – 110 MHz, -55 to 125°C, SOT23, Endura™ Series Oscillator

Features

- Best acceleration sensitivity of 0.1 ppb/*g*
- Any frequencies between 1 MHz and 110 MHz accurate to 6 decimal places
- Supply voltage of 1.8 V or 2.25 V to 3.63 V
- Excellent total frequency stability as low as ±20 ppm
- Low power consumption of 3.8 mA typical at 1.8 V
- LVCMOS/LVTTL compatible output
- AEC-Q100 qualified
- 5-pin SOT23-5 package: 2.9 x 2.8 mm x mm
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free
- Contact SiTime for up-screening and LAT programs

Applications

- Avionics systems
- Field communication systems
- Telemetry applications

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Electrical Characteristics

Table 1. Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and nominal supply voltage.

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	1	–	110	MHz	Refer to Tables 14 to 16 for a list of supported frequencies
Frequency Stability and Aging						
Frequency Stability	F_stab	-20	–	+20	ppm	Inclusive of Initial tolerance at 25°C, 1st year aging at 25°C, and variations over operating temperature, rated power supply voltage and load (15 pF ± 10%).
		-25	–	+25	ppm	
		-30	–	+30	ppm	
		-50	–	+50	ppm	
Operating Temperature Range						
Operating Temperature Range (ambient)	T_use	-40	–	+85	°C	AEC-Q100 Grade 3
		-40	–	+105	°C	AEC-Q100 Grade 2
		-40	–	+125	°C	AEC-Q100 Grade 1
		-55	–	+125	°C	Extended cold, AEC-Q100 Grade1
Rugged Characteristics						
Acceleration (g) sensitivity, Gamma Vector	F_g	–	–	0.1	ppb/*g*	Low sensitivity grade; total gamma over 3 axes; 15 Hz to 2 kHz; MIL-PRF-55310, computed per section 4.8.18.3.1
Supply Voltage and Current Consumption						
Supply Voltage	Vdd	1.62	1.8	1.98	V	All voltages between 2.25 V and 3.63 V including 2.5 V, 2.8 V, 3.0 V and 3.3 V are supported.
		2.25	–	3.63	V	
Current Consumption	Idd	–	4.0	4.8	mA	No load condition, f = 20 MHz, Vdd = 2.25 V to 3.63 V
		–	3.8	4.5	mA	No load condition, f = 20 MHz, Vdd = 1.8 V
LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	All Vdds
Rise/Fall Time	Tr, Tf	–	1.5	3	ns	Vdd = 2.25 V - 3.63 V, 20% - 80%
		–	1.3	2.5	ns	Vdd = 1.8 V, 20% - 80%
Output High Voltage	VOH	90%	–	–	Vdd	IOH = -4 mA (Vdd = 3.0 V or 3.3 V) IOH = -3 mA (Vdd = 2.8 V and Vdd = 2.5 V) IOH = -2 mA (Vdd = 1.8 V)
Output Low Voltage	VOL	–	–	10%	Vdd	IOL = 4 mA (Vdd = 3.0 V or 3.3 V) IOL = 3 mA (Vdd = 2.8 V and Vdd = 2.5 V) IOL = 2 mA (Vdd = 1.8 V)
Input Characteristics						
Input High Voltage	VIH	70%	–	–	Vdd	Pin 1, OE
Input Low Voltage	VIL	–	–	30%	Vdd	Pin 1, OE
Input Pull-up Impedance	Z_in	–	100	–	kΩ	Pin 1, OE logic high or logic low

Table 1. Electrical Characteristics (continued)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Startup and Resume Timing						
Startup Time	T_start	–	–	5.5	ms	Measured from the time Vdd reaches its rated minimum value
Enable/Disable Time	T_oe	–	–	130	ns	f = 110 MHz. For other frequencies, T_oe = 100 ns + 3 * cycles
Standby Current	I_std	–	2.6	–	µA	Vdd = 2.8 V to 3.3 V, $\overline{ST}$ = Low, Output is weakly pulled down
		–	1.4	–	µA	Vdd = 2.5 V, $\overline{ST}$ = Low, Output is weakly pulled down
		–	0.6	–	µA	Vdd = 1.8 V, $\overline{ST}$ = Low, Output is weakly pulled down
Jitter						
RMS Period Jitter	T_jitt	–	1.6	2.5	ps	f = 75 MHz, 2.25V to 3.63V
		–	1.9	3.0	ps	f = 75 MHz, 1.8V
RMS Phase Jitter (random)	T_phj	–	0.5	–	ps	f = 75 MHz, Integration bandwidth = 900 kHz to 7.5 MHz
		–	1.3	–	ps	f = 75 MHz, Integration bandwidth = 12 kHz to 20 MHz

Table 2. Pin Description

Pin	Symbol	Functionality	
1	GND	Power	Electrical ground
2	NC	No Connect	No connect
3	OE/NC	Output Enable	H[1]: specified frequency output L: output is high impedance. Only output driver is disabled.
		No Connect	Any voltage between 0 and Vdd or Open[1]: Specified frequency output. Pin 3 has no function.
4	VDD	Power	Power supply voltage[2]
5	OUT	Output	Oscillator output

Top View

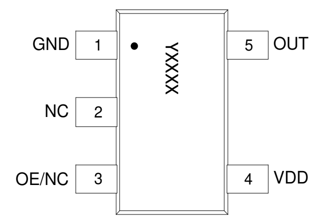


Figure 1. Pin Assignments

Notes:

1. In OE or ST mode, a pull-up resistor of 10 kΩ or less is recommended if pin 3 is not externally driven. If pin 3 needs to be left floating, use the NC option.
2. A capacitor of value 0.1 µF or higher between Vdd and GND is required.

Table 3. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
Vdd	-0.5	4	V
Electrostatic Discharge	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C
Junction Temperature[3]	–	150	°C

Note:

3. Exceeding this temperature for extended period of time may damage the device.

Table 4. Thermal Consideration[4]

Package	θJA, 4 Layer Board (°C/W)	θJC, Bottom (°C/W)
SOT23-5	421	175

Note:

4. Refer to JESD51 for θJA and θJC definitions, and reference layout used to determine the θJA and θJC values in the above table.

Table 5. Maximum Operating Junction Temperature[5]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
85°C	95°C
105°C	115°C
125°C	135°C

Note:

5. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 6. Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensitivity Level	MSL1 @ 260°C

Test Circuit and Waveform

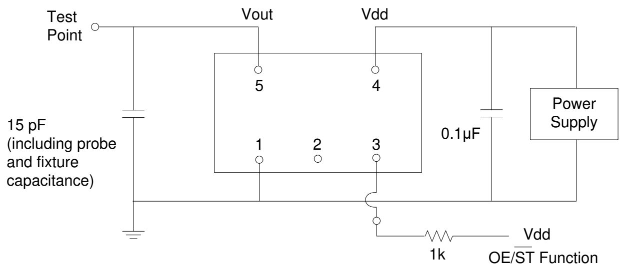


Figure 2. Test Circuit[6]

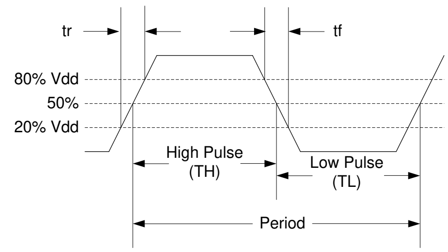


Figure 3. Waveform[6]

Note:

6. Duty Cycle is computed as Duty Cycle = TH/Period.

Timing Diagrams

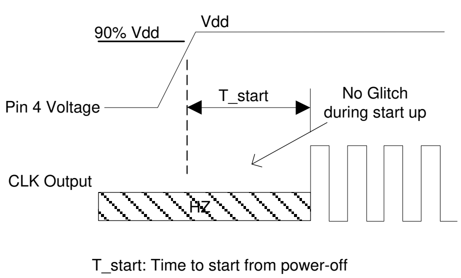


Figure 4. Startup Timing (OE Mode)[7]

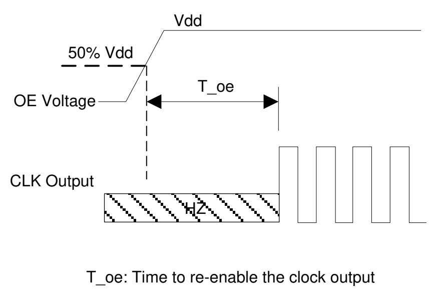


Figure 5. OE Enable Timing (OE Mode Only)

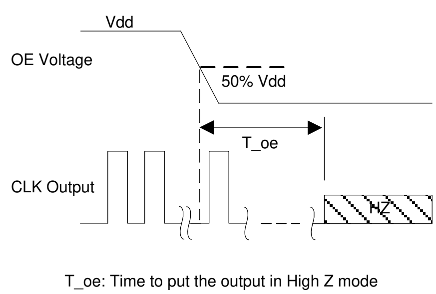


Figure 6. OE Disable Timing (OE Mode Only)

Note:

7. SiT2044 has “no runt” pulses and “no glitch” output during startup or resume.

Performance Plots[8]

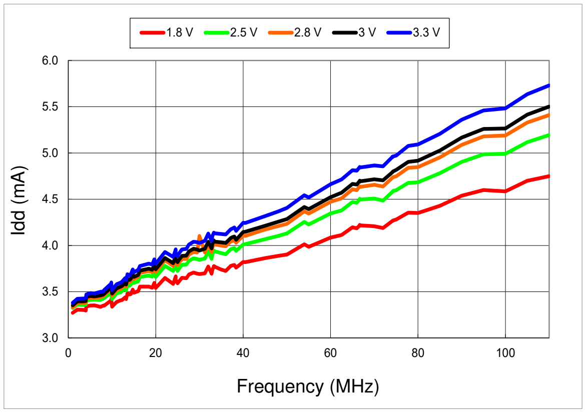


Figure 7. Idd vs Frequency

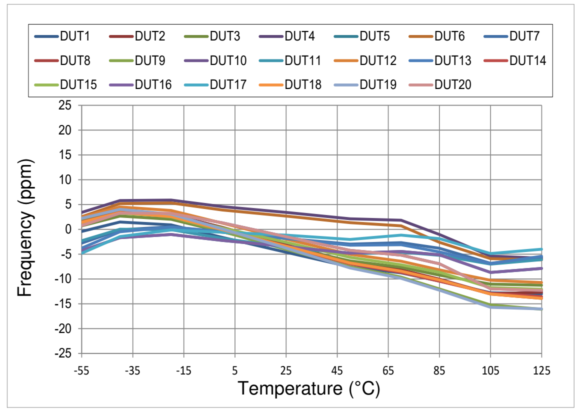


Figure 8. Frequency vs Temperature

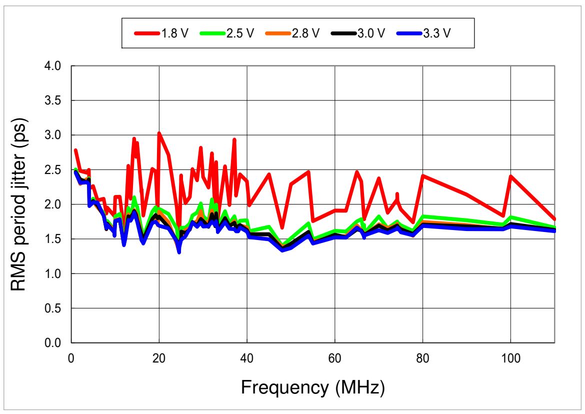


Figure 9. RMS Period Jitter vs Frequency

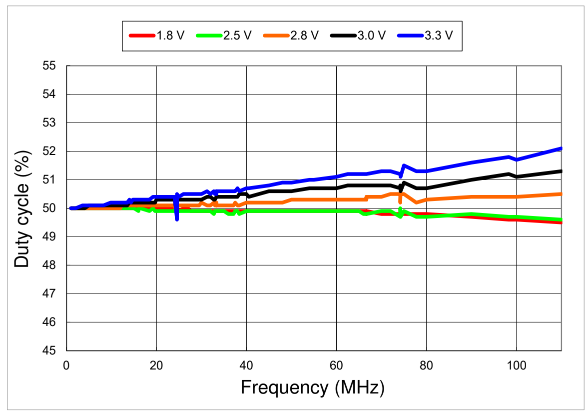


Figure 10. Duty Cycle vs Frequency

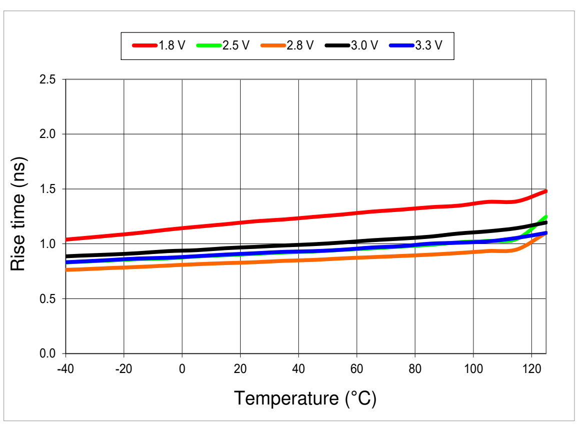


Figure 11. 20%-80% Rise Time vs Temperature

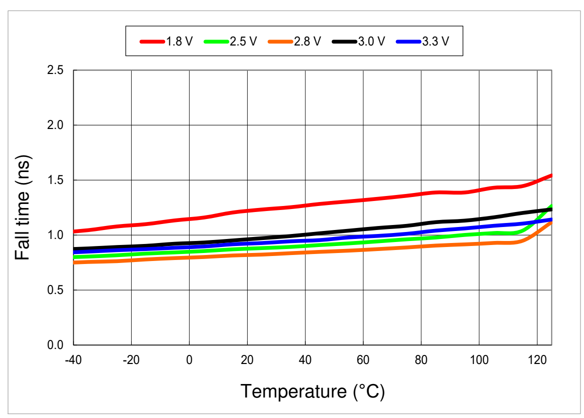


Figure 12. 20%-80% Fall Time vs Temperature

Performance Plots[8]

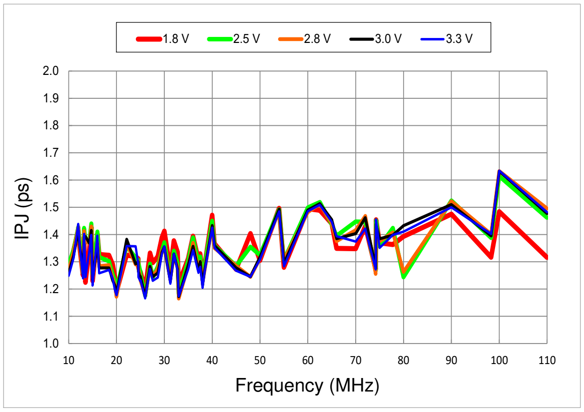


Figure 13. RMS Integrated Phase Jitter Random (12 kHz to 20 MHz) vs Frequency[9]

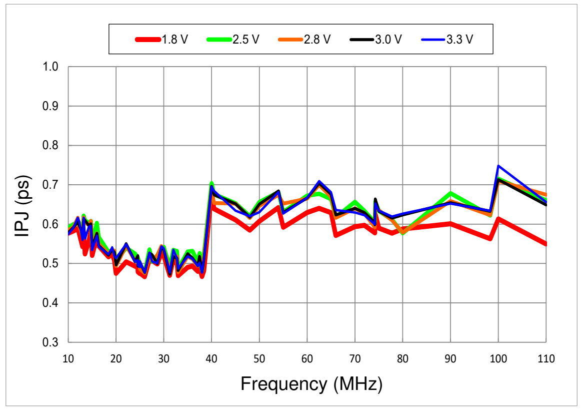


Figure 14. RMS Integrated Phase Jitter Random (900 kHz to 20 MHz) vs Frequency[9]

Notes:

8. All plots are measured with 15 pF load at room temperature, unless otherwise stated.
9. Phase noise plots are measured with Agilent E5052B signal source analyzer. Integration range is up to 5 MHz for carrier frequencies below 40 MHz.

Programmable Drive Strength

The SiT2044 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time.
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, see the SiTime Application Notes section.

EMI Reduction by Slowing Rise/Fall Time

Figure 15 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

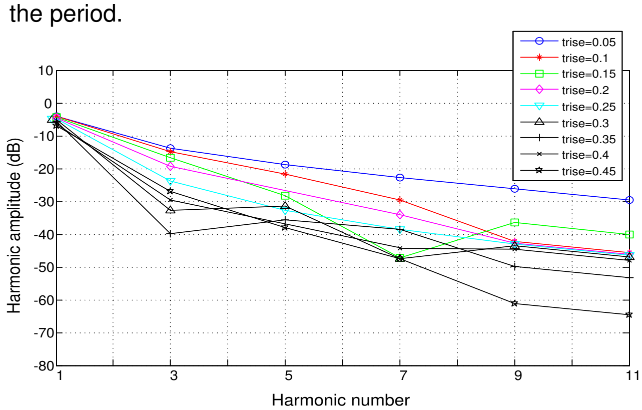


Figure 15. Harmonic EMI reduction as a Function of Slower Rise/Fall Time

Jitter Reduction with Faster Rise/Fall Time

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to speed up the rise/fall time of the input clock. Some chipsets may also require faster rise/fall time in order to reduce their sensitivity to this type of jitter. Refer to the Rise/Fall Time Tables (Table 7 to Table 11) to determine the proper drive strength.

High Output Load Capability

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a 3.3 V SiT2044 device with default drive strength setting, the typical rise/fall time is 1 ns for 15 pF output load. The typical rise/fall time slows down to 2.6 ns when the output load increases to 45 pF. One can choose to speed up the rise/fall time to 1.83 ns by then increasing the drive strength setting on the SiT2044.

The SiT2044 can support up to 60 pF in maximum capacitive loads with drive strength settings. Refer to the Rise/Tall Time Tables (Table 7 to 11) to determine the proper drive strength for the desired combination of output load vs. rise/fall time.

SiT2044 Drive Strength Selection

Tables 7 through 11 define the rise/fall time for a given capacitive load and supply voltage.

1. Select the table that matches the SiT2044 nominal supply voltage (1.8 V, 2.5 V, 2.8 V, 3.0 V, 3.3 V).
2. Select the capacitive load column that matches the application requirement (5 pF to 60 pF)
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

Calculating Maximum Frequency

Based on the rise and fall time data given in Tables 7 through 11, the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature can be calculated as:

$$\text{Max Frequency} = \frac{1}{5 \times \text{Trf\_20/80}}$$

where Trf_20/80 is the typical value for 20%-80% rise/fall time.

Example 1

Calculate f_{MAX} for the following condition:

- Vdd = 3.3 V (Table 11)
- Capacitive Load: 30 pF
- Desired Tr/f time = 1.31 ns
  (rise/fall time part number code = F)

Part number for the above example:

SiT2044BM**E**S2-18EA66.666660

Drive strength code is inserted here. Default setting is "-"

Rise/Fall Time (20% to 80%) vs C_{LOAD} Tables

Table 7. Vdd = 1.8V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	**5 pF**	**15 pF**	**30 pF**	**45 pF**	**60 pF**
L	6.16	11.61	22.00	31.27	39.91
A	3.19	6.35	11.00	16.01	21.52
R	2.11	4.31	7.65	10.77	14.47
B	1.65	3.23	5.79	8.18	11.08
T	0.93	1.91	3.32	4.66	6.48
E	0.78	1.66	2.94	4.09	5.74
U	0.70	1.48	2.64	3.68	5.09
F or "-": default	0.65	1.30	2.40	3.35	4.56

Table 8. Vdd = 2.5V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	**5 pF**	**15 pF**	**30 pF**	**45 pF**	**60 pF**
L	4.13	8.25	12.82	21.45	27.79
A	2.11	4.27	7.64	11.20	14.49
R	1.45	2.81	5.16	7.65	9.88
B	1.09	2.20	3.88	5.86	7.57
T	0.62	1.28	2.27	3.51	4.45
E or "-": default	0.54	1.00	2.01	3.10	4.01
U	0.43	0.96	1.81	2.79	3.65
F	0.34	0.88	1.64	2.54	3.32

Table 9. Vdd = 2.8V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	**5 pF**	**15 pF**	**30 pF**	**45 pF**	**60 pF**
L	3.77	7.54	12.28	19.57	25.27
A	1.94	3.90	7.03	10.24	13.34
R	1.29	2.57	4.72	7.01	9.06
B	0.97	2.00	3.54	5.43	6.93
T	0.55	1.12	2.08	3.22	4.08
E or "-": default	0.44	1.00	1.83	2.82	3.67
U	0.34	0.88	1.64	2.52	3.30
F	0.29	0.81	1.48	2.29	2.99

Table 10. Vdd = 3.0V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	**5 pF**	**15 pF**	**30 pF**	**45 pF**	**60 pF**
L	3.60	7.21	11.97	18.74	24.30
A	1.84	3.71	6.72	9.86	12.68
R	1.22	2.46	4.54	6.76	8.62
B	0.89	1.92	3.39	5.20	6.64
T or "-": default	0.51	1.00	1.97	3.07	3.90
E	0.38	0.92	1.72	2.71	3.51
U	0.30	0.83	1.55	2.40	3.13
F	0.27	0.76	1.39	2.16	2.85

Table 11. Vdd = 3.3V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	**5 pF**	**15 pF**	**30 pF**	**45 pF**	**60 pF**
L	3.39	6.88	11.63	17.56	23.59
A	1.74	3.50	6.38	8.98	12.19
R	1.16	2.33	4.29	6.04	8.34
B	0.81	1.82	3.22	4.52	6.33
T or "-": default	0.46	1.00	1.86	2.60	3.84
E	0.33	0.87	1.64	2.30	3.35
U	0.28	0.79	1.46	2.05	2.93
F	0.25	0.72	1.31	1.83	2.61

Pin 3 Configuration Options (OE or NC)

Pin 3 of the SiT2044 can be factory-programmed to support three modes: Output Enable (OE) or No Connect (NC).

Output Enable (OE) Mode

In the OE mode, applying logic low to the OE pin only disables the output driver and puts it in Hi-Z mode. The core of the device continues to operate normally. Power consumption is reduced due to the inactivity of the output. When the OE pin is pulled High, the output is typically enabled in <1µs.

No Connect (NC) Mode

In the NC mode, the device always operates in its normal mode and outputs the specified frequency regardless of the logic level on pin 3.

Table 12 below summarizes the key relevant parameters in the operation of the device in OE or NC mode.

Table 12. OE vs. NC

	OE	NC
Active current 20 MHz (max, 1.8V)	4.5 mA	4.5 mA
OE disable current (max. 1.8V)	3.8 mA	N/A
OE enable time at 110 MHz (max)	130 ns	N/A
Output driver in OE disable	High Z	N/A

Output on Startup and Resume

The SiT2044 comes with gated output. Its clock output is accurate to the rated frequency stability within the first pulse from initial device startup.

In addition, the SiT2044 supports "no runt" pulses and "no glitch" output during startup or when the output driver is re-enabled from the OE disable mode as shown in the waveform captures in Figure 16 and Figure 17.

Figure 16. Startup Waveform vs. Vdd

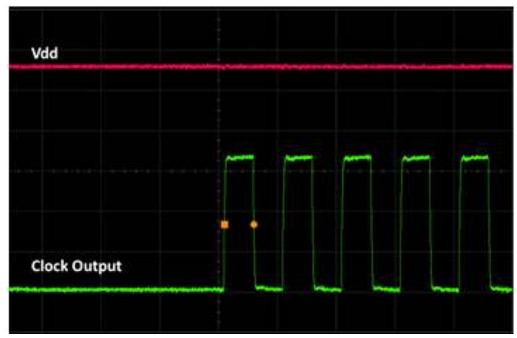
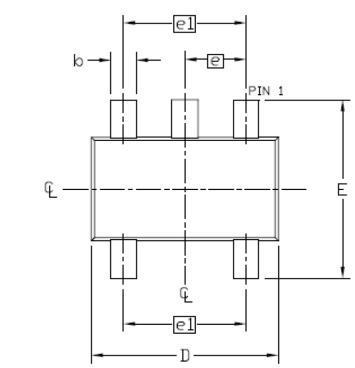
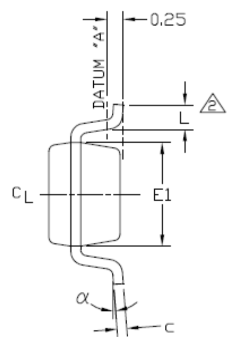
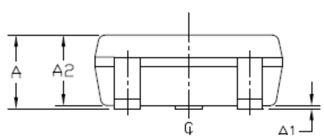
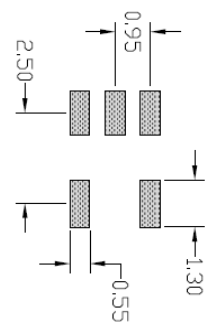


Figure 17. Startup Waveform vs. Vdd
(Zoomed-in View of Figure 16)

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[10]	Recommended Land Pattern (Unit: mm)[11]
2.90 x 2.80 mm SOT23-5  TOP VIEW  BOTTOM VIEW  SIDE VIEW	

Notes:

10. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
11. A capacitor value of 0.1 µF between Vdd and GND is required.

Table 13. Dimension Table

Symbol	Min.	Nom.	Max.
A	0.90	1.27	1.45
A1	0.00	0.07	0.15
A2	0.90	1.20	1.30
b	0.30	0.35	0.50
c	0.14	0.15	0.20
D	2.75	2.90	3.05
E	2.60	2.80	3.00
E1	1.45	1.60	1.75
L	0.30	0.38	0.55
L1	0.25 REF		
e	0.95 BSC.		
e1	1.90 BSC.		
α	0°	–	8°

Ordering Information

The following part number guide is for reference only. To customize and build an exact part number, use the SiTime Part Number Generator.

SiT2044BM-S2-18EA25.000625D

Part Family
"SiT2044"

Revision Letter
"B" is the revision

Temperature Range
"I" -40ºC to 85ºC, AEC-Q100 Grade3
"E" -40ºC to 105ºC, AEC-Q100 Grade2
"A" -40ºC to 125ºC, AEC-Q100 Grade1
"M" -55ºC to 125ºC, Ext. cold AEC-Q100 Grade1

Output Drive Strength
"–" Default (datasheet limits)
See Tables 7 to 11 for rise/fall times

"L"	"T"
"A"	"E"
"R"	"U"
"B"	"F"

Package Size
"S" SOT23-5 (2.9 x 2.8 mm)

Packing Method
"D": 8 mm Tape & Reel, 3ku reel
"E": 8 mm Tape & Reel, 1ku reel
"F": 12 mm Cut Tape, from 25 u to 999 u
(blank): Bulk, up to 24 u, sampling only

Frequency
Refer to the Supported Frequencies Tables below

Special Features
"A" for Low *g*-Sensitivity, 0.1 ppb/*g*

Feature Pin
"E" for Output Enable
"S" for Standby
"N" for No Connect

Supply Voltage[12]
"18" for 1.8V ±10%
"25" for 2.5V ±10%
"28" for 2.8V ±10%
"30" for 3.0V ±10%
"33" for 3.3V ±10%
"XX" for 2.5V -10% to 3.3V +10%

Frequency Stability
"1" for ±20 ppm
"2" for ±25 ppm
"8" for ±30 ppm
"3" for ±50 ppm

Note:

12. The voltage portion of the SiT2044 part number consists of two characters that denote the specific supply voltage of the device. The SiT2044 supports either 1.8V ±10% or any voltage between 2.25V and 3.62V. In the 1.8V mode, one can simply insert 18 in the part number. In the 2.5V to 3.3V mode, two digits such as 18, 25 or 33 can be used in the part number to reflect the desired voltage. Alternatively, "XX" can be used to indicate the entire operating voltage range from 2.25V to 3.63V.

Table 14. Supported Frequencies (-40°C to +85°C) [13]

Frequency Range	
Min.	Max.
1.000000 MHz	110.000000 MHz

Table 15. Supported Frequencies (-40°C to +105°C or -40°C to +125°C) [13,14]

Frequency Range	
Min.	Max.
1.000000 MHz	61.222999 MHz
61.974001 MHz	69.795999 MHz
70.485001 MHz	79.062999 MHz
79.162001 MHz	81.427999 MHz
82.232001 MHz	91.833999 MHz
92.155001 MHz	94.248999 MHz
94.430001 MHz	94.874999 MHz
94.994001 MHz	97.713999 MHz
98.679001 MHz	110.000000 MHz

Table 16. Supported Frequencies (-55°C to +125°C) [13,14]

Frequency Range	
Min.	Max.
1.000000 MHz	61.222999 MHz
61.974001 MHz	69.239999 MHz
70.827001 MHz	78.714999 MHz
79.561001 MHz	80.159999 MHz
80.174001 MHz	80.779999 MHz
82.632001 MHz	91.833999 MHz
95.474001 MHz	96.191999 MHz
96.209001 MHz	96.935999 MHz
99.158001 MHz	110.000000 MHz

Notes:

13. Any frequency within the min and max values in the above table are supported with 6 decimal places of accuracy.
14. Please contact SiTime for frequencies that are not listed in the tables above.

Table 17. Revision History

Revision	Release Date	Change Summary
0.5	22-Jul-2019	Fist release
1.00	24-Jul-2020	Revised startup time specification Final release
1.01	21-Nov-2022	Updated Ordering packaging information with F option Updated hyperlinks and icons on page 1. Disclaimer update

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439