ISL28290

Dual Single Supply Ultra-Low Noise, Ultra-Low Distortion, Rail-to-Rail Output, Op Amp

The ISL28290 is a dual ultra-low noise, ultra-low distortion operational amplifiers. Fully specified to operated down to +3V single supply. The amplifier has outputs that swing rail-to-rail, and an input common mode voltage that extends below ground (ground sensing).

The ISL28290 is unity gain stable with an input referred voltage noise of 1nV/√Hz. The part features 0.00017% THD+N at 1kHz.

The ISL28290 is available in the 10 Ld UTQFN (1.8mmx1.4mm), 10 Ld MSOP and 8 LD SOIC packages. Device operation is guaranteed over −40°C to +125°C.

Related Information

For a full list of related documents, visit our website:

- ISL28290 device page

Features

- 1nV/√Hz input voltage noise
- 1kHz THD+N typical 0.00017% at $2V_{P-P}$ V_{OUT}
- Harmonic Distortion −87dBc, −90dBc, f_O = 1MHz
- 170MHz −3dB bandwidth
- 50V/µs slew rate
- 700µV maximum offset voltage
- 10µA typical input bias current
- 103dB typical CMRR
- 3V to 5.5V single supply voltage range
- Rail-to-rail output
- Ground sensing
- Enable pin (not available in the 8 Ld SOIC package option)
- Pb-free (RoHS compliant)

Applications

- Low noise signal processing
- Low noise microphones/preamplifiers
- ADC buffers
- DAC output amplifiers
- Digital scales
- Strain gauges/sensor amplifiers
- Radio systems
- Portable equipment
- Infrared detectors

Contents

1. Overview

1.1 Ordering Information

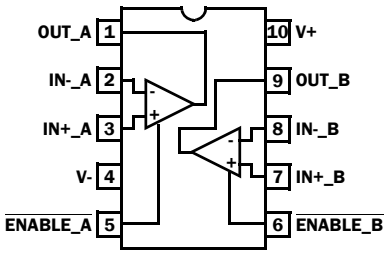
Part Number	Part[1] Marking	Temp Range (°C)	Tape and Reel[2] (Units)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL28290FUZ	8290Z	−40 to +125		10 Ld MSOP	M10.118A
ISL28290FUZ-T7	8290Z	−40 to +125	1.5k	10 Ld MSOP	M10.118A
ISL28290FRUZ-T7	E	−40 to +125	3k	10 Ld UTQFN	L10.1.8x1.4A
ISL28290FBZ	28290 FBZ	−40 to +125		8 Ld SOIC	M8.15E
ISL28290FBZ-T7	28290 FBZ	−40 to +125	1k	8 Ld SOIC	M8.15E
ISL28290EVAL1Z	Evaluation Board				

1. The part marking is located on the bottom of the part.
2. See TB347 for details about reel specifications.

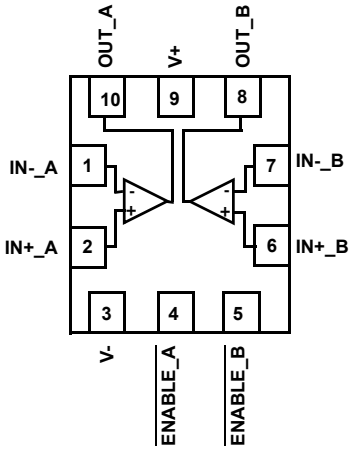
2. Pin Information

2.1 Pin Configuration

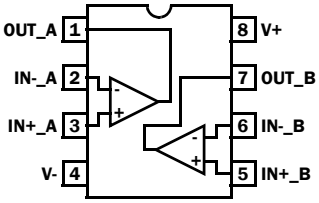
ISL28290
(10 Ld MSOP)
Top View



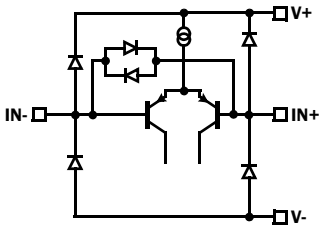
ISL28290
(10 Ld UTQFN)
Top View

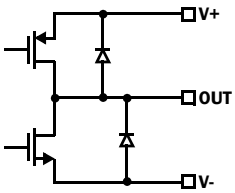
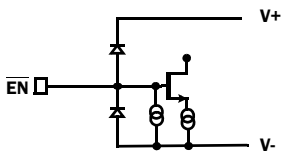


ISL28290
(8 Ld SOIC)
Top View



2.2 Pin Descriptions

ISL28290 (10 Ld MSOP)	ISL28290 (10 Ld UTQFN)	ISL28290 (8 Ld SOIC)	Pin Name	Function	Equivalent Circuit
2 (A) 8 (B)	1 (A) 7 (B)	2 (A) 6 (B)	IN− IN−_A IN−_B	Inverting input	 Circuit 1
3 (A) 7 (B)	2 (A) 6 (B)	3 (A) 5 (B)	IN+ IN+_A IN+_B	Non-inverting input	(See Circuit 1)
4	3	4	V−	Negative supply	

ISL28290 (10 Ld MSOP)	ISL28290 (10 Ld UTQFN)	ISL28290 (8 Ld SOIC)	Pin Name	Function	Equivalent Circuit
1 (A) 9 (B)	10 (A) 8 (B)	1 (A) 7 (B)	OUT OUT_A OUT_B	Output	 Circuit 2
10	9	8	V+	Positive supply	
5 (A) 6 (B)	4 (A) 5 (B)	N/A	EN EN_A EN_B	Enable BAR pin internal pull-down; Logic “1” selects the disabled state; Logic “0” selects the enabled state.	 Circuit 3

3. Specifications

3.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Supply Voltage		5.5	mA
Supply Turn-On Voltage Slew Rate		1	V/µs
Differential Input Current		5	mA
Differential Input Voltage		0.5	V
Input Voltage	V- − 0.5	V+ + 0.5	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	3		kV
Machine Model	300		V
Charged Device Model (Tested per JS-002-2014)	1200		V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

3.2 Thermal Information

Thermal Resistance (Typical)[1] [2] [3] [4]	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC Package	110	82
10 Ld MSOP Package	175	90
10 Ld UTQFN Package	190	140

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with direct attach features. See Tech Brief TB379.
3. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.
4. For θ_{JC}, the case temperature location is taken at the package top center.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+125	°C
Maximum Storage Temperature Range	−65	+150	°C
Pb-Free Reflow Profile	see TB493		

3.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage		5.0	V
Ambient Temperature	−40	+125	°C

3.4 Electrical Specifications

$V+ = 5.0V$, $V- = GND$, R_L = Open, $R_F = 1k\Omega$, $A_V = -1$ unless otherwise specified. Parameters are per amplifier. Typical values are at $V+ = 5V$, $T_A = +25°C$. Boldface limits apply over the operating temperature range, −40°C to +125°C, temperature data established by characterization.

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
DC Specifications						
Input Offset Voltage	V_{OS}		−1100	240	700	µV
					900	
Input Offset Drift vs Temperature	$\frac{\Delta V_{OS}}{\Delta T}$	See Figure 21		1.9		µV/°C
Input Offset Current	I_{IO}			40	500	nA
					900	
Input Bias Current	I_B			10	16	µA
					18	
Common-Mode Voltage Range	V_{CM}		**0**		**3.8**	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0V to 3.8V	78	103		dB
Power Supply Rejection Ratio	PSRR	V_S = 3V to 5V	74	80		dB
Large Signal Voltage Gain	A_{VOL}	V_O = 0.5V to 4V, $R_L = 1k\Omega$	94	102		dB
			90			
Maximum Output Voltage Swing	V_{OUT}	Output low, $R_L = 1k\Omega$		20	50	mV
					80	
		Output high, $R_L = 1k\Omega$, $V+ = 5V$	4.95	4.97		V
			4.92			
Supply Current per Channel, Enabled	$I_{S,ON}$			8.5	11	mA
					13	
Supply Current, Disabled	$I_{S,OFF}$			26	35	µA
					52	
Short-Circuit Output Current	I_O+	$R_L = 10\Omega$	95	144		mA
			90			

V+ = 5.0V, V− = GND, R_L = Open, R_F = 1kΩ, A_V = −1 unless otherwise specified. Parameters are per amplifier. Typical values are at V+ = 5V, T_A = +25°C. Boldface limits apply over the operating temperature range, −40°C to +125°C, temperature data established by characterization.(Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Short-Circuit Output Current	I_O−	R_L = 10Ω	95	135		mA
			90			
Supply Operating Range	V_{SUPPLY}	V+ to V−	**3**		**5.5**	V
$\overline{EN}$ High Level	$V_{\overline{ENH}}$	Referred to V−	**2**			V
$\overline{EN}$ Low Level	$V_{\overline{ENL}}$	Referred to V−			**0.8**	V
$\overline{EN}$ Pin Input High Current	$I_{\overline{ENH}}$	$V_{\overline{EN}}$ = V+		0.8	1.2	µA
					1.4	
$\overline{EN}$ Pin Input Low Current	$I_{\overline{ENL}}$	$V_{\overline{EN}}$ = V−		20	80	nA
					100	
AC Specifications						
−3dB Unity Gain Bandwidth	GBW	R_F = 0Ω C_L = 20pF, A_V = 1, R_L = 10kΩ		170		MHz
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, VOUT + $2V_{P-P}$, A_V = +1, R_L = 10kΩ		0.000 17		%
2nd Harmonic Distortion	HD (1MHz)	V_{OUT} = $2V_{P-P}$, A_V = 1		−87		dBc
3rd Harmonic Distortion				−90		dBc
Off-state Isolation f_O = 100kHz	ISO	A_V = +1; V_{IN} = 100mV_{P-P}; R_F = 0Ω, C_L = 20pF, A_V = 1, R_L = 10kΩ		−38		dB
Channel-to-Channel Crosstalk f_O = 100kHz	X-TALK	V_S = ±2.5V; A_V = +1; V_{IN} = $1V_{P-P}$, R_F = 0Ω, C_L = 20pF, A_V = 1, R_L = 10kΩ		−105		dB
Power Supply Rejection Ratio f_O = 100kHz	PSRR	V_S = ±2.5V; A_V = +1; V_{SOURCE} = $1V_{P-P}$, R_F = 0Ω, C_L = 20pF, A_V = 1, R_L = 10kΩ		−70		dB
Common Mode Rejection Ratio f_O = 100kHz	CMRR	V_S = ±2.5V; A_V = +1; V_{CM} = $1V_{P-P}$, R_F = 0Ω, C_L = 20pF, A_V = 1, R_L = 10kΩ		−65		dB
Input Referred Voltage Noise	e_n	f_O = 1kHz		1		nV/√Hz
Input Referred Current Noise	i_n	f_O = 10kHz		2.1		pA/√Hz
Transient Response						
Slew Rate	SR		30	50		V/µs
			25			
Propagation Delay 10% V_{IN} − 10% V_{OUT}	t_{pd}	A_V = 1, V_{OUT} = 100mV_{P-P}, R_F = 0Ω, C_L = 1.2pF		1.0		ns
Rise Time, t_r 10% to 90%	t_r, t_f, Small Signal	A_V = +1, V_{OUT} = $0.1V_{P-P}$, R_F = 0Ω, C_L = 1.2pF		3.3		ns
Fall Time, t_f 10% to 90%				6.3		ns

$V+ = 5.0V$, $V- = GND$, R_L = Open, $R_F = 1k\Omega$, $A_V = -1$ unless otherwise specified. Parameters are per amplifier. Typical values are at $V+ = 5V$, $T_A = +25°C$. Boldface limits apply over the operating temperature range, −40°C to +125°C, temperature data established by characterization.(Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Rise Time, t_r 10% to 90%	t_r, t_f Large Signal	A_V = +2, V_{OUT} = $1V_{P-P}$, $R_F = R_G = 499\Omega$, $R_L = 10k\Omega$, C_L = 1.2pF		44		ns
Fall Time, t_f 10% to 90%				51		ns
Rise Time, t_r 10% to 90%		A_V = +2, V_{OUT} = $4.7V_{P-P}$, $R_F = R_G = 499\Omega$, $R_L = 10k\Omega$, C_L = 1.2pF		190		ns
Fall Time, t_f 10% to 90%				187		ns
Settling Time to 0.1% 90% V_{OUT} to 0.1% V_{OUT}	t_s	A_V = 1, V_{OUT} = $1V_{P-P}$, $R_F = 0\Omega$, C_L = 1.2pF		45		ns
ENABLE to Output Turn-on Delay Time; 10% $\overline{EN}$ − 10% V_{OUT}	$t_{\overline{EN}}$	A_V = 1, V_{OUT} = 1VDC, $R_L = 10k\Omega$, C_L = 1.2pF		330		ns
ENABLE to Output Turn-off Delay Time; 10% $\overline{EN}$ − 10% V_{OUT}		A_V = 1, V_{OUT} = 0VDC, $R_L = 10k\Omega$, C_L = 1.2pF		50		ns

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

4. Typical Performance Curves

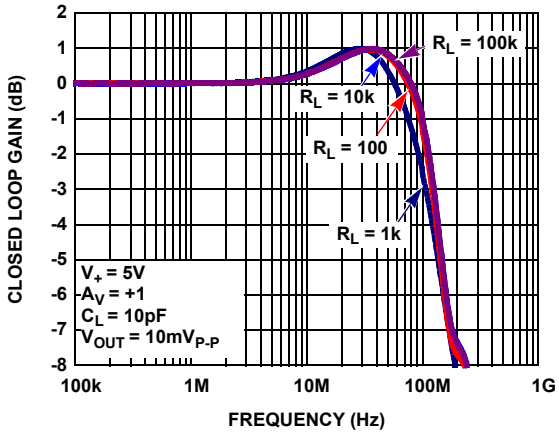


Figure 1. Gain vs Frequency For Various R_{LOAD}

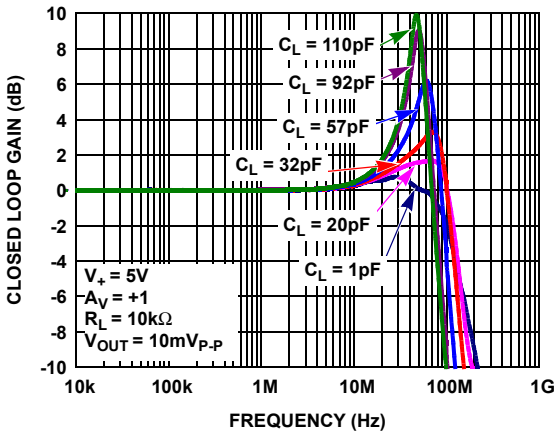


Figure 2. Gain vs Frequency For Various C_{LOAD}

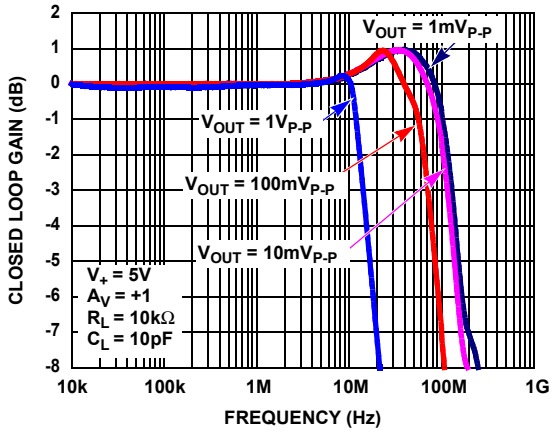


Figure 3. -3dB Bandwidth vs V_{OUT}

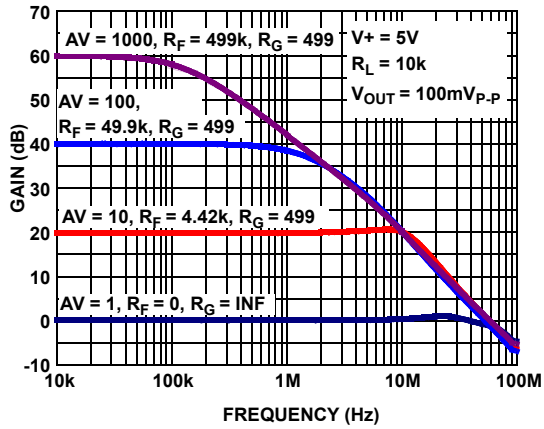


Figure 4. Frequency Response vs Closed Loop Gain

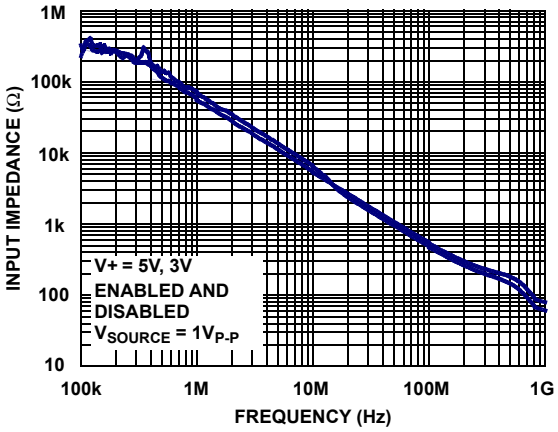


Figure 5. Input Impedance vs Frequency

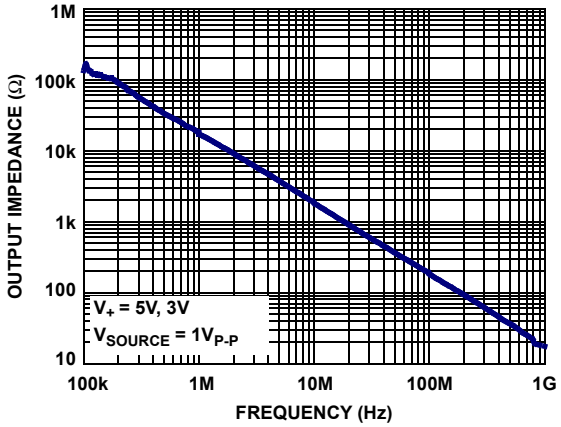


Figure 6. Disabled Output Impedance vs Frequency

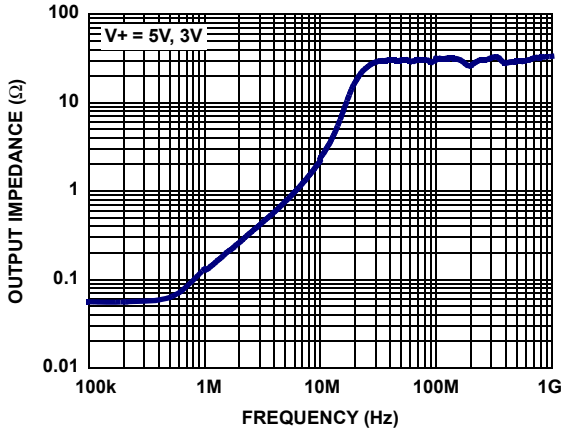


Figure 7. Enabled Output Impedance vs Frequency

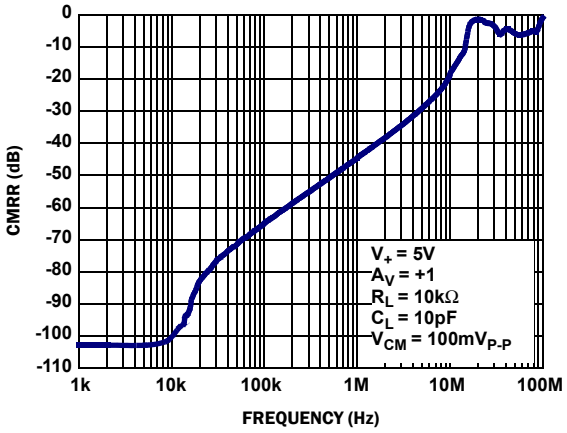


Figure 8. CMRR vs Frequency

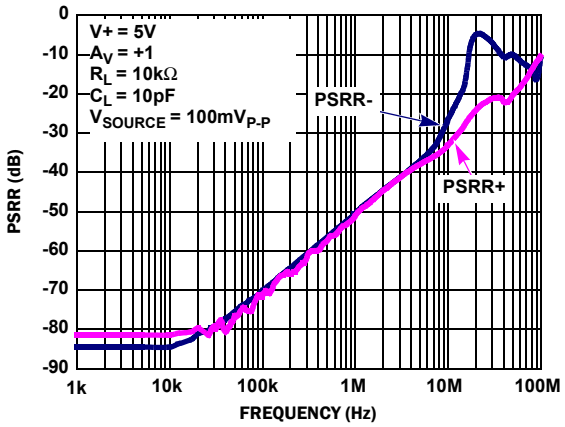


Figure 9. PSRR vs Frequency

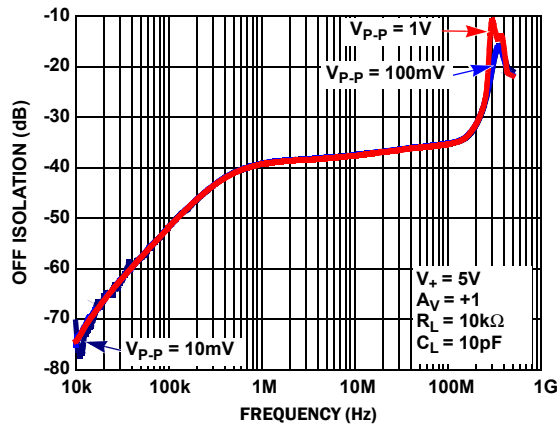


Figure 10. Off Isolation vs Frequency

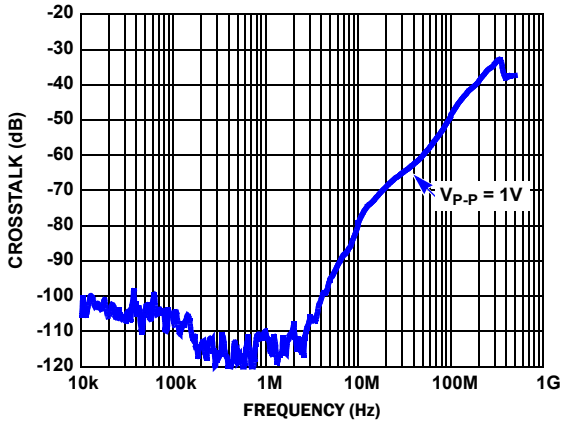


Figure 11. Channel-To-Channel Crosstalk vs Frequency

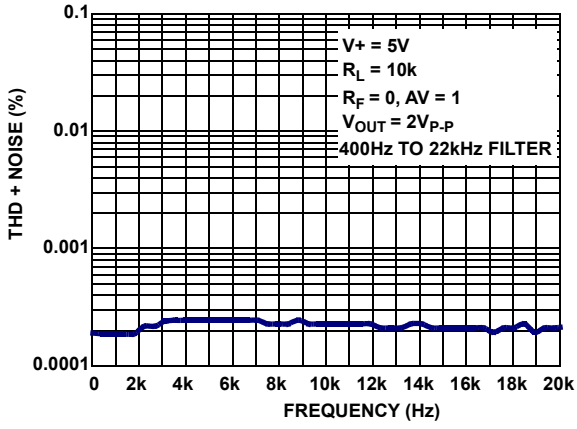


Figure 12. THD+N vs Frequency

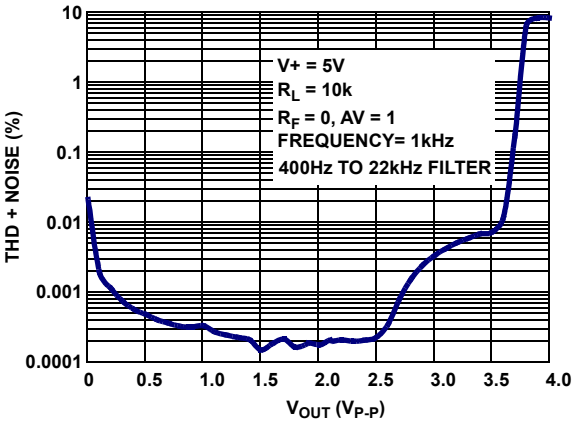


Figure 13. THD+N at 1kHz vs V_{OUT}

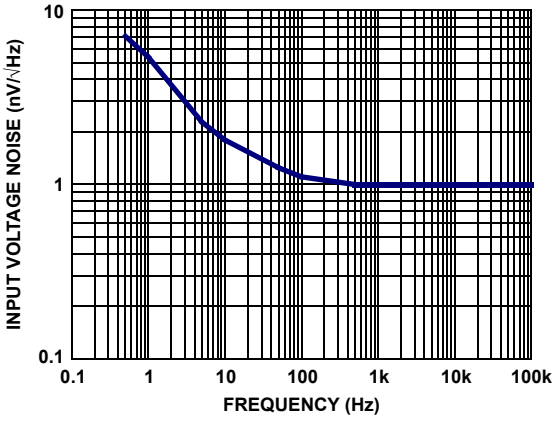


Figure 14. Input Referred Noise Voltage vs Frequency

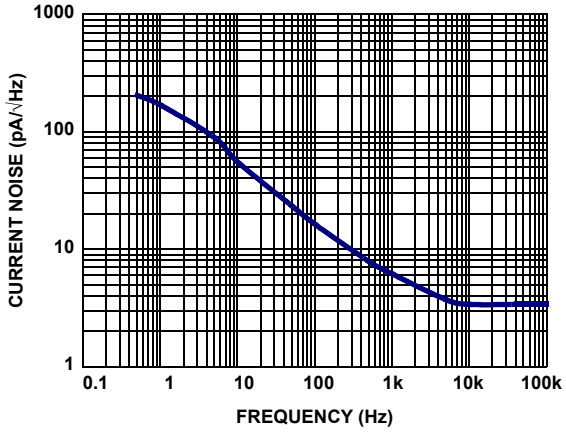


Figure 15. Input Referred Noise Current vs Frequency

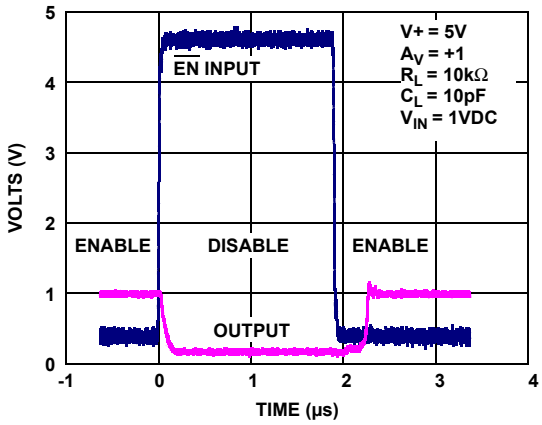


Figure 16. Enable/Disable Timing

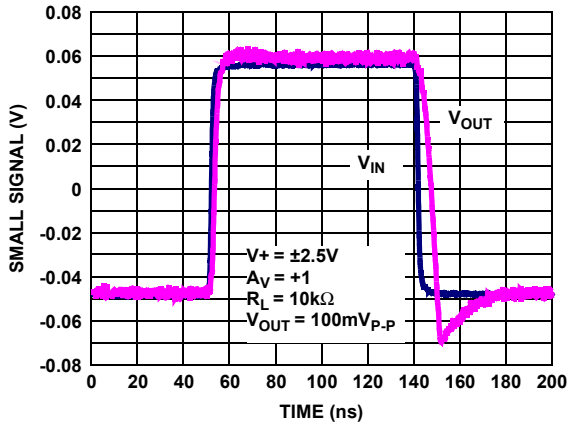


Figure 17. Small Signal Step Response

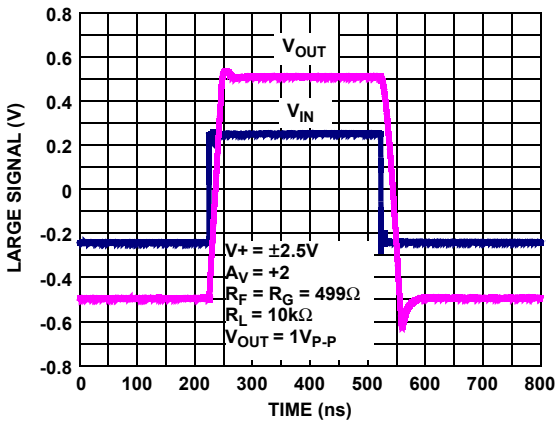


Figure 18. Large Signal (1V) Step Response

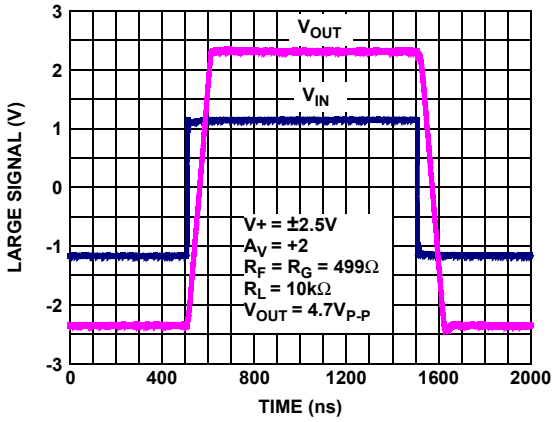


Figure 19. Large Signal (4.7V) Step Response

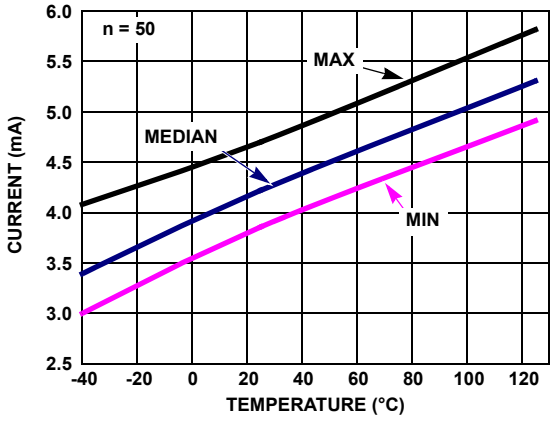


Figure 20. Supply Current vs Temperature, V_S = ±2.5V Enabled, R_L = INF

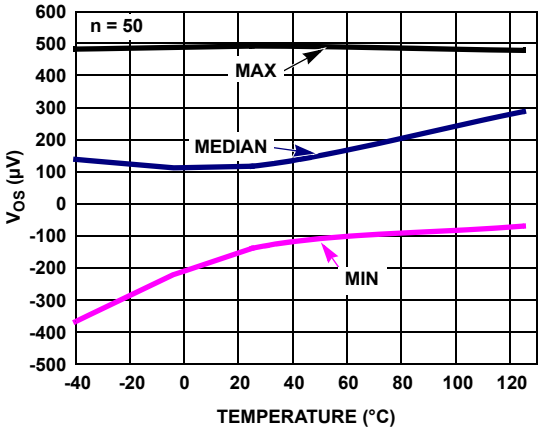


Figure 21. V_{OS} vs Temperature V_S = ±2.5V

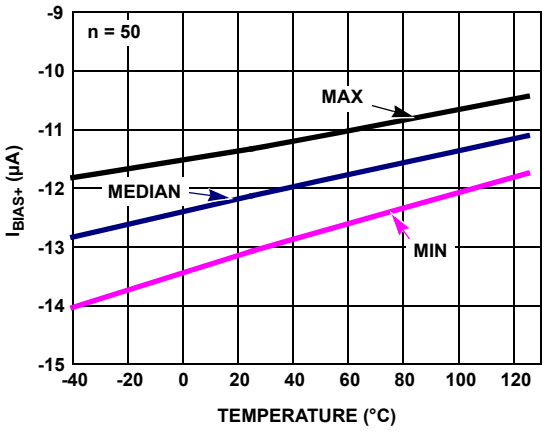


Figure 22. I_{BIAS}+ vs Temperature V_S = ±2.5V

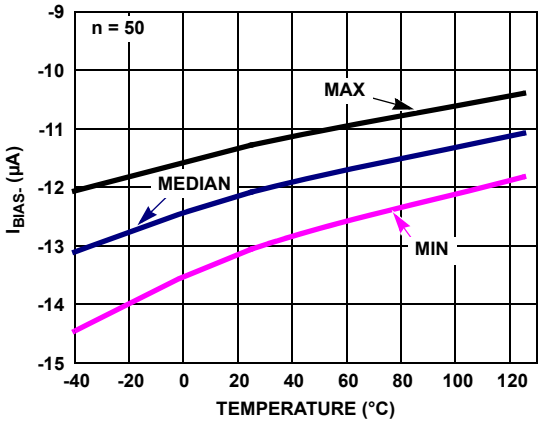


Figure 23. I_{BIAS}- vs Temperature V_S = ±2.5V

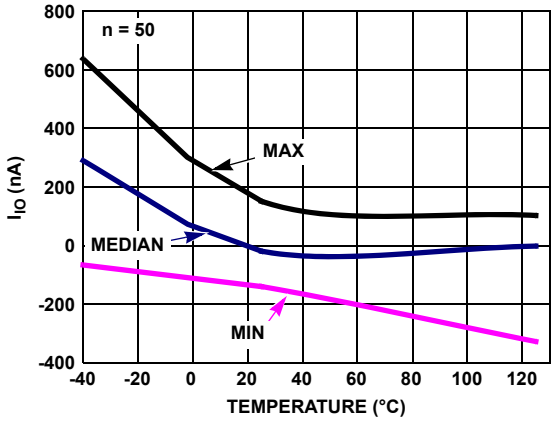


Figure 24. I_{IO} vs Temperature V_S = ±2.5V

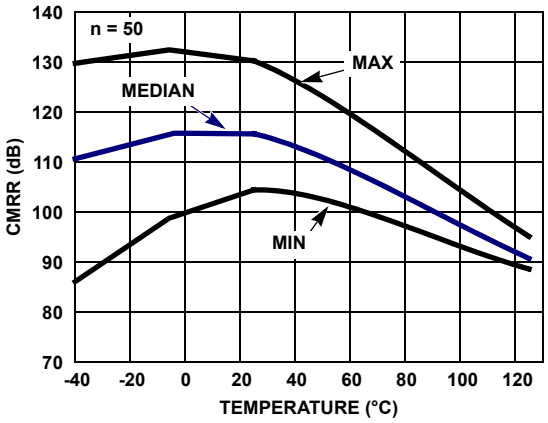


Figure 25. CMRR vs Temperature, VCM = 3.8V, V_S = ±2.5V

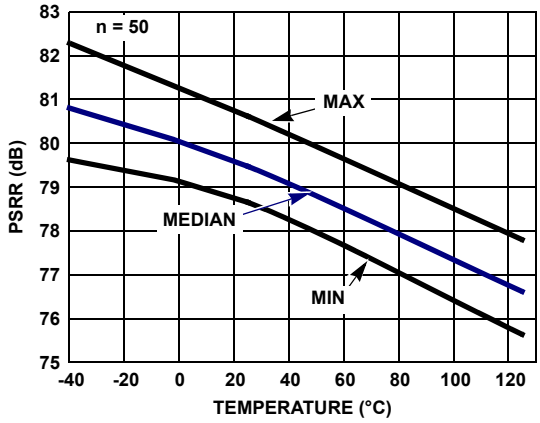


Figure 26. PSRR vs Temperature ±1.5V to ±2.5V

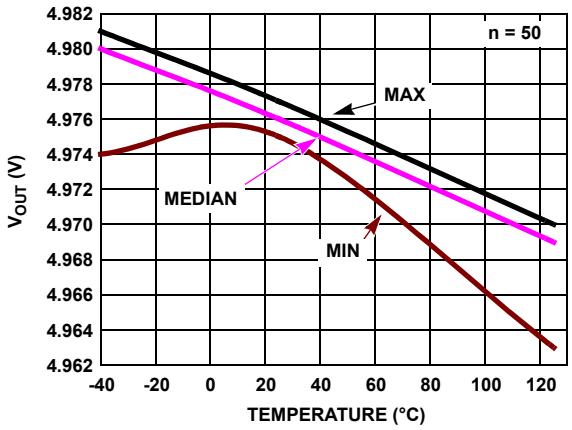


Figure 27. Positive V_{OUT} vs Temperature RL = 1k, V_S = ±2.5V

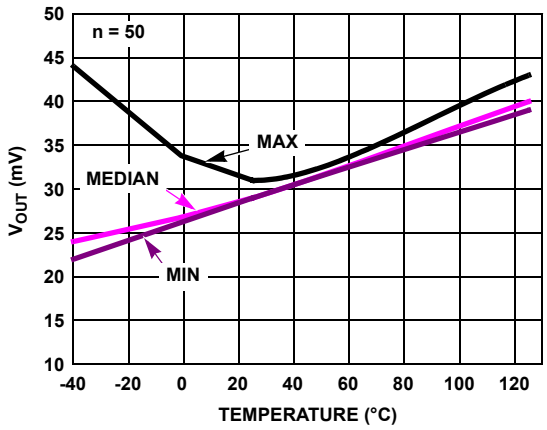


Figure 28. Negative V_{OUT} vs Temperature RL = 1k, V_S = ±2.5V

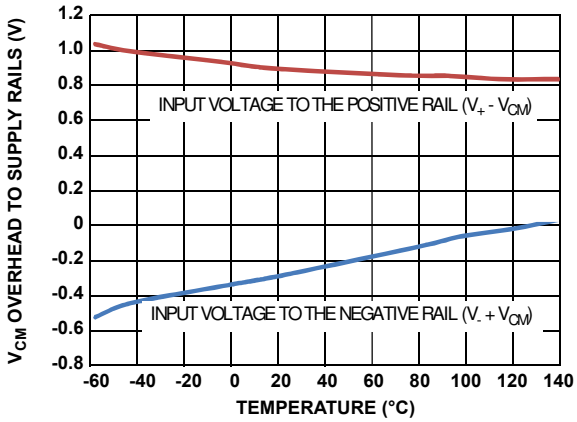


Figure 29. Input Common Mode Voltage vs Temperature

5. Applications Information

5.1 Product Description

The ISL28290 is a voltage feedback operational amplifier designed for communication and imaging applications requiring low distortion, very low voltage and current noise. The part features high bandwidth while drawing moderately low supply current. The ISL28290 uses a classical voltage-feedback topology, which allows it to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier.

5.2 Enable/Power-Down

The ISL28290 amplifier is disabled by applying a voltage greater than 2V to the EN pin, with respect to the V- pin. In this condition, the output(s) will be in a high impedance state and the amplifier current will be reduced to 13µA/Amp. By disabling the part, multiple parts can be connected together as a MUX. The outputs are tied together in parallel and a channel can be selected by the EN pin. The EN pin also has an internal pull-down. If left open, the EN pin will pull to the negative rail and the device will be enabled by default.

5.3 Input Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. The device has additional back-to-back diodes across the input terminals (as shown in Figure 30). In pulse applications where the input Slew Rate exceeds the Slew Rate of the amplifier, the possibility exists for the input protection diodes to become forward biased. This can cause excessive input current and distortion at the outputs. If overdriving the inputs is necessary, the external input current must never exceed 5mA. An external series resistor may be used to limit the current, as shown in Figure 30.

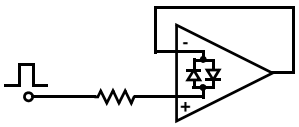


Figure 30. Limiting the Input Current to Less Than 5mA

5.4 Using Only One Channel

The ISL28290 is a Dual channel op amp. If the application only requires one channel when using the ISL28290, the user must configure the unused channel to prevent it from oscillating. Oscillation can occur if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the negative input and ground the positive input (as shown in Figure 31).

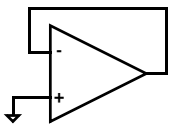


Figure 31. Preventing Oscillations in Unused Channels

5.5 Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Low impedance ground plane construction is essential. Surface mount components are recommended, but if leaded components are used, lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7µF tantalum capacitor in parallel with a 0.01µF capacitor has been shown to work well when placed at each supply pin.

For good AC performance, parasitic capacitance should be kept to a minimum, especially at the inverting input. When ground plane construction is used, it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of additional series inductance. Use of sockets, particularly for the SO package, should be avoided if possible. Sockets add parasitic inductance and capacitance, which will result in additional peaking and overshoot.

5.6 Current Limiting

The ISL28290 has no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device. This is why output short circuit current is specified and tested with RL = 10Ω.

5.7 Power Dissipation

It is possible to exceed the +125°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (TJMAX) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related as follows:

(EQ. 1) $$T_{JMAX} = T_{MAX} + (\theta_{JA} x PD_{MAXTOTAL})$$

where:

- $PD_{MAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PDMAX)
- PD_{MAX} for each amplifier can be calculated as follows:

(EQ. 2) $$PD_{MAX} = 2*V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L}$$

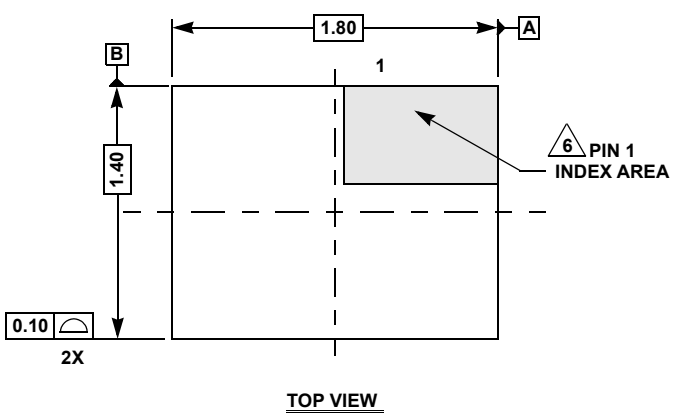
- where T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Supply voltage
- I_{MAX} = Maximum supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

6. Revision History

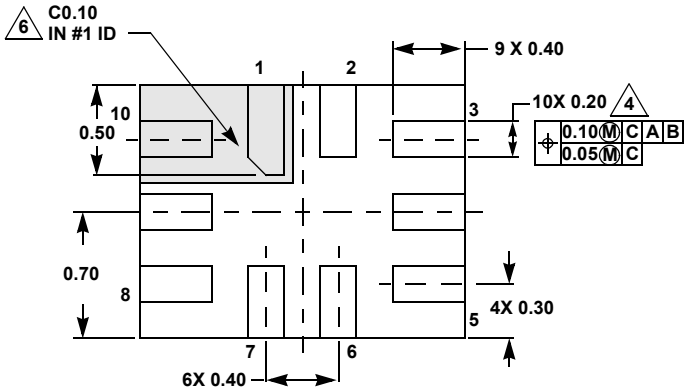
Rev.	Description	Description
12.00	Jan.12.21	Datasheet formatting overhaul. Removed all references to ISL28190.

7. Package Outline Drawings

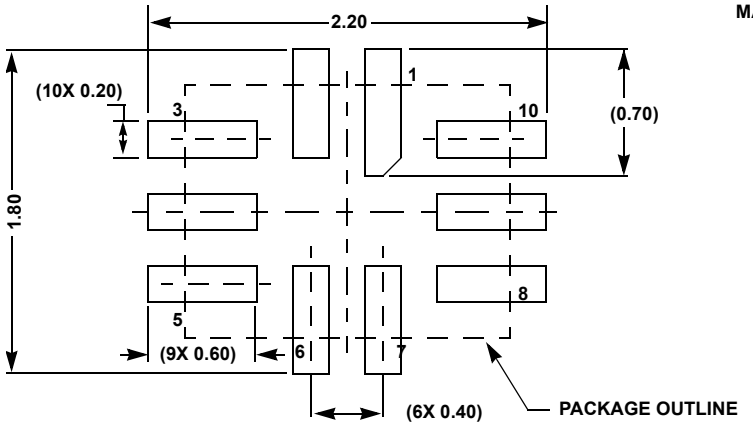
L10.1.8x1.4A
10 Lead Ultra Thin Quad Flat No-lead Plastic Package
Rev 6, 8/13



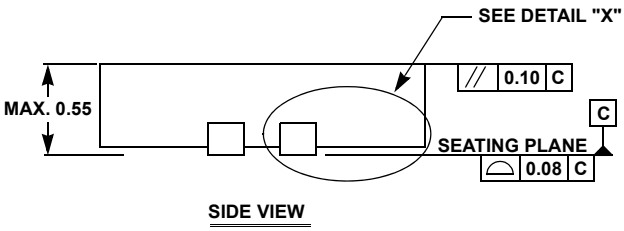
TOP VIEW



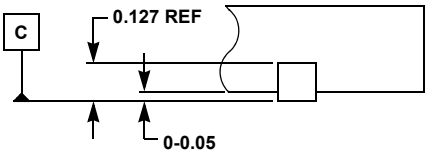
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

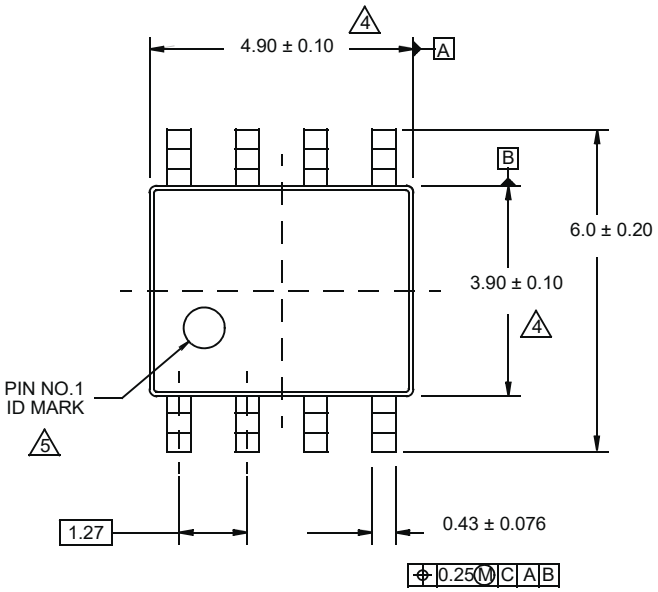


DETAIL "X"

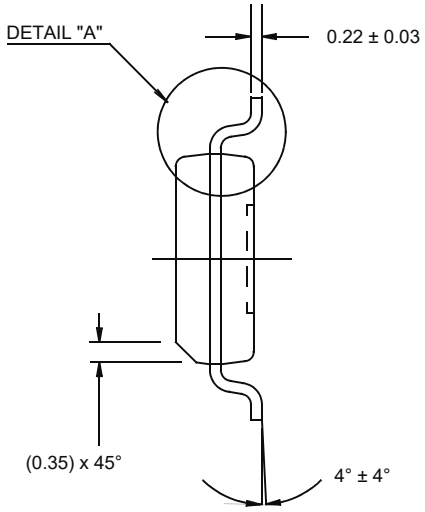
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Lead width dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. JEDEC reference MO-255.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

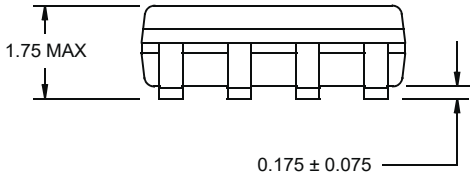
M8.15E
8 Lead Narrow Body Small Outline Plastic Package
Rev 0, 08/09



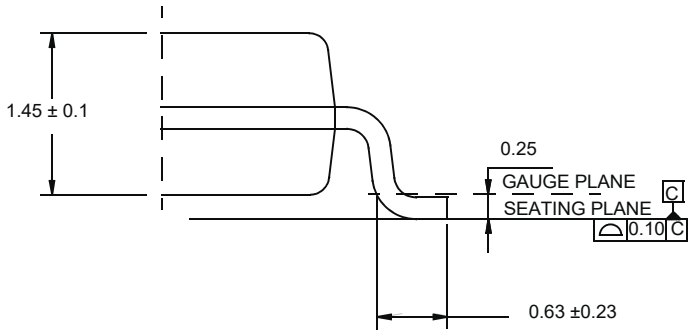
TOP VIEW



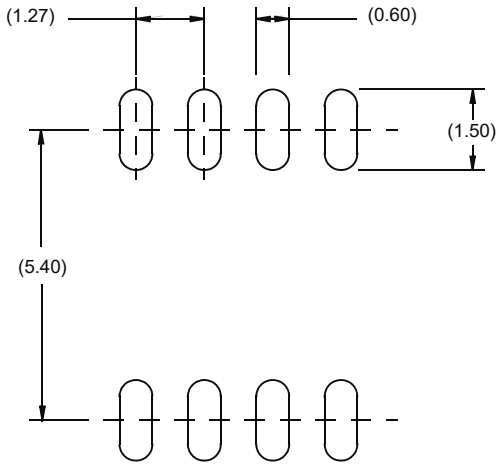
SIDE VIEW “B”



SIDE VIEW “A



DETAIL "A"

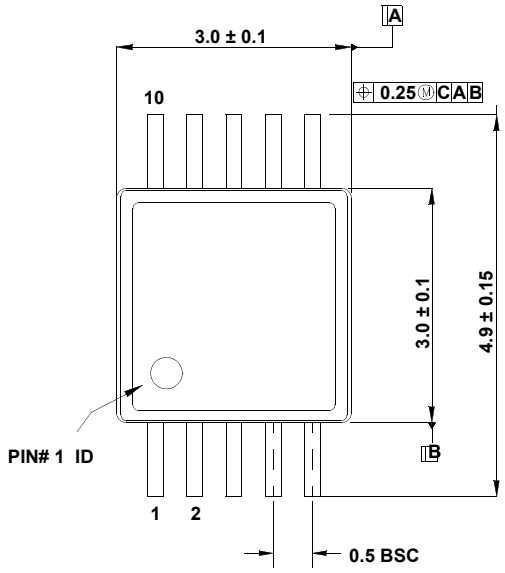


TYPICAL RECOMMENDED LAND PATTERN

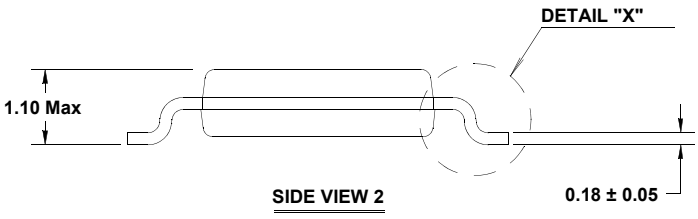
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

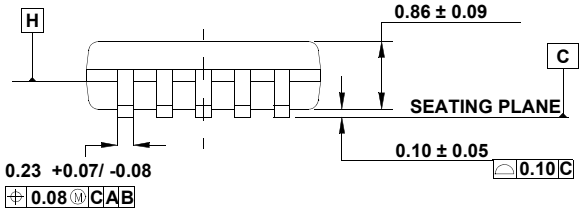
M10.118A (JEDEC MO-187-BA)
10 Lead Mini Small Outline Plastic Package (MSOP)
Rev 0, 9/09



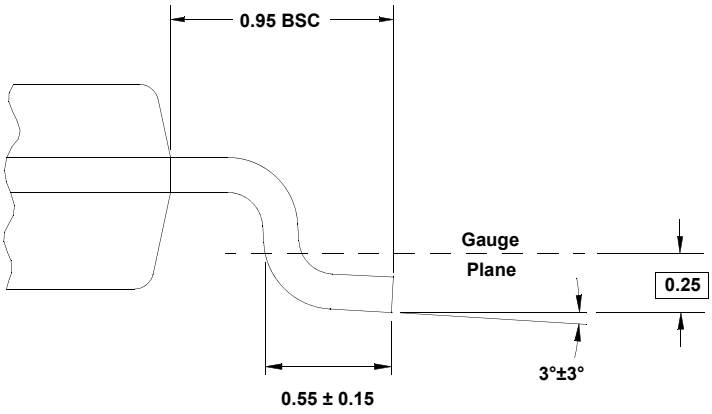
TOP VIEW



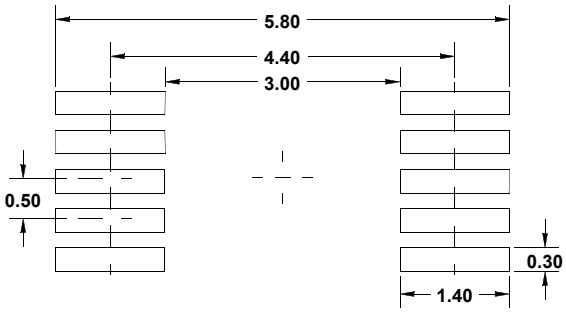
SIDE VIEW 2



SIDE VIEW 1



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.25mm max per side are not included.
5. Dimensions “D” and “E1” are measured at Datum Plane “H”.
6. This replaces existing drawing # MDP0043 MSOP10L.

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