Automotive Qualified, Dual-Channel, Precision ADCs with LIN2.2 Slave Interface

Data Sheet

ADuCM300

FEATURES

- Two precision 20-bit Σ-Δ ADCs
- Programmable ADC conversion rates from 4 Hz to 8000 Hz
- On-chip precision voltage reference
- Primary ADC
  - Differential voltage inputs to a 20-bit Σ-Δ ADC
  - Programmable gain (from 4 to 512)
  - Digital comparator with accumulator
  - ADC absolute input voltage range: −200 mV to +300 mV
- Auxiliary ADC
  - Flexible input mux for input channel selection
  - Single-ended voltage input (can be interfaced to an external temperature sensor), internal temperature sensor input, or diagnostic supply input
- Microcontroller
  - Arm Cortex-M3 32-bit processor
  - 16.384 MHz precision oscillator with 1% accuracy
  - Serial wire download (SWD) port supporting code download and debug
- Automotive qualified integrated LIN transceiver
  - LIN 2.2-compatible slave
  - SAE J-2602-compatible slave
  - Low electromagnetic emissions (EME)
  - High electromagnetic immunity (EMI)
- Memory
  - 128 kB Flash/EE memory, ECC
  - 6 kB SRAM, ECC
  - 4 kB data Flash/EE memory, ECC
  - 10,000 cycle Flash/EE endurance
  - 20-year Flash/EE data retention
- In circuit download via SWD and LIN
- On-chip peripherals: SPI, GPIO port, general-purpose timer, wake-up timer, watchdog timer, and on-chip POR
- Power
  - Operates directly from an external voltage supply, varying from 3.6 V to 18 V
  - Power consumption, 8 mA typical (16 MHz) at T_A = −40°C to +115°C
  - Low power monitor mode
- Package and temperature range
  - 6 mm × 6 mm, 32-lead LFCSP
  - Fully specified for −40°C to +115°C operation, additional specifications are available for +115°C to +125°C operation
  - AEC-Q100 qualified for automotive applications

APPLICATIONS

- LIN sensor interface for automotive applications
- General powertrain, body and chassis sensing
- Current and voltage sensing for industrial applications

Rev. 0
Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

6/2019—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

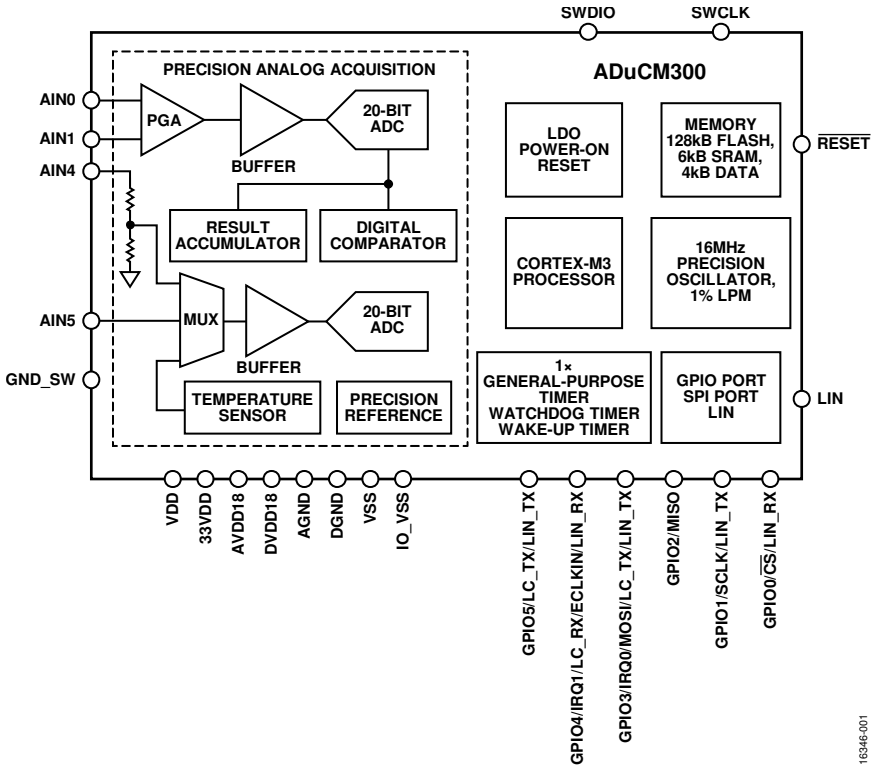

Figure 1.

GENERAL DESCRIPTION

The ADuCM300 is a fully integrated, 8 kSPS (8000 Hz conversion rate) data acquisition system that incorporates dual, high performance, Σ-Δ analog-to-digital converters (ADCs), a 32-bit Arm® Cortex®-M3 processor, and microcontroller unit (MCU) subsystem. The ADuCM300 has a 128 kB program Flash/EE, 4 kB data Flash/EE, and 6 kB static random access memory (SRAM).

The ADuCM300 is a complete system solution for external precision sensor voltage measurements in automotive applications. Minimizing external system components, the device can be powered directly from an external voltage supply that varies from 3.6 V to 18 V. On-chip, low dropout (LDO) regulators generate the supply voltages for the integrated digital and analog subsystems.

The analog subsystem consists of two 20-bit Σ-Δ ADCs: a primary ADC and an auxiliary ADC. The primary ADC accepts a differential input and is ideally suited to interface external sensors with low level signal amplitude outputs integrating a low noise, programmable gain amplifier (PGA), and precision, low drift reference. The auxiliary ADC is connected to a flexible input multiplexer and can measure external single-ended sensor input voltages (AIN5/GND_SW), the internal (on-chip) temperature sensor, or monitor the supply voltage connected to AIN4 (see Figure 1).

The ADuCM300 operates from an on-chip, 16.384 MHz, high frequency oscillator that supplies the system clock. This clock is routed through a programmable clock divider from which the core clock operating frequency is generated. The device also contains a 32 kHz oscillator for low power operation.

The ADuCM300 integrates a range of on-chip peripherals that can be configured under core software control as required in the application. These peripherals include a serial peripheral interface (SPI) input/output communication controller, six general-purpose input/output (GPIO) pins, one general-purpose timer, a wake-up timer (WUT), and a watchdog timer (WDT).

The ADuCM300 operates in battery-powered applications where low power operation is critical. The microcontroller core can be configured in normal operating mode, resulting in an overall system current consumption of <18.5 mA when all peripherals are active. The device can also be configured in a number of low power operating modes under direct program control, consuming <100 µA. The ADuCM300 includes a local interconnect network (LIN) physical interface for single wire, high voltage communications in automotive environments.

The device operates from an external 3.6 V to 18 V (on VDD, Pin 26) voltage supply and is specified over the −40°C to +115°C temperature range, with additional specifications available for the +115°C to +125°C temperature range.

For more information and register details, see the ADuCM300 Hardware Reference Manual.

SPECIFICATIONS

Specifications are valid for VDD = 3.6 V to 18 V, Arm core frequency (f_{CORE}) = 16.384 MHz, clock divider bits = 0, and voltage reference (V_{REF}) = 1.2 V (internal), unless otherwise stated. The device is fully specified for the temperature range of T_A = −40°C to +115°C. Parameters specified in the 115°C to 125°C temperature range of operation are functional within this range, but with degraded performance. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise stated.

Table 1.

		T_A = −40°C to +115°C			T_A = 115°C to 125°C[1]			
Parameter	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
ADC SPECIFICATIONS								
Conversion Rate[1]	ADC normal operating mode	4		8000				Hz
	ADC low power mode, chop on	1		656				Hz
Primary ADC (AIN0/AIN1 Only)								
No Missing Codes[1]	Valid for all ADC update rates and ADC modes	20						Bits
Total Gain Error[1, 2, 3, 4]	Factory calibrated at a gain of 8, normal mode	−0.5	±0.1	+0.5		±0.15		%
	Low power mode	−1	±0.2	±1				%
Integral Nonlinearity (INL)[1, 5, 6]	ADCFLT = 0x10001, 0x08101, 0x00007	−200	±10	+200		±80		ppm of full-scale range (FSR)
Offset Error[1, 3, 4]	Chop off, gain = 4, 8, or 16, external short, after user system calibration at 25°C, 1 LSB = 2.28 µV ÷ gain	−100	±24	+100				LSBs
	Chop off, gain = 32 or 64, external short, after user system calibration at 25°C, 1 LSB = 2.28 µV ÷ gain	−160	±48	+160				LSBs
	Chop off, gain = 512, external short, after user system calibration at 25°C, 1 LSB = 2.28 µV ÷ gain	−1400	±60	+1400				LSBs
	Chop on, external short, low power mode, gain = 64 or 512, processor powered down	−300	±50	+250		±250		nV
	Chop on, external short, after user system calibration at 25°C, VDD = 18 V	−1.5		+1.5				µV
Offset Error Drift[1, 5, 7]	Chop off, gains of 4 to 64, normal mode		±0.48					LSB/°C
	Chop on		±5			±5		nV/°C
Gain Drift[1, 8]			±3			±3		ppm/°C
PGA Gain Mismatch Error			±0.1			±0.1		%
Output Noise[1]	Register ADC0CON, PGASCALE bits (Bits[11:10]) = 0x3							
	Gain = 64, ADCFLT = 0x08101		0.80			1.2		µV rms
	Gain = 64, ADCFLT = 0x00007		0.75					µV rms
	Gain = 32, ADCFLT = 0x08101		1.00			1.3		µV rms
	Gain = 32, ADCFLT = 0x00007		0.80					µV rms
	Gain = 16, ADCFLT = 0x08101		1.50			2.0		µV rms
	Gain = 16, ADCFLT = 0x00007		1.10					µV rms
	Gain = 8, ADCFLT = 0x08101		2.10			2.5		µV rms
	Gain = 8, ADCFLT = 0x00007		1.60					µV rms
	Gain = 4, ADCFLT = 0x08101		3.40			4.0		µV rms
	Gain = 4, ADCFLT = 0x00007		2.60					µV rms
	Gain = 64, ADCFLT = 0x10001		1.60			1.85		µV rms
	Gain = 32, ADCFLT = 0x10001		1.70			2.0		µV rms
	Gain = 16, ADCFLT = 0x10001		2.00			2.1		µV rms
	Gain = 8, ADCFLT = 0x10001		2.40			3.0		µV rms
	Gain = 4, ADCFLT = 0x10001		4.35			5.0		µV rms
	ADC low power mode, 221 Hz update rate, chop enabled, gain = 64		0.6			0.8		µV rms

Parameter	Test Conditions/Comments	T_A = −40°C to +115°C			T_A = 115°C to 125°C[1]			Unit
		Min	Typ	Max	Min	Typ	Max	
Auxiliary ADC, AIN4 Only[1, 9]								
No Missing Codes	Valid at all ADC update rates	20						Bits
Total Gain Error[3, 4, 10]	Includes resistor mismatch	−0.25	±0.06	+0.25		±0.1		%
	T_A = −25°C to +65°C	−0.15	±0.03	+0.15				%
INL	From 6 V to 18 V, ADCFLT = 0x10001, 0x08101, 0x00007	−350	±10	+350		±150		ppm of FSR
Offset Error[3, 4]	Chop off, 1 LSB = 27.4 µV, after two-point calibration	−160	±16	+160				LSB
	Chop on, after two-point calibration, offset measured using a 0 V differential voltage into the ADC voltage (V_{ADC}) auxiliary pins	−16	±4.8	+16		±4.8		LSB
Offset Error Drift[7]	Chop off		±0.48			±3		LSB/°C
Gain Drift[8]	Includes resistor mismatch drift		±3					ppm/°C
Output Noise[11]	10 Hz update rate, chop on		50					µV rms
	ADCFLT = 0x00007		180					µV rms
	ADCFLT = 0x08101		280			300		µV rms
	ADCFLT = 0x10001		400			470		µV rms
Auxiliary ADC, AIN5 Only[1]								
No Missing Codes	Valid at all ADC update rates	20						Bits
Total Gain Error[3, 12]		−0.25	±0.06	+0.25		±0.10		%
INL	ADCFLT = 0x10001, 0x08101, 0x00007	−60	±10	+60		±15		ppm of FSR
Offset Error[3, 12]								
Chop Off	Chop off, 1 LSB = 1.14 µV (unipolar mode), after two-point calibration	−160	±48	+160				LSB
Chop On	Chop on	−80	+16	+80		+16		LSB
Offset Error Drift	Chop off		±0.48			±0.48		LSB/°C
Gain Drift[8]			3			3		ppm/°C
Output Noise	1 kHz update rate, ADCFLT = 0x00007		7.5			10		µV rms
ADC SPECIFICATIONS, ANALOG INPUT	Register ADC0CON, PGASCALE bits (Bits[11:10]) = 0x3							
Primary ADC[1]								
Absolute Input Voltage Range	Applies to both AIN0 and AIN1	−200		+300				mV
Input Voltage Range[13]								
	Gain = 4, limited by absolute input voltage range		±300					mV
	Gain = 8		±150					mV
	Gain = 32		±37.5					mV
	Gain = 512		±2.3					mV
Input Leakage Current[14]		−3		+3		±0.2		nA
Input Offset Current[14]			0.2	0.8		0.4		nA
Auxiliary ADC, AIN4 Only								
Absolute Input Voltage Range[1]	Voltage ADC specifications valid in this range	6		18				V
Input Voltage Range[1]			0 to 28.8					V
Input Current	AIN4 = 18 V	5	9	13		11		µA

Parameter	Test Conditions/Comments	T_A = −40°C to +115°C Min	Typ	Max	T_A = 115°C to 125°C[1] Min	Typ	Max	Unit
Auxiliary ADC, AIN5 Only	VREF = AVDD18 and GND_SW							
Absolute Input Voltage Range[1, 15]		100		1500				mV
Input Voltage Range[1]			0 to 1.4					V
Input Current[1]			2.5	10		3.5		nA
VOLTAGE REFERENCE								
Internal Reference			1.2			1.2		V
Power-Up Time[1]			0.5			0.5		ms
Initial Accuracy[1]	Measured at T_A = 25°C	−0.15		+0.15				%
Temperature Coefficient[1, 16]		−20	±5	+20		±8		ppm/°C
Long-Term Stability[17, 18]			100					ppm/1000 hours
ADC DIAGNOSTICS								
AVDD18 ÷ 136 Accuracy[1, 5, 19]	At any gain setting	12		14				mV
Voltage Attenuator Current Source Accuracy	Differential voltage increases on the attenuator when current on	2.4		3.2		2.8		V
RESISTIVE ATTENUATOR								
Divider Ratio			24					
Resistor Mismatch Drift	Implicit in the auxiliary ADC total gain error specification		±3					ppm/°C
ADC GROUND SWITCH								
Resistor to Ground		45	60	75				kΩ
TEMPERATURE SENSOR[1, 20]	Processor in hibernate mode							
Accuracy		−3	±1	+3	−3.5	±1	+3.5	°C
	T_A = −25°C to +85°C	−2.5	±0.5	+2.5				°C
	T_A = −10°C to +55°C	−2	±0.5	+2				°C
POWER-ON RESET (POR)[1]	Refers to voltage at the VDD pin							
Trip Level		2.8	3.1	3.4		3.3		V
Hysteresis			0.1					V
LOW VOLTAGE FLAG								
Low Voltage Flag Level	Refers to voltage at the VDD pin	2.6	2.75	3.00				V
WDT								
Shortest Timeout Period	32,768 Hz clock with a prescaler of 1		30.5			30.5		µs
Longest Timeout Period	32,768 Hz clock with a prescaler of 4096		8192					sec
FLASH/EE MEMORY								
Program Flash Size			128					kB
Data Flash Size			4					kB
Endurance[21]		10,000						Cycles
Data Retention[22]		20						Years
LOGIC INPUTS[1]								
Input Voltage								
Low (V_{INL})				0.4				V
High (V_{INH})		2.0						V
LOGIC OUTPUTS[1]	All logic outputs, measured with ±1 mA load							
Output Voltage								
High (V_{OH})		33VDD − 0.4						V
Low (V_{OL})				0.4				V

Parameter	Test Conditions/Comments	T_A = −40°C to +115°C Min	Typ	Max	T_A = 115°C to 125°C[1] Min	Typ	Max	Unit
DIGITAL INPUTS[1]	All digital inputs except $\overline{\text{RESET}}$, SWDIO, and SWCLK							
Input Current (Leakage Current)								
Logic 1	V_{INH} = 3.3 V	−10	±1	+10				µA
Logic 0	V_{INL} = 0 V	−10	±1	+10				µA
Input Capacitance			10					pF
ON-CHIP OSCILLATORS								
Low Frequency Oscillator			32,768					Hz
Accuracy			±5					%
	After a calibration from high frequency oscillator	−6		+6				%
High Frequency Oscillator			16.384					MHz
Accuracy								
LINCAL[1, 23]		−0.7	±0.5	+0.75				%
High Precision Mode		−1		+1				%
Low Precision Mode		−3		+3				%
PROCESSOR START-UP TIME[1]								
At Power-On	Includes kernel power-on execution time, VDD drops to <0.8 V		18					ms
Brownout	VDD drops below POR voltage but not below 0.8 V		1.15					ms
After Reset Event	Includes kernel power-on execution time		1.25					ms
Wake-Up from LIN			0.15					ms
LIN INPUT/OUTPUT GENERAL[1]								
Baud Rate		1000		20,000				Bits/sec
VDD	Supply voltage range for which the LIN interface is functional	7		18				V
LIN Comparator Response Time			38	90				µs
LIN DC PARAMETERS								
Current Limit for Driver when LIN Bus is in Dominant State ($I_{LIN\_DOM\_MAX}$)	VBAT = VBAT (maximum)	40		200				mA
Driver Off ($I_{LIN\_PAS\_REC}$)[1]	7.0 V < voltage of LIN bus (V_{BUS}) < 18 V, VDD = input leakage voltage (V_{LIN}) − 0.7 V			20				µA
Input Leakage Current at Receiver ($I_{LIN\_PAS\_DOM}$)[1]	V_{LIN} = 0 V, VBAT = 12 V, driver off	−1						mA
Control Unit Disconnected from Ground ($I_{LIN\_NO\_GND}$)[1, 24]	Ground = VDD, 0 V < V_{LIN} < 18 V, VBAT = 12 V	−1		+1				mA
VBAT Disconnected ($I_{BUS\_NO\_BAT}$)[1]	VDD = ground, 0 V < V_{BUS} < 18 V			30				µA
LIN Receiver Dominant State (V_{LIN_DOM})[1]	VDD > 7.0 V			0.4 × VDD				V
LIN Receiver Recessive State (V_{LIN_REC})[1]	VDD > 7.0 V	0.6 × VDD						V
LIN Receiver Threshold Center (V_{LIN_CNT})[1]	V_{LIN_CNT} = (receiver threshold of recessive to dominant bus edge (V_{TH_DOM}) + receiver threshold of dominant to recessive bus edge (V_{TH_REC}))/2, VDD > 7.0 V	0.475 × VDD	0.5 × VDD	0.525 × VDD				V

Parameter	Test Conditions/Comments	T_A = −40°C to +115°C Min	Typ	Max	T_A = 115°C to 125°C[1] Min	Typ	Max	Unit
LIN Receiver Threshold Hysteresis (V_{HYS})[1]	$V_{HYS} = V_{TH\_REC} - V_{TH\_DOM}$			0.175 × VDD				V
LIN Dominant Output Voltage with Supply Voltage Low ($V_{LIN\_DOM\_DRV\_LOSUP}$)[1]	VDD = 7.0 V							
Load Resistance (R_L) = 500 Ω				1.2				V
R_L = 1000 Ω		0.6						V
LIN Dominant Output Voltage with Supply Voltage High ($V_{LIN\_DOM\_DRV\_HISUP}$)[1]	VDD = 18 V							
R_L = 500 Ω				2				V
R_L = 1000 Ω		0.8						V
LIN Recessive Output Voltage ($V_{LIN\_RECESSIVE}$)[1]		0.8 × VDD						V
VBAT Shift[1, 24]		0		0.115 × VDD				V
Ground Shift[1, 24]		0		0.115 × VDD				V
Slave Termination Resistance (R_{SLAVE})		20	30	47		30		kΩ
Voltage Drop at the Serial Diode (V_{SERIAL_DIODE})[1]		0.4	0.7	1				V
LIN AC PARAMETERS[1]	Bus load conditions (bus capacitance (C_{BUS})||bus resistance (R_{BUS})): 1 nF||1 kΩ or 6.8 nF||660 Ω or 10 nF||500 Ω							
Duty Cycle 1 (D1)	Threshold recessive maximum ($TH_{REC(MAX)}$) = 0.744 × VBAT, threshold dominant maximum ($TH_{DOM(MAX)}$) = 0.581 × VBAT, supply voltage at transceiver (V_{SUP}) = 7.0 V to 18 V, time of one bit on the LIN bus (t_{BIT}) = 50 µs, D1 = minimum time for a bus recessive signal ($t_{BUS\_REC(MIN)}$)/(2 × t_{BIT})	0.396						
Duty Cycle 2 (D2)	Threshold recessive minimum ($TH_{REC(MIN)}$) = 0.284 × VBAT, threshold dominant minimum ($TH_{DOM(MIN)}$) = 0.422 × VBAT, V_{SUP} = 7.0 V to 18 V, t_{BIT} = 50 µs, D2 = maximum time for a bus recessive signal ($t_{BUS\_REC(MAX)}$)/(2 × t_{BIT})			0.581				
Duty Cycle 3 (D3)[24]	$TH_{REC(MAX)}$ = 0.778 × VBAT, $TH_{DOM(MAX)}$ = 0.616 × VBAT, VDD = 7.0 V to 18 V, t_{BIT} = 96 µs, D3 = $t_{BUS\_REC(MIN)}$/(2 × t_{BIT})	0.417						
Duty Cycle 4 (D4)[24]	$TH_{REC(MIN)}$ = 0.389 × VBAT, $TH_{DOM(MIN)}$ = 0.251 × VBAT, VDD = 7.0 V to 18 V, t_{BIT} = 96 µs, D4 = $t_{BUS\_REC(MAX)}$/(2 × t_{BIT})			0.590				
Propagation Delay of Receiver (t_{RX_PD})[24]				6				µs
Symmetry of Receiver Propagation Delay Rising Edge (t_{RX_SYM})[24]	With respect to falling edge (t_{RX_SYM} = propagation delay rising edge (t_{RX_PDR}) − propagation delay falling edge (t_{RX_PDF}))	−2		+2				µs
V_{HYS}[1]	$V_{HYS} = V_{TH\_REC} - V_{TH\_DOM}$			0.175 × VDD				V
$V_{LIN\_DOM\_DRV\_LOSUP}$[1]	VDD = 7.0 V							

Parameter	Test Conditions/Comments	T_A = −40°C to +115°C			T_A = 115°C to 125°C[1]			Unit
		Min	Typ	Max	Min	Typ	Max	
POWER CONSUMPTION								
Supply Current (I_{DD}) Processor, Normal Mode[25]	Clock Divider 0 (CD0) (peripheral clock (PCLK) = 16 MHz), 16 MHz, 1% mode, ADCs off, reference buffer off, executing code from program flash		8	17				mA
	Clock Divider 1 (CD1) (PCLK = 8 MHz), 16 MHz, 1% mode, ADCs off, reference buffer off, executing code from program flash		6					mA
	CD0 (PCLK = 16 MHz), 16 MHz, 1% mode, ADCs on, reference buffer on, executing code from program flash		9.5	18.5				mA
I_{DD} Processor Powered Down	Precision oscillator off, ADC off, external LIN master pull-up resistor present, measured with wake-up and watchdog timers clocked from low power oscillator, maximum value at 105°C, and VDD = 18 V		60	100		120		µA
	Precision oscillator off, ADC off, external LIN master pull-up resistor present, measured with wake-up and watchdog timers clocked from low power oscillator, maximum value at 125°C, and VDD = 18 V						126	µA
I_{DD} LIN			500					µA
I_{DD} Primary ADC	Gain = 4, 8, or 16		700					µA
	Gain = 32 or 64		800					µA
	Low power mode, gain = 64		350					µA
I_{DD} Auxiliary ADC (AIN5)			550					µA
I_{DD} Internal Reference (1.2 V)			150					µA
I_{DD} High Frequency Oscillator	Reduction from 1% to 3% mode		50					µA

[1] Not guaranteed by production test but by design and/or characterization data at production release.
[2] Includes internal reference temperature drift.
[3] These specifications include temperature drift.
[4] A user system calibration removes this error at a given temperature (and at a given gain for the primary ADC).
[5] Valid for PGA primary ADC gain settings of 4, 8, 16, 32, and 64.
[6] System chopping enabled.
[7] The offset error drift is included in the offset error. This typical specification is an indicator of the offset error due to temperature drift. This typical value is the mean of the temperature drift characterization data distribution.
[8] The gain drift is included in the total gain error. This typical specification is an indicator of the gain error due to the temperature drift in the ADC. This typical value is the mean of the temperature drift characterization data distribution.
[9] Voltage channel specifications include resistive attenuator input stage, unless otherwise stated.
[10] Includes internal reference temperature drift.
[11] Output noise is referred to the voltage attenuator input. For example, at an ADC data output frequency (f_{ADC}) = 1 kHz, the typical output noise at the ADC input is 7.5 µV and scaling by the attenuator (24) yields the input referred noise figures.
[12] Valid after an initial self calibration.
[13] It is possible to extend the ADC input voltage range by up to 10% by modifying the factory set value of the gain calibration register or by using system calibration. This approach can also be used to reduce the ADC input range (LSB size).
[14] Valid for a differential input of < 10 mV.
[15] The absolute value of the voltage of AIN5 and GND_SW must be 100 mV (minimum) for accurate operation of the temperature analog-to-digital converter (T_{ADC}).
[16] Measured using box method.
[17] The long-term stability specification is accelerated and noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.
[18] Based on results from high temperature operating life at 125°C for 1000 hours and electrical test performed at −40°C, +25°C and +115°C.
[19] Valid after an initial self gain calibration.
[20] Die temperature.
[21] Endurance is qualified to 10,000 cycles, as per JEDEC Standard 22, Method A117, and measured at −40°C, +25 °C, and +115°C. Typical endurance at 25°C is 100,000 cycles.
[22] Data retention lifetime equivalent at junction temperature (T_J) = 85°C, as per JEDEC Standard 22 Method A117. Data retention lifetime derates with junction temperature.
[23] Measured with LIN communication active.
[24] Not production tested but are supported by LIN compliance testing.
[25] Typical additional supply current consumed during Flash/EE memory programming is 3 mA, and typical additional supply current consumed during erase cycles is 1 mA.

ABSOLUTE MAXIMUM RATINGS

The ADuCM300 operates directly from a variable 3.6 V to 18 V voltage supply and is fully specified over the −40°C to +115°C temperature range, unless otherwise noted.

Table 2.

Parameter	Rating
AGND to DGND to VSS to IO_VSS	−0.3 V to +0.3 V
AIN4 to AGND	−22 V to +40 V
VDD to VSS	−0.3 V to +40 V
LIN to IO_VSS	−18 V to +40 V
Digital Input/Output Voltage to DGND	−0.3 V to DVDD33 + 0.3 V
ADC Inputs to AGND	−0.3 V to AVDD18 + 0.3 V
ESD (Human Body Model) Rating HBM-ADI0082 (Based on ANSI/ESD STM5.1-2007)	
All Pins Except LIN and AIN4	±2.0 kV
LIN	±6 kV
AIN4	±4 kV
IEC 61000-4-2	
LIN and AIN4	±8 kV
Storage Temperature Range	−55°C to +150°C
Junction Temperature (T_J)	
Transient	150°C
Continuous	130°C
Lead Temperature	
Soldering Reflow[1]	260°C
Lifetime[2]	
Normal Mode	480 hours at −40°C
	1600 hours at 23°C
	5200 hours at 60°C
	640 hours at 85°C
	80 hours at 105°C
Standby Mode	12,648 hours at −40°C
	60,000 hours at 25°C
	50,000 hours at 50°C

[1] JEDEC Standard J-STD-020.
[2] Using an activation energy of 0.7 eV, verified using high temperature operating life at 125°C for 1000 hours.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

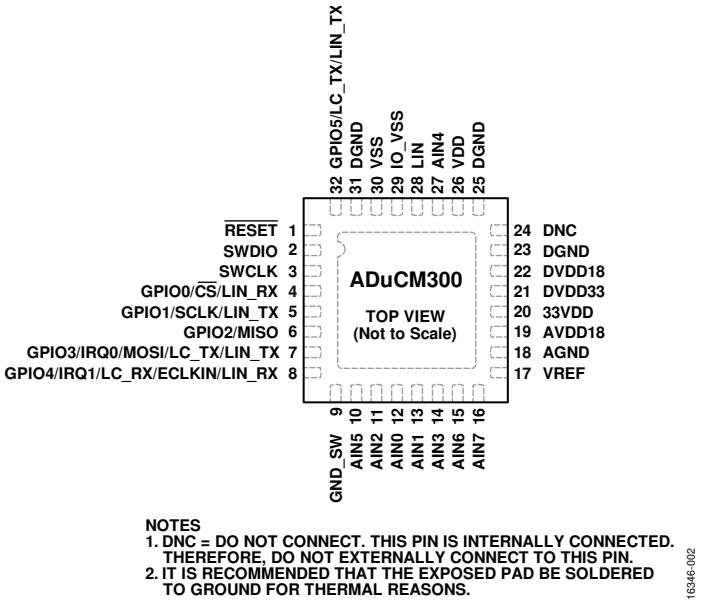

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	$\overline{\text{RESET}}$	Input	Reset Input. Active low. This pin has an internal pull-up resistor connected to 33VDD.
2	SWDIO	Input/output	Arm Cortex-M3 Debug Data Input and Output Channel. At power-on, this output pin is disabled and pulled high via an internal pull-up resistor. Leave this pin disconnected when not in use.
3	SWCLK	Input	Arm Cortex-M3 Debug Clock Input. This pin is an input only and has an internal pull-up resistor. Leave this pin disconnected when not in use.
4	GPIO0/ $\overline{\text{CS}}$/LIN_RX	Input/output	General-Purpose Input/Output 0 (GPIO0). By default, this pin is configured as an input. The pin has an internal 25 kΩ pull-up resistor connected to 33VDD. When not in use, leave this pin disconnected. Chip Select ($\overline{\text{CS}}$). When configured, this pin operates the SPI chip select input. Local Interconnect Network Receiver (LIN_RX). This pin can be configured as the receiver pin for LIN frames in external transceiver mode.
5	GPIO1/SCLK/ LIN_TX	Input/output	General-Purpose Input/Output 1 (GPIO1). By default, this pin is configured as an input. In external mode, the kernel uses this pin. See the ADuCM300 Hardware Reference Manual for more information. The pin has an internal 25 kΩ pull-up resistor connected to 33VDD. When not in use, leave this pin disconnected. Serial Clock Input (SCLK). When configured, this pin operates the SPI serial clock input. Local Interconnect Network Transmitter (LIN_TX). This pin can be configured as the transmitter pin for LIN frames in external transceiver mode.
6	GPIO2/MISO	Input/output	General-Purpose Input/Output 2 (GPIO2). By default, this pin is configured as an input. The pin has an internal 25 kΩ pull-up resistor connected to 33VDD. When not in use, leave this pin disconnected. Master Input/Slave Output (MISO). When configured, this pin also operates the SPI master input/slave output.
7	GPIO3/IRQ0/ MOSI/LC_TX/ LIN_TX	Input/output	General-Purpose Input/Output 3 (GPIO3). By default, this pin is configured as an input. In external mode, the kernel uses this pin. See the ADuCM300 Hardware Reference Manual for more information. The pin has an internal 25 kΩ pull-up resistor connected to 33VDD. When not in use, leave this pin disconnected. Interrupt Request (IRQ0). This pin can be configured as External Interrupt Request 0. Master Output/Slave Input (MOSI). This pin can be configured as an SPI master output/slave input pin. LIN Conformance Transmitter (LC_TX). This pin can be connected to the LIN physical transmitter for LIN conformance testing. Local Interconnect Network Transmitter (LIN_TX). This pin can also be connected as the transmitter pin for LIN frames in external transceiver mode.

Pin No.	Mnemonic	Type	Description
8	GPIO4/IRQ1/ LC_RX/ECLKIN/ LIN_RX	Input/output	General-Purpose Input/Output 4 (GPIO4). By default, this pin is configured as an input. In external mode, the kernel uses this pin. See the ADuCM300 Hardware Reference Manual for more information. The pin has an internal 25 kΩ pull-up resistor connected to 33VDD. When not in use, leave this pin disconnected. Interrupt Request (IRQ1). This pin can be configured as External Interrupt Request 1. LIN Conformance Receiver (LC_RX). This pin can be connected to the LIN physical receiver for LIN conformance testing. External Clock (ECLKIN). This pin can be configured as the external clock input. Local Interconnect Network Receiver (LIN_RX). This pin can be configured as the receiving pin for LIN frames in external transceiver mode.
9	GND_SW	Input	Switch to Internal Analog Ground Reference. This pin is the negative input for the external temperature channel.
10	AIN5	Input	Single-Ended Voltage Input for the Primary ADC. This pin can also interface with an external temperature sensor.
11	AIN2	Supply	Auxiliary Positive Differential Input for the Primary ADC. Connect this pin to AGND.
12	AIN0	Input	Positive Differential Input for Primary ADC.
13	AIN1	Input	Negative Differential Input for Primary ADC.
14	AIN3	Supply	Auxiliary Negative Differential Input for the Primary ADC. Connect this pin to AGND.
15	AIN6	Supply	Auxiliary Positive Differential Input for the Auxiliary ADC. Connect this pin to AGND.
16	AIN7	Supply	Auxiliary Negative Differential Input for the Auxiliary ADC. Connect this pin to AGND.
17	VREF	Supply	Voltage Reference Pin. Connect this pin via a 0.47 µF capacitor to ground. This pin can also be used to input an external voltage reference. This pin cannot be used to supply an external circuit.
18	AGND	Supply	Ground Reference for On-Chip Precision Analog Circuits.
19	AVDD18	Supply	Supply from Analog LDO. Do not connect this pin to an external circuit. Using the 1.8 V or 3.3 V supply to power an external circuit can have POR, electromagnetic compatibility (EMC), and self heating implications. Device evaluation and testing completed without an external load attached.
20	33VDD	Supply	3.3 V Supply Input. Connect to Pin 21 (DVDD33). Do not connect this pin to an external circuit. Using the 1.8 V or 3.3 V supply to power an external circuit can have POR, EMC, and self heating implications. Device evaluation and testing completed without an external load attached.
21	DVDD33	Supply	3.3 V Regulated Supply Input. Connect to Pin 20 (33VDD). Do not connect this pin to an external circuit. Using the 1.8 V or 3.3 V supply to power an external circuit can have POR, EMC, and self heating implications. Device evaluation and testing completed without an external load attached.
22	DVDD18	Supply	1.8 V Supply. Do not connect this pin to an external circuit. Using the 1.8 V or 3.3 V supply to power an external circuit can have POR, EMC, and self heating implications. Device evaluation and testing completed without an external load attached.
23, 25, 31	DGND	Supply	Ground Reference for On-Chip Digital Circuits.
24	DNC		Do Not Connect. This pin is internally connected. Therefore, do not externally connect to this pin.
26	VDD	Supply	Battery Power Supply for On-Chip Regulator.
27	AIN4	Supply	12 V Supply Monitor.
28	LIN	Input/output	LIN Physical Interface Input/Output.
29	IO_VSS	Supply	Ground Reference for the LIN Pin.
30	VSS	Supply	Ground Reference for the Internal Voltage Regulators.
32	GPIO5/ LC_TX/LIN_TX	Input/output	General-Purpose Input/Output 5 (GPIO5). By default, this pin is configured as an input. In external mode, the kernel uses this pin. See the ADuCM300 Hardware Reference Manual for more information. The pin has an internal 25 kΩ pull-up resistor connected to 33VDD. When not in use, leave this pin disconnected. LIN Conformance Transmitter (LC_TX). This pin can be connected to the LIN physical transmitter for LIN conformance testing. Local Interconnect Network Transmitter (LIN_TX). This pin can be configured as the transmitter pin for LIN frames in external transceiver mode.
	EPAD		Exposed Pad. It is recommended that the exposed pad be soldered to ground for thermal reasons.

TERMINOLOGY

Conversion Rate
The conversion rate specifies the rate at which an output result is available from the ADC after the ADC has settled.

The Σ-Δ conversion techniques used on this device means that although the ADC front-end signal is oversampled at a relatively high sample rate, a subsequent digital filter is used to decimate the output, giving a valid 20-bit data conversion result at output rates from 4 Hz to 8 kHz.

Note that when the software switches from one input to another (on the same ADC), the digital filter must first be cleared and then allowed to average a new result. Depending on the configuration of the ADC and the type of filter, this averaging can require multiple conversion cycles.

Integral Nonlinearity
INL is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (0.5 LSB below the first code transition) and full scale (0.5 LSB above the last code transition, 111…110 to 111…111). The error is expressed as ppm of FSR.

Positive INL is defined as the deviation from a straight line through 0.5 LSB above midscale code transition to 0.5 LSB above the last code transition.

Negative INL is defined as the deviation from a straight line from 0.5 LSB below the first code transition to 0.5 LSB above the midscale code transition.

No Missing Codes
No missing codes is a measure of the differential nonlinearity of the ADC. The error is expressed in bits and specifies the number of codes (ADC results) as 2^N bits, where N = no missing codes, guaranteed to occur through the full ADC input range.

Offset Error
Offset error is the deviation of the first code transition ADC input voltage from the ideal first code transition.

Offset Error Drift
Offset error drift is the variation in absolute offset error with respect to temperature. This error is expressed as LSB/°C or nV/°C.

Gain Error
Gain error is a measure of the span error of the ADC. It is a measure of the difference between the measured and the ideal span between any two points in the transfer function.

Output Noise
The output noise is specified as the standard deviation (or 1 × Σ) of ADC output codes distribution collected when the ADC input voltage is at a dc voltage. The output noise is expressed as μV rms or nV rms. The output, or rms noise, is used to calculate the effective resolution of the ADC as defined by the following equation:

$$\textit{Effective Resolution} = \log_2(\textit{Full-Scale Range/RMS Noise})$$

The peak-to-peak noise is defined as the deviation of codes that fall within 6.6 × Σ of the distribution of ADC output codes collected when the ADC input voltage is at dc. The peak-to-peak noise is therefore calculated as 6.6 × the rms noise.

The peak-to-peak noise can be used to calculate the ADC (noise free, code) resolution for which there is no code flicker within a 6.6 × Σ limit as defined by the following equation:

$$\textit{Noise Free Code Resolution} = \log_2(\textit{Full-Scale Range/Peak-to-Peak Noise})$$

APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting design and layout of the ADuCM300 on a printed circuit board (PCB), it is recommended that the user become familiar with the following guidelines that describe any special circuit considerations and layout requirements needed.

POWER AND GROUND RECOMMENDATIONS

Connect capacitors to the ADuCM300 as close to the pins of the device as possible, with minimal trace length.

Capacitors connected to the 33VDD pin, AVDD18 pin, and DVDD18 pin must have a low equivalent series resistance (ESR) rating.

All components must be rated according to the temperature range expected by the application.

EXPOSED PAD THERMAL RECOMMENDATIONS

Solder the exposed pad on the underside of the ADuCM300 to ground to achieve the best electrical and thermal performance. Connect an exposed continuous copper plane on the PCB to the ADuCM300 exposed pad. To achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB, ensure that the copper plane has several vias. These vias must be solder filled or plugged.

GENERAL RECOMMENDATIONS

It is highly recommended to use the component values specified in Figure 3. The component values shown in Figure 3 were chosen based on the characterization tests and evaluated for optimum performance of the ADuCM300.

Configure the GPIOs as inputs with pull-up resistors enabled to obtain the lowest possible current consumption in hibernate mode.

Set the Arm Cortex-M3 core clock speed to the minimum required speed to meet the application requirements.

RECOMMENDED EXTERNAL COMPONENTS SCHEMATIC

Figure 3 shows the recommended external components schematic for proper operation of the ADuCM300 using an external negative temperature coefficient (NTC) circuit as an example of a single-ended voltage input to the AIN5 pin.

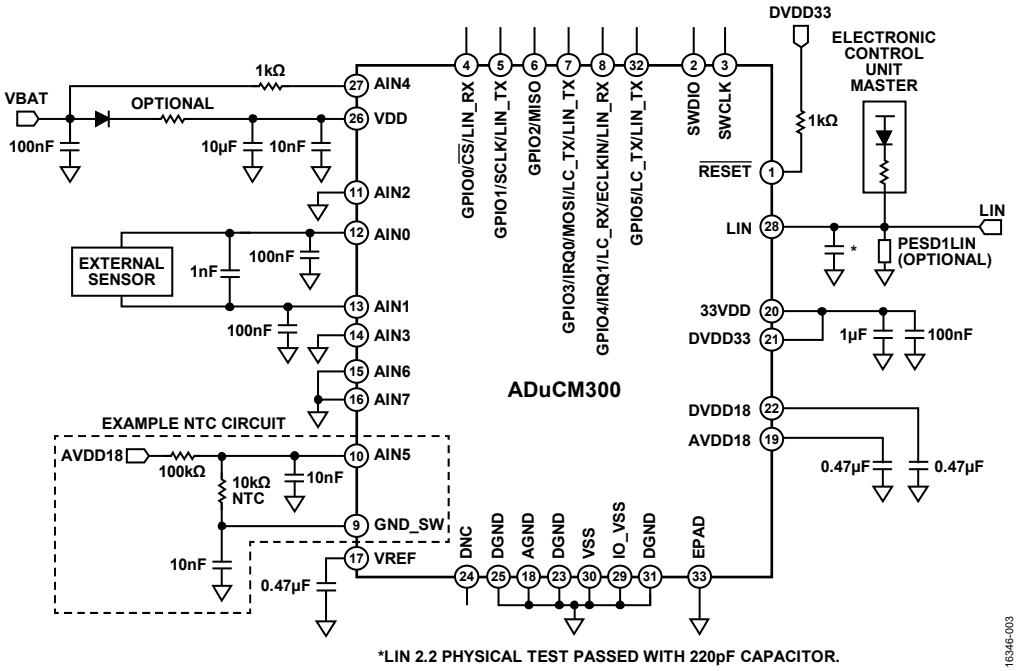

Figure 3. Recommended External Components Schematic When Using an External NTC Sensor

OUTLINE DIMENSIONS

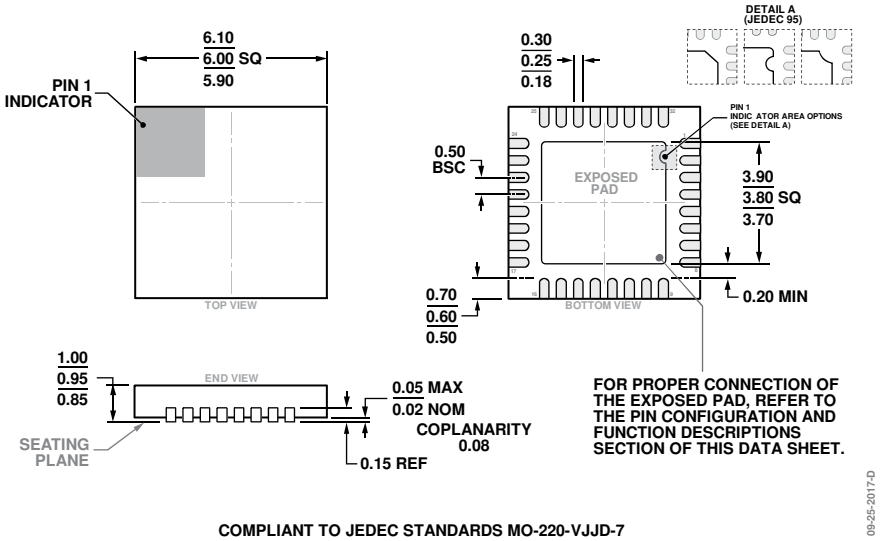

Figure 4. 32-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.95 mm Package Height
(CP-32-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Program Flash/ Data Flash/SRAM	Package Description	Package Option
ADuCM300WBCPZ	−40°C to +115°C	128 kB/4 kB/6 kB	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-15
EVAL-ADuCM300QSPZ			Socketed Evaluation Board with Switches and LEDs	

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADuCM300W model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that this automotive model may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade product shown is available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for this model.