CY29972

3.3 V, 125-MHz Multi-Output Zero Delay Buffer

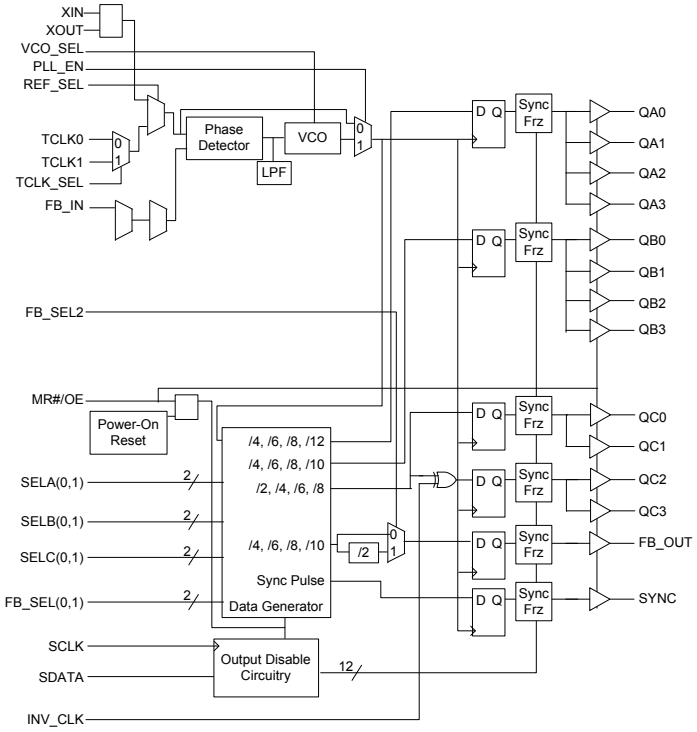
Features

- Output frequency up to 125 MHz
- 12 Clock outputs: frequency configurable
- 350 ps max. output-to-output skew
- Configurable output disable
- Two reference clock inputs for dynamic toggling
- Oscillator or crystal reference input
- Spread-spectrum-compatible
- Glitch-free output clocks transitioning
- 3.3 V power supply
- Pin-compatible with MPC972
- Industrial temperature range: –40 °C to +85 °C
- 52-pin thin quad flat package (TQFP) package

Table 1. Frequency Table [1]

VC0_SEL	FB_SEL2	FB_SEL1	FB_SEL0	F_{VC0}
0	0	0	0	8x
0	0	0	1	12x
0	0	1	0	16x
0	0	1	1	20x
0	1	0	0	16x
0	1	0	1	24x
0	1	1	0	32x
0	1	1	1	40x
1	0	0	0	4x
1	0	0	1	6x
1	0	1	0	8x
1	0	1	1	10x
1	1	0	0	8x
1	1	0	1	12x
1	1	1	0	16x
1	1	1	1	20x

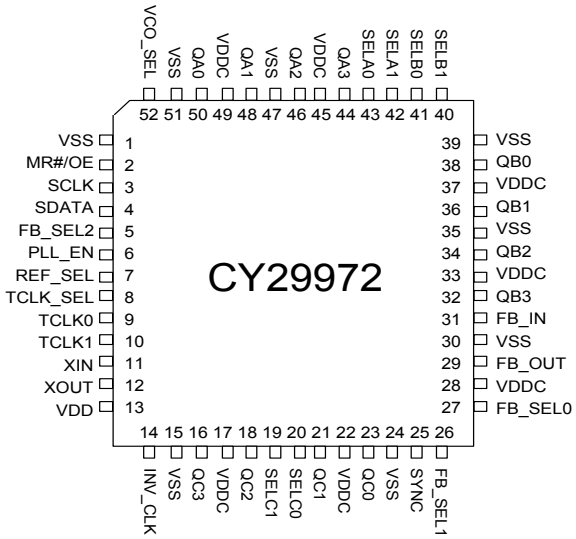
Block Diagram



Note
1. x = the reference input frequency, 200 MHz < F_{VCO} < 480 MHz.

Contents

Pin Configuration



Pin Description

Pin [2]	Name	PWR	I/O	Type	Description
11	X_{IN}	–	I	–	**Oscillator input**. Connect to a crystal.
12	X_{OUT}	–	O	–	**Oscillator output**. Connect to a crystal.
9	T_{CLK0}	–	I	PU	**External reference/test clock input**.
10	T_{CLK1}	–	I	PU	**External reference/test clock input**.
44, 46, 48, 50	QA(3:0)	V_{DDC}	O	–	**Clock outputs**. See Table 2 on page 5 for frequency selections.
32, 34, 36, 38	QB(3:0)	V_{DDC}	O	–	**Clock outputs**. See Table 2 on page 5 for frequency selections.
16, 18, 21, 23	QC(3:0)	V_{DDC}	O	–	**Clock outputs**. See Table 2 on page 5 for frequency selections.
29	FB_OUT	V_{DDC}	O	–	**Feedback clock output**. Connect to FB_IN for normal operation. The divider ratio for this output is set by FB_SEL(0:2). See Table 1 on page 1. A bypass delay capacitor at this output will control Input Reference/ Output Banks phase relationships.
25	SYNC	V_{DDC}	O	–	**Synchronous pulse output**. This output is used for system synchronization. The rising edge of the output pulse is in sync with both the rising edges of QA(0:3) and QC(0:3) output clocks regardless of the divider ratios selected.
42, 43	SELA(1,0)	–	I	PU	**Frequency select inputs**. These inputs select the divider ratio at QA(0:3) outputs. See Table 2 on page 5.
40, 41	SELB(1,0)	–	I	PU	**Frequency select inputs**. These inputs select the divider ratio at QB(0:3) outputs. See Table 2 on page 5.
19, 20	SELC(1,0)	–	I	PU	**Frequency select inputs**. These inputs select the divider ratio at QC(0:3) outputs. See Table 2 on page 5.
5, 26, 27	FB_SEL(2:0)	–	I	PU	**Feedback select inputs**. These inputs select the divide ratio at FB_OUT output. See Table 1 on page 1.
52	VCO_SEL	–	I	PU	**VCO divider select input**. When set LOW, the VCO output is divided by 2. When set HIGH, the divider is bypassed. See Table 1 on page 1.
31	FB_IN	–	I	PU	**Feedback clock input**. Connect to FB_OUT for accessing the PLL.
6	PLL_EN	–	I	PU	**PLL enable input**. When asserted HIGH, PLL is enabled; when LOW, PLL is bypassed.
7	REF_SEL	–	I	PU	**Reference select input**. When HIGH, the crystal oscillator is selected; when LOW, TCLK (0,1) is the reference clock.
8	TCLK_SEL	–	I	PU	**TCLK select input**. When LOW, TCLK0 is selected and when HIGH TCLK1 is selected.
2	MR#/OE	–	I	PU	**Master reset/output enable input**. When asserted LOW, resets all of the internal flip-flops and also disables all of the outputs. When pulled high, releases the internal flip-flops from reset and enables all of the outputs.
14	INV_CLK	–	I	PU	**Inverted clock input**. When set HIGH, QC(2,3) outputs are inverted. When set LOW, the inverter is bypassed.
3	S_{CLK}	–	I	PU	**Serial clock input**. Clocks data at SDATA into the internal register.
4	S_{DATA}	–	I	PU	**Serial data input**. Input data is clocked to the internal register to enable/disable individual outputs. This provides flexibility in power management.
17, 22, 28, 33,37, 45, 49	V_{DDC}	–	–	–	3.3 V power supply for output clock buffers.
13	V_{DD}	–	–	–	3.3 V power supply for PLL.
1, 15, 24, 30, 35, 39, 47, 51	V_{SS}	–	–	–	Common ground.

Note
2. A bypass capacitor (0.1 mF) should be placed as close as possible to each positive power (< 0.2”). If these bypass capacitors are not close to the pins, their high-frequency filtering characteristics will be cancelled by the lead inductance of the traces.

Description

The CY29972 has an integrated PLL that provides low skew and low jitter clock outputs for high-performance microprocessors. Three independent banks of four outputs and an independent PLL feedback output (FB_OUT) provide exceptional flexibility for possible output configurations. The PLL is ensured stable operation given that the V_{CO} is configured to run between 200 MHz and 480 MHz. This allows a wide range of output frequencies up to 125 MHz.

The phase detector compares the input reference clock to the external feedback input. For normal operation, the external feedback input (FB_IN) is connected to the feedback output (FB_OUT). The internal V_{CO} is running at multiples of the input reference clock set by FB_SEL(0:2) and VCO_SEL select inputs (refer to Frequency Table). The V_{CO} frequency is then divided to provide the required output frequencies. These dividers are set by SELA(0,1), SELB(0,1), SELC(0,1) select inputs (see the following Table). For situations were the V_{CO} needs to run at relatively low frequencies and hence might not be stable, assert VCO_SEL low to divide the VCO frequency by 2. This maintains the desired output relationships but provides an enhanced PLL lock range.

The CY29972 is also capable of providing inverted output clocks. When INV_CLK is asserted HIGH, QC2 and QC3 output clocks are inverted. These clocks could be used as feedback outputs to the CY29972 or a second PLL device to generate early or late clocks for a specific design. This inversion does not affect the output to output skew.

Glitch-Free Output Frequency Transitions

Customarily, when output buffers have their internal counters changed “on the fly,” their output clock periods will:

1. contain short or “runt” clock periods. These are clock cycles in which the cycle(s) are shorter in period than either the old or new frequencies to which the cycles are being transitioned.
2. contain stretched clock periods. These are clock cycles in which the cycle(s) are longer in period than either the old or new frequencies to which the cycles are being transitioned.

This device specifically includes logic to guarantee that runt and stretched clock pulses do not occur if the device logic levels of any or all of the following pins changed “on the fly” while it is operating: SELA, SELB, SELC, and VCO_SEL.

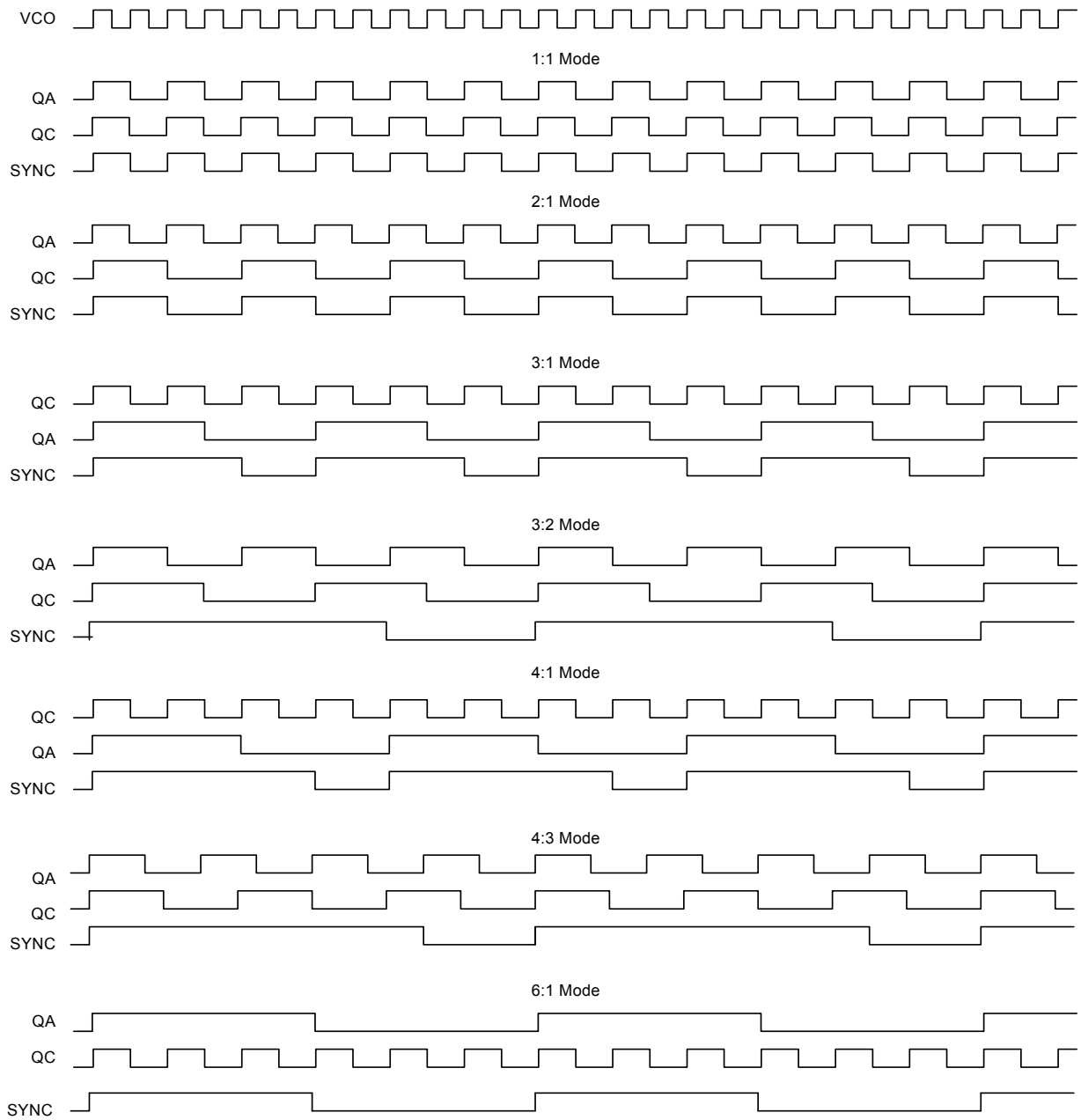
Table 2. Frequency Selection Table

VCO_SEL	SELA1	SELA0	QA	SELB1	SELB0	QB	SELC1	SELC0	QC
0	0	0	VCO/8	0	0	VCO/8	0	0	VCO/4
0	0	1	VCO/12	0	1	VCO/12	0	1	VCO/8
0	1	0	VCO/16	1	0	VCO/16	1	0	VCO/12
0	1	1	VCO/24	1	1	VCO/20	1	1	VCO/16
1	0	0	VCO/4	0	0	VCO/4	0	0	VCO/2
1	0	1	VCO/6	0	1	VCO/6	0	1	VCO/4
1	1	0	VCO/8	1	0	VCO/8	1	0	VCO/6
1	1	1	VCO/12	1	1	VCO/10	1	1	VCO/8

SYNC Output

In situations where output frequency relationships are not integer multiples of each other, the SYNC output provides a signal for system synchronization. The CY29972 monitors the relationship between the QA and QC output clocks. It provides a LOW-going pulse, one period in duration, one period prior to the coincident rising edges of the QA and QC outputs. The duration and placement of the pulse depend on the higher of the QA and QC output frequencies. The following timing diagram illustrates various waveforms for the SYNC output. Note that the SYNC output is defined for all possible combinations of QA and QC outputs, even though under some relationships the lower frequency clock could be used as a synchronizing signal.

Figure 1. Timing Diagram

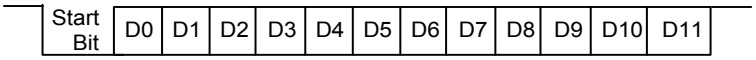


Power Management

The individual output enable/freeze control of the CY29972 allows the user to implement unique power management schemes into the design. The outputs are stopped in the logic '0' state when the freeze control bits are activated. The serial input register contains one programmable freeze enable bit for 12 of the 14 output clocks. The QC0 and FB_OUT outputs can not be frozen with the serial port, this avoids any potential lock up situation should an error occur in the loading of the serial data.

An output is frozen when a logic '0' is programmed and enabled when a logic '1' is written. The enabling and freezing of individual outputs is done in such a manner as to eliminate the possibility of partial "runt" clocks.

The serial input register is programmed through the SDATA input by writing a logic '0' start bit followed by 12 NRZ freeze enable bits. The period of each SDATA bit equals the period of the free running SCLK signal. The SDATA is sampled on the rising edge of SCLK.



D0-D3 are the control bits for QA0-QA3, respectively
D4-D7 are the control bits for QB0-QB3, respectively
D8-D10 are the control bits for QC1-QC3, respectively
D11 is the control bit for SYNC

Table 3. Suggested Oscillator Crystal Parameters

Parameter	Characteristic	Min	Typ	Max	Unit	Conditions
T_C	Frequency tolerance	–	–	±100	ppm	Note 3
T_S	Frequency temperature stability	–	–	±100	ppm	(T_A –10 to +60 °C) [3]
T_A	Aging	–	–	5	ppm/ Yr	(first 3 years at 25 °C) [3]
C_L	Load capacitance	–	20	–	pF	The crystal's rated load [3]
R_{ESR}	Effective series resistance (ESR)	–	40	80	ohms	Note 4

Absolute Maximum Ratings

Exceeding maximum ratings [5] may shorten the useful life of the device. User guidelines are not tested.

Maximum input voltage relative to V_{SS} ..... V_{SS} – 0.3 V

Maximum input voltage relative to V_{DD} ..... V_{DD} + 0.3 V

Storage temperature ..... –65 °C to +150 °C

Operating temperature ..... –40 °C to +85 °C

Maximum ESD protection ..... 2 kV

Maximum power supply ..... 5.5 V

Maximum input current ..... ±20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range:

$V_{SS} < (V_{IN}$ or $V_{OUT}) < V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

Notes
3. For best performance and accurate frequencies from this device, It is recommended but not mandatory that the chosen crystal meet or exceed these specifications.
4. Larger values may cause this device to exhibit oscillator start-up problems.
5. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.

DC Parameters

V_{DD} = 2.9 V to 3.6 V, V_{DDC} = 3.3 V ± 10%, T_A = –40 °C to +85 °C

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low voltage		V_{SS}	–	0.8	V
V_{IH}	Input High voltage		2.0	–	V_{DD}	V
I_{IL}	Input Low current [6]		–	–	–120	µA
I_{IH}	Input High current		–	–	10	µA
V_{OL}	Output Low voltage [7]	I_{OL} = 20 mA	–	–	0.5	V
V_{OH}	Output High voltage [7]	I_{OH} = –20 mA	2.4	–	–	V
I_{DDQ}	Quiescent supply current		–	10	15	mA
I_{DDA}	PLL supply current	V_{DD} only	–	15	20	mA
I_{DD}	Dynamic supply current	QA and QB at 60 MHz, QC at 120 MHz, C_L = 30 pF	–	225	–	mA
		QA and QB at 25 MHz, QC at 50 MHz, C_L = 30 pF	–	125	–	
C_{IN}	Input pin capacitance		–	4	–	pF

AC Parameters

V_{DD} = 2.9 V to 3.6 V, V_{DDC} = 3.3 V ±10%, T_A = –40 °C to +85 °C

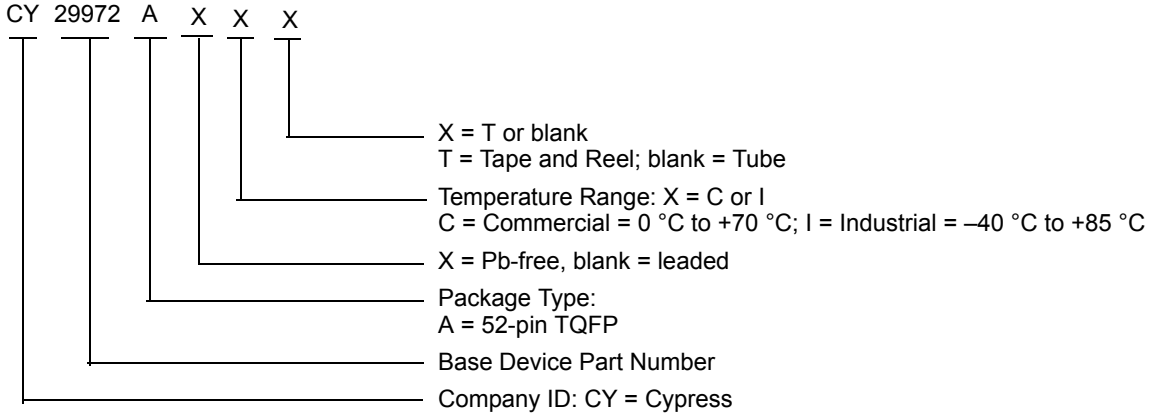
Parameter [8]	Description		Conditions	Min	Typ	Max	Unit
T_R / T_F	T_{CLK} input rise/fall			–	–	3.0	ns
F_{REF}	Reference input frequency			Note 9	–	Note 9	MHz
F_{XTAL}	Crystal Oscillator Frequency		see Table 3 on page 7	10	–	25	MHz
F_{REFDC}	Reference input duty cycle			25	–	75	%
F_{VCO}	PLL VCO lock range			200	–	480	MHz
t_{LOCK}	Maximum PLL lock time			–	–	10	ms
t_R / t_F	Output clocks rise / fall time [10]		0.8 V to 2.0 V	0.15	–	1.2	ns
F_{OUT}	Maximum Output Frequency		Q (³2)	–	–	125	MHz
			Q (³4)	–	–	120	
			Q (³6)	–	–	80	
			Q (³8)	–	–	60	
F_{OUTDC}	Output duty cycle [10]			$T_{CYCLE}/2 – 750$	–	$T_{CYCLE}/2 + 750$	ps
t_{PZL}, t_{PZH}	Output enable time [10] (all outputs)			2	–	10	ns
t_{PLZ}, t_{PHZ}	Output disable time [10] (all outputs)			2	–	8	ns
T_{CCJ}	Cycle to cycle jitter [10] (peak to peak)			–	± 100	–	ps
T_{SKEW}	Any output to any output skew [10, 11]			–	250	350	ps
T_{PD}	Propagation delay [11, 12]	T_{CLK0}	QFB = (³8)	–270	130	530	ps
		T_{CLK1}		–330	70	470	

Notes
6. Inputs have pull-up/pull-down resistors that effect input current.
7. Driving series or parallel terminated 50 Ω (or 50 Ω to $V_{DD}/2$) transmission lines.
8. Parameters are guaranteed by design and characterization. Not 100% tested in production.
9. Maximum and minimum input reference is limited by VC0 lock range.
10. Outputs loaded with 30 pF each.
11. 50Ω transmission line terminated into $V_{DD/2}$.
12. Tpd is specified for a 50-MHz input reference. Tpd does not include jitter.

Ordering Information

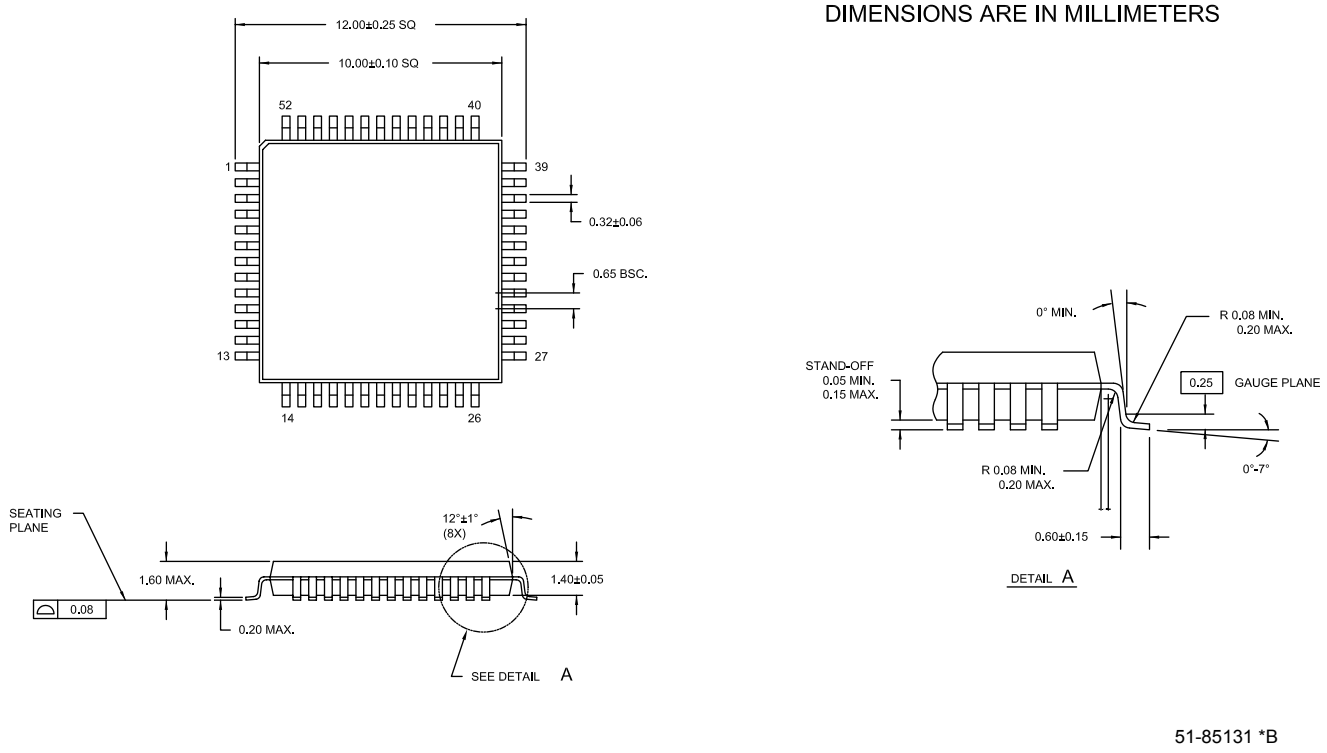
Part Number	Package Type	Production Flow
Pb-free		
CY29972AXI	52-pin TQFP	Industrial, –40 °C to +85 °C
CY29972AXIT	52-pin TQFP - Tape and Reel	Industrial, –40 °C to +85 °C

Ordering Code Definitions



Package Diagram

Figure 2. 52-pin TQFP (10 × 10 × 1.4 mm) A52SA Package Outline, 51-85131



Acronyms

Acronym	Description
I/O	input/output
PLL	phase locked loop
TQFP	thin quad flat pack

Document Conventions

Units of Measure

Symbol	Units of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
ns	nanosecond
pF	picofarad
ps	picosecond
V	volt

Document History Page

Document Title: CY29972, 3.3 V, 125-MHz Multi-Output Zero Delay Buffer Document Number: 38-07290				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111101	02/07/02	BRK	New data sheet
*A	122882	12/22/02	RBI	Added power up requirements to Maximum Ratings
*B	387764	See ECN	RGL	Changed the package drawing and dimension to Cypress Standard Added Pb-free devices
*C	404340	See ECN	RGL	Minor Change: corrected the package diagram
*D	3270575	06/03/2011	BASH	Updated as per template Updated package diagram 51-85131. Added Acronyms and Units of Measure Table
*E	3402187	10/11/2011	BASH	Updated Ordering Information (Removed prune part numbers CY29972AI and CY29972AIT). Updated Package Diagram.

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