

Analog Peripherals

- **10-Bit ADC**
 - Up to 500 ksps
 - Built-in analog multiplexer with single-ended and differential mode
 - VREF from external pin, internal reference, or V_{DD}
 - Built-in temperature sensor
 - External conversion start input option
- **Two comparators**
- **Internal voltage reference**
- **Brown-out detector and POR Circuitry**

USB Function Controller

- USB specification 2.0 compliant
- Full speed (12 Mbps) or low speed (1.5 Mbps) operation
- Integrated clock recovery; no external crystal required for full speed or low speed
- Supports eight flexible endpoints
- 1 kB USB buffer memory
- Integrated transceiver; no external resistors required

On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (No emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

Voltage Supply Input: 2.7 to 5.25 V

- Voltages from 2.7 to 5.25 V supported using On-Chip Voltage Regulators

High Speed 8051 μ C Core

- Pipelined instruction architecture; executes 70% of Instructions in 1 or 2 system clocks
- Up to 48 MIPS operation
- Expanded interrupt handler

Memory

- 4352 RAM
- 64 kB Flash; In-system programmable in 512-byte sectors

Digital Peripherals

- 40 Port I/O; All 5 V tolerant with high sink current
- Hardware enhanced SPI™, two I²C/SMBus™, and two enhanced UART serial ports
- Six general purpose 16-bit counter/timers
- 16-bit programmable counter array (PCA) with five capture/compare modules
- External Memory Interface (EMIF)

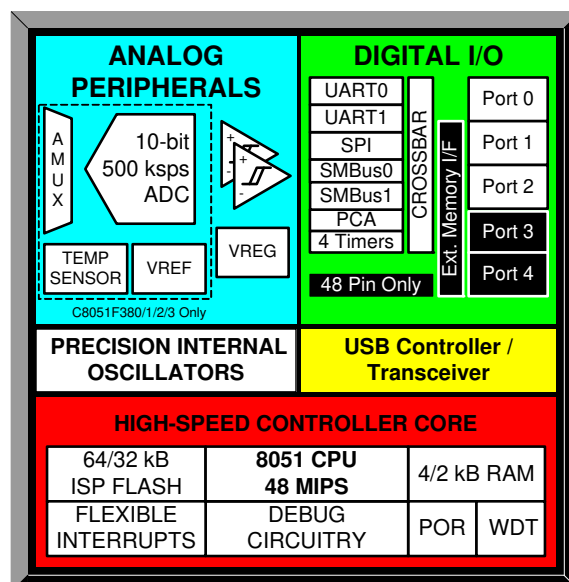
Clock Sources

- Internal Oscillator: $\pm 0.25\%$ accuracy with clock recovery enabled. Supports all USB and UART modes
- External Oscillator: Crystal, RC, C, or clock (1 or 2 Pin modes)
- Low Frequency (80 kHz) Internal Oscillator
- Can switch between clock sources on-the-fly

Temperature Range: -40 to +85 °C

Full Technical Data Sheet

- C8051F380/1/2/3/4/5/6/7



C8051F380-GDI

1. Ordering Information

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory (kB)*	RAM (Bytes)	USB with 1k Endpoint RAM	SMBus/I ² C	UARTs	Enhanced SPI	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	10-bit 500 kbps ADC	External Memory Interface (EMIP)	Internal Voltage Reference	Temperature Sensor	Analog Comparators	Package
C8051F380-GDI	48	64	4352	✓	2	2	✓	6	✓	40	✓	✓	✓	✓	2	Tested Die in Wafer Form
*Note: 1024 bytes reserved for factory use																

2. Pin Definitions

Table 2.1 lists the pin definitions for the C8051F380-GDI. For a full description of the operation of each pin, refer to the C8051F380/1/2/3/4/5/6/7 data sheet.

Table 2.1. Pin Definitions for the C8051F380-GDI

Name	Physical Pad Number	Type	Description
V _{IO}	49	Power In	2.7–3.6 V Power Supply Voltage Input.
V _{DD}	50	Power Out	3.3 V Voltage Regulator Output (when 5 V regulator is used; otherwise it is a 2.7 to 3.6 V input).
GND	7		Ground.
RST/ C2CK	12	D I/O D I/O	Device Reset. Open-drain output of internal POR or V _{DD} monitor. An external source can initiate a system reset by driving this pin low for at least 15 μs. Clock signal for the C2 Debug Interface.
C2D	13	D I/O	Bi-directional data signal for the C2 Debug Interface.
REGIN	51	Power In	5 V Regulator Input. This pin is the input to the on-chip voltage regulator.
VBUS	11	D In	VBUS Sense Input. This pin should be connected to the VBUS signal of a USB network. A 5 V signal on this pin indicates a USB network connection.
D+	8	D I/O	USB D+.
D-	9	D I/O	USB D-.
P0.0	6	D I/O or A In	Port 0.0.
P0.1	5	D I/O or A In	Port 0.1.
P0.2	4	D I/O or A In	Port 0.2.
P0.3	3	D I/O or A In	Port 0.3.
P0.4	2	D I/O or A In	Port 0.4.
P0.5	1	D I/O or A In	Port 0.5.
P0.6	48	D I/O or A In	Port 0.6.

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Table 2.1. Pin Definitions for the C8051F380-GDI (Continued)

Name	Physical Pad Number	Type	Description
P0.7	47	D I/O or A In	Port 0.7.
P1.0	46	D I/O or A In	Port 1.0.
P1.1	45	D I/O or A In	Port 1.1.
P1.2	44	D I/O or A In	Port 1.2.
P1.3	43	D I/O or A In	Port 1.3.
P1.4	42	D I/O or A In	Port 1.4.
P1.5	41	D I/O or A In	Port 1.5.
P1.6	40	D I/O or A In	Port 1.6.
P1.7	39	D I/O or A In	Port 1.7.
P2.0	38	D I/O or A In	Port 2.0.
P2.1	37	D I/O or A In	Port 2.1.
P2.2	36	D I/O or A In	Port 2.2.
P2.3	35	D I/O or A In	Port 2.3.
P2.4	34	D I/O or A In	Port 2.4.
P2.5	33	D I/O or A In	Port 2.5.
P2.6	32	D I/O or A In	Port 2.6.
P2.7	31	D I/O or A In	Port 2.7.
P3.0	30	D I/O or A In	Port 3.0.

Table 2.1. Pin Definitions for the C8051F380-GDI (Continued)

Name	Physical Pad Number	Type	Description
P3.1	29	D I/O or A In	Port 3.1.
P3.2	28	D I/O or A In	Port 3.2.
P3.3	27	D I/O or A In	Port 3.3.
P3.4	26	D I/O or A In	Port 3.4.
P3.5	25	D I/O or A In	Port 3.5.
P3.6	24	D I/O or A In	Port 3.6.
P3.7	22	D I/O or A In	Port 3.7.
P4.0	21	D I/O or A In	Port 4.0.
P4.1	20	D I/O or A In	Port 4.1.
P4.2	19	D I/O or A In	Port 4.2.
P4.3	18	D I/O or A In	Port 4.3.
P4.4	17	D I/O or A In	Port 4.4.
P4.5	16	D I/O or A In	Port 4.5.
P4.6	15	D I/O or A In	Port 4.6.
P4.7	14	D I/O or A In	Port 4.7.

C8051F380-GDI

3. Bonding Instructions

Table 3.1. Bond Pad Coordinates (Relative to Center of Die)

Physical Pad Number	Example Package Pin Number (QFP-48)	Package Pin Name	Physical Pad X (μm)	Physical Pad Y (μm)
1	1	P0.5	-978	-1021
2	2	P0.4	-836	-1021
3	3	P0.3	-659	-1021
4	4	P0.2	-516	-1021
5	5	P0.1	-359	-1021
6	6	P0.0	-217	-1021
7	7	GND	-91	-1021
8	8	D+	124	-1020
9	9	D-	434	-1020
10	Reserved*	—	666	-1021
11	12	VBUS	947	-1021
12	13	RST/C2CK	1181	-818
13	14	C2D	1181	-676
14	15	P4.7	1181	-519
15	16	P4.6	1181	-377
16	17	P4.5	1181	-199
17	18	P4.4	1181	-57
18	19	P4.3	1181	100
19	20	P4.2	1181	242
20	21	P4.1	1181	419
21	22	P4.0	1181	561
22	23	P3.7	1181	718
23	Reserved*	—	1177	850
24	24	P3.6	966	1020
25	25	P3.5	809	1020
26	26	P3.4	667	1020

***Note:** Pins marked “Reserved” should not be connected.

Table 3.1. Bond Pad Coordinates (Relative to Center of Die) (Continued)

Physical Pad Number	Example Package Pin Number (QFP-48)	Package Pin Name	Physical Pad X (μm)	Physical Pad Y (μm)
27	27	P3.3	510	1020
28	28	P3.2	368	1020
29	29	P3.1	211	1020
30	30	P3.0	69	1020
31	31	P2.7	-88	1020
32	32	P2.6	-231	1020
33	33	P2.5	-387	1020
34	34	P2.4	-530	1020
35	35	P2.3	-686	1020
36	36	P2.2	-829	1020
37	37	P2.1	-985	1020
38	38	P2.0	-1181	822
39	39	P1.7	-1181	666
40	40	P1.6	-1181	523
41	41	P1.5	-1181	367
42	42	P1.4	-1181	224
43	43	P1.3	-1181	67
44	44	P1.2	-1181	-75
45	45	P1.1	-1181	-232
46	46	P1.0	-1181	-374
47	47	P0.7	-1181	-531
48	48	P0.6	-1181	-818
49	10	VDD	625	-802
50	10	VDD	700	-802
51	11	REGIN	775	-802
52	Reserved*	—	280	-634
53	Reserved*	—	490	-634
54	Reserved*	—	917	-634

***Note:** Pins marked “Reserved” should not be connected.

C8051F380-GDI

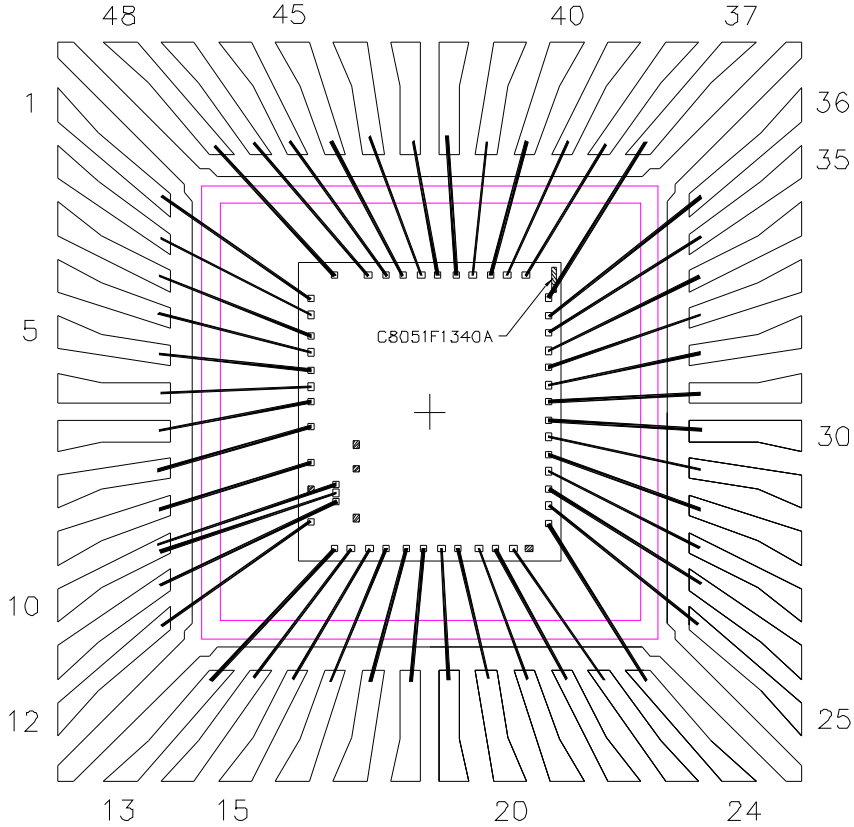


Figure 3.1. Die Bonding (QFP-48)

Table 3.2. Wafer and Die Information

Wafer ID	C8051F1340A
Wafer Dimensions	8 in
Die Dimensions	2.26 mm x 2.58 mm
Wafer Thickness	12 mil ±1 mil
Wafer Identification	Notch
Scribe Line Width	80 µm
Die Per Wafer*	Contact Sales for info
Passivation	Standard
Wafer Packaging Detail	Wafer Jar
Bond Pad Dimensions	60 µm x 60 µm
Maximum Processing Temperature	250 °C
Electronic Die Map Format	.txt
Bond Pad Pitch Minimum	75 mil
*Note: This is the Expected Known Good Die yielded per wafer and represents the batch order quantity (one wafer).	

C8051F380-GDI

4. Wafer Storage Guidelines

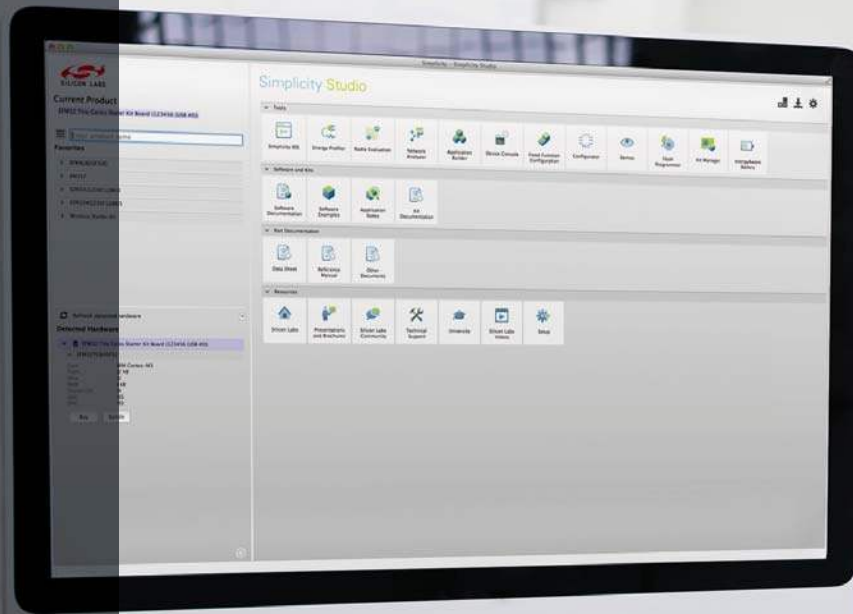
It is necessary to conform to appropriate wafer storage practices to avoid product degradation or contamination.

- Wafers may be stored for up to 18 months in the original packaging supplied by Silicon Labs.
- Wafers must be stored at a temperature of 18–24 °C.
- Wafers must be stored in a humidity-controlled environment with a relative humidity of <30%.
- Wafers should be stored in a clean, dry, inert atmosphere (e.g. nitrogen or clean, dry air).

DOCUMENT CHANGE LIST

Revision 1.0 to Revision 1.1

- Changed Wafer Packaging Detail to “Wafer Jar” in Table 3.2 on page 9.



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