National Semiconductor

93L415A 1024 x 1-Bit Static Random Access Memory

General Description

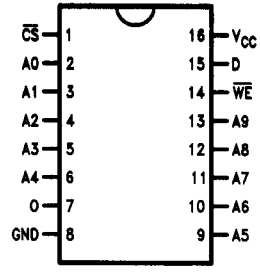
The 93L415A is a 1024-bit read write Random Access Memory (RAM), organized 1024 words by one bit. It is designed for high speed cache, control and buffer storage applications. The device includes full on-chip decoding, separate Data input and non-inverting Data output, as well as an active LOW Chip Select line.

Features

- New design to replace old 93415/93L415
- Improved ESD thresholds
- Alpha hard without die coat
- Commercial address access time
  93L415A 25 ns max
- Features open collector output
- Power dissipation decreases with increasing temperature

Connection Diagram

16-Pin DIP



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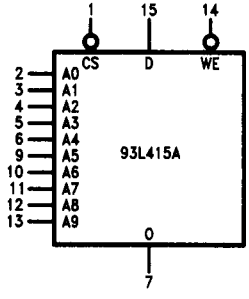
Top View

Order Number 93L415ADC or 93L415APC
See NS Package Number J16A* and N16E*

Optional Processing QR = Burn-In

*For most current package information, contact product marketing.

Logic Symbol



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Pin Names

$\overline{CS}$	Chip Select Input Active LOW
A0–A9	Address Inputs
$\overline{WE}$	Write Enable Input Active LOW
D	Data Input
O	Data Output

V_{CC} = Pin 16
GND = Pin 8

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Supply Voltage Range	−0.5V to +7.0V
Input Voltage (DC) (Note 1)	−0.5V to V_{CC}
Input Current (DC)	−12 mA to +5.0 mA
Voltage Applied to Outputs (Note 2)	−0.5V to 5.5V
Lead Temperature (Soldering, 10 sec.)	300°C
Maximum Junction Temperature (T_J)	+175°C
Output Current	+20 mA

Guaranteed Operating Ranges

Supply Voltage (V_{CC}) Commercial	5.0V ±5%
Case Temperature (T_C) Commercial	0°C to +75°C

DC Characteristics over operating temperature ranges (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 16 mA			0.45	V
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage for All Inputs (Notes 4, 5, & 6)	2.1			
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage for All Inputs (Notes 4, 5, & 6)			0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IN} = 0.4V		−180	−300	μA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IN} = 4.5V		1.0	40	μA
I_{IHB}	Input Breakdown Current	V_{CC} = Max, V_{IN} = V_{CC}			1.0	mA
V_{IC}	Input Diode Clamp Voltage	V_{CC} = Max, I_{IN} = −10 mA		−1.0	−1.5	V
I_{CEX}	Output Leakage Current	V_{CC} = Max, V_{OUT} = 4.5V		1.0	100	μA
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs = GND Output is Open			65	mA

AC Electrical Characteristics (Note 6) V_{CC} = 5.0 ±5%, GND = 0V, T_C = 0°C to + 75°C

Symbol	Parameter	Conditions	Min	Max	Units
READ TIMING					
t_{ACS}	Chip Select Access Time	*Figures 3a, 3b*		15	ns
t_{RCS}	Chip Select Recovery Time			15	ns
t_{AA}	Address Access Time (Note 7)			25	ns
WRITE TIMING					
t_W	Write Pulse Width to Guarantee Writing (Note 8)	*Figure 4*	20		ns
t_{WSD}	Data Setup Time Prior to Write		5		ns
t_{WHD}	Data Hold Time after Write		5		ns
t_{WSA}	Address Setup Time Prior to Write (Note 8)		5		ns
t_{WHA}	Address Hold Time after Write		5		ns
t_{WSCS}	Chip Select Setup Time Prior to Write		5		ns
t_{WHCS}	Chip Select Hold Time after Write		5		ns
t_{WS}	Write Enable to Output Disable			15	ns
t_{WR}	Write Recovery Time			15	ns

Note 1: Either input voltage limit or input current limit sufficient to protect the inputs.

Note 2: Output current limit required.

Note 3: Typical values are at V_{CC} = 5.0V, T_C = +25°C and maximum loading.

Note 4: Tested under static condition only.

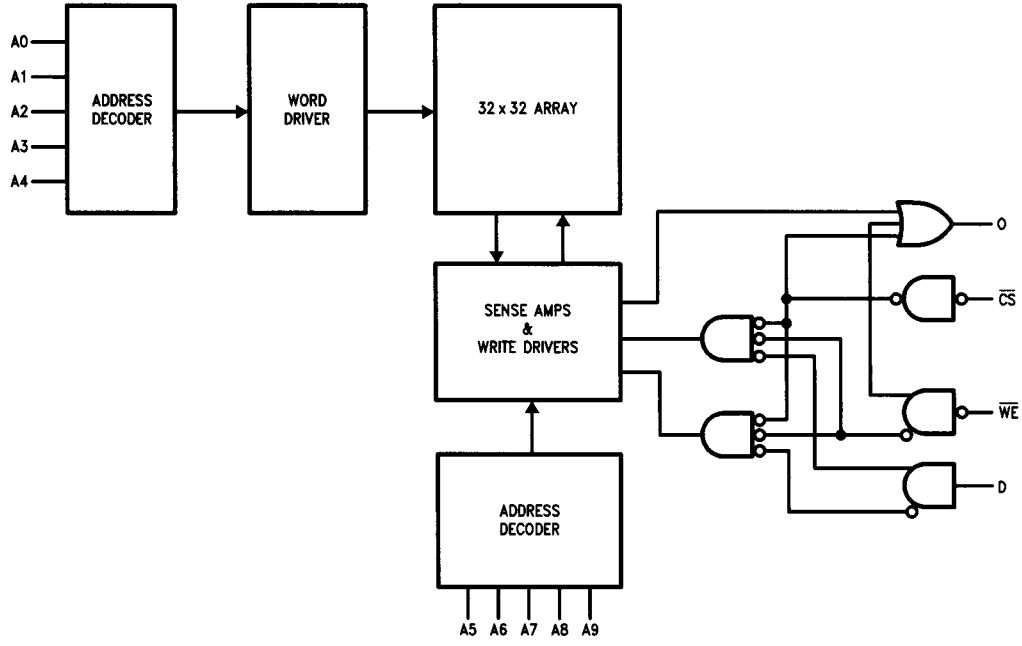
Note 5: Functional testing done at input levels V_{IL} = 0.45V (V_{OL} Max) and V_{IH} = 2.4V (V_{OH} Min).

Note 6: AC testing done at input levels V_{IH} = 3V, V_{IL} = 0V.

Note 7: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Note 8: t_W measured at t_{WSA} = Min. t_{WSA} measured at t_W = Min.

Logic Diagram



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Truth Table

Inputs			Outputs	Mode
$\overline{CS}$	$\overline{WE}$	D	O	
H	X	X	H	Not Selected
L	L	L	H	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH Voltage Level: 2.4V
L = LOW Voltage Level: 0.45V
X = Don't Care (HIGH or LOW)

Functional Description

The 93L415A is a fully decoded 1024-bit read/write Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address A0 through A9.

One Chip Select input is provided for easy memory array expansion of up to 2048 bits without the need for external decoding. For larger memories, the fast chip select access time permits direct address decoding without an increase in overall memory access time.

The read and write functions of the 93L415A are controlled by the state of the active low chip select ($\overline{CS}$) input. The write function is controlled by the active low write enable ($\overline{WE}$) input. With $\overline{CS}$ held low and $\overline{WE}$ held low, the data (D) is written into the memory location specified by addresses (A0 through A9). To assure a valid write, data setup (t_{WSD}), address setup (t_{WSA}), data hold (t_{WHD}), and address hold (t_{WHA}) times must be met. When $\overline{WE}$ is held HIGH and the chip selected, data is read from the addressed location and presented at the output O.

An open collector output is provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93L415As can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of R_L value must be used to provide a HIGH at the output when the chip is deselected. Any R_L value within the range specified below may be used.

$$\frac{V_{CC}\,(Max)}{I_{OL} - FO\,(1.6)} \leq R_L \leq \frac{V_{CC}\,(Min) - V_{OH}}{n\,(I_{CEX}) + FO\,(0.04)}$$

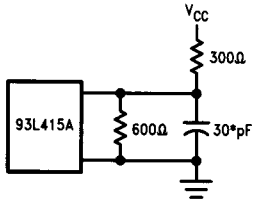
R_L is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output HIGH Level at Output Node
I_{OL} = Output LOW Current

The minimum R_L value is limited by the output current sinking ability. The maximum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}.

One Unit Load = 40 μA HIGH/1.6 mA LOW.

FO_{MAX} = 5 UL.

Functional Description (Continued)



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*Includes jig and probe capacitance

FIGURE 1. AC Test Circuit

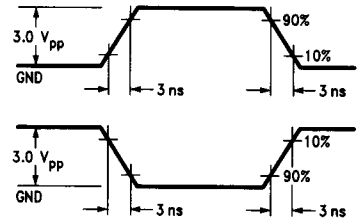

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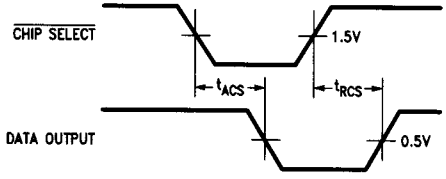
FIGURE 2. AC Test Input Levels



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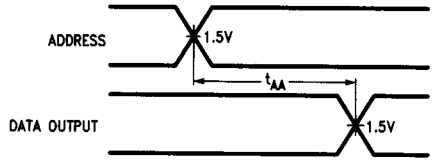
a. Read Mode Propagation Delay from Chip Select



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b. Read Mode Propagation Delay from Address Valid

FIGURE 3. Read Mode Timing

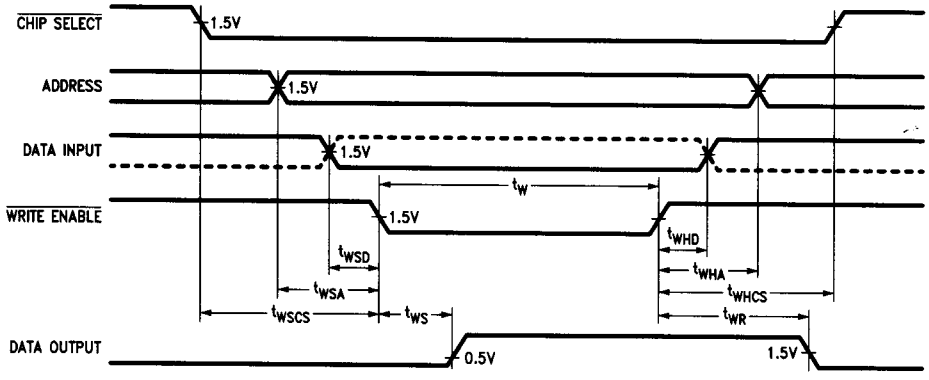

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FIGURE 4. Write Mode Timing

Note 1: Timing Diagram represents one solution which results in an optimium cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Note 2: Input voltage levels for worst case AC test are 3.0V/0V.