

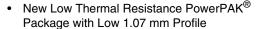


N-Channel Reduced Q_g, Fast Switching MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	$R_{DS(on)}(\Omega)$ $I_D(A$		
30	0.007 at V _{GS} = 10 V	19	
	0.010 at V _{GS} = 4.5 V	15	

FEATURES

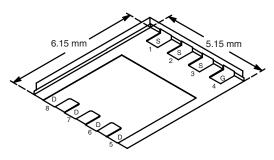
- · Halogen-free available
- TrenchFET[®] Power MOSFET



100 % R_g Tested



PowerPAK SO-8



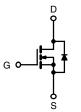
Bottom View

Ordering Information: Si7388DP-T1-E3 (Lead (Pb)-free)

Si7388DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

• DC/DC Synchronous Rectifier



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	$T_A = 25 ^{\circ}C$, unles	ss otherwise n	oted		
Parameter	Symbol	10 s	Steady State	Unit	
Drain-Source Voltage		V _{DS}	30		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current (T _{.I} = 150 °C) ^a	T _A = 25 °C	I _D	19	12	A
Continuous Diain Current (1 j = 150 °C)	T _A = 70 °C		15	9	
Pulsed Drain Current		I _{DM}	± 50		A
Continuous Source Current (Diode Conduction) ^a		I _S	4.1	1.6	
Maximum Power Dissipation ^a	T _A = 25 °C	- P _D	5	1.9	W
Maximum Power Dissipation	T _A = 70 °C		3.2	1.2	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b, c}		-	260		C

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Manipulation to Ambient (MACCET)	t ≤ 10 s	R _{thJA}	20	25	°C/W	
Maximum Junction-to-Ambient (MOSFET) ^a	Steady State		55	65		
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	2.0	2.6		

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
- b. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

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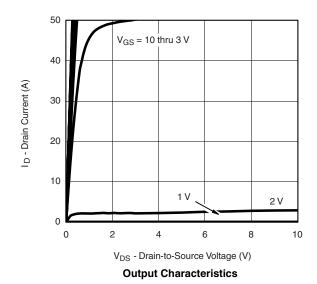
SPECIFICATIONS T _J = 25 °C	, unless ot	herwise noted					
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.80		1.6	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 12 V$			± 100	nA	
Zava Cata Valtaga Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	1	
Zero Gate Voltage Drain Current		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 70 ^{\circ}\text{C}$			5	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	40			Α	
Durin Occurs Oc Olate Desistance	B	V _{GS} = 10 V, I _D = 19 A		0.0058	0.007	0	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 15 \text{ A}$		0.008	0.010	Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 19 A		40		S	
Diode Forward Voltage ^a	V_{SD}	I _S = 4.1 A, V _{GS} = 0 V		0.75	1.1	V	
Dynamic ^b							
Total Gate Charge	Q_g			16.3	24		
Gate-Source Charge	Q_{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 5.0 \text{ V}, I_D = 19 \text{ A}$		4		nC	
Gate-Drain Charge	Q_{gd}			5.9			
Gate Resistance	R_g		0.5		2.2	Ω	
Turn-On Delay Time	t _{d(on)}			14	20		
Rise Time	t _r	V_{DD} = 15 V, R_L = 15 Ω		10	15	ns	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 1.0 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 6 \Omega$		44	70		
Fall Time	t _f			20	30		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 3 A, di/dt = 100 A/μs		40	70		

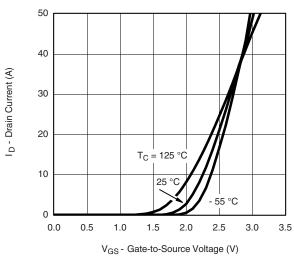
Notes:

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



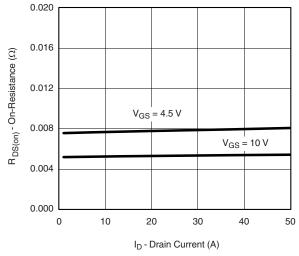




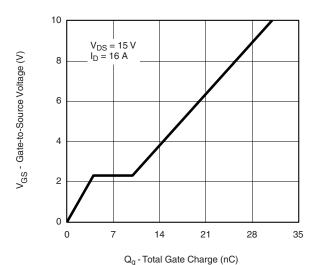




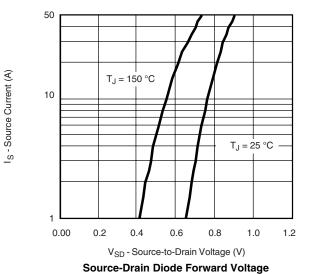
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



On-Resistance vs. Drain Current



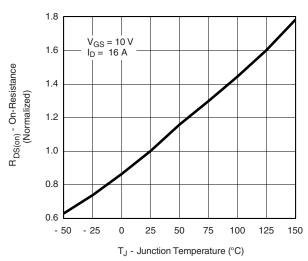
Gate Charge



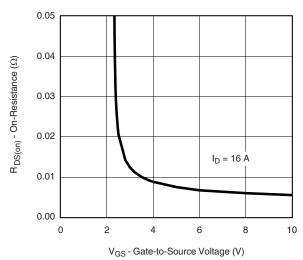
2500 2000 $\mathsf{C}_{\mathsf{iss}}$ C - Capacitance (pF) 1500 1000 Coss 500 0 0 5 10 15 20 25 30

V_{DS} - Drain-to-Source Voltage (V)

Capacitance



On-Resistance vs. Junction Temperature

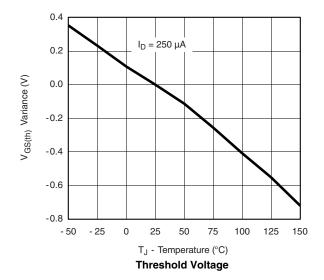


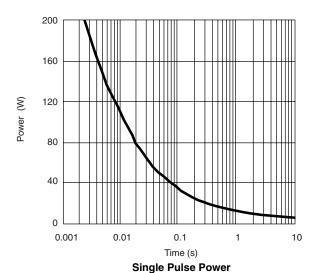
On-Resistance vs. Gate-to-Source Voltage

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

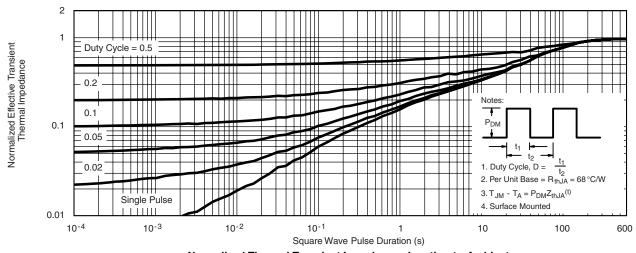




100 by R_{DS(on)}** 10 ms 10 ms 100 ms 100 ms 100 ms 100 ms 100 ms 100 single Pulse DC

 $V_{DS} \text{ - Drain-to-Source Voltage (V)} \\ ^*V_{GS} \text{ > minimum } V_{GS} \text{ at which } R_{DS(on)} \text{ is specified} \\$

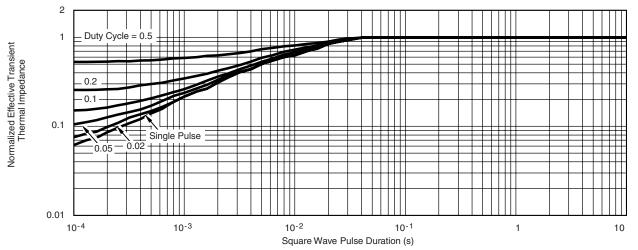
Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

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