A 0.65V/1µA Nanopower Voltage Detector with Dual Outputs

FEATURES

- Nanopower Voltage Detector in Single 4 mm^2 Package
- Ultra Low Total Supply Current: 1µA (max)
- Supply Voltage Operation: 0.65V to 2.5V
- Preset 0.78V UVLO Trip Threshold
- Internal ±10mV Hysteresis
- Resettable Latched Comparator
- Complimentary and Open-drain Comparator Outputs
- Separate Comparator Output Supply Pin

APPLICATIONS

Power-Fail Indicator
Low-Battery Detection
Battery-Backup Detection
CPU, Microprocessor, and Logic Reset Controller
Battery-powered Systems

DESCRIPTION

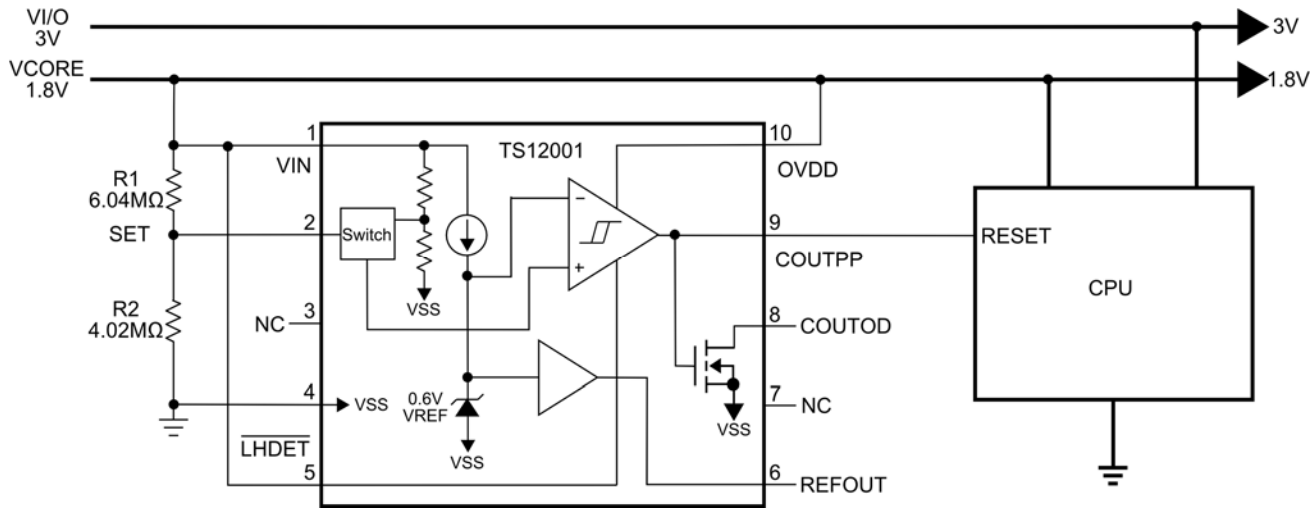
The TS12001 voltage detector combines a 0.58V reference and a comparator with resettable comparator latch in a single package. The TS12001 operates from a single 0.65V to 2.5V power supply and consumes less than 1µA total supply current. Optimized for ultra-long life operation, the TS12001 expands the growing "NanoWatt Analog™" high-performance analog integrated circuits portfolio.

The voltage detector exhibits a preset UVLO threshold voltage of 0.78V (typ) or can be set to other threshold voltages with two external resistors. The comparator exhibits ±10mV of internal hysteresis for clean, chatter-free output switching. The TS12001 also offers both push-pull and open-drain outputs. When compared against similar products, the TS12001 offers a factor-of-2 lower power consumption and at least a 33% reduction in pcb area.

The TS12001 is fully specified over the -40°C to +85°C temperature range and is available in a low-profile, 10-pin 2x2mm TDFN package with an exposed back-side paddle.

TYPICAL APPLICATION CIRCUIT

A Nanopower 1.8V Core System Voltage Detector



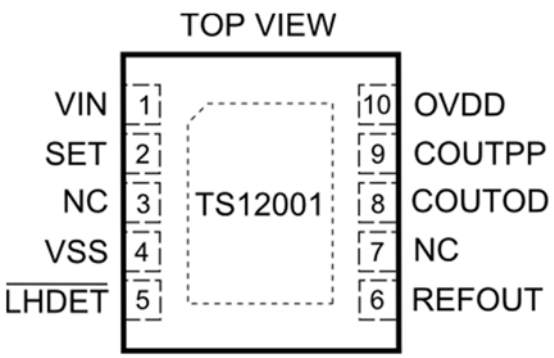
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{IN} to V_{SS}) .....+2.75V
Supply Voltage (OV_{DD} to V_{SS}) .....+2.75V
Input Voltage
SET.....V_{SS} – 0.3V to V_{IN} + 0.3V
$\overline{LHDET}$.....V_{SS} - 0.3V to +5.5V
Output Voltage
REFOUT..... V_{SS} – 0.3V to V_{IN} + 0.3V
COUTPP..... V_{SS} - 0.3V to OV_{DD} + 0.3V
COUTOD..... V_{SS} - 0.3V to +5.5V

Output Current
COUTPP, COUTOD.....20mA
Short-Circuit Duration
(REFOUT, COUTPP, COUTOD).....Continuous
Continuous Power Dissipation (T_A = +70°C)
10-Pin TDFN (Derate at 13.48mW/°C above +70°C) 1078mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (Soldering, 10s)..... +300°C

Electrical and thermal stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to any absolute maximum rating conditions for extended periods may affect device reliability and lifetime.

PACKAGE/ORDERING INFORMATION



2mm x 2mm x 0.75mm DFN-EP 10L
TD1022 Package

ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TS12001ITD1022	AAN	Tape & Reel	-----
TS12001ITD1022T		Tape & Reel	3000

Lead-free Program: Silicon Labs supplies only lead-free packaging.

Consult Silicon Labs for products specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

V_{IN} = OV_{DD} = 0.8V; V_{SS} = 0V; V_{SET} = V_{SS}; V_{COUTPP} = HiZ; V_{COUTOD} = HiZ; T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. See note 1.

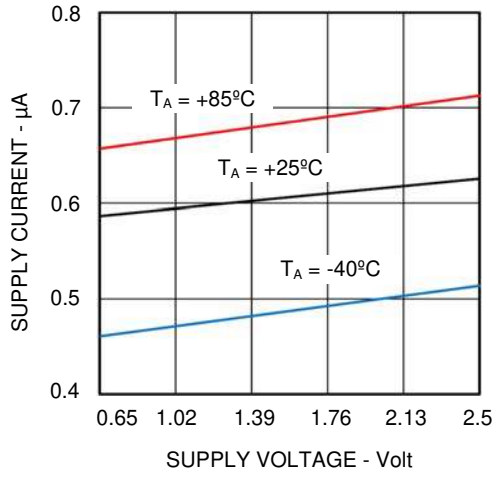
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{IN}			0.65		2.5	V
Supply Current	I_{IN}	REFOUT = open	T_A = +25°C			0.8	µA
			-40°C ≤ T_A ≤ 85°C			1	
UVLO Output Driver Supply Voltage	OV_{DD}			0.65		2.5	V
Output Driver Supply Current	I_{ODD}					0.1	µA
Preset UVLO Trip Point		V_{IN} falling until COUTPP switches LOW		725	761	797	mV
		V_{IN} rising until COUTPP switches HIGH		743	781	818	
SET Trip Point		V_{SET} falling until COUTPP switches LOW	T_A = +25°C	540	567	595	
			-40°C ≤ T_A ≤ 85°C	534		604	
		V_{SET} rising until COUTPP switches HIGH	T_A = +25°C	560	587	615	
			-40°C ≤ T_A ≤ 85°C	550		620	
SET Trip Response Time		V_{SET} rising			13		µs
		V_{SET} falling			10		
Preset UVLO Trip Hysteresis					±10		mV
SET Enable Threshold		See Note 2		90			mV
SET Input Leakage		V_{SET} = V_{SS}; V_{SET} = V_{IN}				20	nA
$\overline{LHDET}$ Input Low Voltage	V_{IL}	Comparator Latched Output Enabled	0.78V ≤ V_{IN} ≤ 1.1V			0.1	V
			1.1V < V_{IN} ≤ 2.5V			0.2	
$\overline{LHDET}$ Input High Voltage	V_{IH}	Comparator Latched Output Disabled	0.78V ≤ V_{IN} ≤ 1.1V	V_{IN} -0.1			V
			1.1V < V_{IN} ≤ 2.5V	1			
$\overline{LHDET}$ Input Leakage		$V_{\overline{LHDET}}$ = V_{SS}; $V_{\overline{LHDET}}$ = 5.5V				100	nA
Reference Output Voltage	V_{REF}		T_A = +25°C	555	577	600	mV
			-40°C ≤ T_A ≤ 85°C	552		602	
Reference Load Regulation		I_{OUT} = ±100nA				0.5	%
Output High Voltage	V_{OH}	COUTPP; I_{OUT} = -100µA		V_{IN} – 0.1			V
Output Low Voltage	V_{OL}	COUTPP; I_{OUT} = 100µA				V_{SS} + 0.1	V
Output Low Voltage	V_{OL}	COUTOD; I_{OUT} = 100µA				V_{SS} + 0.11	V
Output Short-Circuit Current,	I_{SC}	Sourcing; V_{COUTPP} = V_{SS}		0.1			mA
		Sinking; V_{COUTPP} = V_{IN}		0.5			mA
		Sinking; V_{COUTOD} = V_{IN}			1.4		mA
Open Drain Leakage		COUTOD; V_{COUTOD} = 5V				20	nA

Note 1: All devices are 100% production tested at T_A = +25°C and are guaranteed by characterization for T_A = T_{MIN} to T_{MAX}, as specified.
Note 2: A SET voltage above this threshold voltage enables the SET pin voltage to control the comparator output.

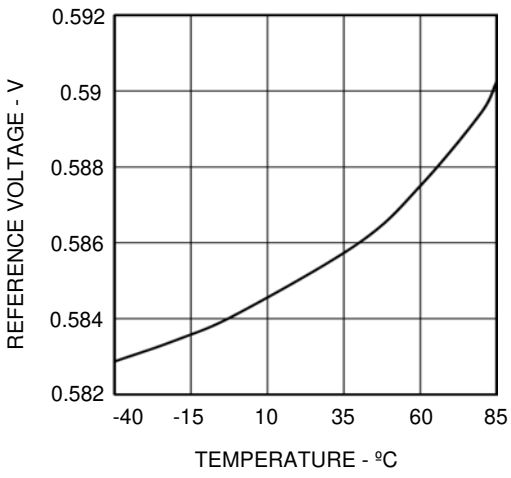
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = OV_{DD} = 2.5V; V_{SS} = 0V; V_{SET} = V_{SS}; V_{COUTPP} = HiZ; V_{COUTOD} = HiZ, unless otherwise noted. Typical values are at T_A = +25°C.

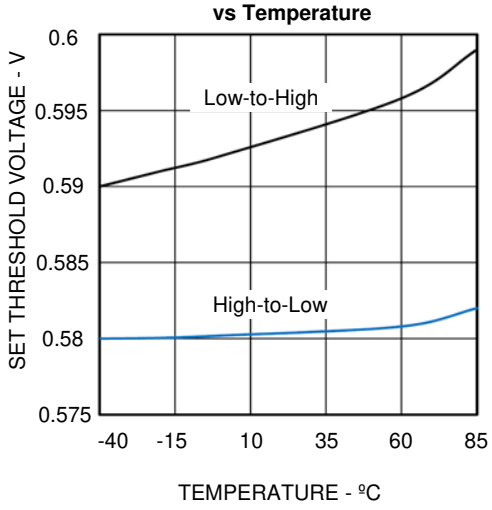
Supply Current vs Supply Voltage and Temperature



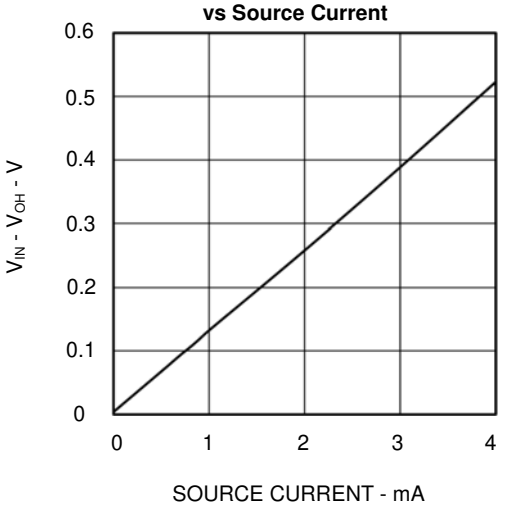
Reference Voltage vs Temperature



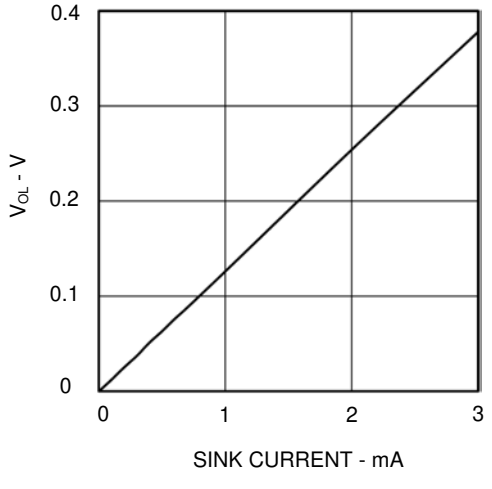
SET Threshold Voltage vs Temperature



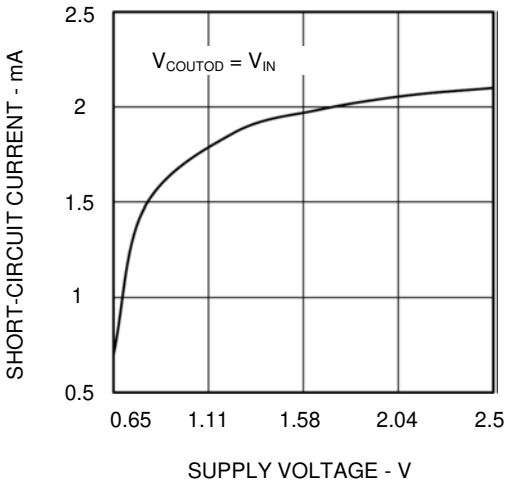
COUTPP Output Voltage High vs Source Current



COUTPP Output Voltage Low vs Sink Current



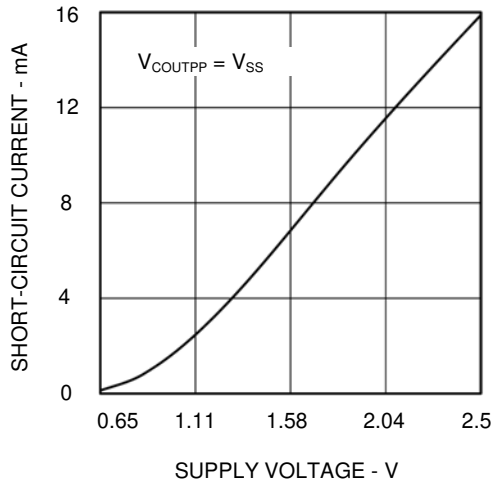
COUTOD Short-Circuit Current vs Supply Voltage



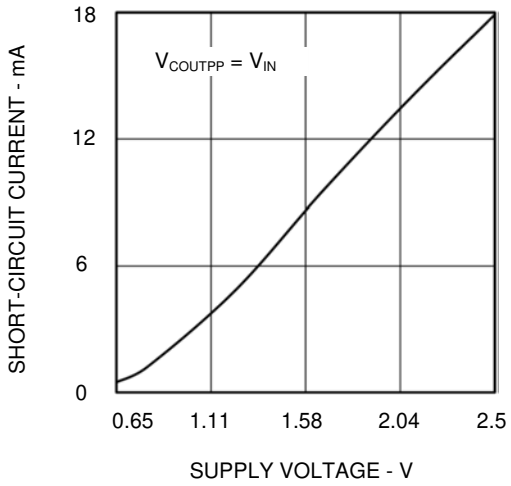
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = OV_{DD} = 2.5V; V_{SS} = 0V; V_{SET} = V_{SS}; V_{COUTPP} = HiZ; V_{COUTOD} = HiZ, unless otherwise noted. Typical values are at T_A = +25°C.

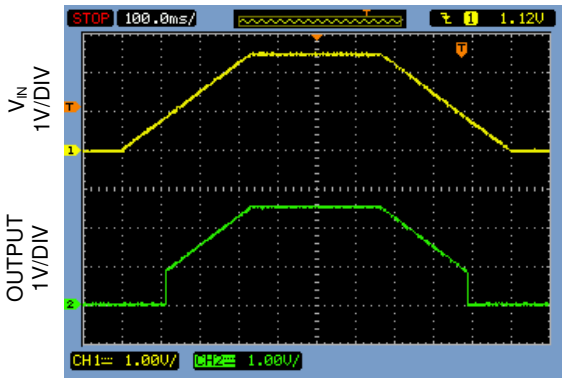
COUTPP Short-Circuit Current vs Supply Voltage



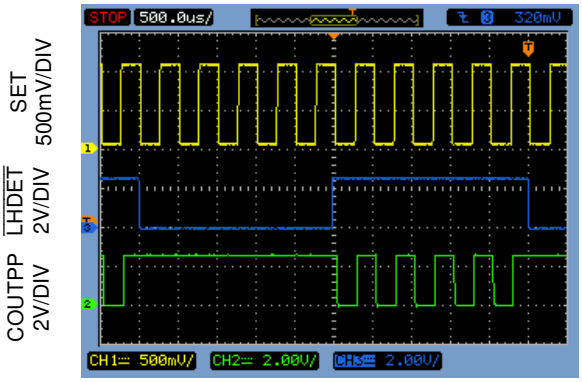
COUTPP Short-Circuit Current vs Supply Voltage



COUTPP Power-Up Transient Response
V_{SET} = 2.5V, C_{LOAD} = 15pF



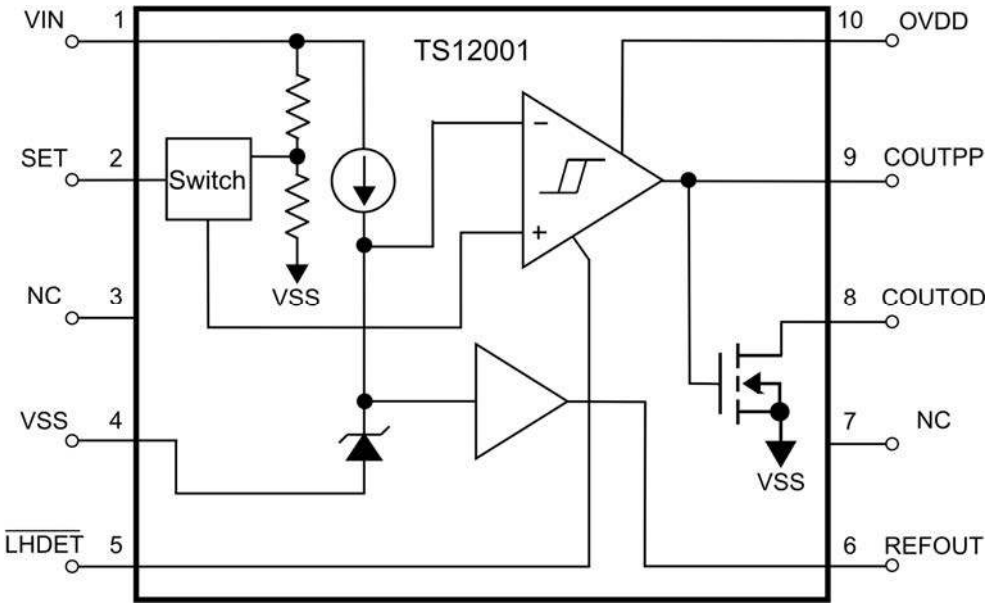
COUTPP Transient Response with $\overline{LHDET}$
V_{IN} = OV_{DD} = 2.5V, C_{LOAD} = 15pF



PIN FUNCTIONS

PIN	NAME	FUNCTION
1	VIN	Positive Supply Voltage. Connect a 0.1µF bypass capacitor from this pin to analog VSS/GND.
2	SET	External UVLO Trip Threshold Set Pin. When this pin is set to VSS, the internal preset 0.78V UVLO trip threshold controls the comparator output. When the applied voltage to this pin is higher than 90mV, the SET pin sets the trip threshold and controls the comparator output. If the SET pin is not used, connect the pin to to VSS.
3	NC	No Connection
4	VSS	Negative Supply Voltage.
5	$\overline{\text{LHDET}}$	Latch Enable Pin. When $\overline{\text{LHDET}}$ is set HIGH, the outputs of the comparator will toggle normally based on the inputs to the comparator. When $\overline{\text{LHDET}}$ is set LOW and COUTPP is HIGH, COUTPP will remain HIGH despite any changes to the input of the comparator. COUTPP will once again respond to changes to the input when $\overline{\text{LHDET}}$ is toggled HIGH. If COUTPP is initially LOW and the $\overline{\text{LHDET}}$ is then LOW, COUTPP will stay LOW. If a LOW-to-HIGH transition occurs on COUTPP, COUTPP will switch to HIGH and stay HIGH and not respond to any changes at the input. The $\overline{\text{LHDET}}$ pin must always be set to a known state. For unlatched comparator operation, set $\overline{\text{LHDET}}$ to HIGH. The open-drain output (COUTOD) is the inverted version of the COUTPP output.
6	REFOUT	0.58V Reference Output
7	NC	No Connection
8	COUTOD	Comparator Open-Drain Output
9	COUTPP	Comparator Push-Pull Output
10	OVDD	Output Driver Positive Supply Voltage. Connect a 0.1µF bypass capacitor from this pin to analog VSS/GND.
EP	----	Exposed paddle is electrically connected to VSS/GND.

BLOCK DIAGRAM



THEORY OF OPERATION

The TS12001 combines a 0.58V ±4.5% reference and an analog comparator with a resettable comparator latch in a single package. The TS12001 operates from a single 0.65V to 2.5V power supply and consumes less than 1µA total supply current. The TS12001 comparator has a push-pull and open-drain output driver. The push-pull output driver is powered from a separate supply voltage, OV_{DD}. The open-drain output stage allows for easy output voltage level translation as may be required when driving systems powered with a different power supply rail. The analog comparator exhibits ±10mV of internal hysteresis for clean, chatter-free output switching. The internal reference was designed to sink or source up to 0.1µA load currents.

The TS12001 has a preset UVLO threshold voltage of 0.78V (typ) or can be set to other threshold voltages with two external resistors where the divided voltage is applied to the SET pin. When the SET pin voltage is grounded or it is less than approximately 90mV, the internal preset UVLO threshold circuit will control the comparator outputs. If the SET pin is above approximately 90mV, the external voltage divider circuit will control the comparator outputs. The 0.58V reference voltage is tied to the inverting input of the comparator and the output of a switch is connected to the non-inverting input of the comparator. The output of the switch is either the SET voltage or the internal UVLO threshold voltage, depending on whether the SET pin voltage is above or below approximately 90mV. If the switch output is above 0.58V, the push-pull output (COUTPP) will be HIGH and the open-drain output (COUTOD) will be LOW and vice versa. For proper operation, the supply voltage V_{IN} must be applied before the output driver supply voltage (OV_{DD}) is applied.

The TS12001 has a latch enable pin ($\overline{LHDET}$) that

allows the output of the comparator to latch to a HIGH state under certain conditions. If $\overline{LHDET}$ is set HIGH, the COUTPP output will switch based on the input to the comparator. When $\overline{LHDET}$ is set LOW and COUTPP is HIGH, COUTPP will remain HIGH until $\overline{LHDET}$ goes HIGH. If COUTPP is initially LOW instead, COUTPP will remain LOW until a LOW-to-HIGH transition occurs on the COUTPP output. After this event, COUTPP will remain HIGH and be unresponsive to any changes at the input of the comparator until $\overline{LHDET}$ goes HIGH. In essence, the $\overline{LHDET}$ pin offers a LOW-to-HIGH detection. However, $\overline{LHDET}$ must not be left open. The open-drain output, COUTOD, is the inverter version of the COUTPP output. Connect $\overline{LHDET}$ to V_{IN} for normal operation or to V_{SS} for $\overline{LHDET}$ enable.

If the SET pin is not used, it cannot be left unconnected and should be tied to V_{SS}.

Comparator

The TS12001 has an internal comparator that can eliminate supply glitches that commonly occur when output transitions occur. In addition, the input exhibits ±10mV of internal hysteresis in order to insure clean output switching behavior. The outputs can swing to within 100mV of the supply rails. The COUTPP output can source and sink 0.1mA and 0.5mA of current. The COUTD outputs can sink 1.4mA of current with V_{COUTOD} = 0.78V

Internal Reference

The TS12001's on-board 0.58V ±4.5% reference voltage can source and sink 0.1µA and 0.1µA of current and can drive a capacitive load less than 50pF and greater than 50nF with a maximum capacitive load of 250nF. The higher the capacitive load, the lower the noise on the reference voltage and the longer the time needed for the reference voltage to respond and become available on the REFOUT pin. With a 250nF capacitive load, the response time is approximately 20ms. While also available as a separate pin as REFOUT, the reference is tied internally to the inverting input of the comparator.

APPLICATIONS INFORMATION

External Voltage Detector Design

Depending on the battery voltage used and the voltage one wishes to detect, the TS12001 can be designed accordingly. As shown in Figure 1, R1 and R2 can be selected based on the desired voltage to detect. Table 1. provides R1 and R2 resistor combinations for detecting various V_{IN} voltages.

V_{IN} Threshold Voltage(V)	R1(MΩ)	R2(MΩ)
0.9	2.2	4.02
1.07	3.32	4.02
1.28	4.75	4.02
1.52	6.49	4.02
1.85	8.66	4.02

Table 1. Resistor Combinations for Several V_{IN} Threshold Voltages

The design equation for this circuit is shown below. The SET pin voltage (V_{SET}) that will cause a HIGH-to-LOW transition on the output is approximately 580mV. To design the circuit, R1 or R2 can be selected along with the desired battery voltage to detect.
Then, the second resistor value can be evaluated using the voltage divider equation below.

$$R1 = \frac{V_{IN} \times R2 - V_{SET} \times R2}{V_{SET}}$$

A Nanopower 1.8V Core System Voltage Detector

When power supply rails sag in any system, it is important to alert the CPU. A CPU can be used to detect when I/O or core system voltages sag below a prescribed threshold as shown Figure 2. In this circuit, a 1.8V core system voltage detector is designed around the TS12001 providing a low battery detect signal. R1 and R2 were selected to set a SET voltage at 582mV so that when VCORE drops below 1.77V, the TS12001 output transitions to LOW. It is recommended to use 1% resistors for optimal accuracy. The circuit consumes approximately 0.75µA of current when VCORE = 1.8V.

PC Board Layout and Power-Supply Bypassing

While power-supply bypass capacitors are not typically required, it is good engineering practice to use 0.1uF bypass capacitors close to the device's

power supply pins. When the power supply impedance is high, the power supply leads are long, or there is excessive noise on the power supply traces. To reduce stray capacitance, it is also good engineering practice to make signal trace lengths as short as possible. Also recommended are a ground plane and surface mount resistors and capacitors.

Input Noise

Radiated noise is common in low power circuits that require high impedance circuits. To minimize this effect, all traces between any of the inputs and passive component networks should be made as short as possible.

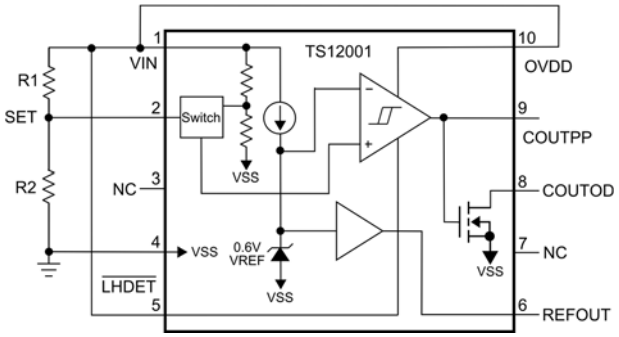


Figure 1. External Voltage Detector Design Circuit

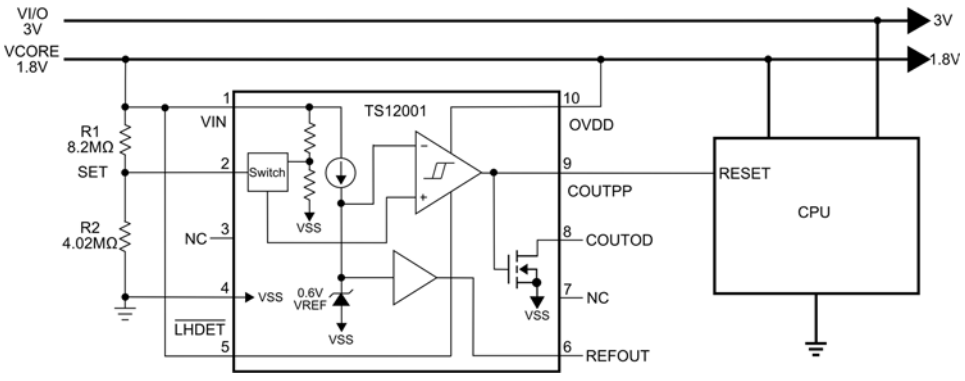
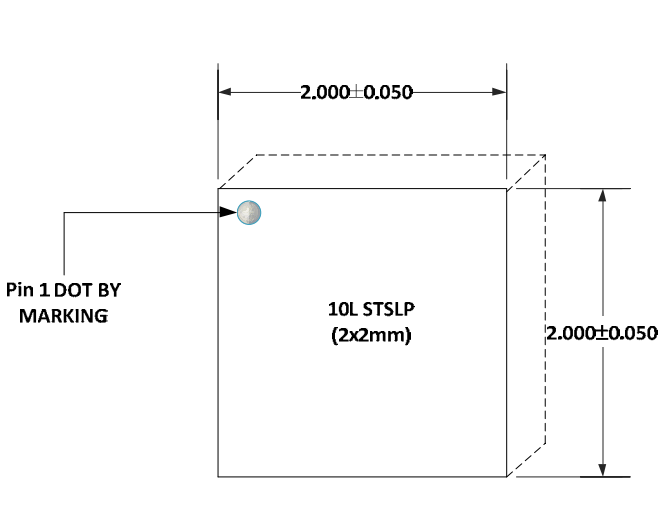


Figure 2. A Nanopower 1.8V Core System Voltage Detector Circuit

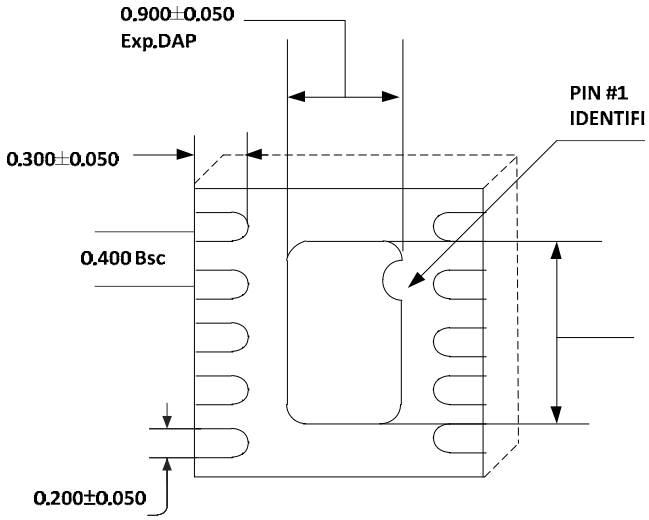
PACKAGE OUTLINE DRAWING

10-Pin TDFN22 Package Outline Drawing

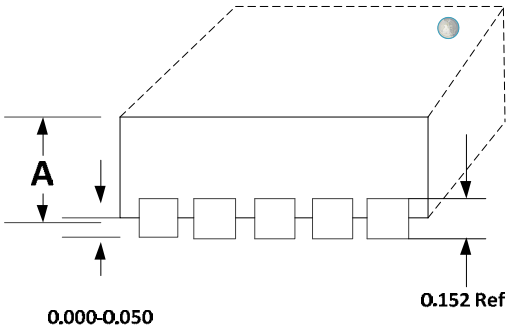
(N.B., Drawings are not to scale)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

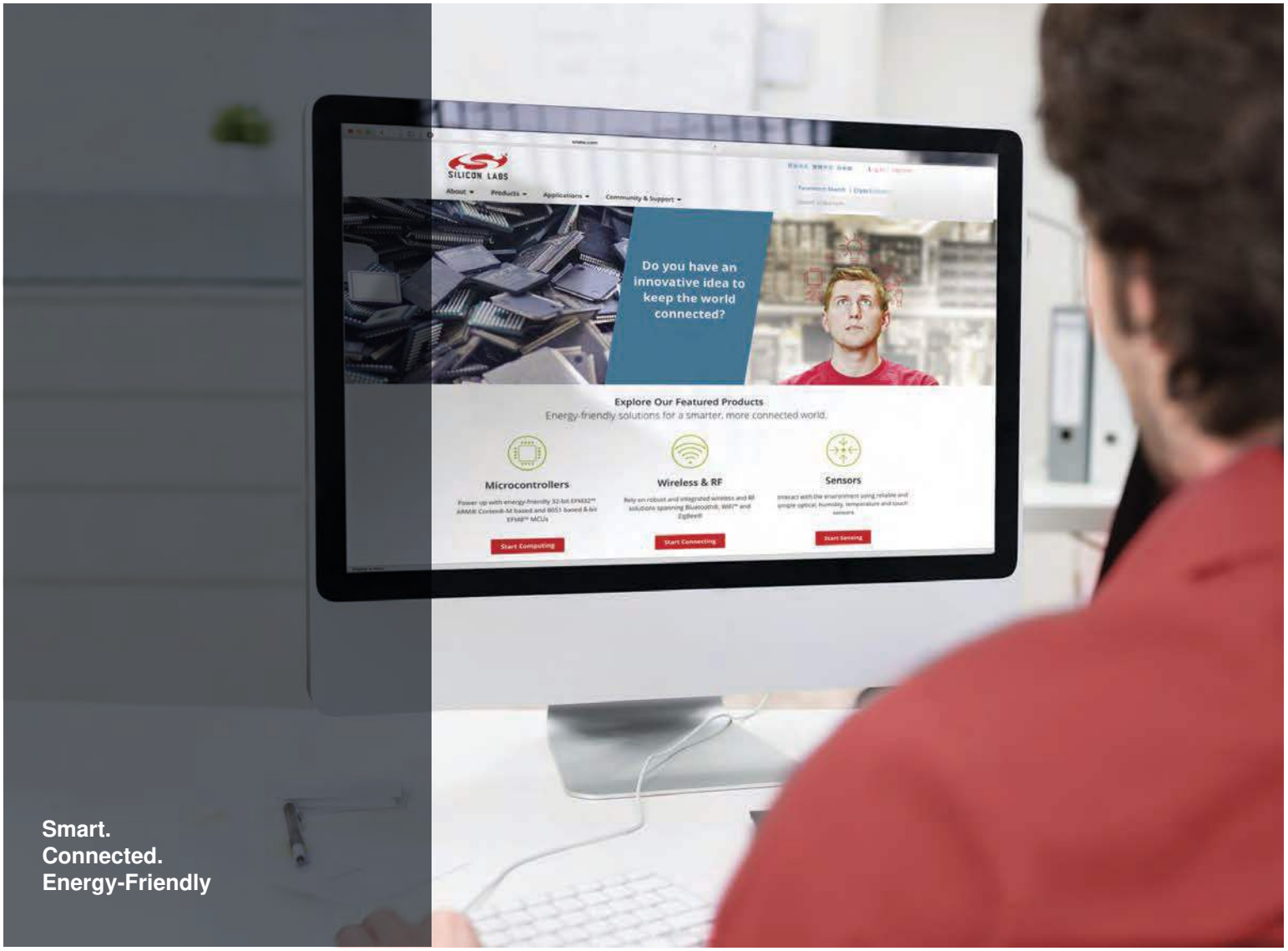
NOTE!

- All dimensions in mm.
- This part is compliant with JEDEC MO-22

A	MAX.	0.600
	NOM.	0.550
	MIN.	0.500

Patent Notice

Silicon Labs invests in research and development to help our customers differentiate in the market with innovative low-power, small size, analog-intensive mixed-signal solutions. Silicon Labs' extensive patent portfolio is a testament to our unique approach and world-class engineering team.



Products
www.silabs.com/products

Quality
www.silabs.com/quality

Support and Community
community.silabs.com

SILICON LABS®

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com