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## General Description

The Cypress CYBLE-416045-02 is a fully certified and qualified module supporting Bluetooth® Low Energy (BLE) wireless communication. The CYBLE-416045-02 is a turnkey solution and includes onboard crystal oscillators, trace antenna, passive components, and the Cypress PSoC® 63 BLE silicon device. Refer to the PSoC 63 BLE [datasheet](#) for additional details on the capabilities of the PSoC 63 BLE device used on this module.

The EZ-BLE™ Creator module is a scalable and reconfigurable platform architecture. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. The CYBLE-416045-02 also includes digital programmable logic, high-performance analog-to-digital conversion (ADC), low-power comparators, and standard communication and timing peripherals.

The CYBLE-416045-02 includes a royalty-free BLE stack compatible with Bluetooth 5.0 and provides up to 36 GPIOs in a 14 × 18.5 × 2.00 mm package.

The CYBLE-416045-02 is a complete solution and an ideal fit for applications seeking a high-performance BLE wireless solution.

## Module Description

- Module size: 14.0 mm × 18.5 mm × 2.00 mm (with shield)
- 1 MB Application Flash with 32-KB EEPROM area and 32-KB Secure Flash
- 288-KB SRAM with Selectable Retention Granularity
- Up to 36 GPIOs with programmable drive modes, strengths, and slew rates
- Bluetooth 5.0 qualified single-mode module
  - QDID: [D040144](#)
  - Declaration ID: [112778](#)
- Certified to FCC, CE, MIC, and ISED regulations
- Industrial temperature range: -40 °C to +85 °C
- 150-MHz Arm® Cortex®-M4F CPU with single-cycle multiply (Floating Point Unit (FPU) and Memory Protection Unit (MPU))
- 100-MHz Cortex-M0+ CPU with single-cycle multiply and MPU
- OTP eFuse memory for validation and security

## Power Consumption

- TX output power: -20 dbm to +4 dbm
- Received signal strength indication (RSSI) with 4-dB resolution
- TX current consumption of 5.7 mA (radio only, 0 dbm)
- RX current consumption of 6.7 mA (radio only)

## Low-Power 1.71 V to 3.6 V Operation

- Active, Low-power Active, Sleep, Low-power Sleep, Deep Sleep, and Hibernate modes for fine-grained power management
- Deep Sleep mode current with 64K SRAM retention is 7 µA with 3.3-V external supply and internal buck
- On-chip Single-In Multiple Out (SIMO) DC-DC Buck converter, less than 1 µA quiescent current
- Backup domain with 64 bytes of memory and Real-Time-Clock (RTC) programmable analog

## Serial Communication

- Five independent runtime reconfigurable serial communication blocks (SCBs), each is software configurable as I<sup>2</sup>C, SPI, or UART

## Timing and Pulse-Width Modulation (TCPWM)

- Thirty-two TCPWM blocks
- Center-aligned, Edge, and Pseudo-random modes
- Comparator-based triggering of Kill signals

## Up to 36 Programmable GPIOs

- Any GPIO pin can be CapSense®, analog/digital

## Audio Subsystem

- I<sup>2</sup>S interface; up to 192 kilosamples (ksps) word clock
- Two pulse-density modulation (PDM) channels for stereo digital microphones

## Programmable Analog

- 12-bit 1 Msps SAR ADC with differential and single-ended modes and Sequencer with signal averaging
- One 12-bit voltage mode DAC with less than 5 µs settling time
- Two opamps with low-power operation modes
- Two low-power comparators that operate in Deep Sleep and Hibernate modes
- Built-in temperature sensor connected to ADC

## Programmable Digital

- 12 programmable logic blocks, each with eight macrocells and an 8-bit data path (called universal digital blocks or UDBs)
- Usable as drag-and-drop Boolean primitives (gates, registers), or as Verilog programmable blocks
- Cypress-provided peripheral component library using UDBs to implement functions such as communication peripherals (for example, LIN, UART, SPI, I<sup>2</sup>C, S/PDIF and other protocols), waveform generators, pseudo-random sequence (PRS) generation, and other functions.
- Smart I/O (Programmable I/O) blocks enable Boolean operations on signals coming from, and going to, GPIO pins

- Two ports with Smart I/O block capability are provided and are available during Deep Sleep

### Capacitive Sensing

- Cypress Capacitive Sigma-Delta (CSD) provides best-in-class SNR, liquid tolerance, and proximity sensing
- Mutual capacitance sensing (Cypress CSX) with dynamic usage of both self and mutual sensing
- Wake-on-Touch (WOT) with very low current
- Cypress-supplied software component makes capacitive sensing design fast and easy
- Automatic hardware tuning (SmartSense)

### Energy Profiler

- Block that provides history of time spent in different power modes
- Software energy profiling to observe and optimize energy consumption

### Security Built into Platform Architecture

- Multi-faceted secure architecture based on ROM-based root of trust
- Secure boot uninterruptible until system protection attributes are established

- Authentication during boot using hardware hashing
- Step-wise authentication of execution images
- Secure execution of code in execute only mode for protected routines
- All debug and test ingress paths can be disabled

### Cryptography Accelerators

- Hardware acceleration for Symmetric and Asymmetric Cryptographic methods (AES, 3DES, RSA, and ECC) and Hash functions (SHA-512, SHA-256)
- True Random Number Generator (TRNG) function

## More Information

Cypress provides a wealth of data at [www.cypress.com](http://www.cypress.com) to help you to select the right module for your design, and to help you to quickly and effectively integrate the module into your design.

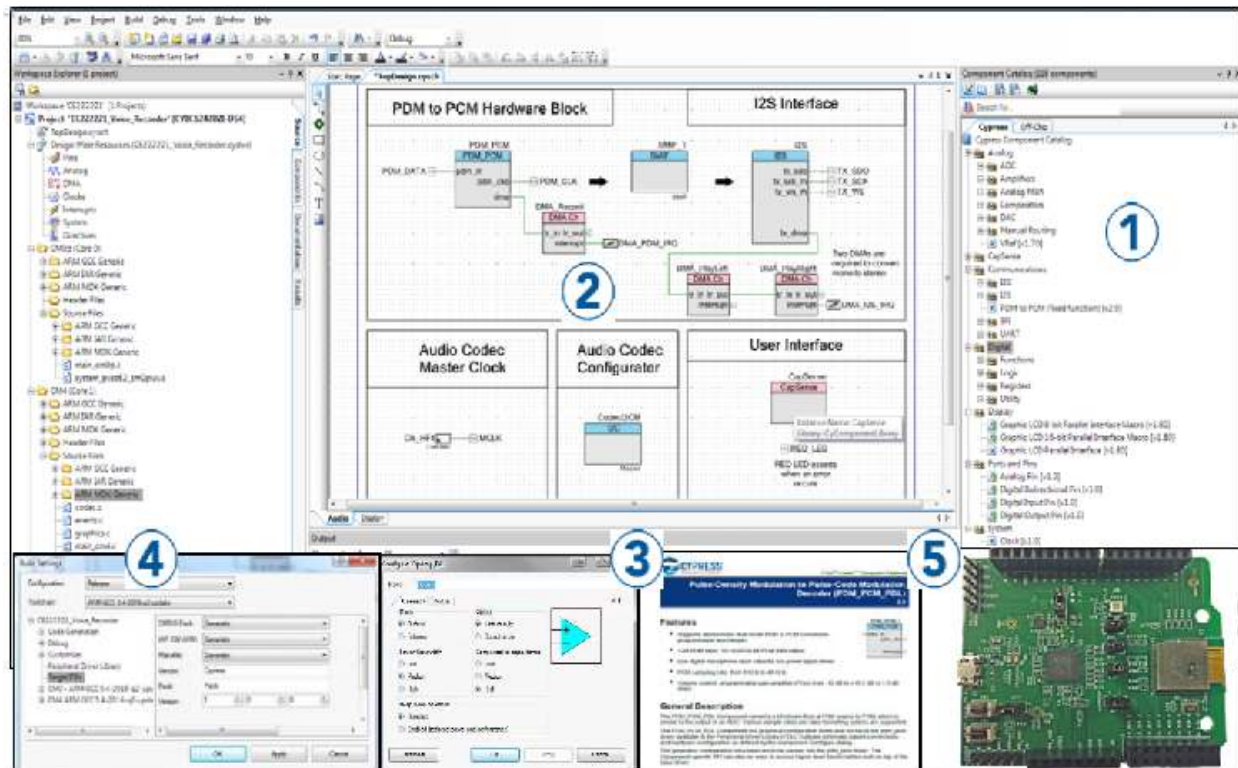
- Overview: [Module Roadmap](#)
- [PSoC 63 BLE Silicon Datasheet](#)
- Application Notes:
  - [AN96841](#) - Getting Started with EZ-BLE Module
  - [AN210781](#) - Getting Started with PSoC 6 MCU BLE
  - [AN215656](#) - PSoC 6 MCU Dual-CPU System Design
  - [AN91162](#) - Creating a BLE Custom Profile
  - [AN217666](#) - PSoC 6 MCU Interrupts
  - [AN91445](#) - Antenna Design and RF Layout Guidelines
  - [AN213924](#) - PSoC 6 MCU Bootloader Guide
  - [AN219528](#) - PSoC 6 MCU Power Reduction Techniques
- Technical Reference Manual (TRM):
  - PSoC 63 with BLE Architecture [Technical Reference Manual](#)
  - PSoC 63 with BLE Registers [Technical Reference Manual](#)
- Knowledge Base Articles
  - [KBA97095](#) - EZ-BLE™ Module Placement
  - [KBA213976](#) - FAQ for BLE and Regulatory Certifications with EZ-BLE modules
  - [KBA210802](#) - Queries on BLE Qualification and Declaration Processes
- Development Kits:
  - [CYBLE-416045-EVAL](#), CYBLE-416045-02 Evaluation Board
  - [CY8CKIT-062-BLE](#), PSoC 63 BLE Pioneer Kit
- Test and Debug Tools:
  - [CYSmart](#), Bluetooth LE Test and Debug Tool (Windows)
  - [CYSmart Mobile](#), Bluetooth LE Test and Debug Tool (Android/iOS Mobile App)

## PSoC Creator™ Integrated Design Environment (IDE)

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables you to design hardware and firmware systems concurrently, based on PSoC 6 MCU. As shown below, with PSoC Creator, you can:

1. Explore the library of 200+ Components in PSoC Creator
2. Drag and drop Component icons to complete your hardware system design in the main design workspace
3. Configure Components using the Component Configuration Tools and the Component Datasheets
4. Co-design your application firmware and hardware in the PSoC Creator IDE or build project for 3rd party IDE
5. Prototype your solution with the CYBLE-416045-02 Evaluation Kit. If a design change is needed, PSoC Creator and Components enable you to make changes on the fly without the need for hardware revisions

Figure 1. PSoC Creator Schematic Entry and Components



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## Functional Definition

### CPU and Memory Subsystem

#### *CPU*

The CPU subsystem in the CYBLE-416045-02 consists of two Arm Cortex cores and their associated buses and memories: M4 with FPU and MPU, and M0+ with an MPU. The M4 and M0+ cores have 8-KB instruction caches (I-Cache) with a four-way set associativity. This subsystem also includes independent DMA controllers with 32 channels each, a cryptographic accelerator block, 1 MB of on-chip Flash, 288 KB of SRAM, and 128 KB of ROM.

The Cortex-M0+ provides a secure, uninterruptible boot function. This guarantees that post-boot, system integrity is checked and privileges enforced. Shared resources can be accessed through the normal Arm multilayer bus arbitration and exclusive accesses are supported by an Inter-Processor Communication (IPC) scheme, which implements hardware semaphores and protection. Active power consumption for the Cortex-M4 is 22  $\mu\text{A}/\text{MHz}$  and 15  $\mu\text{A}/\text{MHz}$  for the Cortex-M0+, both at 3.3-V supply voltage with the internal buck enabled and at 0.9 V internal supply. Note that at Cortex-M4 speeds above 100 MHz, the M0+ and Peripheral subsystem are limited to half the M4 speed. If the M4 is running at 150 MHz, the M0+ and peripheral subsystem is limited to 75 MHz.

#### *DMA Controllers*

There are two DMA controllers with 16 channels each. They support independent accesses to peripherals using the AHB multilayer bus.

#### *Flash*

CYBLE-416045-02 has 1 MB of flash with additional 32K of flash that can be used for EEPROM emulation for longer retention and a separate 32 KB block of flash that can be securely locked and is only accessible via a key lock that cannot be changed (OTP).

#### *SRAM with 32-KB Retention Granularity*

There is 288 KB of SRAM memory, which can be fully retained or retained in increments of user-designated 32-KB blocks.

#### *SROM*

There is a supervisory 128 KB ROM that contains boot and configuration routines. This ROM will guarantee Secure Boot if authentication of user flash is required.

#### *OTP eFuse*

The 1024-bit OTP memory can provide a unique and unalterable Identifier on a per chip basis. This unalterable key can be used to access secured flash.

## System Resources

### *Power System*

The power system provides assurance that voltage levels are as required for each respective mode and will either delay mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper function or generate resets (brownout detect (BOD)) when the power supply drops below specified levels. The design will guarantee safe chip operation between power supply voltage dropping below specified levels (for example, below 1.71 V) and the reset occurring. There are no voltage sequencing requirements. The  $V_{DD}$  core logic supply (1.71 to 3.6 V) will feed an on-chip buck, which will produce the core logic supply of either 1.1 V or 0.9 V selectable. Depending on the frequency of operation, the buck converter will have a quiescent current of  $<1 \mu\text{A}$ . A separate power domain called Backup is provided; note this is not a power mode. This domain is powered from the  $V_{BACKUP}$  domain and includes the 32-kHz watch crystal oscillator (WCO), RTC, and backup registers. It is connected to VDD when not used as a backup domain. Port 0 is powered from this supply. Pin 5 of Port 0 (P0.5) can be assigned as a PMIC wakeup output (timed by the RTC); P0.5 is driven to the resistive pull-up mode by default.

### *Clock System*

The CYBLE-416045-02 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for the CYBLE-416045-02 consists of the internal main oscillator (IMO) and internal low-speed oscillator (ILO), crystal oscillators: external crystal oscillator (ECO) and WCO, PLL, frequency-locked loop (FLL), and provision for an external clock. An FLL will provide fast wake-up at high clock speeds without waiting for a PLL lock event (which can take up to 50  $\mu\text{s}$ ). Clocks may be buffered and brought out to a pin on a Smart I/O port.

The 32-kHz oscillator is trimmable to within 2 ppm using a higher accuracy clock. The ECO will deliver  $\pm 20$  ppm accuracy and will use an external crystal.

#### *IMO Clock Source*

The IMO is the primary source of internal clocking in CYBLE-416045-02. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 8 MHz. IMO tolerance is  $\pm 2\%$  and its current consumption is less than 10  $\mu\text{A}$ .

#### *ILO Clock Source*

The ILO is a very low-power oscillator, nominally 32 kHz, which may be used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

### Watchdog Timer (WDT)

A WDT is implemented in the clock block running from the ILO or from the WCO; this allows watchdog operation during Deep Sleep and Hibernate modes, and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

### Clock Dividers

Integer and Fractional clock dividers are provided for peripheral use and timing purposes. There are eight 8-bit integer and sixteen 16-bit integer clock dividers. There is also one 24.5-bit fractional and four 16.5-bit fractional clock dividers.

### Reset

The CYBLE-416045-02 can be reset from a variety of sources including software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is present through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

## BLE Radio and Subsystem

CYBLE-416045-02 incorporates a Bluetooth Smart subsystem that contains the PHY and Link Layer (LL) engines with an embedded security engine. The physical layer consists of the digital PHY and the RF transceiver that transmits and receives GFSK packets at 2 Mbps over a 2.4-GHz ISM band, which is compliant with Bluetooth Smart Bluetooth Specification 5.0. The baseband controller is a composite hardware and firmware implementation that supports both master and slave modes. Key protocol elements, such as Host controller Interface (HCI) and link control, are implemented in firmware. Time-critical functional blocks, such as encryption, CRC, data whitening, and access code correlation, are implemented in hardware (in the LL engine).

The RF transceiver contains an integrated balun, which provides a single-ended RF port pin to drive a 50  $\Omega$  antenna via a matching/filtering network. In the receive direction, this block converts the RF signal from the antenna to a digital bit stream after performing GFSK demodulation. In the transmit direction, this block performs GFSK modulation and then converts a digital baseband signal to a radio frequency before transmitting it to air through the antenna.

Key features of BLESS are as follows:

- Master and Slave single-mode protocol stack with logical link control and adaptation protocol (L2CAP), attribute (ATT), and security manager (SM) protocols
- API access to generic attribute profile (GATT), generic access profile (GAP), and L2CAP
- L2CAP connection-oriented channel (Bluetooth 4.1 feature)
- GAP features
  - Broadcaster, Observer, Peripheral, and Central roles
  - Security mode 1: Level 1, 2, and 3
  - User-defined advertising data
  - Multiple bond support

- GATT features

- GATT client and server
- Supports GATT sub-procedures
- 32-bit universally unique identifier (UUID) (Bluetooth 4.1 feature)

- Security Manager (SM)

- Pairing methods: Just works, Passkey Entry, and Out of Band
- LE Secure Connection Pairing model
- Authenticated man-in-the-middle (MITM) protection and data signing

- LL

- Master and slave roles
- 128-bit AES engine
- Low-duty cycle advertising
- LE Ping

- Supports all SIG-adopted BLE profiles

- Power levels for advertisement (1.28s, 32 bytes, 0 dBm) and Connection (300 ms, 0 byte, 0 dBm) are 42  $\mu$ W and 70  $\mu$ W respectively

## Analog Blocks

### 12-bit SAR ADC

The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to  $\pm 1\%$ ) and by providing the choice of three internal voltage references,  $V_{DD}$ ,  $V_{DD}/2$ , and  $V_{REF}$  (nominally 1.024 V), as well as an external reference through a GPIO pin. The sample and hold (S/H) aperture is programmable; it allows the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. System performance will be 65 dB for true 12-bit precision provided appropriate references are used and system noise levels permit it. To improve the performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an eight-input sequencer. The sequencer cycles through the selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is the buffering of each channel to reduce CPU interrupt-service requirements. To accommodate signals with varying source impedances and frequencies, it is possible to have different sample times programmable for each channel. Also, the signal range specification through a pair of range registers (low- and high-range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software. There are sixteen channels of which any thirteen can be sampled in a single scan.

The SAR is able to digitize the output of the on-chip temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 3.6 V.

#### *Temperature Sensor*

Part Number has an on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value by using a Cypress-supplied software that includes calibration and linearization.

#### *12-bit DAC*

There is a 12-bit voltage mode DAC on the chip, which can settle in less than 5  $\mu$ s. The DAC may be driven by the DMA controllers to generate user-defined waveforms. The DAC output from the chip can either be the resistive ladder output (highly linear near ground) or a buffered output.

#### *Continuous Time Block (CTB) with two Opamps*

This block consists of two opamps, which have their inputs and outputs connected to fixed pins and have three power modes and a comparator mode. The outputs of these opamps can be used as buffers for the SAR Inputs. The non-inverting inputs of these opamps can be connected to either of two pins, thus allowing independent sensors to be used at different times. The pin selection can be made via firmware. The opamps can be set to one of the four power levels; the lowest level allowing operation in Deep Sleep mode in order to preserve lower performance Continuous-Time functionality in Deep Sleep mode. The DAC output can be buffered through an opamp.

#### *Low-Power Comparators*

CYBLE-416045-02 has a pair of low-power comparators, which can also operate in Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during Deep Sleep and Hibernate modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wakeup circuit is activated by a comparator-switch event.

One of the low-power comparators (lpcomp1) has dedicated connections to minimize the signal path. lpcomp1 can also be routed to other I/Os via the analog mux bus, if needed.

The second low-power comparator (lpcomp0) has one dedicated connection exposed on the module (P5.6 – positive input); however, the negative input must be routed via the analog mux bus to an I/O.

### **Programmable Digital**

#### *Smart I/O*

There are two Smart I/O blocks, which allow Boolean operations on signals going to the GPIO pins from the subsystems of the chip or on signals coming into the chip. Operation can be synchronous or asynchronous and the blocks operate in low-power modes, such as Deep Sleep and Hibernate. This allows, for example, detection of logic conditions that can indicate that the CPU should wakeup instead of waking up on

general I/O interrupts, which consume more power and can generate spurious wakeups.

#### *Universal Digital Blocks (UDBs) and Port Interfaces*

The CYBLE-416045-02 has twelve UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control.

### **Fixed-Function Digital**

#### *Timer/Counter/PWM Block*

The timer/counter/PWM block consists of thirty-two counters with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow the use as deadband programmable complementary PWM outputs. It also has a kill input to force outputs to a predetermined state; for example, this is used in motor-drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention. There are eight 32-bit counters and twenty-four 16-bit counters.

#### *Serial Communication Blocks (SCB)*

CYBLE-416045-02 has five SCBs, which can each implement an I<sup>2</sup>C, UART, or SPI Interface. Two SCBs (SCB\_6 and SCB\_8) share the same pin connections and cannot be used at the same time. One of these SCBs (SCB\_8) will operate in Deep Sleep with an external clock, this SCB will only operate in Slave mode (requires external clock).

**I<sup>2</sup>C Mode:** The hardware I<sup>2</sup>C block implements a full multimaster and Slave Interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode plus) and has flexible buffering options to reduce the interrupt overhead and latency for the CPU. It also supports EZI<sup>2</sup>C that creates a mailbox address range in the memory of CYBLE-416045-02 and effectively reduces the I<sup>2</sup>C communication to reading from and writing to an array in the memory. In addition, the block supports a 256 byte-deep FIFO for receive and transmit, which, by increasing the time given for the CPU to read the data, greatly reduces the need for clock stretching caused by the CPU not having read the data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I<sup>2</sup>C peripheral is compatible with I<sup>2</sup>C Standard-mode, Fast-mode, and Fast-Mode Plus devices as defined in the NXP I<sup>2</sup>C-bus specification and user manual (UM10204). The I<sup>2</sup>C bus I/O is implemented with GPIO in open-drain modes.

**UART Mode:** This is a full-feature UART operating at up to 8 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break



detect, and frame error are supported. A 256 byte-deep FIFO allows much greater CPU service latencies to be tolerated.

**SPI Mode:** The SPI mode supports full Motorola SPI, TI Secure Simple Pairing (SSP) (essentially adds a start pulse that is used to synchronize SPI codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO and supports an EZSPI mode in which the data interchange is reduced to reading and writing an array in memory. The SPI Interface will operate with a 25-MHz SPI Clock.

## GPIO

CYBLE-416045-02 has up to thirty-six GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL)
- Hold mode for latching previous state (used for retaining the I/O state in Deep Sleep and Hibernate modes)
- Selectable slew rates for  $dV/dt$ -related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix (HSIOM) is used to multiplex between various signals that may connect to an I/O pin. Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an IRQ and ISR vector associated with it. Six GPIO pins are capable of over-voltage tolerant (OVT) operation where the input voltage may be higher than  $V_{DD}$  (these may be used for I<sup>2</sup>C functionality to allow powering the chip off while maintaining physical connection to an operating I<sup>2</sup>C bus without affecting its functionality).

GPIO pins can be ganged to sink 16 mA or higher values of sink current. GPIO pins, including OVT pins, may not be pulled-up higher than 3.6 V.

## Special-Function Peripherals

### CapSense

CapSense is supported on all pins in the CYBLE-416045-02 through a CapSense Sigma-Delta (CSD) block that can be connected to an analog multiplexed bus. Any GPIO pin can be connected to this AMUX bus through an analog switch. CapSense function can thus be provided on any pin or a group of pins in a system under software control. Cypress provides a software component for the CapSense block for ease-of-use.

Shield Voltage can be driven on another mux bus to provide water tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and ground to null out power-supply related noise.

The CapSense block has two 7-bit IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available). A (slow) 10-bit Slope ADC may be realized by using one of the IDACs.

The block can implement Swipe, Tap, Wake-on-Touch (< 3  $\mu$ A at 1.8 V), mutual capacitance, and other types of sensing functions.

### Audio Subsystem

This subsystem consists of an I<sup>2</sup>S block and two PDM channels. The PDM channels interface to a PDM microphone's bit-stream output. The PDM processing channel provides drop correction and can operate with clock speeds ranging from 384 kHz to 3.072 MHz and produce word lengths of 16 to 24 bits at audio sample rates of up to 48 ksps.

The I<sup>2</sup>S Interface supports both master and slave modes with Word Clock rates of up to 192 ksps (8-bit to 32-bit words).

## Module Overview

### Module Description

The CYBLE-416045-02 module is a complete module designed to be soldered to the main host board.

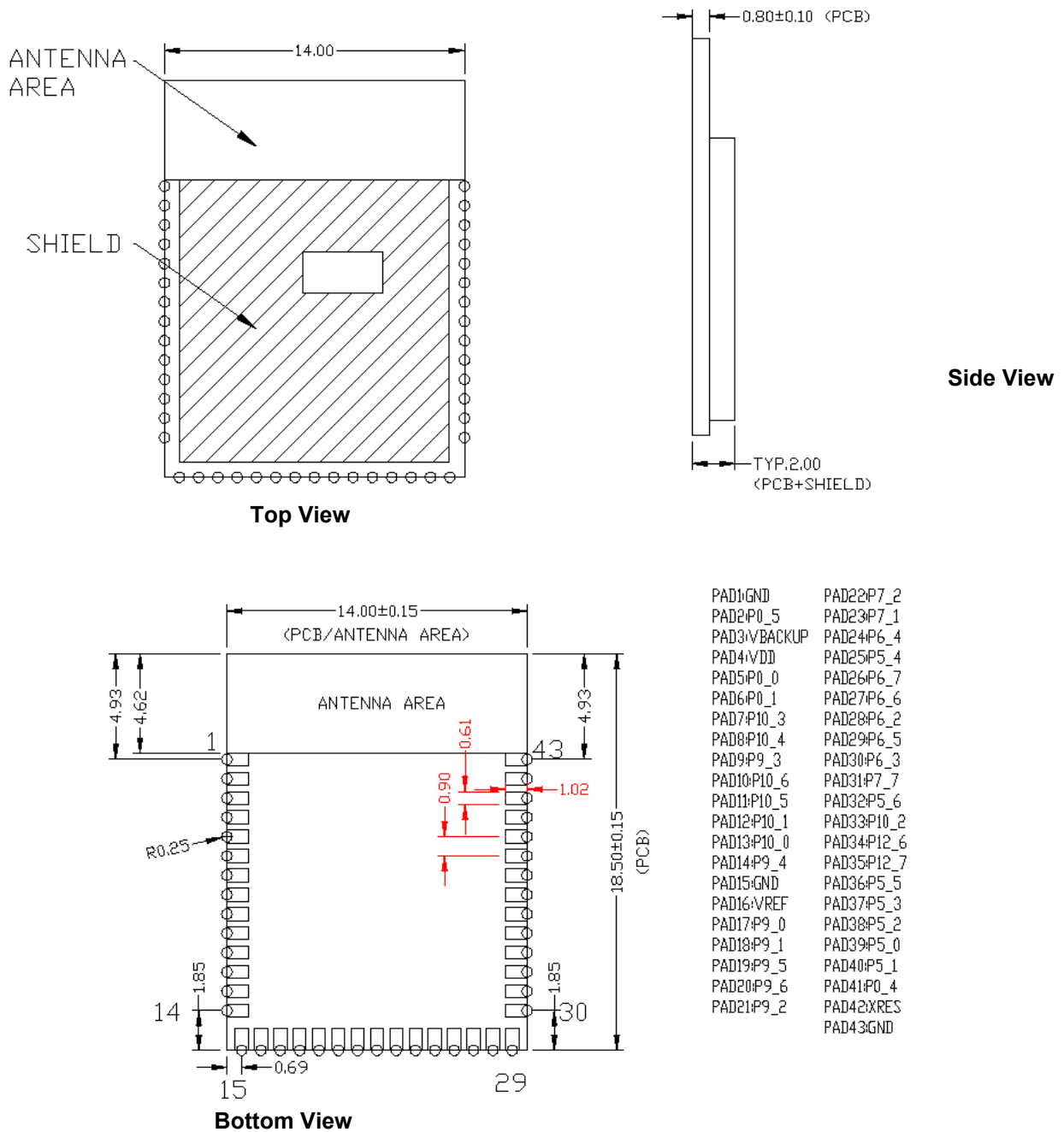
#### *Module Dimensions and Drawing*

Cypress reserves the right to select components (including the appropriate BLE device) from various vendors to achieve the BLE module functionality. Such selections will guarantee that all height restrictions of the component area are maintained. Designs should be completed with the physical dimensions shown in the mechanical drawings in [Figure 2](#). All dimensions are in millimeters (mm).

**Table 1. Module Design Dimensions**

| Dimension Item   |            | Specification            |
|--|------------|--------------------------|
| Module dimensions  | Length (X) | 14.00 ± 0.15 mm          |
|  | Width (Y)  | 18.50 ± 0.15 mm          |
| Antenna location dimensions                                    | Length (X) | 14.00 ± 0.15 mm          |
|  | Width (Y)  | 4.62 ± 0.15 mm           |
| PCB thickness  | Height (H) | 0.80 ± 0.10 mm           |
| Shield height  | Height (H) | 1.20 ± 0.10 mm           |
| Maximum component height                                       | Height (H) | 1.20 mm typical (shield) |
| Total module thickness (bottom of module to highest component) | Height (H) | 2.00 mm typical          |

See [Figure 2](#) on page 10 for the mechanical reference drawing for CYBLE-416045-02.

**Figure 2. Module Mechanical Drawing<sup>[1]</sup>**

**Note**

1. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see [Figure 4](#) on page 11, [Figure 5](#) and [Figure 6](#) on page 12, and [Figure 7](#) and [Table 3](#) on page 13.

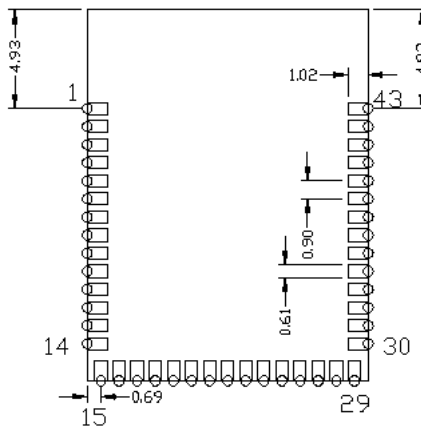
### Pad Connection Interface

As shown in the bottom view of [Figure 2](#) on page 10, the CYBLE-416045-02 connects to the host board via solder pads on the back of the module. [Table 2](#) and [Figure 3](#) detail the solder pad length, width, and pitch dimensions of the CYBLE-416045-02 module.

**Table 2. Solder Pad Connection Description**

| Name | Connections | Connection Type | Pad Length Dimension | Pad Width Dimension | Pad Pitch |
|------|-------------|-----------------|----------------------|---------------------|-----------|
| SP   | 43          | Solder Pads     | 1.02 mm              | 0.61 mm             | 0.90 mm   |

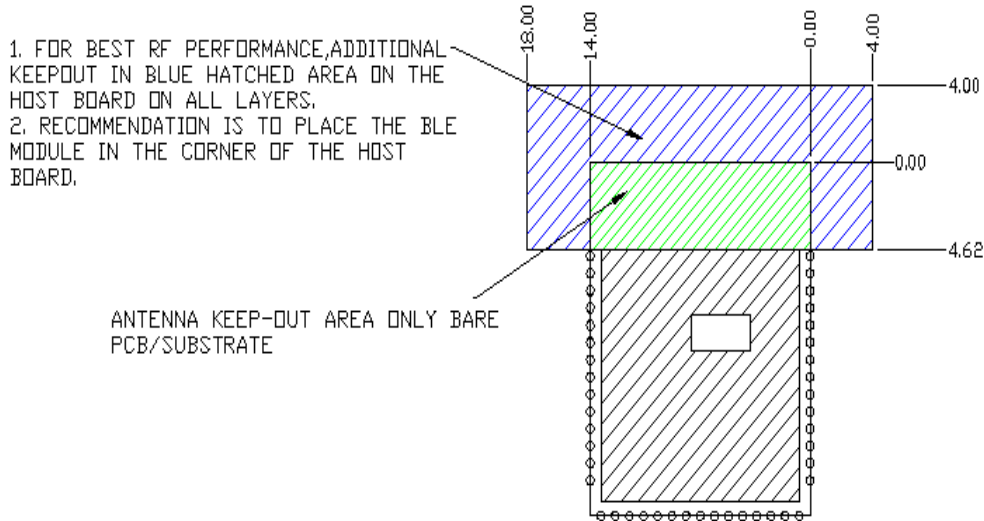
**Figure 3. Solder Pad Dimensions**



To maximize RF performance, the host layout should follow these recommendations:

1. The ideal placement of the Cypress BLE Module is in a corner of the host board with the antenna located on the edge of the host board. This placement minimizes the additional recommended keep-out area stated in item 2. Refer to [AN96841](#) for module placement best practices.
2. To maximize RF performance, the area immediately around the Cypress BLE Module trace antenna should contain an additional keep-out area, where no grounding or signal traces are contained. The keep-out area applies to all layers of the host board. The recommended dimensions of the host PCB keep-out area are shown in [Figure 4](#) (dimensions are in mm).

**Figure 4. Recommended Host PCB Keep-Out Area Around the CYBLE-416045-02 Trace Antenna**



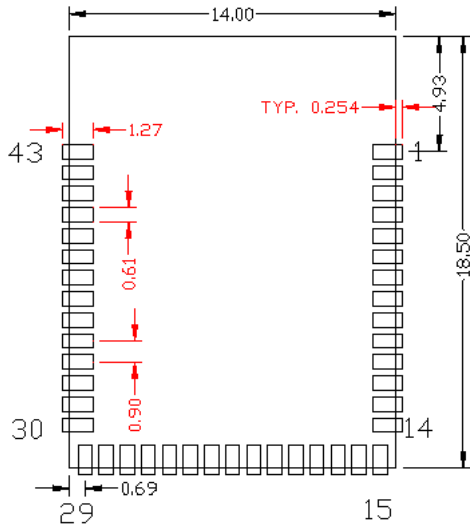
**Host PCB Keep-out area Around Trace Antenna**

### Recommended Host PCB Layout

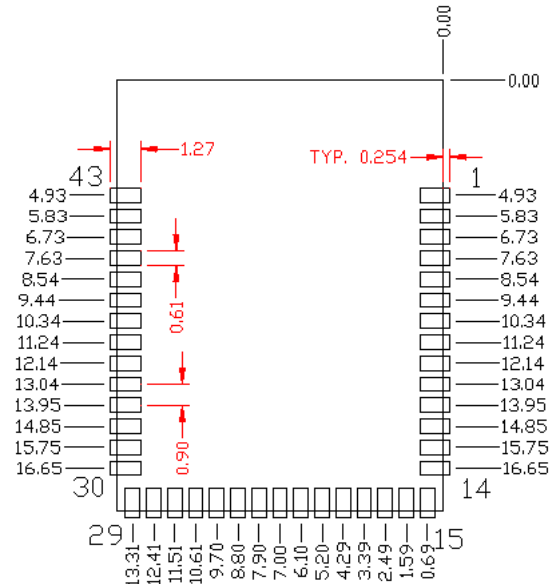
Figure 5 through Figure 7 and Table 3 provide details that can be used for the recommended host PCB layout pattern for the CYBLE-416045-02. Dimensions are in millimeters unless otherwise noted. Pad length of 0.99 mm (0.494 mm from center of the pad on either side) shown in Figure 7 is the minimum recommended host pad length. The host PCB layout pattern can be completed using either Figure 5, Figure 6, or Figure 7. It is not necessary to use all figures to complete the host PCB layout pattern.

**Figure 5. Host Layout Pattern for CYBLE-416045-02**

**Figure 6. Module Pad Location from Origin**



**Top View**



**Top View**

Table 3 provides the center location for each solder pad on the CYBLE-416045-02. All dimensions reference the to the center of the solder pad. Refer to Figure 7 for the location of each module solder pad.

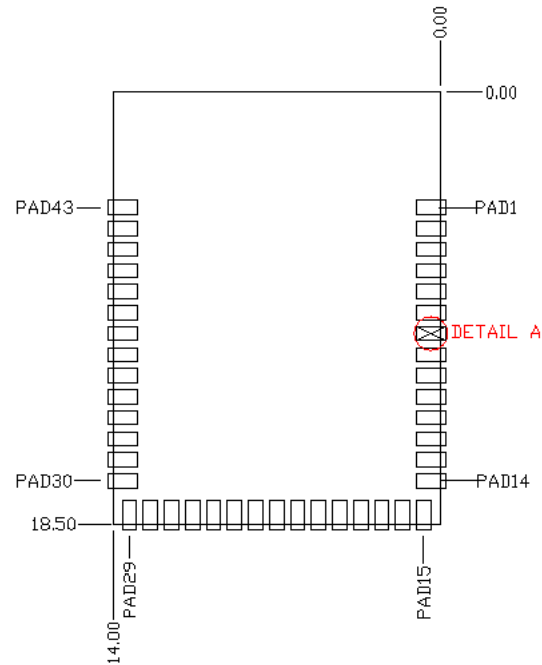
**Table 3. Module Solder Pad Location**

| Solder Pad (Center of Pad) | Location (X,Y) from Origin (mm) | Dimension from Origin (mils) |
|----------------------------|---------------------------------|------------------------------|
| 1                          | (0.38, 4.93)                    | (14.96, 194.09)              |
| 2                          | (0.38, 5.83)                    | (14.96, 229.53)              |
| 3                          | (0.38, 6.73)                    | (14.96, 264.96)              |
| 4                          | (0.38, 7.63)                    | (14.96, 300.39)              |
| 5                          | (0.38, 8.54)                    | (14.96, 336.22)              |
| 6                          | (0.38, 9.44)                    | (14.96, 371.65)              |
| 7                          | (0.38, 10.34)                   | (14.96, 407.09)              |
| 8                          | (0.38, 11.24)                   | (14.96, 442.52)              |
| 9                          | (0.38, 12.14)                   | (14.96, 477.95)              |
| 10                         | (0.38, 13.04)                   | (14.96, 513.38)              |
| 11                         | (0.38, 13.95)                   | (14.96, 549.21)              |
| 12                         | (0.38, 14.85)                   | (14.96, 584.64)              |
| 13                         | (0.38, 15.75)                   | (14.96, 620.08)              |
| 14                         | (0.38, 16.65)                   | (14.96, 655.51)              |
| 15                         | (0.69, 18.12)                   | (27.17, 713.38)              |
| 16                         | (1.59, 18.12)                   | (62.60, 713.38)              |
| 17                         | (2.49, 18.12)                   | (98.03, 713.38)              |
| 18                         | (3.39, 18.12)                   | (133.46, 713.38)             |
| 19                         | (4.29, 18.12)                   | (168.90, 713.38)             |
| 20                         | (5.20, 18.12)                   | (204.72, 713.38)             |
| 21                         | (6.10, 18.12)                   | (240.16, 713.38)             |
| 22                         | (7.00, 18.12)                   | (275.59, 713.38)             |
| 23                         | (7.90, 18.12)                   | (311.02, 713.38)             |
| 24                         | (8.80, 18.12)                   | (346.46, 713.38)             |
| 25                         | (9.70, 18.12)                   | (381.89, 713.38)             |
| 26                         | (10.61, 18.12)                  | (417.72, 713.38)             |
| 27                         | (11.51, 18.12)                  | (453.15, 713.38)             |
| 28                         | (12.41, 18.12)                  | (488.58, 713.38)             |
| 29                         | (13.31, 18.12)                  | (524.01, 713.38)             |
| 30                         | (13.62, 16.65)                  | (536.22, 655.51)             |
| 31                         | (13.62, 15.75)                  | (536.22, 620.08)             |
| 32                         | (13.62, 14.85)                  | (536.22, 584.64)             |
| 33                         | (13.62, 13.95)                  | (536.22, 549.21)             |
| 34                         | (13.62, 13.04)                  | (536.22, 513.38)             |
| 35                         | (13.62, 12.14)                  | (536.22, 477.95)             |
| 36                         | (13.62, 11.24)                  | (536.22, 442.52)             |
| 37                         | (13.62, 10.34)                  | (536.22, 407.09)             |
| 38                         | (13.62, 9.44)                   | (536.22, 371.65)             |
| 39                         | (13.62, 8.54)                   | (536.22, 336.22)             |
| 40                         | (13.62, 7.63)                   | (536.22, 300.39)             |

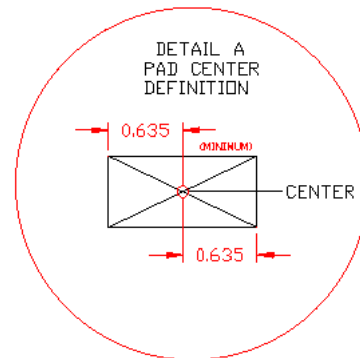
**Table 3. Module Solder Pad Location (continued)**

| Solder Pad (Center of Pad) | Location (X,Y) from Origin (mm) | Dimension from Origin (mils) |
|----------------------------|---------------------------------|------------------------------|
| 41                         | (13.62, 6.73)                   | (536.22, 264.96)             |
| 42                         | (13.62, 5.83)                   | (536.22, 229.53)             |
| 43                         | (13.62, 4.93)                   | (536.22, 194.09)             |

**Figure 7. Solder Pad Reference Location**



**Top View**



## Digital and Analog Capabilities and Connections

Table 4 and Table 5 detail the solder pad connection definitions and available functions for each connection pad. Table 4 lists the solder pads on CYBLE-416045-02, the BLE device port-pin, and denotes whether the digital function shown is available for each solder pad. Table 5 denotes whether the analog function shown is available for each solder pad. Each connection is configurable for a single option shown with a ✓.

**Table 4. Digital Peripheral Capabilities**

| Pad Number | Device Port Pin     | UART  | SPI          | I <sup>2</sup> C | TCPWM [2, 3]                                      | EXT_CLK_IN | Audio     | SWD/JTAG    | GPIO |
|------------|---------------------|---|--------------|------------------|---|------------|-----------|-------------|------|
| 1          | GND <sup>[4]</sup>  | Ground Connection                                     |              |                  |   |            |           |             |      |
| 2          | P0.5                | –   | –            | –                | tcpwm[0].line_compl[2]<br>tcpwm[1].line_compl[2]  | ✓          | –         | –           | ✓    |
| 3          | V <sub>BACKUP</sub> | Battery Backup Domain Input Voltage (1.71 V to 3.6 V) |              |                  |   |            |           |             |      |
| 4          | V <sub>DD</sub>     | Power Supply Input Voltage (1.71 V to 3.6 V)          |              |                  |   |            |           |             |      |
| 5          | P0.0                | –   | –            | –                | tcpwm[0].line[0]<br>tcpwm[1].line[0]              | ✓          | –         | –           | ✓    |
| 6          | P0.1                | –   | –            | –                | tcpwm[0].line_compl[0]<br>tcpwm[1].line_compl[0]  | –          | –         | ✓(JTAG RST) | ✓    |
| 7          | P10.3               | ✓(scb1_CTS)   | ✓(scb1_SS0)  | –                | tcpwm[0].line_compl[7]<br>tcpwm[1].line_compl[23] | –          | –         | –           | ✓    |
| 8          | P10.4               | –   | ✓(scb1_SS1)  | –                | tcpwm[0].line[0]<br>tcpwm[1].line[0]              | –          | ✓PDM_CLK  | –           | ✓    |
| 9          | P9.3                | ✓(scb2_CTS)   | ✓(scb2_SS0)  | –                | tcpwm[0].line_compl[5]<br>tcpwm[1].line_compl[21] | –          | –         | –           | ✓    |
| 10         | P10.6               | –   | ✓(scb1_SS3)  | –                | tcpwm[0].line[1]<br>tcpwm[1].line[2]              | –          | –         | –           | ✓    |
| 11         | P10.5               | –   | ✓(scb1_SS2)  | –                | tcpwm[0].line_compl[0]<br>tcpwm[1].line_compl[0]  | –          | ✓PDM_DATA | –           | ✓    |
| 12         | P10.1               | ✓(scb1_TX)  | ✓(scb1_MISO) | ✓(scb1_SDA)      | tcpwm[0].line_compl[6]<br>tcpwm[1].line_compl[22] | –          | –         | –           | ✓    |
| 13         | P10.0               | ✓(scb1_RX)  | ✓(scb1_MOSI) | ✓(scb1_SCL)      | tcpwm[0].line[6]<br>tcpwm[1].line[22]             | –          | –         | –           | ✓    |
| 14         | P9.4                | –   | ✓(scb2_SS1)  | –                | tcpwm[0].line[7]<br>tcpwm[1].line[0]              | –          | –         | –           | ✓    |
| 15         | GND                 | Ground Connection                                     |              |                  |   |            |           |             |      |
| 16         | V <sub>REF</sub>    | Voltage Reference Input (Optional)                    |              |                  |   |            |           |             |      |
| 17         | P9.0                | ✓(scb2_RX)  | ✓(scb2_MOSI) | ✓(scb2_SCL)      | tcpwm[0].line[4]<br>tcpwm[1].line[20]             | –          | –         | –           | ✓    |
| 18         | P9.1                | ✓(scb2_TX)  | ✓(scb2_MISO) | ✓(scb2_SDA)      | tcpwm[0].line_compl[4]<br>tcpwm[1].line_compl[20] | –          | –         | –           | ✓    |

**Table 4. Digital Peripheral Capabilities (continued)**

| Pad Number | Device Port Pin | UART        | SPI                         | I <sup>2</sup> C           | TCPWM [2, 3]                                      | EXT - CLK_IN | Audio                    | SWD/JTAG                 | GPIO |
|------------|-----------------|-------------|-----------------------------|----------------------------|---|--------------|--------------------------|--------------------------|------|
| 19         | P9.5            | –           | ✓(scb2_SS2)                 | –                          | tcpwm[0].line_compl[7]<br>tcpwm[1].line_compl[0]  | –            | –                        | –                        | ✓    |
| 20         | P9.6            | –           | ✓(scb2_SS3)                 | –                          | tcpwm[0].line[0]<br>tcpwm[1].line[1]              | –            | –                        | –                        | ✓    |
| 21         | P9.2            | ✓(scb2_RTS) | ✓(scb2_SCLK)                | –                          | tcpwm[0].line[5]<br>tcpwm[1].line[21]             | –            | –                        | –                        | ✓    |
| 22         | P7.2            | –           | –                           | –                          | tcpwm[0].line[5]<br>tcpwm[1].line[13]             | –            | –                        | –                        | ✓    |
| 23         | P7.1            | –           | –                           | –                          | tcpwm[0].line_compl[4]<br>tcpwm[1].line_compl[12] | –            | –                        | –                        | ✓    |
| 24         | P6.4            | ✓(scb6_RX)  | ✓(scb6_MOSI)<br>(scb8_MOSI) | ✓(scb8_SCL)<br>(scb6_SCL)  | tcpwm[0].line[2]<br>tcpwm[1].line[10]             | –            | –                        | ✓(JTAG TDO)              | ✓    |
| 25         | P5.4            | –           | ✓(scb5_SS1)                 | –                          | tcpwm[0].line[6]<br>tcpwm[1].line[6]              | –            | ✓I <sup>2</sup> S_SCK_RX | –                        | ✓    |
| 26         | P6.7            | ✓(scb6_CTS) | ✓(scb6_SS0)<br>(scb8_SS0)   | –                          | tcpwm[0].line_compl[3]<br>tcpwm[1].line_compl[11] | –            | –                        | ✓(SWDCLK)<br>(JTAG TCLK) | ✓    |
| 27         | P6.6            | ✓(scb6_RTS) | ✓(scb6_SCLK)<br>(scb8_SCLK) | –                          | tcpwm[0].line[3]<br>tcpwm[1].line[11]             | –            | –                        | ✓(SWDIO)<br>(JTAG TMS)   | ✓    |
| 28         | P6.2            |             | ✓(scb8_SCLK)                | –                          | tcpwm[0].line[1]<br>tcpwm[1].line[9]              | –            | –                        | –                        | ✓    |
| 29         | P6.5            | ✓(scb6_TX)  | ✓(scb6_MISO)<br>(scb8_MISO) | ✓(scb8_SDA)<br>✓(scb6_SDA) | tcpwm[0].line_compl[2]<br>tcpwm[1].line_compl[10] | –            | –                        | ✓(JTAG TDI)              | ✓    |
| 30         | P6.3            | –           | ✓(scb8_SS0)                 | –                          | tcpwm[0].line_compl[1]<br>tcpwm[1].line_compl[9]  | –            | –                        | –                        | ✓    |
| 31         | P7.7            | –           | –                           | –                          | tcpwm[0].line_compl[7]<br>tcpwm[1].line_compl[15] | –            | –                        | –                        | ✓    |
| 32         | P5.6            | –           | ✓(scb5_SS3)                 | –                          | tcpwm[0].line[7]<br>tcpwm[1].line[7]              | –            | ✓I <sup>2</sup> S_SDI_RX | –                        | ✓    |
| 33         | P10.2           | ✓(scb1_RTS) | ✓(scb1_SCLK)                | –                          | tcpwm[0].line[7]<br>tcpwm[1].line[23]             | –            | –                        | –                        | ✓    |
| 34         | P12.6           | –           | ✓(scb6_SS3)                 | –                          | tcpwm[0].line[7]<br>tcpwm[1].line[7]              | –            | –                        | –                        | ✓    |
| 35         | P12.7           | –           | –                           | –                          | tcpwm[0].line_compl[7]<br>tcpwm[1].line_compl[7]  | –            | –                        | –                        | ✓    |
| 36         | P5.5            | –           | ✓(scb5_SS2)                 | –                          | tcpwm[0].line_compl[6]<br>tcpwm[1].line_compl[6]  | –            | ✓I <sup>2</sup> S_WS_RX  | –                        | ✓    |
| 37         | P5.3            | ✓(scb5_CTS) | ✓(scb5_SS0)                 | –                          | cpwm[0].line_compl[5]<br>tcpwm[1].line_compl[5]   | –            | ✓I <sup>2</sup> S_SDO_TX | –                        | ✓    |



**Table 4. Digital Peripheral Capabilities** (continued)

| Pad Number | Device Port Pin    | UART                        | SPI          | I <sup>2</sup> C | TCPWM [2, 3]                                     | EXT -<br>CLK_IN | Audio             | SWD/JTAG | GPIO |
|------------|--------------------|-----------------------------|--------------|------------------|--|-----------------|-------------------|----------|------|
| 38         | P5.2               | ✓(scb5_RTS)                 | ✓(scb5_SCLK) | –                | tcpwm[0].line[5]<br>tcpwm[1].line[5]             | –               | ✓I2S_WS_TX        | –        | ✓    |
| 39         | P5.0               | ✓(scb5_RX)                  | ✓(scb5_MOSI) | ✓(scb5_SCL)      | tcpwm[0].line[4]<br>tcpwm[1].line[4]             | –               | ✓I2S_EX-<br>T_CLK | –        | ✓    |
| 40         | P5.1               | ✓(scb5_TX)                  | ✓(scb5_MISO) | ✓(scb5_SDA)      | tcpwm[0].line_compl[4]<br>tcpwm[1].line_compl[4] | –               | ✓I2S_CLK_TX       | –        | ✓    |
| 41         | P0.4               | –                           | –            | –                | tcpwm[0].line[2]<br>tcpwm[1].line[2]             | –               | –                 | –        | ✓    |
| 42         | XRES               | External Reset (Active Low) |              |                  |  |                 |                   |          |      |
| 43         | GND <sup>[4]</sup> | Ground Connection           |              |                  |  |                 |                   |          |      |

**Notes**

2. TCPWM stands for timer, counter, and PWM. If supported, the pad can be configured to any of these peripheral functions.
3. TCPWM connections on ports 0, 1, 2, and 3 can be routed through the Digital Signal Interconnect (DSI) to any of the TCPWM blocks and can be either positive or negative polarity.
4. The main board needs to connect both GND connections (Pad 1 and Pad 32) on the module to the common ground of the system.

**Table 5. Additional Analog and Digital Capabilities**

| Pad Number | Device Port Pin     | Analog Functionality                                  | Universal Digital Block (UDB) | CapSense | Smart IO     |
|------------|---------------------|---|-------------------------------|----------|--------------|
| 1          | GND                 | Ground Connection                                     |                               |          |              |
| 2          | P0.5                | –   | ✓                             | ✓        | –            |
| 3          | V <sub>BACKUP</sub> | Battery Backup Domain Input Voltage (1.71 V to 3.6 V) |                               |          |              |
| 4          | VDD                 | Power Supply Input Voltage (1.71 V to 3.6 V)          |                               |          |              |
| 5          | P0.0                | wco_in  | ✓                             | ✓        | –            |
| 6          | P0.1                | wco_out   | ✓                             | ✓        | –            |
| 7          | P10.3               | sarmux[3]   | ✓                             | ✓        | –            |
| 8          | P10.4               | sarmux[4]   | ✓                             | ✓        | –            |
| 9          | P9.3                | ctb_oa1_out   | ✓                             | ✓        | SMARTIO10[3] |
| 10         | P10.6               | sarmux[6]   | ✓                             | ✓        | –            |
| 11         | P10.5               | sarmux[5]   | ✓                             | ✓        | –            |
| 12         | P10.1               | sarmux[1]   | ✓                             | ✓        | –            |
| 13         | P10.0               | sarmux[0]   | ✓                             | ✓        | –            |
| 14         | P9.4                | ctb_oa1-  | ✓                             | ✓        | SMARTIO9[4]  |
| 15         | GND                 | Ground Connection                                     |                               |          |              |
| 16         | V <sub>REF</sub>    | Reference Voltage Input (Optional)                    |                               |          |              |
| 17         | P9.0                | ctb_oa0+  | ✓                             | ✓        | SMARTIO9[0]  |
| 18         | P9.1                | ctb_oa0-  | ✓                             | ✓        | SMARTIO9[1]  |
| 19         | P9.5                | ctb_oa1+  | ✓                             | ✓        | SMARTIO9[5]  |
| 20         | P9.6                | ctb_oa0+  | ✓                             | ✓        | SMARTIO9[6]  |
| 21         | P9.2                | ctb_oa0_out   | ✓                             | ✓        | SMARTIO9[2]  |
| 22         | P7.2                | csd.csh_tankpadd<br>csd.csh_tankpads                  | ✓                             | ✓        | –            |
| 23         | P7.1                | csd.cmodpadd<br>csd.cmodpads                          | ✓                             | ✓        | –            |
| 24         | P6.4                | –   | ✓                             | ✓        | –            |
| 25         | P5.4                | –   | ✓                             | ✓        | –            |
| 26         | P6.7                | –   | ✓                             | ✓        | –            |
| 27         | P6.6                | –   | ✓                             | ✓        | –            |
| 28         | P6.2                | lpcomp.inp_comp1                                      | ✓                             | ✓        | –            |
| 29         | P6.5                | –   | ✓                             | ✓        | –            |
| 30         | P6.3                | lpcomp.inn_comp1                                      | ✓                             | ✓        | –            |
| 31         | P7.7                | csd.cshieldpads                                       | ✓                             | ✓        | –            |
| 32         | P5.6                | lpcomp.inp_comp0                                      | ✓                             | ✓        | –            |
| 33         | P10.2               | sarmux[2]   | ✓                             | ✓        | –            |
| 34         | P12.6               | –   | ✓                             | ✓        | –            |
| 35         | P12.7               | –   | ✓                             | ✓        | –            |
| 36         | P5.5                | –   | ✓                             | ✓        | –            |
| 37         | P5.3                | –   | ✓                             | ✓        | –            |
| 38         | P5.2                | –   | ✓                             | ✓        | –            |
| 39         | P5.0                | –   | ✓                             | ✓        | –            |
| 40         | P5.1                | –   | ✓                             | ✓        | –            |
| 41         | P0.4                | –   | ✓                             | ✓        | –            |
| 42         | XRES                | External Reset (Active Low)                           |                               |          |              |
| 43         | GND                 | Ground Connection                                     |                               |          |              |

## Power

The power connection diagram (see [Figure 8](#)) shows the general requirements for power pins on the CYBLE-416045-02. The CYBLE-416045-02 contains a single power supply connection ( $V_{DD}$ ) and a backup voltage input ( $V_{BACKUP}$ ).

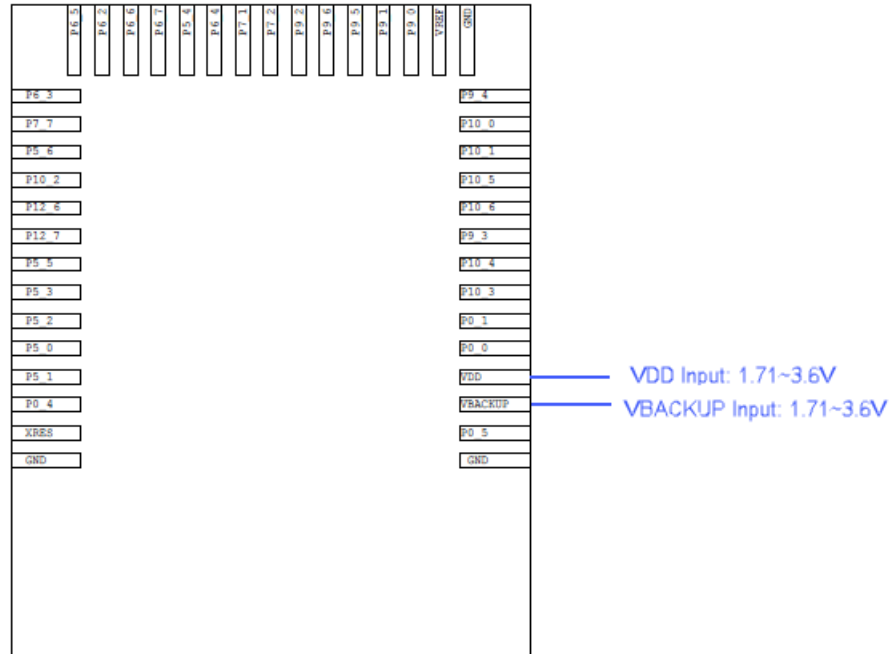
Description of the power pins is as follows:

- $V_{BACKUP}$  is the supply to the backup domain. The backup domain includes the 32-kHz WCO, real-time clock (RTC), and backup registers. It can generate a wakeup interrupt to the chip via the RTC timers or an external input. It can also generate an output to wakeup external circuitry. It is connected to VDD when not used as a separate battery backup domain.  $V_{BACKUP}$  provides the supply for Port 0.
- $V_{DD}$  is the main power supply input (1.71 V to 3.6 V). It provides the power input to the digital, analog, and radio domains. Isolation required for these domains is integrated on-module; therefore, no additional isolation is required for the CYBLE-416045-02.

The supply voltage range is 1.71 to 3.6 V with all functions and circuits operating over that range. All ground connections specified must be connected to system ground.

$V_{DD}$  and  $V_{BACKUP}$  may be shorted together externally. They are not required to be separate input voltages.

**Figure 8. CYBLE-416045-02 Power Connections**



### 32-kHz Crystal Oscillator

The CYBLE-416045-02 includes connections for a 32-kHz oscillator to provide accurate timing during low-power operations. Figure 9 shows the 32-kHz XTAL oscillator with external components and Table 6 lists the oscillators characteristics. This oscillator can be operated with a 32-kHz or 32.768-kHz crystal oscillator, or be driven with a clock input at similar frequency. The XTAL must have an accuracy of  $\pm 250$  ppm or better according to the BLE specification over temperature and including aging. The values for C1 and C2 are used to fine-tune the oscillator. The external 32-kHz XTAL is optional, and the precision internal low-speed oscillator (PIL0) can be used if precise timing is not required. Precise timing will improve overall system power consumption, as shown in Table 11.

Figure 9. 32-kHz Oscillator Block Diagram

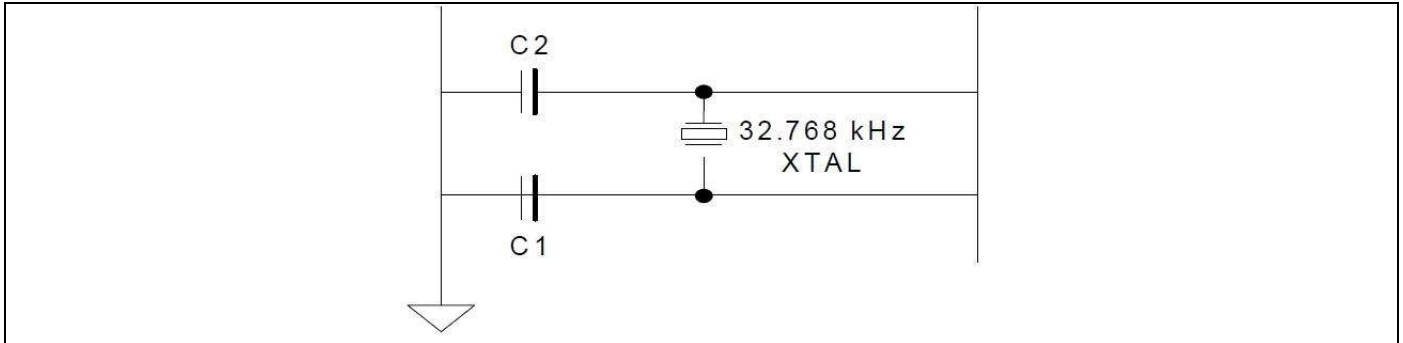
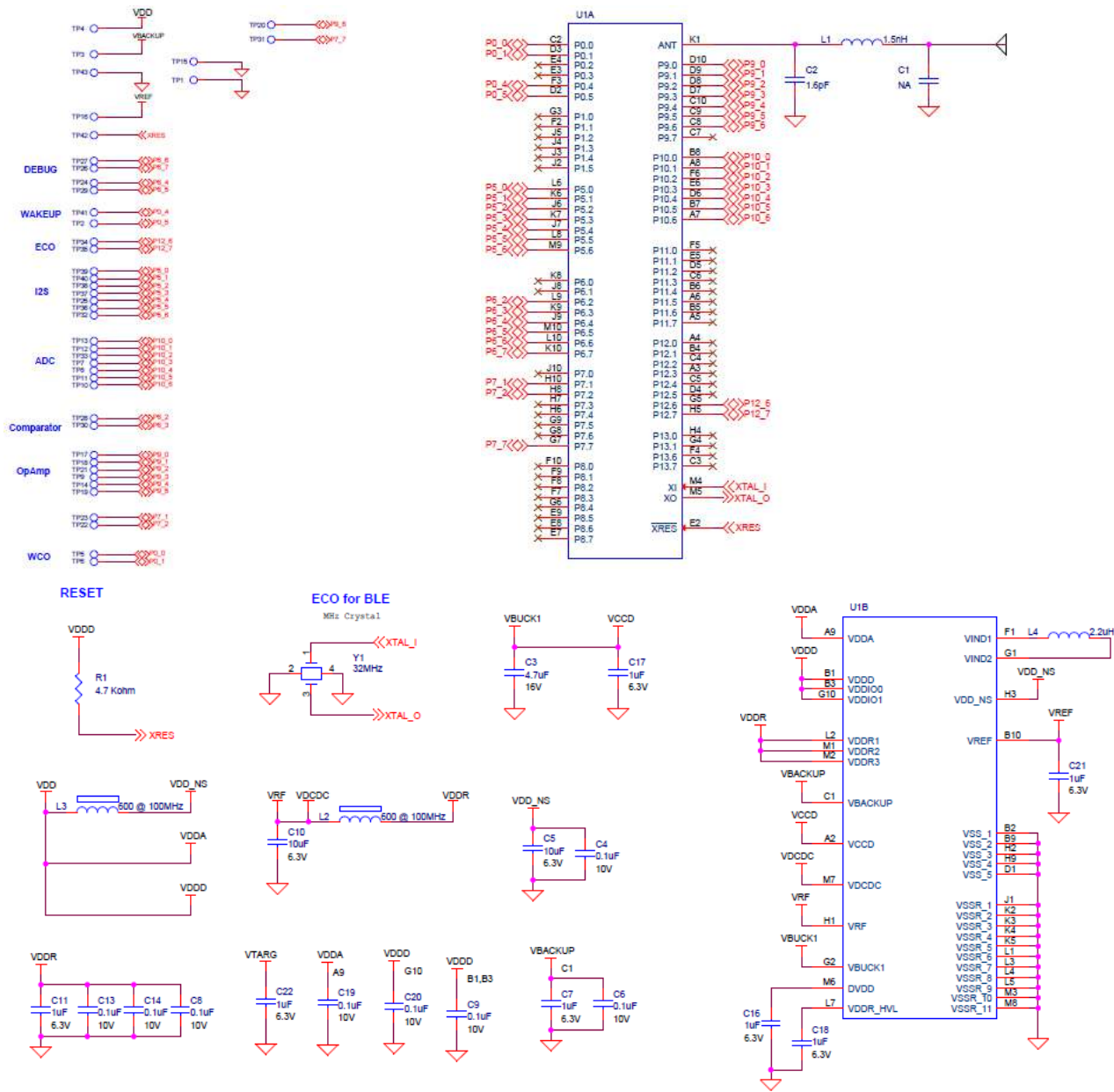


Table 6. XTAL Oscillator Characteristics

| Parameter   | Description                  | Minimum | Typical | Maximum | Unit       | Details/Conditions |
|-------------|------------------------------|---------|---------|---------|------------|--------------------|
| $F_{WCO}$   | Crystal frequency            | –       | 32.768  | –       | kHz        |                    |
| $F_{TOL}$   | Frequency tolerance          | –       | 50      | –       | ppm        |                    |
| ESR         | Equivalent series resistance | –       | 70      | –       | k $\Omega$ |                    |
| PD          | Drive level                  | –       | –       | 1       | $\mu$ W    |                    |
| $T_{START}$ | Startup time                 | –       | –       | 500     | ms         |                    |
| $C_L$       | Crystal load capacitance     | 6       | –       | 12.5    | pF         |                    |
| $C_0$       | Crystal shunt capacitance    | –       | 1.35    | –       | pF         |                    |

The CYBLE-416045-02 schematic is shown in Figure 10.

Figure 10. CYBLE-416045-02 Schematic Diagram



## Critical Components List

Table 7 details the critical components used in the CYBLE-416045-02 module.

**Table 7. Critical Component List**

| Component | Reference Designator | Description   |
|-----------|----------------------|---|
| Silicon   | U1                   | 116-pin BGA Programmable System-on-Chip (PSoC 6) with BLE |
| Crystal   | Y1                   | 32.000 MHz, 10 PF   |

## Antenna Design

Table 8 details the PCB trace antenna used on the CYBLE-416045-02 module.

**Table 8. Trace Antenna Specifications**

| Item            | Description      |
|-----------------|------------------|
| Frequency Range | 2400 – 2500 MHz  |
| Peak Gain       | -0.5 dBi typical |
| Return Loss     | 10 dB minimum    |

## Electrical Specification

Table 9 details the absolute maximum electrical characteristics for the Cypress BLE Module.

**Table 9. CYBLE-416045-02 Absolute Maximum Ratings<sup>[5]</sup>**

| Parameter                   | Description   | Min  | Typ | Max                  | Unit | Details/Conditions                                     |
|-----------------------------|---|------|-----|----------------------|------|--|
| V <sub>DDD_ABS</sub>        | V <sub>DD</sub> , V <sub>DDA</sub> , and V <sub>DDR</sub> supply relative to V <sub>SS</sub> (V <sub>SSD</sub> = V <sub>SSA</sub> ) | -0.5 | -   | 4                    | V    | Absolute maximum                                       |
| V <sub>CCD_ABS</sub>        | Direct digital core voltage input relative to V <sub>SSD</sub>  | -0.5 | -   | 1.2                  | V    | Absolute maximum                                       |
| V <sub>DDD_RIPPLE</sub>     | Maximum power supply ripple for V <sub>DD</sub> , V <sub>DDA</sub> , and V <sub>DDR</sub> input voltage                             | -    | -   | 100                  | mV   | 3.0 V supply<br>Ripple frequency of 100 kHz to 750 kHz |
| V <sub>GPIO_ABS</sub>       | GPIO voltage  | -0.5 | -   | V <sub>DD</sub> +0.5 | V    | Absolute maximum                                       |
| I <sub>GPIO_ABS</sub>       | Maximum current per GPIO  | -25  | -   | 25                   | mA   | Absolute maximum                                       |
| I <sub>GPIO_injection</sub> | GPIO injection current per pin  | -0.5 | -   | 0.5                  | mA   | Absolute maximum current injected per pin              |
| LU                          | Pin current for latch up  | -100 |     | 100                  | mA   | Absolute maximum                                       |

### Device-Level Specifications

All specifications are valid for -40 °C ≤ TA ≤ 85 °C and for 1.71 V to 3.6 V except where noted.

**Table 10. Power Supply Range, CPU Current, and Transition Time Specifications**

| Parameter  | Description  | Min  | Typ | Max  | Unit | Details/Conditions                                  |
|--|--|------|-----|------|------|---|
| <b>DC Specifications</b>   |  |      |     |      |      |   |
| V <sub>DDD</sub>   | Internal regulator and Port 1 GPIO supply  | 1.71 | -   | 3.6  | V    | -   |
| V <sub>DDA</sub>   | Analog power supply voltage. Shorted to V <sub>DDIOA</sub> on PCB                    | 1.71 | -   | 3.6  | V    | Internally unregulated supply                       |
| V <sub>DDIO1</sub>   | GPIO supply for Ports 5 to 8 when present  | 1.71 | -   | 3.6  | V    | V <sub>DDIO_1</sub> must be ≥ to V <sub>DDA</sub> . |
| V <sub>DDIO0</sub>   | GPIO supply for Ports 11 to 13 when present  | 1.71 | -   | 3.6  | V    |   |
| V <sub>DDIO0</sub>   | Supply for eFuse programming   | 2.38 | 2.5 | 2.62 | V    | eFuse programming voltage                           |
| V <sub>DDIOR</sub>   | GPIO supply for Ports 2 to 4 on BGA 124 only   | 1.71 | -   | 3.6  | V    | -   |
| V <sub>DDIOA</sub>   | GPIO supply for Ports 9 to 10. Shorted to V <sub>DDA</sub> on PCB                    | 1.71 | -   | 3.6  | V    | -   |
| V <sub>BACKUP</sub>  | Backup power and GPIO Port 0 supply when present                                     | 1.71 | -   | 3.6  | V    | Minimum is 1.4 V in Backup mode                     |
| V <sub>CCD1</sub>  | Output voltage (for core logic bypass)   | -    | 1.1 | -    | V    | High-speed mode                                     |
| V <sub>CCD2</sub>  | Output voltage (for core logic bypass)   | -    | 0.9 | -    |      | ULP mode. Valid for -20 to 85 °C                    |
| C <sub>EFC</sub>   | External regulator voltage (V <sub>CCD</sub> ) bypass                                | 3.8  | 4.7 | 5.6  | μF   | X5R ceramic or better                               |
| C <sub>EXC</sub>   | Power supply decoupling capacitor  | -    | 10  | -    | μF   | X5R ceramic or better                               |
| <b>LP Range Power Specifications (for V<sub>CCD</sub> = 1.1 V with Buck and LDO)</b> |  |      |     |      |      |   |
| <b>Cortex-M4 - Active Mode</b>   |  |      |     |      |      |   |
| <b>Execute with Cache Disabled (Flash)</b>   |  |      |     |      |      |   |
| I <sub>DD1</sub>   | Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO and FLL. While(1) | -    | 2.3 | 3.2  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C     |
|  |  | -    | 3.1 | 3.6  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C     |
|  |  | -    | 4.2 | 5.1  |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60 °C  |
| I <sub>DD2</sub>   | Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While(1)           | -    | 0.9 | 1.5  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C     |
|  |  | -    | 1.2 | 1.6  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C     |
|  |  | -    | 1.6 | 2.4  |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60 °C  |

#### Note

- Usage above the absolute maximum conditions listed in Table 9 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

**Table 10. Power Supply Range, CPU Current, and Transition Time Specifications (continued)**

| Parameter                                  | Description  | Min | Typ  | Max  | Unit | Details/Conditions                                 |
|--|--|-----|------|------|------|--|
| <b>Execute with Cache Enabled</b>          |  |     |      |      |      |  |
| I <sub>DD3</sub>                           | Execute from Cache; CM4 Active 150 MHz, CM0+ Sleep 75 MHz. IMO and FLL. Dhrystone  | –   | 6.3  | 7    | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|  |  | –   | 9.7  | 11.2 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
|  |  | –   | 13.2 | 13.7 |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60 °C |
| I <sub>DD4</sub>                           | Execute from Cache; CM4 Active 100 MHz, CM0+ Sleep 100 MHz. IMO and FLL. Dhrystone | –   | 4.8  | 5.8  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|  |  | –   | 7.4  | 8.4  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
|  |  | –   | 10.1 | 10.7 |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60 °C |
| I <sub>DD5</sub>                           | Execute from Cache; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. IMO and FLL. Dhrystone   | –   | 2.4  | 3.4  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|  |  | –   | 3.7  | 4.1  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
|  |  | –   | 5.1  | 5.8  |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60 °C |
| I <sub>DD6</sub>                           | Execute from Cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. IMO. Dhrystone             | –   | 0.90 | 1.5  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|  |  | –   | 1.27 | 1.75 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
|  |  | –   | 1.8  | 2.6  |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60 °C |
| <b>Cortex-M0+. Active Mode</b>             |  |     |      |      |      |  |
| <b>Execute with Cache Disabled (Flash)</b> |  |     |      |      |      |  |
| I <sub>DD7</sub>                           | Execute from Flash; CM4 OFF, CM0+ Active 50 MHz. With IMO and FLL. While (1).      | –   | 2.4  | 3.3  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|  |  | –   | 3.2  | 3.7  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
|  |  | –   | 4.1  | 4.8  |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60 °C |
| I <sub>DD8</sub>                           | Execute from Flash; CM4 OFF, CM0+ Active 8 MHz. With IMO. While (1)                | –   | 0.8  | 1.5  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|  |  | –   | 1.1  | 1.6  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
|  |  | –   | 1.45 | 1.9  |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60 °C |
| <b>Execute with Cache Enabled</b>          |  |     |      |      |      |  |
| I <sub>DD9</sub>                           | Execute from Cache; CM4 OFF, CM0+ Active 100 MHz. With IMO and FLL. Dhrystone      | –   | 3.8  | 4.5  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|  |  | –   | 5.9  | 6.5  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
|  |  | –   | 7.7  | 8.2  |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60 °C |
| I <sub>DD10</sub>                          | Execute from Cache; CM4 OFF, CM0+ Active 8 MHz. With IMO. Dhrystone                | –   | 0.80 | 1.3  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|  |  | –   | 1.2  | 1.7  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
|  |  | –   | 1.41 | 2    |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60 °C |
| <b>Cortex-M4. Sleep Mode</b>               |  |     |      |      |      |  |
| I <sub>DD11</sub>                          | CM4 Sleep 100 MHz, CM0+ Sleep 25 MHz. With IMO and FLL                             | –   | 1.5  | 2.2  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|  |  | –   | 2.2  | 2.7  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
|  |  | –   | 2.9  | 3.5  |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60 °C |
| I <sub>DD12</sub>                          | CM4 Sleep 50 MHz, CM0+ Sleep 25 MHz. With IMO and FLL                              | –   | 1.20 | 1.9  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|  |  | –   | 1.70 | 2.2  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
|  |  | –   | 2.20 | 2.8  |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60 °C |
| I <sub>DD13</sub>                          | CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO  | –   | 0.7  | 1.3  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|  |  | –   | 0.96 | 1.5  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
|  |  | –   | 1.22 | 2    |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60 °C |
| <b>Cortex-M0+. Sleep Mode</b>              |  |     |      |      |      |  |
| I <sub>DD14</sub>                          | CM4 Off, CM0+ Sleep 50 MHz. With IMO and FLL                                       | –   | 1.3  | 2    | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|  |  | –   | 1.94 | 2.4  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
|  |  | –   | 2.57 | 3.2  |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60 °C |
| I <sub>DD15</sub>                          | CM4 Off, CM0+ Sleep 8 MHz. With IMO  | –   | 0.7  | 1.3  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|  |  | –   | 0.95 | 1.5  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
|  |  | –   | 1.25 | 2    |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60 °C |



**Table 10. Power Supply Range, CPU Current, and Transition Time Specifications (continued)**

| Parameter   | Description   | Min | Typ  | Max  | Unit | Details/Conditions                                 |
|---|---|-----|------|------|------|--|
| <b>Cortex-M4. Low-Power Active (LPA) Mode</b>   |   |     |      |      |      |  |
| I <sub>DD16</sub>   | Execute from Flash; CM4 LPA 8 MHz, CM0+ Sleep 8 MHz. With IMO. While (1)              | –   | 0.85 | 1.5  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|   |   | –   | 1.18 | 1.65 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
|   |   | –   | 1.63 | 2.4  |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60 °C |
| I <sub>DD17</sub>   | Execute from Cache; CM4 LPA 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone              | –   | 0.90 | 1.5  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|   |   | –   | 1.27 | 1.75 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
|   |   | –   | 1.77 | 2.5  |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60 °C |
| <b>Cortex-M0+. Low-Power Active (LPA) Mode</b>  |   |     |      |      |      |  |
| I <sub>DD18</sub>   | Execute from Flash; CM4 Off, CM0+ LPA 8 MHz. With IMO. While (1)                      | –   | 0.8  | 1.4  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|   |   | –   | 1.14 | 1.6  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
|   |   | –   | 1.6  | 2.4  |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60 °C |
| I <sub>DD19</sub>   | Execute from Cache; CM4 Off, CM0+ LPA 8 MHz. With IMO. Dhrystone                      | –   | 0.8  | 1.4  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|   |   | –   | 1.15 | 1.65 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
|   |   | –   | 1.62 | 2.4  |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60 °C |
| <b>Cortex-M4. Low-Power Sleep (LPS) Mode</b>  |   |     |      |      |      |  |
| I <sub>DD20</sub>   | CM4 LPS 8 MHz, CM0+ LPS 8 MHz. With IMO   | –   | 0.65 | 1.1  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|   |   | –   | 0.95 | 1.5  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
|   |   | –   | 1.31 | 2.1  |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60 °C |
| <b>Cortex-M0+. Low-Power Sleep (LPS) Mode</b>   |   |     |      |      |      |  |
| I <sub>DD22</sub>   | CM4 OFF, CM0+ LPS 8 MHz. With IMO   | –   | 0.64 | 1.1  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|   |   | –   | 0.93 | 1.45 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
|   |   | –   | 1.29 | 2    |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60 °C |
| <b>ULP Range Power Specifications (for V<sub>CCD</sub> = 0.9 V using the Buck). ULP Mode is valid from -20 to +85 °C.</b> |   |     |      |      |      |  |
| <b>Cortex-M4. Active Mode</b>   |   |     |      |      |      |  |
| <b>Execute with Cache Disabled (Flash)</b>  |   |     |      |      |      |  |
| I <sub>DD3</sub>  | Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO and FLL. While(1)  | –   | 1.7  | 2.2  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|   |   | –   | 2.1  | 2.4  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
| I <sub>DD4</sub>  | Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While (1)           | –   | 0.56 | 0.8  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|   |   | –   | 0.75 | 1    |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
| <b>Execute with Cache Enabled</b>   |   |     |      |      |      |  |
| I <sub>DD10</sub>   | Execute from Cache; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO and FLL. Dhrystone | –   | 1.6  | 2.2  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|   |   | –   | 2.4  | 2.7  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
| I <sub>DD11</sub>   | Execute from Cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone           | –   | 0.65 | 0.8  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|   |   | –   | 0.8  | 1.1  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
| <b>Cortex-M0+. Active Mode</b>  |   |     |      |      |      |  |
| <b>Execute with Cache Disabled (Flash)</b>  |   |     |      |      |      |  |
| I <sub>DD16</sub>   | Execute from Flash; CM4 Off, CM0+ Active 25 MHz. With IMO and FLL. Write(1)           | –   | 1.00 | 1.4  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|   |   | –   | 1.34 | 1.6  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
| I <sub>DD17</sub>   | Execute from Flash; CM4 Off, CM0+ Active 8 MHz. With IMO. While(1)                    | –   | 0.54 | 0.75 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|   |   | –   | 0.73 | 1    |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
| <b>Execute with Cache Enabled</b>   |   |     |      |      |      |  |
| I <sub>DD18</sub>   | Execute from Cache; CM4 Off, CM0+ Active 25 MHz. With IMO and FLL. Dhrystone          | –   | 0.91 | 1.25 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|   |   | –   | 1.34 | 1.6  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |
| I <sub>DD19</sub>   | Execute from Cache; CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone                   | –   | 0.51 | 0.72 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C    |
|   |   | –   | 0.73 | 0.95 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C    |

**Table 10. Power Supply Range, CPU Current, and Transition Time Specifications (continued)**

| Parameter   | Description  | Min | Typ  | Max  | Unit | Details/Conditions                              |
|---|--|-----|------|------|------|---|
| <b>Cortex-M4. Sleep Mode</b>                          |  |     |      |      |      |   |
| I <sub>DD21</sub>                                     | CM4 Sleep 50 MHz, CM0+ Sleep 25 MHz. With IMO and FLL                    | –   | 0.76 | 1.1  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C |
|   |  | –   | 1.1  | 1.4  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C |
| I <sub>DD22</sub>                                     | CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO                              | –   | 0.42 | 0.65 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C |
|   |  | –   | 0.59 | 0.8  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C |
| <b>Cortex-M0+. Sleep Mode</b>                         |  |     |      |      |      |   |
| I <sub>DD23</sub>                                     | CM4 Off, CM0+ Sleep 25 MHz. With IMO and FLL                             | –   | 0.62 | 0.9  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C |
|   |  | –   | 0.88 | 1.1  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C |
| I <sub>DD24</sub>                                     | CM4 Off, CM0+ Sleep 8 MHz. With IMO                                      | –   | 0.41 | 0.6  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C |
|   |  | –   | 0.58 | 0.8  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C |
| <b>Cortex-M4. Ultra Low-Power Active (ULPA) Mode</b>  |  |     |      |      |      |   |
| I <sub>DD25</sub>                                     | Execute from Flash. CM4 ULPA 8 MHz, CM0+ ULPS 8 MHz. With IMO. While(1)  | –   | 0.52 | 0.75 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C |
|   |  | –   | 0.76 | 1    |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C |
| I <sub>DD26</sub>                                     | Execute from Cache. CM4 ULPA 8 MHz, CM0+ ULPS 8 MHz. With IMO. Dhrystone | –   | 0.54 | 0.76 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C |
|   |  | –   | 0.78 | 1    |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C |
| <b>Cortex-M0+. Ultra Low-Power Active (ULPA) Mode</b> |  |     |      |      |      |   |
| I <sub>DD27</sub>                                     | Execute from Flash. CM4 OFF, CM0+ ULPA 8 MHz. With IMO. While (1)        | –   | 0.51 | 0.75 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C |
|   |  | –   | 0.75 | 1    |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C |
| I <sub>DD28</sub>                                     | Execute from Cache. CM4 OFF, CM0+ ULPA 8 MHz. With IMO. Dhrystone        | –   | 0.48 | 0.7  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C |
|   |  | –   | 0.7  | 0.95 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C |
| <b>Cortex-M4. Ultra Low-Power Sleep (ULPS) Mode</b>   |  |     |      |      |      |   |
| I <sub>DD29</sub>                                     | CM4 ULPS 8 MHz, CM0 ULPS 8 MHz. With IMO                                 | –   | 0.4  | 0.6  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C |
|   |  | –   | 0.57 | 0.8  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C |
| <b>Cortex-M0+. Ultra Low-Power Sleep (ULPS) Mode</b>  |  |     |      |      |      |   |
| I <sub>DD31</sub>                                     | CM4 Off, CM0+ ULPS 8 MHz. With IMO.                                      | –   | 0.39 | 0.6  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60 °C |
|   |  | –   | 0.56 | 0.8  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60 °C |
| <b>Deep Sleep Mode</b>                                |  |     |      |      |      |   |
| I <sub>DD33A</sub>                                    | With internal Buck enabled and 64K SRAM retention                        | –   | 7    | –    | μA   | Max value is at 85 °C                           |
| I <sub>DD33A_B</sub>                                  | With internal Buck enabled and 64K SRAM retention                        | –   | 7    | –    | μA   | Max value is at 60 °C                           |
| I <sub>DD33B</sub>                                    | With internal Buck enabled and 256K SRAM retention                       | –   | 9    | –    | μA   | Max value is at 85 °C                           |
| I <sub>DD33B_B</sub>                                  | With internal Buck enabled and 256K SRAM retention                       | –   | 9    | –    | μA   | Max value is at 60 °C                           |
| <b>Hibernate Mode</b>                                 |  |     |      |      |      |   |
| I <sub>DD34</sub>                                     | V <sub>DDD</sub> = 1.8 V   | –   | 300  | –    | nA   | No clocks running                               |
| I <sub>DD34A</sub>                                    | V <sub>DDD</sub> = 3.3 V   | –   | 800  | –    | nA   | No clocks running                               |
| <b>Power Mode Transition Times</b>                    |  |     |      |      |      |   |
| T <sub>LPACT_ACT</sub>                                | Low-Power Active to Active transition time                               | –   | –    | 35   | μs   | Including PLL lock time                         |
| T <sub>DS_LPACT</sub>                                 | Deep Sleep to LP Active transition time                                  | –   | –    | 25   | μs   | Guaranteed by design                            |
| T <sub>DS_ACT</sub>                                   | Deep Sleep to Active transition time                                     | –   | –    | 25   | μs   | Guaranteed by design                            |
| T <sub>HIB_ACT</sub>                                  | Hibernate to Active transition time                                      | –   | 500  | –    | μs   | Including PLL lock time                         |

**Module Level Power Consumption**

 Test Condition:  $V_{DD} = 3.3\text{ V}$ , Execute from Cache, WCO Enable

**Table 11. Module Level Power Consumption**

| Test Items                               | Specification (1.1 V LDO) |                   | Specification (1.1 V Buck) |                   | Condition                              |
|--|---------------------------|-------------------|----------------------------|-------------------|--|
|  | Typ                       | Max               | Typ                        | Max               |  |
| <b>CM0 Power Mode Transition</b>         |                           |                   |                            |                   |  |
| Active                                   | 7.7 mA                    | 8.2 mA            | 3.8 mA                     | 4.5 mA            | CM4 Off, CM0+ Active 100 MHz           |
| Sleep                                    | 2.57 mA                   | 3.2 mA            | 1.3 mA                     | 2 mA              | CM4 Off, CM0+ Sleep 50 MHz             |
| Low-Power Active                         | 1.62 mA                   | 2.4 mA            | 0.8 mA                     | 1.4 mA            | CM4 Off, CM0+ LPA 8 MHz                |
| Low-Power Sleep                          | 1.29 mA                   | 2 mA              | 0.64 mA                    | 1.1 mA            | CM4 Off, CM0+ LPS 8 MHz                |
| <b>CM4 Power Mode Transition</b>         |                           |                   |                            |                   |  |
| Active                                   | 10.1 mA                   | 10.7 mA           | 4.8 mA                     | 5.8 mA            | CM4 Active 100 MHz, CM0+ Sleep 100 MHz |
| Sleep                                    | 2.9 mA                    | 3.5 mA            | 1.5 mA                     | 2.2 mA            | CM4 Sleep 100 MHz, CM0+ Sleep 25 MHz   |
| Low-Power Active                         | 1.77 mA                   | 2.5 mA            | 0.9 mA                     | 1.5 mA            | CM4 LPA 8 MHz, CM0+ Sleep 8 MHz        |
| Low-Power Sleep                          | 1.31 mA                   | 2.1 mA            | 0.65 mA                    | 1.1 mA            | CM4 LPS 8 MHz, CM0+ LPS 8 MHz          |
| <b>BLE RF Current (DIRECT_TEST_MODE)</b> |                           |                   |                            |                   |  |
| TX (0dBm, 1 Mbps)                        | 10 mA                     |                   | 5.7 mA                     |                   | HCI Command                            |
| TX (0dBm, 2 Mbps)                        | 10 mA                     |                   | 5.7 mA                     |                   |  |
| RX (1 Mbps)                              | 11 mA                     |                   | 6.7 mA                     |                   | HCI Command                            |
| RX (2 Mbps)                              | 11.3 mA                   |                   | 7 mA                       |                   |  |
| <b>System Level BLE (System_Level)</b>   |                           |                   |                            |                   |  |
| Test Items                               | PILO (1.1 V Buck)         |                   | WCO (1.1 V Buck)           |                   | Condition                              |
|  | Typ                       | Max               | Typ                        | Max               |  |
| Deep Sleep                               | 90 $\mu\text{A}$          | 120 $\mu\text{A}$ | 7 $\mu\text{A}$            | 14 $\mu\text{A}$  |  |
| Adv 1.28s interval                       | 80 $\mu\text{A}$          | 121 $\mu\text{A}$ | 21 $\mu\text{A}$           | 28 $\mu\text{A}$  | 32 bytes, 0 dBm, 3.3 V, Buck           |
| 300 ms connection interval               | 170 $\mu\text{A}$         | 305 $\mu\text{A}$ | 28 $\mu\text{A}$           | 34 $\mu\text{A}$  | 0 byte, 0 dBm, 3.3 V, Buck             |
| 1s connection interval                   | 75 $\mu\text{A}$          | 106 $\mu\text{A}$ | 18 $\mu\text{A}$           | 23 $\mu\text{A}$  |  |
| 4s connection interval                   | 75 $\mu\text{A}$          | 106 $\mu\text{A}$ | 14 $\mu\text{A}$           | 19 $\mu\text{A}$  |  |
| Hibernate                                | 1.2 $\mu\text{A}$         | 1.8 $\mu\text{A}$ | 2.0 $\mu\text{A}$          | 2.3 $\mu\text{A}$ |  |

**XRES**
**Table 12. XRES**

| Parameter                               | Description                                   | Min | Typ | Max | Unit          | Details/Conditions      |
|---|---|-----|-----|-----|---------------|-------------------------|
| <b>XRES (Active Low) Specifications</b> |   |     |     |     |               |                         |
| <b>XRES AC Specifications</b>           |   |     |     |     |               |                         |
| $T_{XRES\_ACT}$                         | POR or XRES release to active transition time | –   | 750 | –   | $\mu\text{s}$ | Normal mode, 50 MHz M0+ |
| $T_{XRES\_PW}$                          | XRES Pulse width                              | 5   | –   | –   | $\mu\text{s}$ | –                       |

**Notes**

- Cypress-supplied software wakeup routines take approximately 100 CPU clock cycles after hardware wakeup (the 25  $\mu\text{s}$ ) before transition to Application code. With an 8-MHz CPU clock (LP Active), the time before user code executes is  $25 + 12.5 = 37.5\ \mu\text{s}$ .
- Cypress-supplied software wakeup routines take approximately 100 CPU clock cycles after hardware wakeup (the 25  $\mu\text{s}$ ) before transition to Application code. With a 25-MHz CPU clock (FLL), the time before user code executes is  $25 + 4 = 29\ \mu\text{s}$ . With a 100-MHz CPU clock, the time is  $25 + 1 = 26\ \mu\text{s}$ .

**Table 12. XRES (continued)**

| Parameter                     | Description  | Min                   | Typ | Max                   | Unit | Details/Conditions       |
|-------------------------------|--|-----------------------|-----|-----------------------|------|--------------------------|
| <b>XRES DC Specifications</b> |  |                       |     |                       |      |                          |
| T <sub>XRES_IDD</sub>         | I <sub>DD</sub> when XRES asserted                                   | –                     | 300 | –                     | nA   | V <sub>DDD</sub> = 1.8 V |
| T <sub>XRES_IDD_1</sub>       | I <sub>DD</sub> when XRES asserted                                   | –                     | 800 | –                     | nA   | V <sub>DDD</sub> = 3.3 V |
| V <sub>IH</sub>               | Input voltage high threshold   | 0.7 * V <sub>DD</sub> | –   | –                     | V    | CMOS Input               |
| V <sub>IL</sub>               | Input voltage low threshold  | –                     | –   | 0.3 * V <sub>DD</sub> | V    | CMOS Input               |
| C <sub>IN</sub>               | Input capacitance  | –                     | 3   | –                     | pF   | –                        |
| V <sub>HYSXRES</sub>          | Input voltage hysteresis   | –                     | 100 | –                     | mV   | –                        |
| I <sub>DIODE</sub>            | Current through protection diode to V <sub>DD</sub> /V <sub>SS</sub> | –                     | –   | 100                   | μA   | –                        |

GPIO

**Table 13. GPIO Specifications**

| Parameter                     | Description  | Min                    | Typ | Max                   | Unit | Details/Conditions  |
|-------------------------------|--|------------------------|-----|-----------------------|------|---|
| <b>GPIO DC Specifications</b> |  |                        |     |                       |      |   |
| V <sub>IH</sub>               | Input voltage high threshold   | 0.7 * V <sub>DD</sub>  | –   | –                     | V    | CMOS Input  |
| I <sub>IHS</sub>              | Input current when Pad > VDDIO for OVT inputs                        | –                      | –   | 10                    | μA   | Per I <sup>2</sup> C Spec   |
| V <sub>IL</sub>               | Input voltage low threshold  | –                      | –   | 0.3 * V <sub>DD</sub> | V    | CMOS Input  |
| V <sub>IH</sub>               | LVTTL input, V <sub>DD</sub> < 2.7 V                                 | 0.7 * V <sub>DD</sub>  | –   | –                     | V    | –   |
| V <sub>IL</sub>               | LVTTL input, V <sub>DD</sub> < 2.7 V                                 | –                      | –   | 0.3 * V <sub>DD</sub> | V    | –   |
| V <sub>IH</sub>               | LVTTL input, V <sub>DD</sub> ≥ 2.7 V                                 | 2.0                    | –   | –                     | V    | –   |
| V <sub>IL</sub>               | LVTTL input, V <sub>DD</sub> ≥ 2.7 V                                 | –                      | –   | 0.8                   | V    | –   |
| V <sub>OH</sub>               | Output voltage high level  | V <sub>DD</sub> - 0.5  | –   | –                     | V    | I <sub>OH</sub> = 8 mA  |
| V <sub>OL</sub>               | Output voltage low level   | –                      | –   | 0.4                   | V    | I <sub>OL</sub> = 8 mA  |
| R <sub>PULLUP</sub>           | Pull-up resistor   | 3.5                    | 5.6 | 8.5                   | kΩ   | –   |
| R <sub>PULLDOWN</sub>         | Pull-down resistor   | 3.5                    | 5.6 | 8.5                   | kΩ   | –   |
| I <sub>IL</sub>               | Input leakage current (absolute value)                               | –                      | –   | 2                     | nA   | 25 °C, V <sub>DD</sub> = 3.0 V  |
| I <sub>IL_CTBM</sub>          | Input leakage on CTBm input pins                                     | –                      | –   | 4                     | nA   | –   |
| C <sub>IN</sub>               | Input Capacitance  | –                      | –   | 5                     | pF   | –   |
| V <sub>HYSTTL</sub>           | Input hysteresis LVTTL V <sub>DD</sub> > 2.7 V                       | 100                    | 0   | –                     | mV   | –   |
| V <sub>HYS CMOS</sub>         | Input hysteresis CMOS  | 0.05 * V <sub>DD</sub> | –   | –                     | mV   | –   |
| I <sub>DIODE</sub>            | Current through protection diode to V <sub>DD</sub> /V <sub>SS</sub> | –                      | –   | 100                   | μA   | –   |
| I <sub>TOT_GPIO</sub>         | Maximum Total Source or Sink Chip Current                            | –                      | –   | 200                   | mA   | –   |
| <b>GPIO AC Specifications</b> |  |                        |     |                       |      |   |
| T <sub>RISE F</sub>           | Rise time in Fast Strong mode. 10% to 90% of V <sub>DD</sub>         | –                      | –   | 2.5                   | ns   | C <sub>load</sub> = 15 pF, 8 mA drive strength                                  |
| T <sub>FALL F</sub>           | Fall time in Fast Strong mode. 10% to 90% of V <sub>DD</sub>         | –                      | –   | 2.5                   | ns   | C <sub>load</sub> = 15 pF, 8 mA drive strength                                  |
| T <sub>RISE S_1</sub>         | Rise time in Slow Strong mode. 10% to 90% of V <sub>DD</sub>         | 52                     | –   | 142                   | ns   | C <sub>load</sub> = 15 pF, 8 mA drive strength, V <sub>DD</sub> ≤ 2.7 V         |
| T <sub>RISE S_2</sub>         | Rise time in Slow Strong mode. 10% to 90% of V <sub>DD</sub>         | 48                     | –   | 102                   | ns   | C <sub>load</sub> = 15 pF, 8 mA drive strength, 2.7 V < V <sub>DD</sub> ≤ 3.6 V |

**Table 13. GPIO Specifications** (continued)

| Parameter             | Description  | Min                       | Typ | Max  | Unit | Details/Conditions  |
|-----------------------|--|---------------------------|-----|------|------|---|
| T <sub>FALLS_1</sub>  | Fall time in Slow Strong mode. 10% to 90% of V <sub>DD</sub>     | 44                        | –   | 211  | ns   | C <sub>load</sub> = 15 pF, 8 mA drive strength, V <sub>DD</sub> ≤ 2.7 V         |
| T <sub>FALLS_2</sub>  | Fall time in Slow Strong mode. 10% to 90% of V <sub>DD</sub>     | 42                        | –   | 93   | ns   | C <sub>load</sub> = 15 pF, 8 mA drive strength, 2.7 V < V <sub>DD</sub> ≤ 3.6 V |
| T <sub>FALL_I2C</sub> | Fall time (30% to 70% of V <sub>DD</sub> ) in Slow Strong mode   | 20*V <sub>DDIO</sub> /5.5 | –   | 250  | ns   | C <sub>load</sub> = 10 pF to 400 pF, 8-mA drive strength                        |
| F <sub>GPIOUT1</sub>  | GPIO F <sub>out</sub> ; Fast Strong mode                         | –                         | –   | 100  | MHz  | 90/10%, 15-pF load, 60/40 duty cycle  |
| F <sub>GPIOUT2</sub>  | GPIO F <sub>out</sub> ; Slow Strong mode                         | –                         | –   | 16.7 | MHz  | 90/10%, 15-pF load, 60/40 duty cycle  |
| F <sub>GPIOUT3</sub>  | GPIO F <sub>out</sub> ; Fast Strong mode                         | –                         | –   | 7    | MHz  | 90/10%, 25-pF load, 60/40 duty cycle  |
| F <sub>GPIOUT4</sub>  | GPIO F <sub>out</sub> ; Slow Strong mode                         | –                         | –   | 3.5  | MHz  | 90/10%, 25-pF load, 60/40 duty cycle  |
| F <sub>GPIOIN</sub>   | GPIO input operating frequency; 1.71 V ≤ V <sub>DD</sub> ≤ 3.6 V | –                         | –   | 100  | MHz  | 90/10% V <sub>IO</sub>  |

## Analog Peripherals

### Opamp

**Table 14. Opamp Specifications**

| Parameter                | Description                                      | Min | Typ  | Max                   | Unit | Details/Conditions |
|--------------------------|--|-----|------|-----------------------|------|--------------------|
| I <sub>DD</sub>          | Opamp block current. No load.                    | –   | –    | –                     | –    | –                  |
| I <sub>DD_HI</sub>       | Power = HI                                       | –   | 1300 | 1500                  | μA   | –                  |
| I <sub>DD_MED</sub>      | Power = MED                                      | –   | 450  | 600                   | μA   | –                  |
| I <sub>DD_LOW</sub>      | Power = LO                                       | –   | 250  | 350                   | μA   | –                  |
| GBW                      | Load = 20 pF, 0.1 mA<br>V <sub>DDA</sub> = 2.7 V | –   | –    | –                     | –    | –                  |
| G <sub>BW_HI</sub>       | Power = HI                                       | 6   | –    | –                     | MHz  | –                  |
| G <sub>BW_MED</sub>      | Power = MED                                      | 4   | –    | –                     | MHz  | –                  |
| G <sub>BW_LO</sub>       | Power = LO                                       | –   | 1    | –                     | MHz  | –                  |
| I <sub>OUT_MAX</sub>     | V <sub>DDA</sub> ≥ 2.7 V, 500 mV from rail       | –   | –    | –                     | –    | –                  |
| I <sub>OUT_MAX_HI</sub>  | Power = HI                                       | –   | –    | –                     | mA   | –                  |
| I <sub>OUT_MAX_MID</sub> | Power = MID                                      | 10  | –    | –                     | mA   | –                  |
| I <sub>OUT_MAX_LO</sub>  | Power = LO                                       | –   | 5    | –                     | mA   | –                  |
| I <sub>OUT</sub>         | V <sub>DDA</sub> = 1.71 V, 500 mV from rail      | –   | –    | –                     | –    | –                  |
| I <sub>OUT_MAX_HI</sub>  | Power = HI                                       | 4   | –    | –                     | mA   | –                  |
| I <sub>OUT_MAX_MID</sub> | Power = MID                                      | 4   | –    | –                     | mA   | –                  |
| I <sub>OUT_MAX_LO</sub>  | Power = LO                                       | –   | 2    | –                     | mA   | –                  |
| V <sub>IN</sub>          | Input voltage range                              | 0   | –    | V <sub>DDA</sub> -0.2 | V    | –                  |
| V <sub>CM</sub>          | Input common mode voltage                        | 0   | –    | V <sub>DDA</sub> -0.2 | V    | –                  |
| V <sub>OUT</sub>         | V <sub>DDA</sub> ≥ 2.7 V                         | –   | –    | –                     | –    | –                  |
| V <sub>OUT_1</sub>       | Power = HI, I <sub>load</sub> = 10 mA            | 0.5 | –    | V <sub>DDA</sub> -0.5 | V    | –                  |
| V <sub>OUT_2</sub>       | Power = HI, I <sub>load</sub> = 1 mA             | 0.2 | –    | V <sub>DDA</sub> -0.2 | V    | –                  |

**Table 14. Opamp Specifications (continued)**

| Parameter                           | Description   | Min | Typ      | Max                   | Unit       | Details/Conditions  |
|-------------------------------------|---|-----|----------|-----------------------|------------|---|
| V <sub>OUT_3</sub>                  | Power = MED, I <sub>load</sub> = 1 mA   | 0.2 | –        | V <sub>DDA</sub> -0.2 | V          | –   |
| V <sub>OUT_4</sub>                  | Power = LO, I <sub>load</sub> = 0.1 mA  | 0.2 | –        | V <sub>DDA</sub> -0.2 | V          | –   |
| V <sub>OS_UNTR</sub>                | Offset voltage, untrimmed   | –   | –        | –                     | mV         | –   |
| V <sub>OS_TR</sub>                  | Offset voltage, trimmed   | –   | ±0.5     | –                     | mV         | High mode, 0.2 to V <sub>DDA</sub> - 0.2  |
| V <sub>OS_TR</sub>                  | Offset voltage, trimmed   | –   | ±1       | –                     | mV         | Medium mode   |
| V <sub>OS_TR</sub>                  | Offset voltage, trimmed   | –   | ±2       | –                     | mV         | Low mode  |
| V <sub>OS_DR_UNTR</sub>             | Offset voltage drift, untrimmed   | –   | –        | –                     | µV/°C      | –   |
| V <sub>OS_DR_TR</sub>               | Offset voltage drift, trimmed   | –10 | ±3       | 10                    | µV/°C      | High mode, 0.2 to V <sub>DDA</sub> - 0.2  |
| V <sub>OS_DR_TR</sub>               | Offset voltage drift, trimmed   | –   | ±10      | –                     | µV/°C      | Medium mode   |
| V <sub>OS_DR_TR</sub>               | Offset voltage drift, trimmed   | –   | ±10      | –                     | µV/°C      | Low mode  |
| common-mode rejection ratio (CMRR)  | DC common mode rejection ratio  | 67  | 80       | –                     | dB         | V <sub>DDD</sub> = 3.3 V  |
| power supply rejection ratio (PSRR) | Power supply rejection ratio at 1 kHz, 10-mV ripple                               | 70  | 85       | –                     | dB         | V <sub>DDD</sub> = 3.3 V  |
| Noise                               | –   | –   | –        | –                     | –          | –   |
| VN1                                 | Input-referred, 1 Hz - 1 GHz, power = HI  | –   | 100      | –                     | µVrms      | –   |
| VN2                                 | Input-referred, 1 kHz, power = HI   | –   | 180      | –                     | nV/root Hz | –   |
| VN3                                 | Input-referred, 10 kHz, power = HI  | –   | 70       | –                     | nV/root Hz | –   |
| VN4                                 | Input-referred, 100 kHz, power = HI   | –   | 38       | –                     | nV/root Hz | –   |
| CLOAD                               | Stable up to maximum load<br>Performance specs at 50 pF                           | –   | –        | 125                   | pF         | –   |
| SLEW_RATE                           | Output slew rate  | 6   | –        | –                     | V/µs       | C <sub>load</sub> = 50 pF, Power = High, V <sub>DDA</sub> ≥ 2.7 V   |
| T <sub>OP_WAKE</sub>                | From disable to enable, no external RC dominating                                 | –   | 25       | –                     | µs         | –   |
| COMP_MODE                           | Comparator mode; 50-mV overdrive, T <sub>rise</sub> = T <sub>fall</sub> (approx.) | –   | –        | –                     | –          | –   |
| T <sub>PD1</sub>                    | Response time; power = HI   | –   | 150      | –                     | ns         | –   |
| T <sub>PD2</sub>                    | Response time; power = MED  | –   | 400      | –                     | ns         | –   |
| T <sub>PD3</sub>                    | Response time; power = LO   | –   | 2000     | –                     | ns         | –   |
| V <sub>HYST_OP</sub>                | Hysteresis  | –   | 10       | –                     | mV         | –   |
| Deep Sleep mode                     | Mode 2 is lowest current range<br>Mode 1 has higher GBW                           | –   | –        | –                     | –          | Deep Sleep mode operation:<br>V <sub>DDA</sub> ≥ 2.7 V<br>V <sub>IN</sub> is 0.2 to V <sub>DDA</sub> -1.5 |
| I <sub>DD_HI_M1</sub>               | Mode 1, High current  | –   | 130<br>0 | 1500                  | µA         | Typ at 25 °C  |
| I <sub>DD_MED_M1</sub>              | Mode 1, Medium current  | –   | 460      | 600                   | µA         | Typ at 25 °C  |
| I <sub>DD_LOW_M1</sub>              | Mode 1, Low current   | –   | 230      | 350                   | µA         | Typ at 25 °C  |
| I <sub>DD_HI_M2</sub>               | Mode 2, High current  | –   | 120      | –                     | µA         | 25 °C   |
| I <sub>DD_MED_M2</sub>              | Mode 2, Medium current  | –   | 60       | –                     | µA         | 25 °C   |
| I <sub>DD_LOW_M2</sub>              | Mode 2, Low current   | –   | 15       | –                     | µA         | 25 °C   |
| GBW_HI_M1                           | Mode 1, High current  | –   | 4        | –                     | MHz        | 25 °C   |
| GBW_MED_M1                          | Mode 1, Medium current  | –   | 2        | –                     | MHz        | 25 °C   |

**Table 14. Opamp Specifications (continued)**

| Parameter          | Description            | Min | Typ | Max | Unit | Details/Conditions                              |
|--------------------|------------------------|-----|-----|-----|------|---|
| GBW_LOW_M1         | Mode 1, Low current    | –   | 0.5 | –   | MHz  | 25 °C   |
| GBW_HI_M2          | Mode 2, High current   | –   | 0.5 | –   | MHz  | 20-pF load, no DC load 0.2 V to $V_{DDA}-1.5$ V |
| GBW_MED_M2         | Mode 2, Medium current | –   | 0.2 | –   | MHz  | 20-pF load, no DC load 0.2 V to $V_{DDA}-1.5$ V |
| GBW_LOW_M2         | Mode 2, Low current    | –   | 0.1 | –   | MHz  | 20-pF load, no DC load 0.2 V to $V_{DDA}-1.5$ V |
| $V_{OS\_HI\_M1}$   | Mode 1, High current   | –   | 5   | –   | mV   | With trim 25 °C, 0.2 V to $V_{DDA}-1.5$ V       |
| $V_{OS\_MED\_M1}$  | Mode 1, Medium current | –   | 5   | –   | mV   | With trim 25 °C, 0.2 V to $V_{DDA}-1.5$ V       |
| $V_{OS\_LOW\_M1}$  | Mode 1, Low current    | –   | 5   | –   | mV   | With trim 25 °C, 0.2 V to $V_{DDA}-1.5$ V       |
| $V_{OS\_HI\_M2}$   | Mode 2, High current   | –   | 5   | –   | mV   | With trim 25 °C, 0.2 V to $V_{DDA}-1.5$ V       |
| $V_{OS\_MED\_M2}$  | Mode 2, Medium current | –   | 5   | –   | mV   | With trim 25 °C, 0.2 V to $V_{DDA}-1.5$ V       |
| $V_{OS\_LOW\_M2}$  | Mode 2, Low current    | –   | 5   | –   | mV   | With trim 25 °C, 0.2 V to $V_{DDA}-1.5$ V       |
| $I_{OUT\_HI\_M1}$  | Mode 1, High current   | –   | 10  | –   | mA   | Output is 0.5 V to $V_{DDA}-0.5$ V              |
| $I_{OUT\_MED\_M1}$ | Mode 1, Medium current | –   | 10  | –   | mA   | Output is 0.5 V to $V_{DDA}-0.5$ V              |
| $I_{OUT\_LOW\_M1}$ | Mode 1, Low current    | –   | 4   | –   | mA   | Output is 0.5 V to $V_{DDA}-0.5$ V              |
| $I_{OUT\_HI\_M2}$  | Mode 2, High current   | –   | 1   | –   | mA   | Output is 0.5 V to $V_{DDA}-0.5$ V              |
| $I_{OUT\_MED\_M2}$ | Mode 2, Medium current | –   | 1   | –   | mA   | Output is 0.5 V to $V_{DDA}-0.5$ V              |
| $I_{OUT\_LOW\_M2}$ | Mode 2, Low current    | –   | 0.5 | –   | mA   | Output is 0.5 V to $V_{DDA}-0.5$ V              |

**Table 15. Low-Power (LP) Comparator Specifications**

| Parameter                              | Description   | Min | Typ | Max                     | Unit | Details/Conditions         |
|--|---|-----|-----|-------------------------|------|----------------------------|
| <b>LP Comparator DC Specifications</b> |   |     |     |                         |      |                            |
| V <sub>OFFSET1</sub>                   | Input offset voltage for COMP1. Normal power mode     | -10 | -   | 10                      | mV   | COMP0 offset is ±25 mV     |
| V <sub>OFFSET2</sub>                   | Input offset voltage. Low-power mode                  | -25 | ±12 | 25                      | mV   | -                          |
| V <sub>OFFSET3</sub>                   | Input offset voltage. Ultra low-power mode            | -25 | ±12 | 25                      | mV   | -                          |
| V <sub>HYST1</sub>                     | Hysteresis when enabled in Normal mode                | -   | -   | 60                      | mV   | -                          |
| V <sub>HYST2</sub>                     | Hysteresis when enabled in Low-power mode             | -   | -   | 80                      | mV   | -                          |
| V <sub>ICM1</sub>                      | Input common mode voltage in Normal mode              | 0   | -   | V <sub>DDIO1</sub> -0.1 | V    | -                          |
| V <sub>ICM2</sub>                      | Input common mode voltage in Low-power mode           | 0   | -   | V <sub>DDIO1</sub> -0.1 | V    | -                          |
| V <sub>ICM3</sub>                      | Input common mode voltage in Ultra low-power mode     | 0   | -   | V <sub>DDIO1</sub> -0.1 | V    | -                          |
| CMRR                                   | Common mode rejection ratio in Normal power mode      | 50  | -   | -                       | dB   | -                          |
| I <sub>CMP1</sub>                      | Block current, Normal mode                            | -   | -   | 150                     | μA   | -                          |
| I <sub>CMP2</sub>                      | Block current, Low-power mode                         | -   | -   | 10                      | μA   | -                          |
| I <sub>CMP3</sub>                      | Block current in Ultra low-power mode                 | -   | 0.3 | 0.85                    | μA   | -                          |
| Z <sub>CMP</sub>                       | DC input impedance of comparator                      | 35  | -   | -                       | MΩ   | -                          |
| <b>LP Comparator AC Specifications</b> |   |     |     |                         |      |                            |
| T <sub>RESP1</sub>                     | Response time, Normal mode, 100 mV overdrive          | -   | -   | 100                     | ns   | -                          |
| T <sub>RESP2</sub>                     | Response time, Low-power mode, 100 mV overdrive       | -   | -   | 1000                    | ns   | -                          |
| T <sub>RESP3</sub>                     | Response time, Ultra low-power mode, 100 mV overdrive | -   | -   | 20                      | μs   | -                          |
| T <sub>CMP_EN1</sub>                   | Time from enabling to operation                       | -   | -   | 10                      | μs   | Normal and Low-power modes |
| T <sub>CMP_EN2</sub>                   | Time from enabling to operation                       | -   | -   | 50                      | μs   | Ultra low-power mode       |

**Table 16. Temperature Sensor Specifications**

| Parameter            | Description                 | Min | Typ | Max | Unit | Details/Conditions |
|----------------------|-----------------------------|-----|-----|-----|------|--------------------|
| T <sub>SENSACC</sub> | Temperature sensor accuracy | -   | ±1  | 5   | °C   | -40 to +85 °C      |

**Table 17. Internal Reference Specification**

| Parameter          | Description | Min   | Typ | Max   | Unit | Details/Conditions |
|--------------------|-------------|-------|-----|-------|------|--------------------|
| V <sub>REFBG</sub> | -           | 1.188 | 1.2 | 1.212 | V    | -                  |



## SAR ADC

**Table 18. 12-bit SAR ADC DC Specifications**

| Parameter | Description   | Min      | Typ | Max       | Unit      | Details/Conditions                      |
|-----------|---|----------|-----|-----------|-----------|---|
| A_RES     | SAR ADC resolution                                  | –        | –   | 12        | bits      | –                                       |
| A_CHNLS_S | Number of channels - single ended                   | –        | –   | 16        | –         | 8 full speed                            |
| A-CHNKS_D | Number of channels - differential                   | –        | –   | 8         | –         | Differential inputs use neighboring I/O |
| A-MONO    | Monotonicity  | –        | –   | –         | –         | Yes                                     |
| A_GAINERR | Gain error  | –        | –   | ±0.2      | %         | With external reference                 |
| A_OFFSET  | Input offset voltage                                | –        | –   | 2         | mV        | Measured with 1-V reference             |
| A_ISAR_1  | Current consumption at 1 Msps                       | –        | –   | 1         | mA        | At 1 Msps. External bypass capacitor    |
| A_ISAR_2  | Current consumption at 1 Msps. Reference = $V_{DD}$ | –        | –   | 1.25      | mA        | At 1 Msps. External bypass capacitor    |
| A_VINS    | Input voltage range - single-ended                  | $V_{SS}$ | –   | $V_{DDA}$ | V         | –                                       |
| A_VIND    | Input voltage range - differential                  | $V_{SS}$ | –   | $V_{DDA}$ | V         | –                                       |
| A_INRES   | Input resistance                                    | –        | –   | 2.2       | $K\Omega$ | –                                       |
| A_INCAP   | Input capacitance                                   | –        | –   | 10        | pF        | –                                       |

**Table 19. 12-bit SAR ADC AC Specifications**

| Parameter                               | Description  | Min | Typ | Max | Unit | Details/Conditions   |
|---|--|-----|-----|-----|------|--|
| <b>12-bit SAR ADC AC Specifications</b> |  |     |     |     |      |  |
| A_PSR                                   | Power supply rejection ratio   | 70  | –   | –   | dB   | –  |
| A_CMRR                                  | Common mode rejection ratio  | 66  | –   | –   | dB   | Measured at 1 V  |
| <b>One Msp per second mode:</b>         |  |     |     |     |      |  |
| A_SAMP_1                                | Sample rate with external reference bypass capacitor                             | –   | –   | 1   | Msp  | –  |
| A_SAMP_2                                | Sample rate with no bypass capacitor; Reference = $V_{DD}$                       | –   | –   | 250 | Ksps | –  |
| A_SAMP_3                                | Sample rate with no bypass capacitor; Internal reference                         | –   | –   | 100 | Ksps | –  |
| A_SINAD                                 | Signal-to-noise and Distortion ratio (SINAD). $V_{DDA} = 2.7$ to $3.6$ V, 1 Msps | 64  | –   | –   | dB   | $F_{in} = 10$ kHz  |
| A_INL                                   | Integral Non Linearity. $V_{DDA} = 2.7$ to $3.6$ V, 1 Msps                       | –2  | –   | 2   | LSB  | Measured with internal $V_{REF} = 1.2$ V and bypass capacitor                      |
| A_INL                                   | Integral Non Linearity. $V_{DDA} = 2.7$ to $3.6$ V, 1 Msps                       | –4  | –   | 4   | LSB  | Measured with external $V_{REF} \geq 1$ V and $V_{IN}$ common mode $< 2 * V_{REF}$ |
| A_DNL                                   | Differential Non Linearity. $V_{DDA} = 2.7$ to $3.6$ V, 1 Msps                   | –1  | –   | 1.4 | LSB  | Measured with internal $V_{REF} = 1.2$ V and bypass capacitor                      |
| A_DNL                                   | Differential Non Linearity. $V_{DDA} = 2.7$ to $3.6$ V, 1 Msps                   | –1  | –   | 1.7 | LSB  | Measured with external $V_{REF} \geq 1$ V and $V_{IN}$ common mode $< 2 * V_{REF}$ |
| A_THD                                   | Total harmonic distortion. $V_{DDA} = 2.7$ to $3.6$ V, 1 Msps                    | –   | –   | –65 | dB   | $F_{in} = 10$ kHz  |

**Table 20. 12-bit DAC Specifications**

| Parameter                           | Description                                | Min | Typ | Max | Unit | Details/Conditions                      |
|-------------------------------------|--|-----|-----|-----|------|---|
| <b>12-bit DAC DC Specifications</b> |  |     |     |     |      |   |
| DAC_RES                             | DAC resolution                             | –   | –   | 12  | bits | –                                       |
| DAC_INL                             | Integral nonlinearity                      | –4  | –   | 4   | LSB  | –                                       |
| DAC_DNL                             | Differential nonlinearity                  | –2  | –   | 2   | LSB  | Monotonic to 11 bits.                   |
| DAC_OFFSET                          | Output Voltage zero offset error           | –10 | –   | 10  | mV   | For 000 (hex)                           |
| DAC_OUT_RES                         | DAC Output resistance                      | –   | 15  | –   | kΩ   | –                                       |
| DAC_IDD                             | DAC Current                                | –   | –   | 125 | μA   | –                                       |
| DAC_QIDD                            | DAC Current when DAC stopped               | –   | –   | 1   | μA   | –                                       |
| <b>12-bit DAC AC Specifications</b> |  |     |     |     |      |   |
| DAC_CONV                            | DAC Settling time                          | –   | –   | 2   | μs   | Driving through CTBm buffer; 25 pF load |
| DAC_WAKEUP                          | Time from Enabling to ready for conversion | –   | –   | 10  | μs   | –                                       |

**CSD**
**Table 21. CapSense Sigma-Delta (CSD) Specifications**

| Parameter  | Description  | Min  | Typ | Max                    | Unit  | Details/Conditions  |
|--|--|------|-----|------------------------|-------|---|
| <b>CSD V2 Specifications</b>   |  |      |     |                        |       |   |
| V <sub>DD_RIPPLE</sub>   | Max allowed ripple on power supply, DC to 10 MHz           | –    | –   | ±50                    | mV    | V <sub>DDA</sub> > 2 V (with ripple), 25 °C T <sub>A</sub> , Sensitivity = 0.1 pF   |
| V <sub>DD_RIPPLE_1.8</sub>   | Max allowed ripple on power supply, DC to 10 MHz           | –    | –   | ±25                    | mV    | V <sub>DDA</sub> > 1.75 V (with ripple), 25 °C T <sub>A</sub> , Parasitic Capacitance (C <sub>P</sub> ) < 20 pF, Sensitivity ≥ 0.4 pF |
| I <sub>CSD</sub>   | Maximum block current                                      |      |     | 4500                   | µA    |   |
| V <sub>REF</sub>   | Voltage reference for CSD and comparator                   | 0.6  | 1.2 | V <sub>DDA</sub> - 0.6 | V     | V <sub>DDA</sub> - V <sub>REF</sub> ≥ 0.6 V   |
| V <sub>REF_EXT</sub>   | External voltage reference for CSD and comparator          | 0.6  |     | V <sub>DDA</sub> - 0.6 | V     | V <sub>DDA</sub> - V <sub>REF</sub> ≥ 0.6 V   |
| I <sub>DAC1IDD</sub>   | IDAC1 (7-bits) block current                               | –    | –   | 1900                   | µA    |   |
| I <sub>DAC2IDD</sub>   | IDAC2 (7-bits) block current                               | –    | –   | 1900                   | µA    |   |
| V <sub>CSD</sub>   | Voltage range of operation                                 | 1.71 | –   | 3.6                    | V     | 1.71 to 3.6 V   |
| V <sub>COMPIDAC</sub>  | Voltage compliance range of IDAC                           | 0.6  | –   | V <sub>DDA</sub> - 0.6 | V     | V <sub>DDA</sub> - V <sub>REF</sub> ≥ 0.6 V   |
| I <sub>DAC1DNL</sub>   | DNL  | –1   | –   | 1                      | LSB   |   |
| I <sub>DAC1INL</sub>   | INL  | –3   | –   | 3                      | LSB   | If V <sub>DDA</sub> < 2 V then for LSB of 2.4 µA or less  |
| I <sub>DAC2DNL</sub>   | DNL  | –1   | –   | 1                      | LSB   |   |
| I <sub>DAC2INL</sub>   | INL  | –3   | –   | 3                      | LSB   | If V <sub>DDA</sub> < 2 V then for LSB of 2.4 µA or less  |
| <b>SNRC of the following is Ratio of counts of finger to noise. Guaranteed by characterization</b> |  |      |     |                        |       |   |
| SNRC_1   | SRSS Reference. IMO + FLL Clock Source. 0.1-pF sensitivity | 5    | –   | –                      | Ratio | 9.5-pF maximum capacitance  |
| SNRC_2   | SRSS Reference. IMO + FLL Clock Source. 0.3-pF sensitivity | 5    | –   | –                      | Ratio | 31-pF maximum capacitance   |
| SNRC_3   | SRSS Reference. IMO + FLL Clock Source. 0.6-pF sensitivity | 5    | –   | –                      | Ratio | 61-pF maximum capacitance   |
| SNRC_4   | PASS Reference. IMO + FLL Clock Source. 0.1-pF sensitivity | 5    | –   | –                      | Ratio | 12-pF maximum capacitance   |
| SNRC_5   | PASS Reference. IMO + FLL Clock Source. 0.3-pF sensitivity | 5    | –   | –                      | Ratio | 47-pF maximum capacitance   |
| SNRC_6   | PASS Reference. IMO + FLL Clock Source. 0.6-pF sensitivity | 5    | –   | –                      | Ratio | 86-pF maximum capacitance   |
| SNRC_7   | PASS Reference. IMO + PLL Clock Source. 0.1-pF sensitivity | 5    | –   | –                      | Ratio | 27-pF maximum capacitance   |
| SNRC_8   | PASS Reference. IMO + PLL Clock Source. 0.3-pF sensitivity | 5    | –   | –                      | Ratio | 86-pF maximum capacitance   |
| SNRC_9   | PASS Reference. IMO + PLL Clock Source. 0.6-pF sensitivity | 5    | –   | –                      | Ratio | 168-pF maximum capacitance  |
| I <sub>DAC1CRT1</sub>  | Output current of IDAC1 (7 bits) in low range              | 4.2  |     | 5.7                    | µA    | LSB = 37.5 nA typical   |
| I <sub>DAC1CRT2</sub>  | Output current of IDAC1(7 bits) in medium range            | 33.7 |     | 45.6                   | µA    | LSB = 300 nA typical  |
| I <sub>DAC1CRT3</sub>  | Output current of IDAC1(7 bits) in high range              | 270  |     | 365                    | µA    | LSB = 2.4 µA typical  |

**Table 21. CapSense Sigma-Delta (CSD) Specifications (continued)**

| Parameter                 | Description   | Min  | Typ | Max  | Unit | Details/Conditions                      |
|---------------------------|---|------|-----|------|------|---|
| I <sub>DAC1CRT12</sub>    | Output current of IDAC1 (7 bits) in low range, 2X mode                                    | 8    |     | 11.4 | μA   | LSB = 37.5 nA typical 2X output stage   |
| I <sub>DAC1CRT22</sub>    | Output current of IDAC1(7 bits) in medium range, 2X mode                                  | 67   |     | 91   | μA   | LSB = 300 nA typical 2X output stage    |
| I <sub>DAC1CRT32</sub>    | Output current of IDAC1(7 bits) in high range, 2X mode. V <sub>D<sub>DA</sub></sub> > 2 V | 540  |     | 730  | μA   | LSB = 2.4 μA typical 2X output stage    |
| I <sub>DAC2CRT1</sub>     | Output current of IDAC2 (7 bits) in low range   | 4.2  |     | 5.7  | μA   | LSB = 37.5 nA typical                   |
| I <sub>DAC2CRT2</sub>     | Output current of IDAC2 (7 bits) in medium range  | 33.7 |     | 45.6 | μA   | LSB = 300 nA typical                    |
| I <sub>DAC2CRT3</sub>     | Output current of IDAC2 (7 bits) in high range  | 270  |     | 365  | μA   | LSB = 2.4 μA typical                    |
| I <sub>DAC2CRT12</sub>    | Output current of IDAC2 (7 bits) in low range, 2X mode                                    | 8    |     | 11.4 | μA   | LSB = 37.5 nA typical 2X output stage   |
| I <sub>DAC2CRT22</sub>    | Output current of IDAC2(7 bits) in medium range, 2X mode                                  | 67   |     | 91   | μA   | LSB = 300 nA typical 2X output stage    |
| I <sub>DAC2CRT32</sub>    | Output current of IDAC2(7 bits) in high range, 2X mode. V <sub>D<sub>DA</sub></sub> > 2 V | 540  |     | 730  | μA   | LSB = 2.4 μA typical 2X output stage    |
| I <sub>DAC3CRT13</sub>    | Output current of IDAC in 8-bit mode in low range   | 8    |     | 11.4 | μA   | LSB = 37.5 nA typical                   |
| I <sub>DAC3CRT23</sub>    | Output current of IDAC in 8-bit mode in medium range                                      | 67   |     | 91   | μA   | LSB = 300 nA typical                    |
| I <sub>DAC3CRT33</sub>    | Output current of IDAC in 8-bit mode in high range. V <sub>D<sub>DA</sub></sub> > 2 V     | 540  |     | 730  | μA   | LSB = 2.4 μA typical                    |
| I <sub>DACOFFSET</sub>    | All zeros input   | –    | –   | 1    | LSB  | Polarity set by Source or Sink          |
| I <sub>DACGAIN</sub>      | Full-scale error less offset  | –    | –   | ±15  | %    | LSB = 2.4 μA typical                    |
| I <sub>DACMISMATCH1</sub> | Mismatch between IDAC1 and IDAC2 in Low mode  | –    | –   | 9.2  | LSB  | LSB = 37.5 nA typical                   |
| I <sub>DACMISMATCH2</sub> | Mismatch between IDAC1 and IDAC2 in Medium mode   | –    | –   | 6    | LSB  | LSB = 300 nA typical                    |
| I <sub>DACMISMATCH3</sub> | Mismatch between IDAC1 and IDAC2 in High mode   | –    | –   | 5.8  | LSB  | LSB = 2.4 μA typical                    |
| I <sub>DACSET8</sub>      | Settling time to 0.5 LSB for 8-bit IDAC   | –    | –   | 10   | μs   | Full-scale transition. No external load |
| I <sub>DACSET7</sub>      | Settling time to 0.5 LSB for 7-bit IDAC   | –    | –   | 10   | μs   | Full-scale transition. No external load |
| C <sub>MOD</sub>          | External modulator capacitor  | –    | 2.2 | –    | nF   | 5-V rating, X7R or NP0 capacitor        |

**Table 22. CSD ADC Specifications**

| Parameter                       | Description  | Min              | Typ | Max              | Unit | Details/Conditions   |
|---------------------------------|--|------------------|-----|------------------|------|--|
| <b>CSDv2 ADC Specifications</b> |  |                  |     |                  |      |  |
| A_RES                           | Resolution   | –                | –   | 10               | bits | Auto-zeroing is required every millisecond   |
| A_CHNLS_S                       | Number of channels - single ended  | –                | –   | –                | 16   |  |
| A-MONO                          | Monotonicity   | –                | –   | Yes              | –    | V <sub>REF</sub> mode  |
| A_GAINERR_VREF                  | Gain error   | –                | 0.6 | –                | %    | Reference Source: SRSS<br>(V <sub>REF</sub> = 1.20 V, V <sub>DDA</sub> < 2.2 V),<br>(V <sub>REF</sub> = 1.6 V, 2.2 V < V <sub>DDA</sub> < 2.7 V), (V <sub>REF</sub> = 2.13 V,<br>V <sub>DDA</sub> > 2.7 V)         |
| A_GAINERR_VDDA                  | Gain error   | –                | 0.2 | –                | %    | Reference Source: SRSS<br>(V <sub>REF</sub> = 1.20 V, V <sub>DDA</sub> < 2.2 V),<br>(V <sub>REF</sub> = 1.6 V, 2.2 V < V <sub>DDA</sub> < 2.7 V),<br>(V <sub>REF</sub> = 2.13 V, V <sub>DDA</sub> > 2.7 V)         |
| A_OFFSET_VREF                   | Input offset voltage   | –                | 0.5 | –                | LSB  | After ADC calibration, Ref. SRC = SRSS, (V <sub>REF</sub> = 1.20 V, V <sub>DDA</sub> < 2.2 V), (V <sub>REF</sub> = 1.6 V, 2.2 V < V <sub>DDA</sub> < 2.7 V), (V <sub>REF</sub> = 2.13 V, V <sub>DDA</sub> > 2.7 V) |
| A_OFFSET_VDDA                   | Input offset voltage   | –                | 0.5 | –                | LSB  | After ADC calibration, Ref. SRC = SRSS, (V <sub>REF</sub> = 1.20 V, V <sub>DDA</sub> < 2.2 V), (V <sub>REF</sub> = 1.6 V, 2.2 V < V <sub>DDA</sub> < 2.7 V), (V <sub>REF</sub> = 2.13 V, V <sub>DDA</sub> > 2.7 V) |
| A_ISAR_VREF                     | Current consumption  | –                | 0.3 | –                | mA   | CSD ADC Block current  |
| A_ISAR_VDDA                     | Current consumption  | –                | 0.3 | –                | mA   | CSD ADC Block current  |
| A_VINS_VREF                     | Input voltage range - single ended   | V <sub>SSA</sub> | –   | V <sub>REF</sub> | V    | (V <sub>REF</sub> = 1.20 V, V <sub>DDA</sub> < 2.2 V), (V <sub>REF</sub> = 1.6 V, 2.2 V < V <sub>DDA</sub> < 2.7 V), (V <sub>REF</sub> = 2.13 V, V <sub>DDA</sub> > 2.7 V)   |
| A_VINS_VDDA                     | Input voltage range - single ended   | V <sub>SSA</sub> | –   | V <sub>DDA</sub> | V    | (V <sub>REF</sub> = 1.20 V, V <sub>DDA</sub> < 2.2 V), (V <sub>REF</sub> = 1.6 V, 2.2 V < V <sub>DDA</sub> < 2.7 V), (V <sub>REF</sub> = 2.13 V, V <sub>DDA</sub> > 2.7 V)   |
| A_INRES                         | Input charging resistance  | –                | 15  | –                | kΩ   | –  |
| A_INCAP                         | Input capacitance  | –                | 41  | –                | pF   | –  |
| A_PSR                           | Power supply rejection ratio (DC)  | –                | 60  | –                | dB   | –  |
| A_TACQ                          | Sample acquisition time  | –                | 10  | –                | μs   | Measured with 50 Ω source impedance. 10 μs is default software driver acquisition time setting. Settling to within 0.05%.  |
| A_CONV8                         | Conversion time for 8-bit resolution at conversion rate = F <sub>hclk</sub> /(2 × (N + 2)). Clock frequency = 50 MHz.  | –                | 25  | –                | μs   | Does not include acquisition time  |
| A_CONV10                        | Conversion time for 10-bit resolution at conversion rate = F <sub>hclk</sub> /(2 × (N + 2)). Clock frequency = 50 MHz. | –                | 60  | –                | μs   | Does not include acquisition time  |
| A_SND_VRE                       | Signal-to-noise and Distortion ratio (SINAD)   | –                | 57  | –                | dB   | Measured with 50 Ω source impedance  |
| A_SND_VDDA                      | SINAD  | –                | 52  | –                | dB   | Measured with 50 Ω source impedance  |
| A_INL_VREF                      | Integral nonlinearity – 11.6 ksp   | –                | –   | 2                | LSB  | Measured with 50 Ω source impedance  |
| A_INL_VDDA                      | Integral nonlinearity – 11.6 ksp   | –                | –   | 2                | LSB  | Measured with 50 Ω source impedance  |

**Table 22. CSD ADC Specifications (continued)**

| Parameter  | Description                          | Min | Typ | Max | Unit | Details/Conditions                  |
|------------|--------------------------------------|-----|-----|-----|------|-------------------------------------|
| A_DNL_VREF | Differential nonlinearity – 11.6 ksp | –   | –   | 1   | LSB  | Measured with 50 Ω source impedance |
| A_DNL_VDDA | Differential nonlinearity – 11.6 ksp | –   | –   | 1   | LSB  | Measured with 50 Ω source impedance |

## Digital Peripherals

**Table 23. Timer/Counter/PWM (TCPWM) Specifications**

| Parameter             | Description                                      | Min                | Typ | Max | Unit | Details/Conditions  |
|-----------------------|--|--------------------|-----|-----|------|---|
| I <sub>TCPWM1</sub>   | Block current consumption at 8 MHz               | –                  | –   | 70  | μA   | All modes (TCPWM)   |
| I <sub>TCPWM2</sub>   | Block current consumption at 24 MHz              | –                  | –   | 180 | μA   | All modes (TCPWM)   |
| I <sub>TCPWM3</sub>   | Block current consumption at 50 MHz              | –                  | –   | 270 | μA   | All modes (TCPWM)   |
| I <sub>TCPWM4</sub>   | Block current consumption at 100 MHz             | –                  | –   | 540 | μA   | All modes (TCPWM)   |
| TCPWM <sub>FREQ</sub> | Operating frequency                              | –                  | –   | 100 | MHz  | F <sub>cmax</sub> = F <sub>cpu</sub><br>Maximum = 100 MHz   |
| TPWM <sub>ENEXT</sub> | Input trigger pulse width for all trigger events | 2/F <sub>c</sub>   | –   | –   | ns   | Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected |
| TPWM <sub>EXT</sub>   | Output trigger pulse widths                      | 1.5/F <sub>c</sub> | –   | –   | ns   | Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs                |
| TC <sub>RES</sub>     | Resolution of counter                            | 1/F <sub>c</sub>   | –   | –   | ns   | Minimum time between successive counts  |
| PWM <sub>RES</sub>    | PWM resolution                                   | 1/F <sub>c</sub>   | –   | –   | ns   | Minimum pulse width of PWM output   |
| Q <sub>RES</sub>      | Quadrature inputs resolution                     | 2/F <sub>c</sub>   | –   | –   | ns   | Minimum pulse width between Quadrature phase inputs. Delays from pins should be similar                             |

**Table 24. Serial Communication Block (SCB) Specifications**

| Parameter   | Description  | Min | Typ | Max                          | Unit | Details/Conditions                                    |
|---|--|-----|-----|------------------------------|------|---|
| <b>Fixed I<sup>2</sup>C DC Specifications</b>   |  |     |     |                              |      |   |
| I <sub>I2C1</sub>   | Block current consumption at 100 kHz   | –   | –   | 30                           | μA   | –   |
| I <sub>I2C2</sub>   | Block current consumption at 400 kHz   | –   | –   | 80                           | μA   | –   |
| I <sub>I2C3</sub>   | Block current consumption at 1 Mbps  | –   | –   | 180                          | μA   | –   |
| I <sub>I2C4</sub>   | I <sup>2</sup> C enabled in Deep Sleep mode  | –   | –   | 1.7                          | μA   | At 60 °C  |
| <b>Fixed I<sup>2</sup>C AC Specifications</b>   |  |     |     |                              |      |   |
| F <sub>I2C1</sub>   | Bit Rate   | –   | –   | 1                            | Mbps | –   |
| <b>Fixed UART DC Specifications</b>   |  |     |     |                              |      |   |
| I <sub>UART1</sub>  | Block current consumption at 100 Kbps  | –   | –   | 30                           | μA   | –   |
| I <sub>UART2</sub>  | Block current consumption at 1000 Kbps   | –   | –   | 180                          | μA   | –   |
| <b>Fixed UART AC Specifications</b>   |  |     |     |                              |      |   |
| F <sub>UART1</sub>  | Bit Rate   | –   | –   | 3                            | Mbps | ULP mode  |
| F <sub>UART2</sub>  |  | –   | –   | 8                            |      | LP mode   |
| <b>Fixed SPI DC Specifications</b>  |  |     |     |                              |      |   |
| I <sub>SPI1</sub>   | Block current consumption at 1 Mbps  | –   | –   | 220                          | μA   | –   |
| I <sub>SPI2</sub>   | Block current consumption at 4 Mbps  | –   | –   | 340                          | μA   | –   |
| I <sub>SPI3</sub>   | Block current consumption at 8 Mbps  | –   | –   | 360                          | μA   | –   |
| I <sub>SPI4</sub>   | Block current consumption at 25 Mbps   | –   | –   | 800                          | μA   | –   |
| <b>Fixed SPI AC Specifications for LP Mode (1.1 V) unless noted otherwise</b>             |  |     |     |                              |      |   |
| F <sub>SPI</sub>  | SPI operating frequency Master and externally clocked slave                          | –   | –   | 25                           | MHz  | 14-MHz maximum for ULP (0.9 V) mode                   |
| F <sub>SPI_IC</sub>   | SPI Slave internally clocked   | –   | –   | 15                           | MHz  | 5 MHz maximum for ULP (0.9 V) mode                    |
| <b>Fixed SPI Master mode AC Specifications for LP Mode (1.1 V) unless noted otherwise</b> |  |     |     |                              |      |   |
| T <sub>DMO</sub>  | master out, slave in (MOSI) valid after SClk driving edge                            | –   | –   | 12                           | ns   | 20 ns maximum for ULP (0.9 V) mode                    |
| T <sub>DSI</sub>  | MISO valid before SClk capturing edge  | 5   | –   | –                            | ns   | Full clock, late master in, slave out (MISO) sampling |
| T <sub>HMO</sub>  | MOSI data hold time  | 0   | –   | –                            | ns   | Referred to slave capturing edge                      |
| <b>Fixed SPI Slave mode AC Specifications for LP Mode (1.1 V) unless noted otherwise</b>  |  |     |     |                              |      |   |
| T <sub>DMI</sub>  | MOSI valid before SClk capturing edge  | 5   | –   | –                            | ns   | –   |
| T <sub>D<sub>SO</sub>_EXT</sub>   | MISO valid after SClk driving edge in external clock mode                            | –   | –   | 20                           | ns   | 35 ns maximum for ULP (0.9 V) mode                    |
| T <sub>D<sub>SO</sub></sub>   | MISO valid after SClk driving edge in internal clock mode                            | –   | –   | $T_{DSO\_EXT} + 3 * T_{scb}$ | ns   | T <sub>scb</sub> is SCB clock period                  |
| T <sub>D<sub>SO</sub></sub>   | MISO valid after SClk driving edge in internal clock mode with median filter enabled | –   | –   | $T_{DSO\_EXT} + 4 * T_{scb}$ | ns   | T <sub>scb</sub> is SCB clock period                  |
| T <sub>H<sub>SO</sub></sub>   | Previous MISO data hold time   | 5   | –   | –                            | ns   | –   |
| TSSEL <sub>SCK1</sub>   | SSEL valid to first SCK valid edge   | 65  | –   | –                            | ns   | –   |
| TSSEL <sub>SCK2</sub>   | SSEL hold after Last SCK valid edge  | 65  | –   | –                            | ns   | –   |

*LCD Specifications*
**Table 25. LCD Direct Drive DC Specifications**

| Parameter      | Description  | Min | Typ | Max  | Unit    | Details/Conditions                    |
|----------------|--|-----|-----|------|---------|---------------------------------------|
| $I_{LCDLOW}$   | Operating current in low-power mode                | –   | 5   | –    | $\mu A$ | 16 x 4 small segment display at 50 Hz |
| $C_{LDCAP}$    | LCD capacitance per segment/common driver          | –   | 500 | 5000 | pF      | –                                     |
| $LCD_{OFFSET}$ | Long-term segment offset                           | –   | 20  | –    | mV      | –                                     |
| $I_{LCDOP1}$   | PWM mode current.<br>3.3-V bias. 8-MHz IMO. 25 °C. | –   | 0.6 | –    | mA      | 32 x 4 segments 50 Hz                 |
| $I_{LCDOP2}$   | PWM mode current.<br>3.3-V bias. 8-MHz IMO. 25 °C. | –   | 0.5 | –    | mA      | 32 x 4 segments 50 Hz                 |

**Table 26. LCD Direct Drive AC Specifications**

| Parameter | Description    | Min | Typ | Max | Unit | Details/Conditions |
|-----------|----------------|-----|-----|-----|------|--------------------|
| $F_{LCD}$ | LCD frame rate | 10  | 50  | 150 | Hz   | –                  |

**Memory**
**Table 27. Flash Specifications**

| Parameter                      | Description   | Min   | Typ | Max | Unit    | Details/Conditions      |
|--------------------------------|---|-------|-----|-----|---------|-------------------------|
| <b>Flash DC Specifications</b> |   |       |     |     |         |                         |
| VPE                            | Erase and program voltage                           | 1.71  | –   | 3.6 | V       | –                       |
| <b>Flash AC Specifications</b> |   |       |     |     |         |                         |
| $T_{ROWWRITE}$                 | Row (Block) write time (erase & program)            | –     | –   | 16  | ms      | Row (Block) = 512 bytes |
| $T_{ROWERASE}$                 | Row erase time                                      | –     | –   | 11  | ms      | –                       |
| $T_{ROWPROGRAM}$               | Row program time after erase                        | –     | –   | 5   | ms      | –                       |
| $T_{BULKERASE}$                | Bulk erase time (1024 KB)                           | –     | –   | 11  | ms      | –                       |
| $T_{SECTORERASE}$              | Sector erase time (256 KB)                          | –     | –   | 11  | ms      | 512 rows per sector     |
| $T_{SSERIAE}$                  | Sub-sector erase time                               | –     | –   | 11  | ms      | 8 rows per sub-sector   |
| $T_{SSWRITE}$                  | Sub-sector write time; 1 erase plus 8 program times | –     | –   | 51  | ms      | –                       |
| $T_{SWRITE}$                   | Sector write time; 1 erase plus 512 program times   | –     | –   | 2.6 | seconds | –                       |
| $T_{DEVPROG}$                  | Total device program time                           | –     | –   | 15  | seconds | –                       |
| $F_{END}$                      | Flash Endurance                                     | 100 K | –   | –   | cycles  | –                       |
| $F_{RET1}$                     | Flash Retention. $T_a \leq 25$ °C, 100 K P/E cycles | 10    | –   | –   | years   | –                       |
| $F_{RET2}$                     | Flash Retention. $T_a \leq 85$ °C, 10 K P/E cycles  | 10    | –   | –   | years   | –                       |
| $F_{RET3}$                     | Flash Retention. $T_a \leq 55$ °C, 20 K P/E cycles  | 20    | –   | –   | years   | –                       |
| $T_{WS100}$                    | Number of Wait states at 100 MHz                    | 3     | –   | –   | –       | –                       |
| $T_{WS50}$                     | Number of Wait states at 50 MHz                     | 2     | –   | –   | –       | –                       |

**Note**

- It can take as much as 16 ms to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdog. Make certain that these are not inadvertently activated.



**System Resources**
**Table 28. CYBLE-416045-02 System Resources**

| Parameter                                  | Description  | Min  | Typ  | Max  | Unit  | Details/Conditions                           |
|--|--|------|------|------|-------|--|
| <b>POR with Brownout DC Specifications</b> |  |      |      |      |       |  |
| <b>Precise POR (PPOR)</b>                  |  |      |      |      |       |  |
| V <sub>FALLPPOR</sub>                      | BOD trip voltage in Active and Sleep modes, V <sub>DDD</sub> | 1.54 | –    | –    | V     | BOD Reset guaranteed for levels below 1.54 V |
| V <sub>FALLDPSLP</sub>                     | BOD trip voltage in Deep Sleep, V <sub>DDD</sub>             | 1.54 | –    | –    | V     | –  |
| V <sub>DDRAMP</sub>                        | Maximum power supply ramp rate (any supply)                  | –    | –    | 100  | mV/μs | Active mode                                  |
| <b>POR with Brownout AC Specification</b>  |  |      |      |      |       |  |
| V <sub>DDRAMP_DS</sub>                     | Maximum power supply ramp rate (any supply) in Deep Sleep    | –    | –    | 10   | mV/μs | BOD operation guaranteed                     |
| <b>Voltage Monitors DC Specifications</b>  |  |      |      |      |       |  |
| V <sub>HVD0</sub>                          | –  | 1.18 | 1.23 | 1.27 | V     | –  |
| V <sub>HVD1</sub>                          | –  | 1.38 | 1.43 | 1.47 | V     | –  |
| V <sub>HVD2</sub>                          | –  | 1.57 | 1.63 | 1.68 | V     | –  |
| V <sub>HVD3</sub>                          | –  | 1.76 | 1.83 | 1.89 | V     | –  |
| V <sub>HVD4</sub>                          | –  | 1.95 | 2.03 | 2.1  | V     | –  |
| V <sub>HVD5</sub>                          | –  | 2.05 | 2.13 | 2.2  | V     | –  |
| V <sub>HVD6</sub>                          | –  | 2.15 | 2.23 | 2.3  | V     | –  |
| V <sub>HVD7</sub>                          | –  | 2.24 | 2.33 | 2.41 | V     | –  |
| V <sub>HVD8</sub>                          | –  | 2.34 | 2.43 | 2.51 | V     | –  |
| V <sub>HVD9</sub>                          | –  | 2.44 | 2.53 | 2.61 | V     | –  |
| V <sub>HVD10</sub>                         | –  | 2.53 | 2.63 | 2.72 | V     | –  |
| V <sub>HVD11</sub>                         | –  | 2.63 | 2.73 | 2.82 | V     | –  |
| V <sub>HVD12</sub>                         | –  | 2.73 | 2.83 | 2.92 | V     | –  |
| V <sub>HVD13</sub>                         | –  | 2.82 | 2.93 | 3.03 | V     | –  |
| V <sub>HVD14</sub>                         | –  | 2.92 | 3.03 | 3.13 | V     | –  |
| V <sub>HVD15</sub>                         | –  | 3.02 | 3.13 | 3.23 | V     | –  |
| LVI_IDD                                    | Block current  | –    | 5    | 15   | μA    | –  |
| <b>Voltage Monitors AC Specification</b>   |  |      |      |      |       |  |
| T <sub>MONTRIP</sub>                       | Voltage monitor trip time                                    | –    | –    | 170  | ns    | –  |

*SWD Interface*
**Table 29. SWD and Trace Specifications**

| Parameter                      | Description   | Min        | Typ | Max       | Unit | Details/Conditions                   |
|--------------------------------|---|------------|-----|-----------|------|--------------------------------------|
| <b>SWD and Trace Interface</b> |   |            |     |           |      |                                      |
| F_SWCLK2                       | $1.71\text{ V} \leq V_{DD} \leq 3.6\text{ V}$           | –          | –   | 25        | MHz  | LP mode. $V_{CCD} = 1.1\text{ V}$    |
| F_SWCLK2L                      | $1.71\text{ V} \leq V_{DD} \leq 3.6\text{ V}$           | –          | –   | 12        | MHz  | ULP mode. $V_{CCD} = 0.9\text{ V}$ . |
| T_SWDI_SETUP                   | $T = 1/f\text{ SWCLK}$                                  | $0.25 * T$ | –   | –         | ns   | –                                    |
| T_SWDI_HOLD                    | $T = 1/f\text{ SWCLK}$                                  | $0.25 * T$ | –   | –         | ns   | –                                    |
| T_SWDO_VALID                   | $T = 1/f\text{ SWCLK}$                                  | –          | –   | $0.5 * T$ | ns   | –                                    |
| T_SWDO_HOLD                    | $T = 1/f\text{ SWCLK}$                                  | 1          | –   | –         | ns   | –                                    |
| F_TRCLK_LP1                    | With Trace Data setup/hold times of 2/1 ns respectively | –          | –   | 75        | MHz  | LP mode. $V_{DD} = 1.1\text{ V}$     |
| F_TRCLK_LP2                    | With Trace Data setup/hold times of 3/2 ns respectively | –          | –   | 70        | MHz  | LP mode. $V_{DD} = 1.1\text{ V}$     |
| F_TRCLK_ULP                    | With Trace Data setup/hold times of 3/2 ns respectively | –          | –   | 25        | MHz  | ULP mode. $V_{DD} = 0.9\text{ V}$    |

*Internal Main Oscillator*
**Table 30. IMO DC Specifications**

| Parameter         | Description                    | Min | Typ | Max | Unit | Details/Conditions |
|-------------------|--------------------------------|-----|-----|-----|------|--------------------|
| I <sub>IMO1</sub> | IMO operating current at 8 MHz | –   | 9   | 15  | μA   | –                  |

**Table 31. IMO AC Specifications**

| Parameter            | Description                           | Min | Typ | Max | Unit | Details/Conditions |
|----------------------|---------------------------------------|-----|-----|-----|------|--------------------|
| F <sub>IMOTOL1</sub> | Frequency variation centered on 8 MHz | –   | –   | ±2  | %    | –                  |
| T <sub>JITR</sub>    | Cycle-to-Cycle and Period jitter      | –   | 250 | –   | ps   | –                  |

*Internal Low-Speed Oscillator*
**Table 32. ILO DC Specification**

| Parameter         | Description                     | Min | Typ | Max | Unit | Details/Conditions |
|-------------------|---------------------------------|-----|-----|-----|------|--------------------|
| I <sub>ILO2</sub> | ILO operating current at 32 kHz | –   | 0.3 | 0.7 | μA   | –                  |

**Table 33. ILO AC Specifications**

| Parameter              | Description              | Min  | Typ | Max  | Unit | Details/Conditions                     |
|------------------------|--------------------------|------|-----|------|------|--|
| T <sub>STARTILO1</sub> | ILO startup time         | –    | –   | 7    | μs   | Startup time to 95% of final frequency |
| T <sub>LIODUTY</sub>   | ILO duty cycle           | 45   | 50  | 55   | %    | –                                      |
| F <sub>ILOTRIM1</sub>  | 32-kHz trimmed frequency | 28.8 | 32  | 35.2 | kHz  | ±10% variation                         |

**Table 34. UDB AC Specifications**

| Parameter   | Description  | Min | Typ | Max | Unit | Details/Conditions |
|---|--|-----|-----|-----|------|--------------------|
| <b>Data Path Performance</b>  |  |     |     |     |      |                    |
| F <sub>MAX-TIMER</sub>  | Maximum frequency of 16-bit timer in a UDB pair        | –   | –   | 100 | MHz  | –                  |
| F <sub>MAX-ADDER</sub>  | Maximum frequency of 16-bit adder in a UDB pair        | –   | –   | 100 | MHz  | –                  |
| F <sub>MAX-CRC</sub>  | Maximum frequency of 16-bit CRC/PRS in a UDB pair      | –   | –   | 100 | MHz  | –                  |
| <b>PLD Performance in UDB</b>   |  |     |     |     |      |                    |
| F <sub>MAX-PLD</sub>  | Maximum frequency of 2-pass PLD function in a UDB pair | –   | –   | 100 | MHz  | –                  |
| <b>Clock to Output Performance</b>                                      |  |     |     |     |      |                    |
| T <sub>CLK_OUT_UBB1</sub>   | Propagation delay for clock in to data out             | –   | 5   | –   | ns   | –                  |
| <b>UDB Port Adapter Specifications</b>                                  |  |     |     |     |      |                    |
| <i>Conditions: 10-pF load, 3-V V<sub>DDIO</sub> and V<sub>DDD</sub></i> |  |     |     |     |      |                    |
| T <sub>LCLKDO</sub>   | L <sub>CLK</sub> to output delay                       | –   | –   | 11  | ns   | –                  |
| T <sub>DINLCLK</sub>  | Input setup time to L <sub>CLK</sub> rising edge       | –   | –   | 7   | ns   | –                  |
| T <sub>DINLCLKHLD</sub>   | Input hold time from L <sub>CLK</sub> rising edge      | 5   | –   | –   | ns   | –                  |
| T <sub>LCLKHIZ</sub>  | L <sub>CLK</sub> to output tristate                    | –   | –   | 28  | ns   | –                  |
| T <sub>FLCLK</sub>  | L <sub>CLK</sub> frequency                             | –   | –   | 33  | MHz  | –                  |
| T <sub>LCLKDUTY</sub>   | L <sub>CLK</sub> duty cycle (percentage high)          | 40% | –   | 60% | %    | –                  |

**Table 35. Audio Subsystem Specifications**

| Parameter                             | Description                                       | Min   | Typ   | Max    | Unit | Details/Conditions                 |
|---------------------------------------|---|-------|-------|--------|------|------------------------------------|
| <b>Audio Subsystem specifications</b> |   |       |       |        |      |                                    |
| <b>PDM Specifications</b>             |   |       |       |        |      |                                    |
| PDM_IDD1                              | PDM active current, Stereo operation, 1-MHz clock | –     | 175   | –      | μA   | 16-bit audio at 16 ksps            |
| PDM_IDD2                              | PDM active current, Stereo operation, 3-MHz clock | –     | 600   | –      | μA   | 24-bit audio at 48 ksps            |
| PDM_JITTER                            | RMS jitter in PDM clock                           | –200  | –     | 200    | ps   |                                    |
| PDM_CLK                               | PDM clock speed                                   | 0.384 | –     | 3.072  | MHz  |                                    |
| PDM_BLK_CLK                           | PDM block input clock                             | 1.024 | –     | 49.152 | MHz  |                                    |
| PDM_SETUP                             | Data input setup time to PDM_CLK edge             | 10    | –     | –      | ns   |                                    |
| PDM_HOLD                              | Data input hold time to PDM_CLK edge              | 10    | –     | –      | ns   |                                    |
| PDM_OUT                               | Audio sample rate                                 | 8     | –     | 48     | ksps |                                    |
| PDM_WL                                | Word length                                       | 16    | –     | 24     | bits |                                    |
| PDM_SNR                               | Signal-to-noise ratio (A-weighted)                | –     | 100   | –      | dB   | PDM input, 20 Hz to 20 kHz BW      |
| PDM_DR                                | Dynamic range (A-weighted)                        | –     | 100   | –      | dB   | 20 Hz to 20 kHz BW, -60 dB FS      |
| PDM_FR                                | Frequency response                                | –0.2  | –     | 0.2    | dB   | DC to 0.45. DC Blocking filter OFF |
| PDM_SB                                | Stop band   | –     | 0.566 | –      | f    | –                                  |
| PDM_SBA                               | Stop band attenuation                             | –     | 60    | –      | dB   | –                                  |

**Table 35. Audio Subsystem Specifications (continued)**

| Parameter   | Description  | Min                        | Typ | Max                     | Unit | Details/Conditions                                 |
|---|--|----------------------------|-----|-------------------------|------|--|
| PDM_GAIN  | Adjustable gain  | -12                        | -   | 10.5                    | dB   | PDM to PCM, 1.5 dB/step                            |
| PDM_ST  | Startup time   | -                          | 48  | -                       | -    | Word Select (WS) cycles                            |
| <b>I2S Specifications (same for LP and ULP modes unless stated otherwise)</b> |  |                            |     |                         |      |  |
| I <sup>2</sup> S_WORD   | Length of I <sup>2</sup> S word                                  | 8                          | -   | 32                      | bits | -  |
| I <sup>2</sup> S_WS   | Word clock frequency in LP mode                                  | -                          | -   | 192                     | kHz  | 12.288 MHz bit clock with 32-bit word              |
| I <sup>2</sup> S_WS_U   | Word clock frequency in ULP mode                                 | -                          | -   | 48                      | kHz  | 3.072 MHz bit clock with 32-bit word               |
| I <sup>2</sup> S_WS_TDM   | Word clock frequency in TDM mode for LP                          | -                          | -   | 48                      | kHz  | 8 32-bit channels                                  |
| I <sup>2</sup> S_WS_TDM_U   | Word clock frequency in TDM mode for ULP                         | -                          | -   | 12                      | kHz  | 8 32-bit channels                                  |
| <b>I2S Slave Mode</b>   |  |                            |     |                         |      |  |
| TS_WS   | WS setup time to the following rising edge of SCK for LP mode    | 5                          | -   | -                       | ns   | -  |
| TS_WS   | WS setup time to the following rising edge of SCK for ULP mode   | 11                         | -   | -                       | ns   | -  |
| TH_WS   | WS hold time to the following edge of SCK                        | $\frac{TMCLK\_SOC}{5}$     | -   | -                       | ns   | -  |
| TD_SDO  | Delay time of TX_SDO transition from edge of TX_SCK for LP mode  | $-(\frac{TMCLK\_SOC}{25})$ | -   | $\frac{TMCLK\_SOC}{25}$ | ns   | Associated clock edge depends on selected polarity |
| TD_SDO  | Delay time of TX_SDO transition from edge of TX_SCK for ULP mode | $-(\frac{TMCLK\_SOC}{70})$ | -   | $\frac{TMCLK\_SOC}{70}$ | ns   | Associated clock edge depends on selected polarity |
| TS_SDI  | RX_SDI setup time to the following edge of RX_SCK in LP mode     | 5                          | -   | -                       | ns   | -  |
| TS_SDI  | RX_SDI setup time to the following edge of RX_SCK in ULP mode    | 11                         | -   | -                       | ns   | -  |
| TH_SDI  | RX_SDI hold time to the rising edge of RX_SCK                    | $\frac{TMCLK\_SOC}{5}$     | -   | -                       | ns   | -  |
| T <sub>SCKCY</sub>  | TX/RX_SCK bit clock duty cycle                                   | 45                         | -   | 55                      | %    | -  |
| <b>I<sup>2</sup>S Master Mode</b>   |  |                            |     |                         |      |  |
| TD_WS   | WS transition delay from falling edge of SCK in LP mode          | -10                        | -   | 20                      | ns   | -  |
| TD_WS_U   | WS transition delay from falling edge of SCK in ULP mode         | -10                        | -   | 40                      | ns   | -  |
| TD_SDO  | SDO transition delay from falling edge of SCK in LP mode         | -10                        | -   | 20                      | ns   | -  |
| TD_SDO  | SDO transition delay from falling edge of SCK in ULP mode        | -10                        | -   | 40                      | ns   | -  |
| TS_SDI  | SDI setup time to the associated edge of SCK                     | 5                          | -   | -                       | ns   | Associated clock edge depends on selected polarity |

**Table 35. Audio Subsystem Specifications (continued)**

| Parameter   | Description                                 | Min              | Typ | Max    | Unit | Details/Conditions  |
|-------------|---|------------------|-----|--------|------|---|
| TH_SDI      | SDI hold time to the associated edge of SCK | $TMCLK\_SOC + 5$ | –   | –      | ns   | T is TX/RX_SCK bit clock period. Associated clock edge depends on selected polarity |
| T_SCKCY     | SCK bit clock duty cycle                    | 45               | –   | 55     | %    | –   |
| FMCLK_SOC   | MCLK_SOC frequency in LP mode               | 1.024            | –   | 98.304 | MHz  | FMCLK_SOC = 8 * Bit-clock   |
| FMCLK_SOC_U | MCLK_SOC frequency in ULP mode              | 1.024            | –   | 24.576 | MHz  | FMCLK_SOC_U = 8 * Bit-clock   |
| T_MCLKCY    | MCLK_SOC duty cycle                         | 45               | –   | 55     | %    | –   |
| T_JITTER    | MCLK_SOC input jitter                       | –100             | –   | 100    | ps   | –   |

**Table 36. Smart I/O Specifications**

| Parameter | Description              | Min | Typ | Max | Unit | Details/Conditions |
|-----------|--------------------------|-----|-----|-----|------|--------------------|
| SMIO_BYP  | Smart I/O bypass delay   | –   | –   | 2   | ns   | –                  |
| SMIO_LUT  | Smart I/O LUT prop delay | –   | TBD | –   | ns   | –                  |

**Table 37. BLE Subsystem Specifications**

| Parameter                                  | Description   | Min | Typ | Max | Unit | Details/Conditions                             |
|--|---|-----|-----|-----|------|--|
| <b>BLE Subsystem specifications</b>        |   |     |     |     |      |  |
| <b>RF Receiver Specifications (1 Mbps)</b> |   |     |     |     |      |  |
| RXS, IDLE                                  | RX Sensitivity with Ideal Transmitter   | –   | –95 | –   | dBm  | Across RF operating frequency range            |
| RXS, IDLE                                  | RX Sensitivity with Ideal Transmitter   | –   | –93 | –   | dBm  | 255-byte packet length, across frequency range |
| RXS, DIRTY                                 | RX Sensitivity with Dirty Transmitter   | –   | –92 | –   | dBm  | RF-PHY Specification (RCV-LE/CA/01/C)          |
| PRX <sub>MAX</sub>                         | Maximum received signal strength at < 0.1% PER  | –   | 0   | –   | dBm  | RF-PHY Specification (RCV-LE/CA/06/C)          |
| CI1  | Co-channel interference, Wanted Signal at –67 dBm and Interferer at FRX                                   | –   | 9   | 21  | dB   | RF-PHY Specification (RCV-LE/CA/03/C)          |
| CI2  | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 1 MHz                      | –   | 3   | 15  | dB   | RF-PHY Specification (RCV-LE/CA/03/C)          |
| CI3  | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 2 MHz                      | –   | –26 | –17 | dB   | RF-PHY Specification (RCV-LE/CA/03/C)          |
| CI4  | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at ≥ FRX ± 3 MHz                    | –   | –33 | –27 | dB   | RF-PHY Specification (RCV-LE/CA/03/C)          |
| CI5  | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at Image frequency (FIMAGE)         | –   | –20 | –9  | dB   | RF-PHY Specification (RCV-LE/CA/03/C)          |
| CI6  | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at Image frequency (FIMAGE ± 1 MHz) | –   | –28 | –15 | dB   | RF-PHY Specification (RCV-LE/CA/03/C)          |
| <b>RF Receiver Specifications (2 Mbps)</b> |   |     |     |     |      |  |
| RXS, IDLE                                  | RX Sensitivity with Ideal Transmitter   | –   | –92 | –   | dBm  | Across RF operating frequency range            |
| RXS, IDLE                                  | RX Sensitivity with Ideal Transmitter   | –   | –90 | –   | dBm  | 255-byte packet length, across frequency range |
| RXS, DIRTY                                 | RX Sensitivity with Dirty Transmitter   | –   | –89 | –   | dBm  | RF-PHY Specification (RCV-LE/CA/01/C)          |
| PRX <sub>MAX</sub>                         | Maximum received signal strength at < 0.1% PER  | –   | 0   | –   | dBm  | RF-PHY Specification (RCV-LE/CA/06/C)          |
| CI1  | Co-channel interference, Wanted Signal at –67 dBm and Interferer at FRX                                   | –   | 9   | 21  | dB   | RF-PHY Specification (RCV-LE/CA/03/C)          |
| CI2  | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 2 MHz                      | –   | 3   | 15  | dB   | RF-PHY Specification (RCV-LE/CA/03/C)          |
| CI3  | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 4 MHz                      | –   | –26 | –17 | dB   | RF-PHY Specification (RCV-LE/CA/03/C)          |
| CI4  | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at ± FRX ± 6 MHz                    | –   | –33 | –27 | dB   | RF-PHY Specification (RCV-LE/CA/03/C)          |

**Table 37. BLE Subsystem Specifications (continued)**

| Parameter                                       | Description   | Min  | Typ | Max | Unit | Details/Conditions  |
|---|---|------|-----|-----|------|---|
| CI5   | Adjacent channel interference<br>Wanted Signal at -67 dBm and Interferer at<br>Image frequency (FIMAGE)         | -    | -20 | -9  | dB   | RF-PHY Specification<br>(RCV-LE/CA/03/C)                  |
| CI6   | Adjacent channel interference<br>Wanted Signal at -67 dBm and Interferer at<br>Image frequency (FIMAGE ± 2 MHz) | -    | -28 | -15 | dB   | RF-PHY Specification<br>(RCV-LE/CA/03/C)                  |
| <b>RF Receiver Specification (1 and 2 Mbps)</b> |   |      |     |     |      |   |
| OBB1  | Out of Band blocking<br>Wanted Signal at -67 dBm and Interferer at<br>F = 30 -2000 MHz                          | -30  | -27 | -   | dBm  | RF-PHY Specification<br>(RCV-LE/CA/04/C)                  |
| OBB2  | Out of Band blocking<br>Wanted Signal at -67 dBm and Interferer at<br>F = 2003 -2399 MHz                        | -35  | -27 | -   | dBm  | RF-PHY Specification<br>(RCV-LE/CA/04/C)                  |
| OBB3  | Out of Band blocking<br>Wanted Signal at -67 dBm and Interferer at<br>F= 2484-2997 MHz                          | -35  | -27 | -   | dBm  | RF-PHY Specification<br>(RCV-LE/CA/04/C)                  |
| OBB4  | Out of Band blocking<br>Wanted Signal at -67 dBm and Interferer at<br>F= 3000-12750 MHz                         | -30  | -27 | -   | dBm  | RF-PHY Specification<br>(RCV-LE/CA/04/C)                  |
| IMD   | Intermodulation performance<br>Wanted Signal at -64 dBm and 1 Mbps BLE,<br>3rd, 4th and 5th offset channel      | -50  | -   | -   | dBm  | RF-PHY Specification<br>(RCV-LE/CA/05/C)                  |
| RXSE1   | Receiver Spurious emission<br>30 MHz to 1.0 GHz   | -    | -   | -57 | dBm  | 100 kHz measurement<br>bandwidth<br>ETSI EN300 328 V2.1.1 |
| RXSE2   | Receiver Spurious emission<br>1.0 GHz to 12.75 GHz  | -    | -   | -53 | dBm  | 1 MHz measurement<br>bandwidth<br>ETSI EN300 328 V2.1.1   |
| <b>RF Transmitter Specifications</b>            |   |      |     |     |      |   |
| TXP, ACC  | RF Power Accuracy   | -    | -   | 1   | dB   | -   |
| TXP, RANGE                                      | Frequency Accuracy  | -    | 24  | -   | dB   | -20 dBm to +4 dBm   |
| TXP, 0 dBm                                      | Output Power, 0 dB Gain Setting   | -    | 0   | -   | dBm  | -   |
| TXP, MAX  | Output Power, Maximum Power Setting   | -    | 4   | -   | dBm  | -   |
| TXP, MIN  | Output Power, Minimum Power Setting   | -    | -20 | -   | dBm  | -   |
| F2AVG   | Average Frequency Deviation for 10101010<br>pattern   | 185  | -   | -   | kHz  | RF-PHY Specification<br>(TRM-LE/CA/05/C)                  |
| F2AVG_2M  | Average Frequency Deviation for 10101010<br>pattern for 2 Mbps  | 370  | -   | -   | kHz  | RF-PHY Specification<br>(TRM-LE/CA/05/C)                  |
| F1AVG   | Average Frequency Deviation for 11110000<br>pattern   | 225  | 250 | 275 | kHz  | RF-PHY Specification<br>(TRM-LE/CA/05/C)                  |
| F1AVG_2M  | Average Frequency Deviation for 11110000<br>pattern for 2 Mbps  | 450  | 500 | 550 | kHz  | RF-PHY Specification<br>(TRM-LE/CA/05/C)                  |
| EO  | Eye opening = $\Delta F2AVG/\Delta F1AVG$   | 0.8  | -   | -   | -    | RF-PHY Specification<br>(TRM-LE/CA/05/C)                  |
| FTX, ACC  | Frequency Accuracy  | -150 | -   | 150 | kHz  | RF-PHY Specification<br>(TRM-LE/CA/06/C)                  |
| FTX, MAXDR                                      | Maximum Frequency Drift   | -50  | -   | 50  | kHz  | RF-PHY Specification<br>(TRM-LE/CA/06/C)                  |
| FTX, INITDR                                     | Initial Frequency Drift   | -20  | -   | 20  | kHz  | RF-PHY Specification<br>(TRM-LE/CA/06/C)                  |

**Table 37. BLE Subsystem Specifications (continued)**

| Parameter                       | Description  | Min  | Typ  | Max   | Unit               | Details/Conditions                    |
|---------------------------------|--|------|------|-------|--------------------|---------------------------------------|
| FTX, DR                         | Maximum Drift Rate   | -20  | -    | 20    | kHz/<br>50 $\mu$ s | RF-PHY Specification (TRM-LE/CA/06/C) |
| IBSE1                           | In Band Spurious Emission at 2 MHz offset (1 Mbps)<br>In Band Spurious Emission at 4 MHz offset (2 Mbps) | -    | -    | -20   | dBm                | RF-PHY Specification (TRM-LE/CA/03/C) |
| IBSE2                           | In Band Spurious Emission at 3 MHz offset (1 Mbps)<br>In Band Spurious Emission at 6 MHz offset (2 Mbps) | -    | -    | -30   | dBm                | RF-PHY Specification (TRM-LE/CA/03/C) |
| TXSE1                           | Transmitter Spurious Emissions (Averaging), < 1.0 GHz  | -    | -    | -55.5 | dBm                | FCC-15.247                            |
| TXSE2                           | Transmitter Spurious Emissions (Averaging), > 1.0 GHz  |      |      | -41.5 | dBm                | FCC-15.247                            |
| <b>General RF Specification</b> |  |      |      |       |                    |                                       |
| FREQ                            | RF Operating Frequency   | 2400 | -    | 2482  | MHz                | -                                     |
| CHBW                            | Channel Spacing  | -    | 2    | -     | MHz                | -                                     |
| DR1                             | On-air Data Rate (1 Mbps)  | -    | 1000 | -     | Kbps               | -                                     |
| DR2                             | On-air Data Rate (2 Mbps)  | -    | 2000 | -     | Kbps               | -                                     |
| TXSUP                           | Transmitter Startup time   | -    | 80   | 82    | $\mu$ s            | -                                     |
| RXSUP                           | Receiver Startup time  | -    | 80   | 82    | $\mu$ s            | -                                     |
| <b>RSSI Specification</b>       |  |      |      |       |                    |                                       |
| RSSI, ACC                       | RSSI Accuracy  | -4   | -    | 4     | dB                 | -95 dBm to -20 dBm measurement range  |
| RSSI, RES                       | RSSI Resolution  | -    | 1    | -     | dB                 | -                                     |
| RSSI, PER                       | RSSI Sample Period   | -    | 6    | -     | $\mu$ s            | -                                     |

**Table 38. Precision ILO (PILO) Specifications**

| Parameter         | Description                             | Min  | Typ   | Max | Unit    | Details/Conditions            |
|-------------------|---|------|-------|-----|---------|-------------------------------|
| I <sub>PILO</sub> | Operating current                       | -    | 1.2   | 4   | $\mu$ A | -                             |
| F <sub>PILO</sub> | PILO nominal frequency                  | -    | 32768 | -   | Hz      | T = 25 °C with 20 ppm crystal |
| ACC_PILO          | PILO accuracy with periodic calibration | -500 | -     | 500 | ppm     | -                             |



## Environmental Specifications

### Environmental Compliance

This Cypress BLE module is built in compliance with RoHS and Halogen Free (HF) directives. The Cypress module and components used to produce this module are RoHS and HF compliant.

### RF Certification

The CYBLE-416045-02 module is certified under the following RF certification standards:

- FCC ID: WAP6045
- CE
- ISED: 7922A-6045
- MIC: 201-180370

### Environmental Conditions

Table 39 describes the operating and storage conditions for the Cypress BLE module.

**Table 39. Environmental Conditions for CYBLE-416045-02**

| Description  | Minimum Specification | Maximum Specification       |
|--|-----------------------|-----------------------------|
| Operating temperature  | -40 °C                | 85 °C                       |
| Operating humidity (relative, non-condensation)              | 5%                    | 85%                         |
| Thermal ramp rate  | -                     | 3 °C/minute                 |
| Storage temperature  | -40 °C                | 85 °C                       |
| Storage temperature and humidity                             | -                     | 85 °C at 85%                |
| ESD: Module integrated into system components <sup>[9]</sup> | -                     | 15 kV Air<br>2.2 KV Contact |

### ESD and EMI Protection

Exposed components require special attention to ESD and EMI.

A grounded conductive layer inside the device enclosure is suggested for EMI and ESD performance. Any openings in the enclosure near the module should be surrounded by a grounded conductive layer to provide ESD protection and a low-impedance path to ground.

**Device Handling:** Proper ESD protocol must be followed in manufacturing to ensure component reliability.

**Note**

9. This does not apply to the RF pins (ANT, XTALI, and XTALO). RF pins (ANT, XTALI, and XTALO) are tested for 500 V HBM.

## Regulatory Information

### FCC

#### FCC NOTICE:

The device CYBLE-416045-02 complies with Part 15 of the FCC Rules. The device meets the requirements for modular transmitter approval as detailed in FCC public Notice DA00-1407. Transmitter Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

#### CAUTION:

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by Cypress Semiconductor may void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates and can radiate radio frequency energy and, if not installed and used in accordance with the instruction may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

#### LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that FCC labeling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor FCC identifier for this product as well as the FCC Notice above. The FCC identifier is FCC ID: WAP6045.

In any case the end product must be labeled exterior with "Contains FCC ID: WAP6045".

#### ANTENNA WARNING:

This device is tested with a standard SMA connector and with the antennas listed in [Table 8](#) on page 21. When integrated in the OEMs product, these fixed antennas require installation preventing end-users from replacing them with non-approved antennas. Any antenna not in the following table must be tested to comply with FCC Section 15.203 for unique antenna connectors and Section 15.247 for emissions.

#### RF EXPOSURE:

To comply with FCC RF Exposure requirements, the OEM must ensure to install the approved antenna in the previous.

The preceding statement must be included as a CAUTION statement in manuals, for products operating with the approved antennas in [Table 8](#) on page 21, to alert users on FCC RF Exposure compliance. Any notification to the end user of installation or removal instructions about the integrated radio module is not allowed.

The radiated output power of CYBLE-416045-02 is far below the FCC radio frequency exposure limits. Nevertheless, use CYBLE-416045-02 in such a manner that minimizes the potential for human contact during normal operation.

End users may not be provided with the module installation instructions. OEM integrators and end users must be provided with transmitter operating conditions for satisfying RF exposure compliance.

## ISED

### Innovation, Science and Economic Development (ISED) Canada Certification

CYBLE-416045-02 is licensed to meet the regulatory requirements of Innovation, Science and Economic Development (ISED) Canada.

License: IC: 7922A-6045

Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from [www.ic.gc.ca](http://www.ic.gc.ca).

This device has been designed to operate with the antennas listed in [Table 8](#) on page 21, having a maximum gain of -0.5 dBi. Antennas not included in [Table 8](#) on page 21 or having a gain greater than -0.5 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms. The antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

#### ISED NOTICE:

The device CYBLE-416045-02 including the built-in trace antenna complies with Canada RSS-GEN Rules. The device meets the requirements for modular transmitter approval as detailed in RSS-GEN. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

L'appareil CYBLE-416045-02, y compris l'antenne intégrée, est conforme aux Règles RSS-GEN de Canada. L'appareil répond aux exigences d'approbation de l'émetteur modulaire tel que décrit dans RSS-GEN. L'opération est soumise aux deux conditions suivantes: (1) Cet appareil ne doit pas causer d'interférences nuisibles, et (2) Cet appareil doit accepter toute interférence reçue, y compris les interférences pouvant entraîner un fonctionnement indésirable.

#### ISED INTERFERENCE STATEMENT FOR CANADA

This device complies with Innovation, Science and Economic Development (ISED) Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil est conforme à la norme sur l'innovation, la science et le développement économique (ISED) norme RSS exempte de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

#### ISED RADIATION EXPOSURE STATEMENT FOR CANADA

This equipment complies with ISED radiation exposure limits set forth for an uncontrolled environment.

Cet équipement est conforme aux limites d'exposition aux radiations ISED prévues pour un environnement incontrôlé.

#### LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that ISED labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor IC identifier for this product as well as the ISED Notices above. The IC identifier is 7922A-6045. In any case, the end product must be labeled in its exterior with "Contains IC: 7922A-6045".

Le fabricant d'équipement d'origine (OEM) doit s'assurer que les exigences d'étiquetage ISED sont respectées. Cela comprend une étiquette clairement visible à l'extérieur de l'enceinte OEM spécifiant l'identifiant Cypress Semiconductor IC approprié pour ce produit ainsi que l'avis ISED ci-dessus. L'identificateur IC est 7922A-6045. En tout cas, le produit final doit être étiqueté dans son extérieur avec "Contient IC: 7922A-6045".

### European Declaration of Conformity

Hereby, Cypress Semiconductor declares that the Bluetooth module CYBLE-416045-02 complies with the essential requirements and other relevant provisions of Directive 2014. As a result of the conformity assessment procedure described in Annex III of the Directive 2014, the end-customer equipment should be labeled as follows:



All versions of the CYBLE-416045-02 in the specified reference design can be used in the following countries: Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, The Netherlands, the United Kingdom, Switzerland, and Norway.

### MIC Japan

CYBLE-416045-02 is certified as a module with type certification number 201-180370. End products that integrate CYBLE-416045-02 do not need additional MIC Japan certification for the end product.

End product can display the certification label of the embedded module.

Model Name: EZ-BLE PSoC Module

Part Number: CYBLE-416045-02

Manufactured by Cypress Semiconductor.

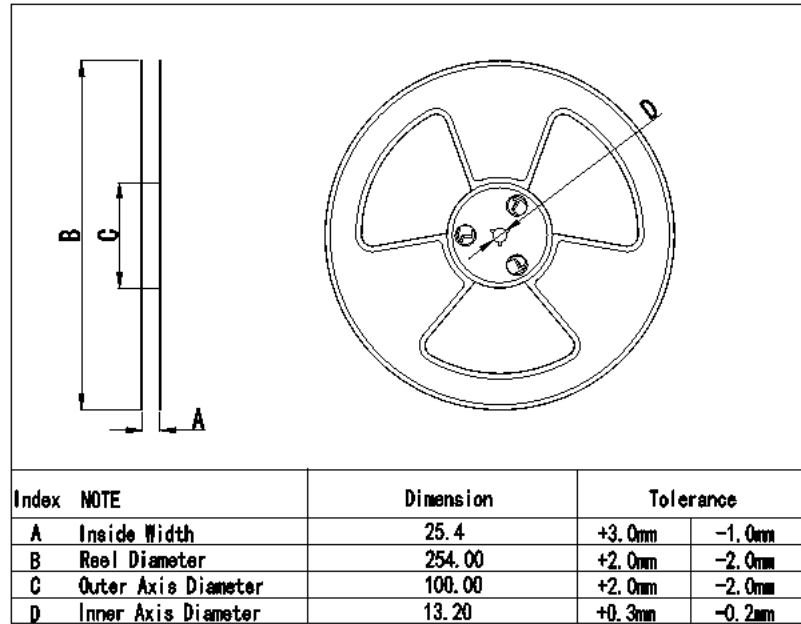


201-180370



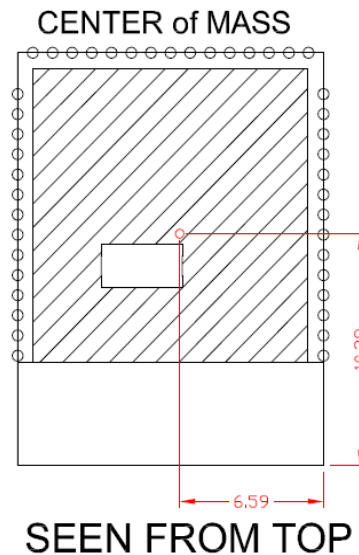
Figure 13 details reel dimensions used for the CYBLE-416045-02.

Figure 13. Reel Dimensions



The CYBLE-416045-02 is designed to be used with pick-and-place equipment in an SMT manufacturing environment. The center-of-mass for the CYBLE-416045-02 is detailed in Figure 14.

Figure 14. CYBLE-416045-02 Center of Mass



## Ordering Information

Table 42 lists the CYBLE-416045-02 part number and features. Table 43 lists the reel shipment quantities for the CYBLE-416045-02.

**Table 42. Ordering Information**

| MPN             | Features       |                 |            |           |     |          |                  |                |                |            |         |      | Package |
|-----------------|----------------|-----------------|------------|-----------|-----|----------|------------------|----------------|----------------|------------|---------|------|---------|
|                 | CPU Speed (M4) | CPU Speed (M0+) | Flash (KB) | SRAM (KB) | UDB | CapSense | Direct LCD Drive | 12-bit SAR ADC | LP Comparators | SCB Blocks | I2S/PDM | GPIO |         |
| CYBLE-416045-02 | 150/50         | 100/25          | 1024       | 288       | 12  | ✓        | ✓                | 1 Msps         | 2              | 5          | ✓       | 36   | 43-SMT  |

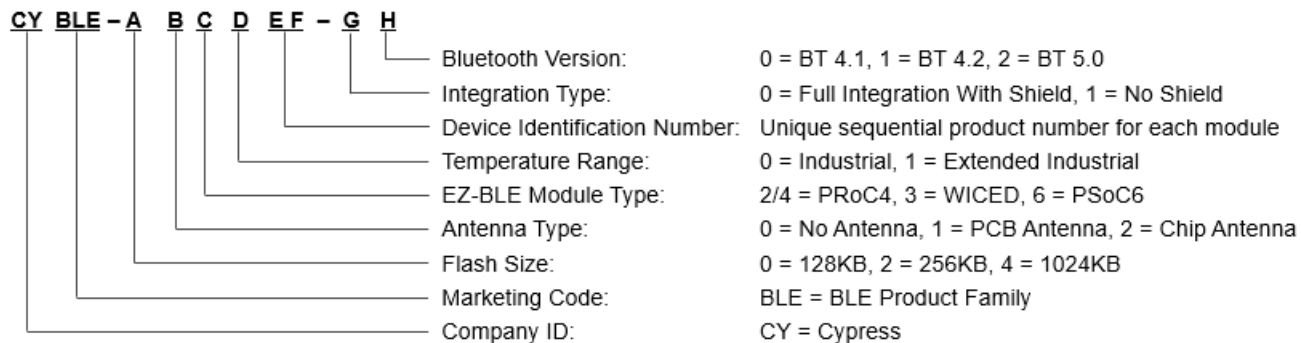
**Table 43. Tape and Reel Package Quantity and Minimum Order Amount**

| Description                  | Minimum Reel Quantity | Maximum Reel Quantity | Comments                           |
|------------------------------|-----------------------|-----------------------|------------------------------------|
| Reel Quantity                | 500                   | 500                   | Ships in 500 unit reel quantities. |
| Minimum Order Quantity (MOQ) | 500                   | –                     |                                    |
| Order Increment (OI)         | 500                   | –                     |                                    |

The CYBLE-416045-02 is offered in tape and reel packaging. The CYBLE-416045-02 ships with a maximum of 500 Unit/reel.

## Part Numbering Convention

The part numbers are of the form CYBLE-ABCDEF-GH where the fields are defined as follows.



For additional information and a complete list of Cypress Semiconductor BLE products, contact your local Cypress sales representative. To locate the nearest Cypress office, visit our website.

|  |  |
|--|--|
| U.S. Cypress Headquarters Address            | 198 Champion Court, San Jose, CA 95134               |
| U.S. Cypress Headquarter Contact Information | (408) 943-2600                                       |
| Cypress Website Address                      | <a href="http://www.cypress.com">www.cypress.com</a> |

## Acronyms

**Table 44. Acronyms Used in this Document**

| Acronym | Description   |
|---------|---|
| 3DES    | Triple Data Encryption Standard   |
| abus    | analog local bus  |
| ADC     | analog-to-digital converter   |
| AES     | Advanced Encryption Standard  |
| AG      | analog global   |
| AHB     | AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm data transfer bus |
| ALU     | arithmetic logic unit   |
| AMUXBUS | analog multiplexer bus  |
| API     | application programming interface   |
| APSR    | application program status register   |
| Arm     | advanced RISC machine, a CPU architecture   |
| ATM     | automatic thump mode  |
| BW      | bandwidth   |
| CAN     | Controller Area Network, a communications protocol  |
| CMRR    | common-mode rejection ratio   |
| CPU     | central processing unit   |
| CTBm    | Continuous Time Block mini  |
| CRC     | cyclic redundancy check, an error-checking protocol   |
| DAC     | digital-to-analog converter, see also IDAC, VDAC  |
| DFB     | digital filter block  |
| DIO     | digital input/output, GPIO with only digital capabilities, no analog. See GPIO.                 |
| DMIPS   | Dhrystone million instructions per second   |
| DMA     | direct memory access, see also TD   |
| DNL     | differential nonlinearity, see also INL   |
| DNU     | do not use  |
| DR      | port write data registers   |
| DSI     | digital system interconnect   |
| DWT     | data watchpoint and trace   |
| ECC     | error correcting code or Elliptic Curve Cryptography  |
| ECO     | external crystal oscillator   |
| EEPROM  | electrically erasable programmable read-only memory   |
| EMI     | electromagnetic interference  |
| EMIF    | external memory interface   |

**Table 44. Acronyms Used in this Document** (continued)

| Acronym                  | Description  |
|--------------------------|--|
| EOC                      | end of conversion                                      |
| EOF                      | end of frame   |
| EPSR                     | execution program status register                      |
| ESD                      | electrostatic discharge                                |
| ETM                      | embedded trace macrocell                               |
| FIR                      | finite impulse response, see also IIR                  |
| FPB                      | flash patch and breakpoint                             |
| FS                       | full-speed   |
| GPIO                     | general-purpose input/output, applies to a PSoC pin    |
| HVI                      | high-voltage interrupt, see also LVI, LVD              |
| IC                       | integrated circuit                                     |
| IDAC                     | current DAC, see also DAC, VDAC                        |
| IDE                      | integrated development environment                     |
| I <sup>2</sup> C, or IIC | Inter-Integrated Circuit, a communications protocol    |
| IIR                      | infinite impulse response, see also FIR                |
| ILO                      | internal low-speed oscillator, see also IMO            |
| IMO                      | internal main oscillator, see also ILO                 |
| INL                      | integral nonlinearity, see also DNL                    |
| I/O                      | input/output, see also GPIO, DIO, SIO, USBIO           |
| IPOR                     | initial power-on reset                                 |
| IPSR                     | interrupt program status register                      |
| IRQ                      | interrupt request                                      |
| ITM                      | instrumentation trace macrocell                        |
| LCD                      | liquid crystal display                                 |
| LIN                      | Local Interconnect Network, a communications protocol. |
| LR                       | link register  |
| LUT                      | lookup table   |
| LVD                      | low-voltage detect, see also LVI                       |
| LVI                      | low-voltage interrupt, see also HVI                    |
| LVTTL                    | low-voltage transistor-transistor logic                |
| MAC                      | multiply-accumulate                                    |
| MCU                      | microcontroller unit                                   |
| MISO                     | master-in slave-out                                    |
| NC                       | no connect   |
| NMI                      | nonmaskable interrupt                                  |
| NRZ                      | non-return-to-zero                                     |
| NVIC                     | nested vectored interrupt controller                   |



**Table 44. Acronyms Used in this Document** (continued)

| Acronym | Description  |
|---------|--|
| NVL     | nonvolatile latch, see also WOL                              |
| opamp   | operational amplifier  |
| PAL     | programmable array logic, see also PLD                       |
| PC      | program counter  |
| PCB     | printed circuit board  |
| PDM     | Pulse-Density Modulation                                     |
| P/E     | Program/Erase  |
| PGA     | programmable gain amplifier                                  |
| PHUB    | peripheral hub   |
| PHY     | physical layer   |
| PICU    | port interrupt control unit                                  |
| PLA     | programmable logic array                                     |
| PLD     | programmable logic device, see also PAL                      |
| PLL     | phase-locked loop  |
| PMDD    | package material declaration data sheet                      |
| POR     | power-on reset   |
| PRES    | precise power-on reset                                       |
| PRS     | pseudo random sequence                                       |
| PS      | port read data register                                      |
| PSoC    | Programmable System-on-Chip                                  |
| PSRR    | power supply rejection ratio                                 |
| PWM     | pulse-width modulator  |
| RAM     | random-access memory   |
| RMS     | root-mean-square   |
| RISC    | reduced-instruction-set computing                            |
| RSA     | Rivest–Shamir–Adleman  |
| RTC     | real-time clock  |
| RTL     | register transfer language                                   |
| RTR     | remote transmission request                                  |
| RX      | receive  |
| SAR     | successive approximation register                            |
| SC/CT   | switched capacitor/continuous time                           |
| SCL     | I <sup>2</sup> C serial clock                                |
| SDA     | I <sup>2</sup> C serial data                                 |
| S/H     | sample and hold  |
| SIG     | Special Interest Group                                       |
| SINAD   | signal to noise and distortion ratio                         |
| SIO     | special input/output, GPIO with advanced features. See GPIO. |
| SOC     | start of conversion  |

**Table 44. Acronyms Used in this Document** (continued)

| Acronym | Description  |
|---------|--|
| SOF     | start of frame   |
| S/PDIF  | Sony/Philips Digital Interface   |
| SPI     | Serial Peripheral Interface, a communications protocol                 |
| SR      | slew rate  |
| SRAM    | static random access memory  |
| SRES    | software reset   |
| SRSS    | System Resources Subsystem   |
| SWD     | serial wire debug, a test protocol                                     |
| SWV     | single-wire viewer   |
| TD      | transaction descriptor, see also DMA                                   |
| THD     | total harmonic distortion  |
| TIA     | transimpedance amplifier   |
| TRM     | technical reference manual   |
| TRNG    | True Random Number Generator   |
| TTL     | transistor-transistor logic  |
| TX      | transmit   |
| UART    | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UDB     | universal digital block  |
| ULP     | Ultra-low power  |
| USB     | Universal Serial Bus   |
| USBIO   | USB input/output, PSoC pins used to connect to a USB port              |
| VDAC    | voltage DAC, see also DAC, IDAC  |
| WDT     | watchdog timer   |
| WOL     | write once latch, see also NVL   |
| WRES    | watchdog timer reset   |
| XRES    | external reset I/O pin   |
| XTAL    | crystal  |

## Document Conventions

### Unit of Measure

Table 45. Unit of Measure

| Symbol | Unit of Measure        |
|--------|------------------------|
| °C     | degrees Celsius        |
| dB     | decibel                |
| dBm    | decibel-milliwatts     |
| fF     | femtofarads            |
| Hz     | hertz                  |
| KB     | 1024 bytes             |
| kbps   | kilobits per second    |
| Khr    | kilohour               |
| kHz    | kilohertz              |
| kΩ     | kilo ohm               |
| ksps   | kilosamples per second |
| LSB    | least significant bit  |
| Mbps   | megabits per second    |
| MHz    | megahertz              |
| MΩ     | mega-ohm               |
| Msp    | megasamples per second |
| μA     | microampere            |
| μF     | microfarad             |
| μH     | microhenry             |
| μs     | microsecond            |
| μV     | microvolt              |
| μW     | microwatt              |
| mA     | milliampere            |
| ms     | millisecond            |
| mV     | millivolt              |
| nA     | nanoampere             |
| ns     | nanosecond             |
| nV     | nanovolt               |
| Ω      | ohm                    |
| pF     | picofarad              |
| ppm    | parts per million      |
| ps     | picosecond             |
| s      | second                 |
| sps    | samples per second     |
| sqrtHz | square root of hertz   |
| V      | volt                   |

## Document History Page

| Document Title: CYBLE-416045-02 EZ-BLE™ Creator Module<br>Document Number: 002-24085 |         |                 |                 |   |
|--|---------|-----------------|-----------------|---|
| Revision   | ECN     | Orig. of Change | Submission Date | Description of Change   |
| **   | 6179687 | DSO             | 06/05/2018      | Preliminary Datasheet for CYBLE-416045-02 Module.   |
| *A   | 6486349 | SHNG            | 02/21/2019      | Updated the <a href="#">Low-Power Comparators</a> and <a href="#">Serial Communication Blocks (SCB)</a> sections.<br>Added the <a href="#">32-kHz Crystal Oscillator</a> section.<br>Added <a href="#">Table 11</a> and Updated <a href="#">Table 37</a> .<br>Updated certification.<br>Updated Tape, unreeling direction, and Center of Mass drawings. |

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