Low Power Multiclock Generator with VCXO
AK8136A

Features

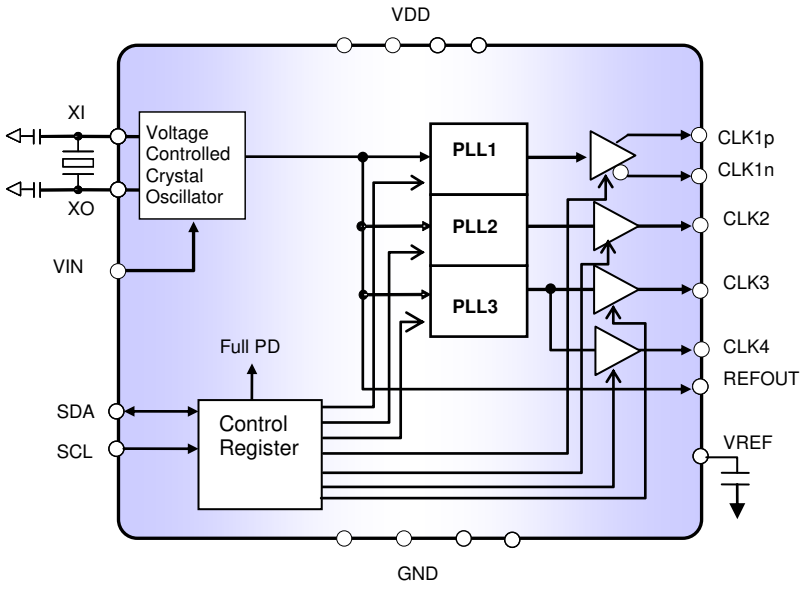
- 27MHz Crystal Input
- One 27MHz-Reference Output
- 2 wire serial register interface
- Selectable Clock out Frequencies:
  - 148.352, 148.5MHz
  - 100.71, 108MHz
  - 22.5792, 24.576, 33.8688, 36.864MHz
  - 27.0MHz
- Built-in VCXO
  - Pull Range: ±150ppm (typ.)
- Low Jitter Performance
  - Period Jitter:
    150 psec (Typ.) at CLK2,CLK3,CLK4
  - TIE:
    100 psec (Max) at CLK1p,CLK1n
  - Long term jitter:
    160 psec (Typ.) at REFOUT
- Low Current Consumption:
  32 mA (Typ.) at 3.3V
- Supply Voltage:
  3.0 – 3.6V
- Operating Temperature Range:
  -20 to +85℃
- Package:
  20-pin SSOP (Lead free, Halogen free)

Description

The AK8136A is a member of AKM's low power multi clock generator family designed for a feature rich DTV or STB, requiring a range of system clocks with high performance. The AK8136A generates different frequency clocks from a 27MHz crystal oscillator and provides them to up to four outputs configured by register-setting. The on-chip VCXO accepts a voltage control input to allow the output clocks to vary by ±150 ppm for synchronizing to the external clock system. Both circuitries of VCXO and PLL in AK8136A are derived from AKM's long-term-experienced clock device technology, and enable clock output to perform low jitter and to operate with very low current consumption. The AK8136A is available in a 20-pin SSOP package.

Applications

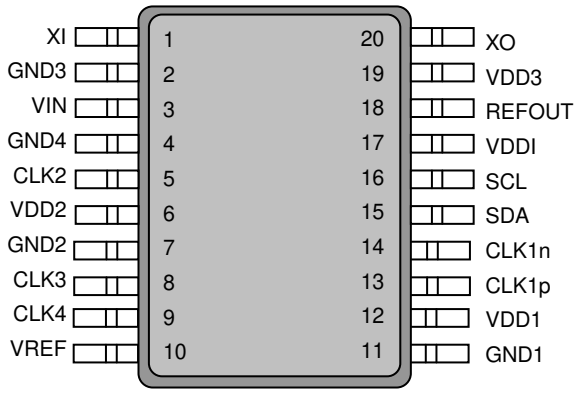
- Set-Top-Boxes



AK8136A Multi Clock Generator

Pin Descriptions

Package: 20-Pin SSOP(Top View)



Pin No.	Pin Name	Pin Type	Description
1	XI	AIN	Crystal connection, Connect to 27.000MHz crystal
2	GND3	PWR	Ground 3
3	VIN	AIN	VCXO Control Voltage Input
4	GND4	PWR	Ground 4
5	CLK2	DO	Clock output 2, See register description. In full power down or disable, this pin is “L”.
6	VDD2	PWR	Power Supply 2
7	GND2	PWR	Ground 2
8	CLK3	DO	Clock output 3, See register description In full power down or disable, this pin is “L”.
9	CLK4	DO	Clock output 4, Copy of CLK3 See register description In full power down or disable, this pin is “L”.
10	VREF	AO	VREF Pin Connect 1uF capacitor. Hi-Z in full power down state.
11	GND1	PWR	Ground 1
12	VDD1	PWR	Power Supply 1
13	CLK1p	DO	Clock output 1, these are differential pair. See register description In full power down or disable, these pins are “L”.
14	CLK1n	DO	
15	SDA	DI/DO	Serial data input and output pin. Open drain.
16	SCL	DI	Serial interface clock input.
17	VDDI	PWR	Power supply for serial interface. 1.8V or 3.3V can be used.
18	REFOUT	DO	Reference Clock Output of VCXO based on 27.000MHz Crystal In full power down or disable, this pin is “L”.
19	VDD3	PWR	Power Supply 3
20	XO	AO	Crystal connection, Connect to 27.000MHz crystal

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8136A	8136A	Tape and Reel	20-pin SSOP	-20 to 85℃

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply voltage	VDD/VDDI	-0.3 to 4.6	V
Input voltage	Vin	VSS-0.3 to VDD+0.3	V
Input current (any pins except supplies)	I_{IN}	±10	mA
Storage temperature	Tstg	-55 to 130	°C

Note

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-20		85	°C
Supply voltage 1(1)	VDDI	Pin: VDDI	1.7		3.6	V
Supply voltage 2(2)	VDD	Pin: VDD1,VDD2,VDD3	3.0	3.3	3.6	V
Output Load Condition	CL1	Pin: CLK1p,CLK1n See Figure 1				
Output Load Capacitance	Cp1	Pin: CLK2,CLK3,CLK4			15	pF
	Cp2	Pin: REFOUT			25	pF

Note:

(1) A decoupling capacitor for power supply line should be installed close to VDDI pin.

(2)Power to VDD1, VDD2, VDD3 requires to be supplied from a single source. A decoupling capacitor for power supply line should be installed close to each VDD pin.

DC Characteristics

VDD: over 3.0 to 3.6V,VDDI:over 1.7 to 3.6V, Ta: -20 to +85℃, 27MHz Crystal, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
High Level Input Voltage	V_{IH}	Pin: SDA,SCL	0.7VDDI			V
Low Level Input Voltage	V_{IL}	Pin: SDA,SCL			0.3VDDI	V
Input Current 1	I_L1	Pin: SDA,SCL	-10		+10	μA
Input Current 2	I_L2	Pin: VIN	-3		+3	μA
High Level Output Voltage	V_{OH}	Pin: CLK2-4, REFOUT I_{OH}=-4mA	0.8VDD			V
Low level Output Voltage	V_{OL}	Pin: CLK2-4, REFOUT I_{OL}=+4mA			0.2VDD	V
Output impedance		Pin:CLK1p,CLK1n Ta=25℃,3.3V	14	20	26	Ω
VREF Voltage	V_{REF}	Pin:VREF C_{vref}=1μF	0.72	0.8	0.88	V
Current Consumption 1	I_{DD1}	No load Clock out selection by note(1) VDD/VDDI=3.3V, Ta=25℃		32		mA
Current Consumption 2	I_{DD2}	On load(2) Clock out selection by note(1) VDD/VDDI=3.3V, Ta=25℃		46		mA
Current Consumption 3	I_{DDPD}	***FULL_PD***="H" VDD/VDDI=3.3V, Ta=25℃		0	150	μA

(1) CLK1p/1n:148.5MHz, CLK2=108MHz,CLK3/4=36.864MHz,REFOUT=27.0MHz

(2) CLK1p/1n: Figure1, CLK2-4: Cp1=15pF, REFOUT:Cp2=25pF

AC Characteristics (Clock signals)

VDD: over 3.0 to 3.6V, VDDI over 1.7 to 3.6V,Ta: over -20 to +85°C, 27MHz Crystal, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Crystal Clock Frequency	F_{osc}	Pin:XI,XO		27.0000		MHz
Output Clock Accuracy	$F_{accuracy}$	Pin:CLK2 100.71MHz Relative to 27.0MHz		106.25		ppm
VCXO Pullable Range (1)	PR_{vcxo}	VIN at over 0 to VDD V		±150		ppm
VCXO Gain	G_{VCXO}	VIN range at 1.5V±1.0V		150		ppm/V
Period Jitter (5)	$Jit_{\_period}$	Pin:REFOUT(2),CLK2-4(3)		150 (6 σ)		ps
Time Interval Error (6)	$Jit_{\_tie}$	Pin:CLK1(4)			100	ps
Long Term Jitter (7)	$Jit_{\_long}$	Pin:REFOUT 1000 cycle delay		160		ps
Output Clock Duty Cycle	DtyCyc	Pin: CLK1p,n(4) Figure.3 CLK2-4 (3)	45	50	55	%
		Pin: REFOUT (2)	40	50	60	%
Output Clock Slew Rate	$Slew_{\_rise\_fall}$	Pin:CLK1p,n (4) Figure.3	2.5		8.0	V/ns
Slew rate matching	$Slew_{\_ver}$	Pin:CLK1p,n (4) Figure.2			20	%
Differential output swing	$V_{\_swing}$	Pin:CLK1p,n (4) Figure.3	300			mV
Crossing point voltage	$V_{\_cross}$	Pin:CLK1p,n (4) Figure.2	300		550	mV
Variation of Vcrs	$V_{\_cross\_delta}$	Pin:CLK1p,n (4) Figure.2			140	mV
Maximum output voltage	$V_{\_max}$	Pin:CLK1p,n (4) Figure.2			1.15	V
Minimum output voltage	$V_{\_min}$	Pin:CLK1p,n (4) Figure.2	-0.3			V
Output Clock Rise Time	$T_{\_rise}$	Pin: CLK2-4 (3)		1.0	3.0	ns
		Pin: REFOUT (2)		2.5	5.0	ns
Output Clock Fall Time	$T_{\_fall}$	Pin: CLK2-4 (3)		1.0	3.0	ns
		Pin: REFOUT (2)		2.5	5.0	ns
Output enable/disable Time(8)	$T_{\_en\_dis}$	Pin: REFOUT,CLK1p,n CLK2-4			500	ns
Power-up Time 1(9)	$T_{\_put1}$	Pin: REFOUT,CLK1p,n CLK2-4			4	ms
Power-up Time 2(10)	$T_{\_put2}$	Pin: REFOUT,CLK1p,n CLK2-4			150	ms

(1) Pullable range depends on crystal characteristics, on-chip load capacitance, and stray capacity of PCB. Typ. ±150ppm is applied to AKM's authorized test condition.
Please contact us when you plan the use of other crystal unit.

(2) Measured with load capacitance of 25pF

(3) Measured with load capacitance of 15pF

(4) Measured with load condition shown in Figure.1

(5) ±3σ in 10000 sampling or more

(6) 16ms accumulate with higher than 10GSa/s.

(7) ±3σ in 10000 sampling or more

(8) Refer to Figure.7 on Clock enable and disable sequence.

(9) Time to settle output into 0.1% of specified frequency from ***FULL_PD*** is "L". Refer to Figure.6 on "Full Power Down sequence".

(10) Refer to Figure.5 on "Power on Reset sequence".

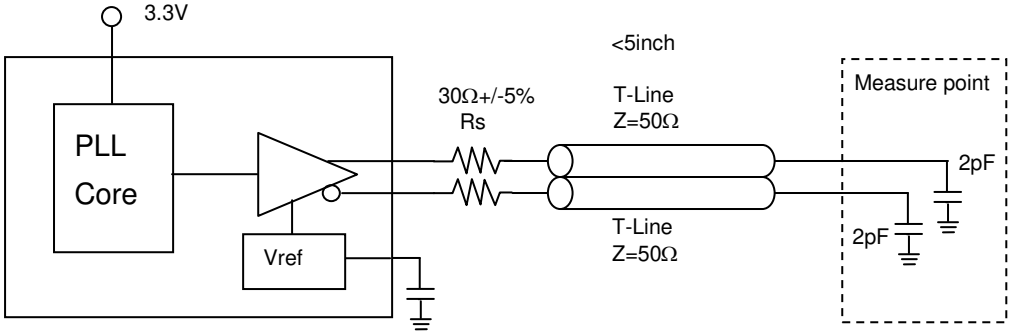


Figure.1 CLK1 Load condition

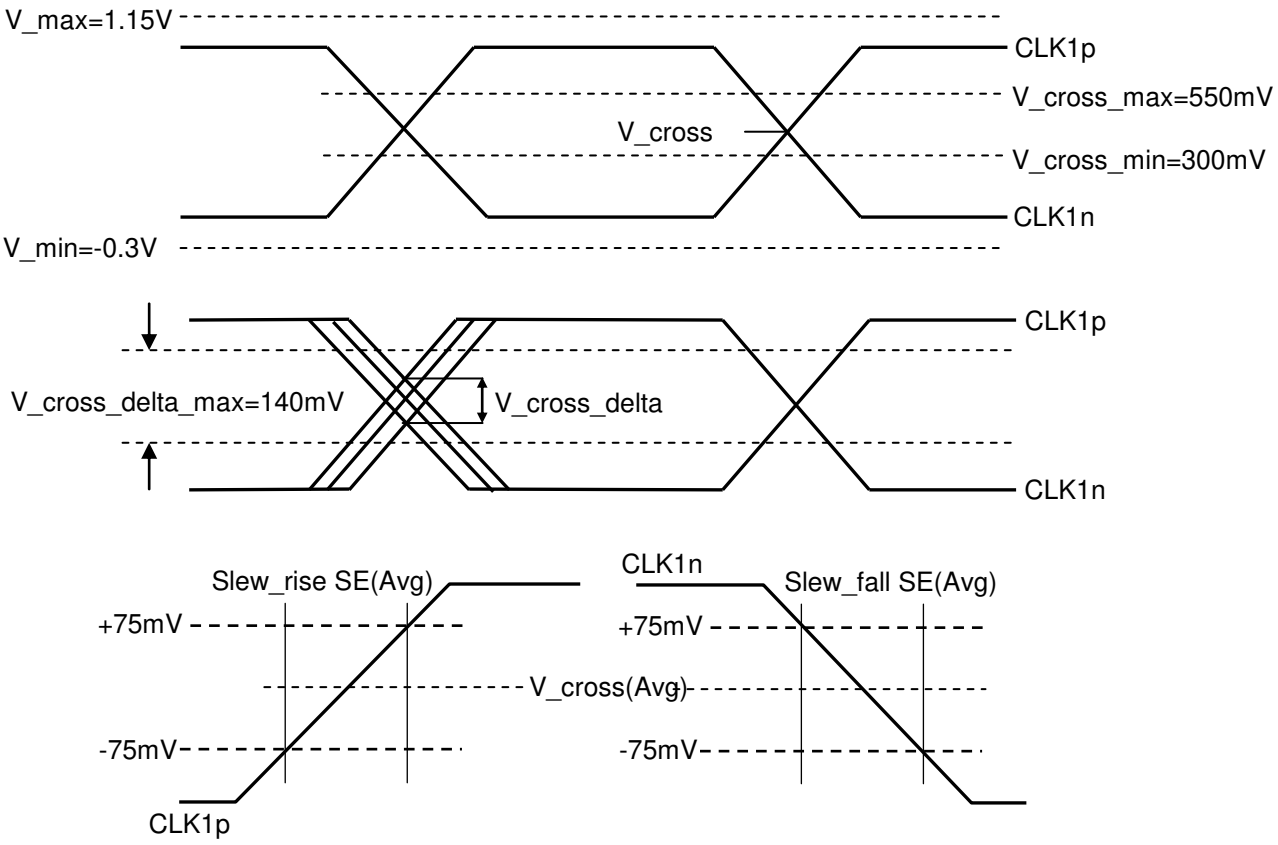


Figure.2 Single ended (SE) measurement waveforms

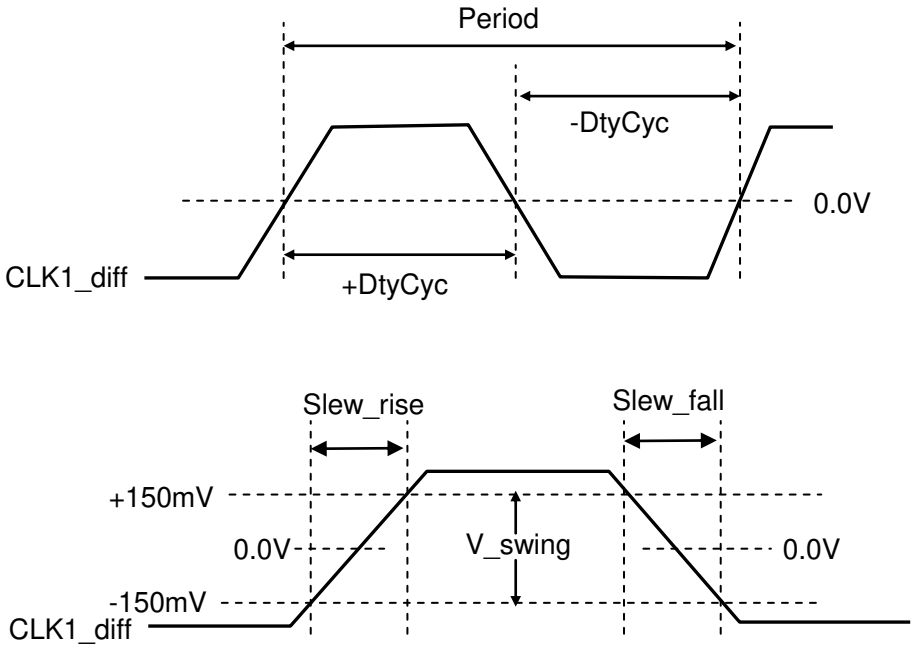


Figure.3 Differential (DIFF) measurement waveforms

AC Characteristics (**Serial interface**)

VDD: over 3.0 to 3.6V, VDDI over 1.7 to 3.6V,Ta: over -20 to +85℃, 27MHz Crystal, unless otherwise noted

Parameter	Symbol	Conditions	MIN	MAX	Unit
SCL clock frequency	fSCL			400	kHz
SCL Clock Low Period	tLOW		1.3		μs
SCL Clock High Period	tHIGH		0.6		μs
Pulse width of spikes which must be suppressed	tI			50	ns
SLC Low to SDA Data Out	tAA		0.3		μs
Bus free time between a STOP and START condition	tBUF		1.3		μs
Start Condition Hold Time	tHD.STA		0.6		μs
Start Condition Setup Time (for a Repeated Start condition)	tSU.STA		0.6		ms
Data in Hold Time	tHD.DAT		0		s
Data in Setup Time	tSU.DAT		100		ns
SDA and SCL Rise Time	tR			0.3	μs
SDA and SCL Fall Time	tF			0.3	μs
Stop Condition Setup Time	tSU.STO		0.6		μs
Bus Line Load	Cb			200	pF

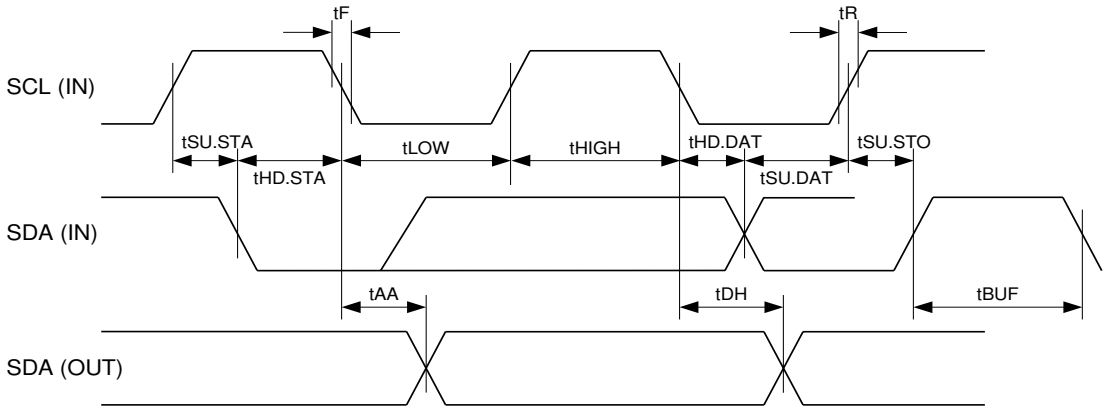


Figure.4 Serial Interface Timing

Function Description

Power On Reset sequence

AK8136A has the POR(Power On Reset) circuit. In power up, the POR works and the register is set to the initial value and all clock output becomes enable without glitch.

Note1) The assumption power start time to reach 90 % of VDD is within 20 ms.
Note2) The first register setting should be done after the 150 ms elapse after the power on.

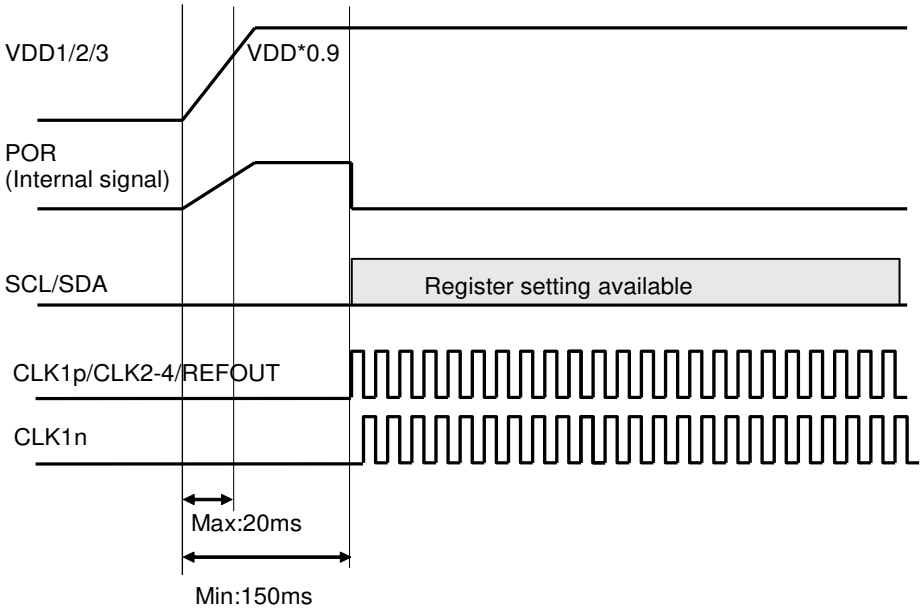
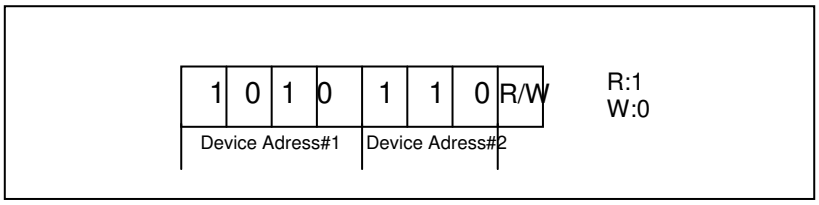


Figure.5 Recommend Power Up Sequence

Serial interface

Read/Write performance of serial interface is expressed below. The device address #1 of AK8136A is fixed as ”1010”. The device address #2 is “110”.

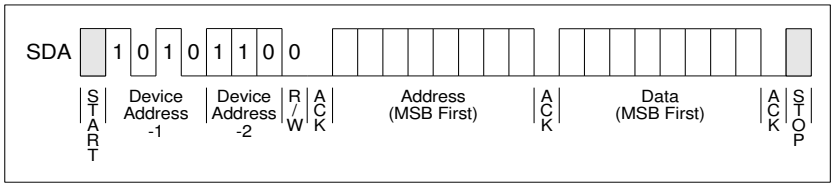
Device address of AK8136A



Byte wtire operation

Byte write operation is described below. Data must be sent after sending 8 bits address and receiving ACK.

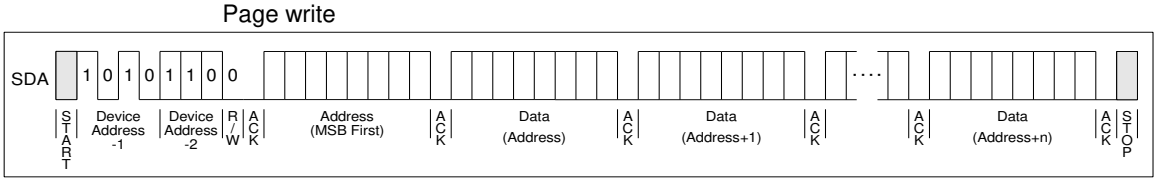
Byte write



Page write operation

Page write operation is described below. Only lower 4 bits of address are valid. Upper 4 bits are fixed as “1111”. Therefore the address which is written after “1111 1111” becomes “1111 1110”.

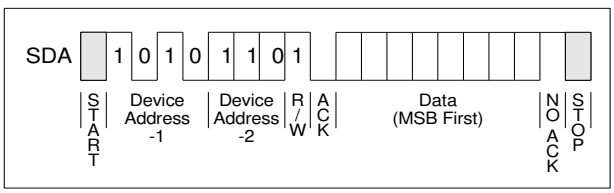
Page write



Current address read

Current address read operation is described below. The data that is read by this operation is obtained as “last accessed address + 1”. Therefore, It is consequent to return “1111 1110” after accessing the address “1111 1111”.

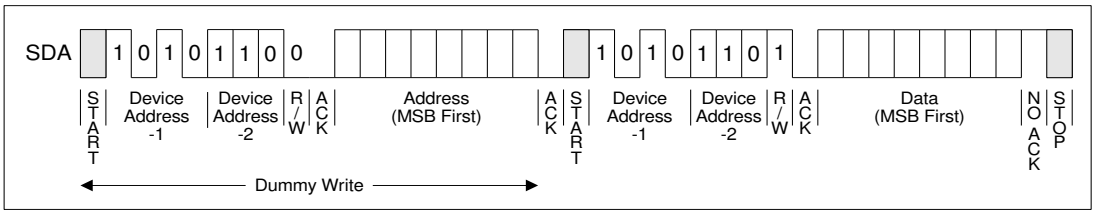
Current address read



Random read

Random read operation is described below. It is necessary to operate “dummy write” before sending read command. Dummy write is to send the address to read.

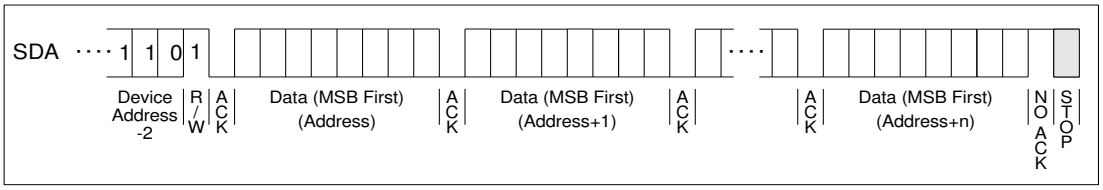
Random read



Sequential read

Sequential read operation is described below. It is possible to read next address sequentially by sending ACK instead of stop condition.

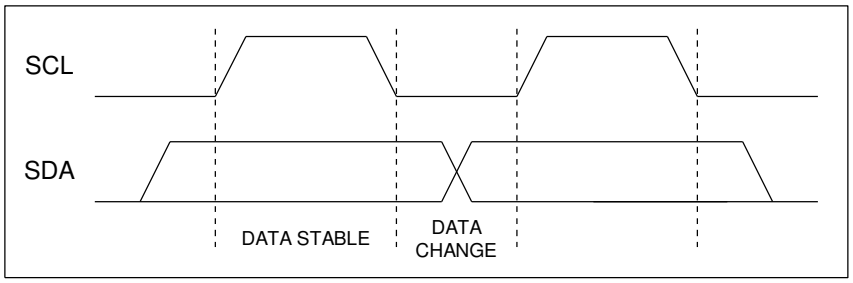
Sequential read



Change data

Change data operation is described below. It is available when SCL is Low.

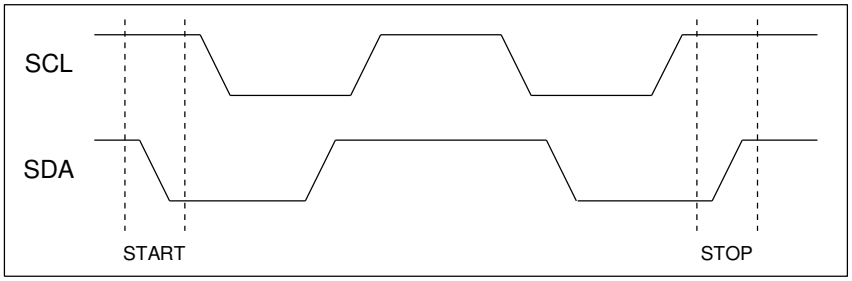
Change data



Start / Stop timing

Start / Stop timing is described below. The sequence is started when SDA goes from high to low during SCL is high. The sequence is stopped when SDA goes from low to high during SCL is high.

Start / Stop timing



Register description

The AK8136A generates a range of low-jitter and hi-accuracy clock frequencies with three built-in PLLs and provides to up to five assigned outputs. A frequency selection at assigned output pin and power down control is configured by register-setting.

Register Map

Address	D7	D6	D5	D4	D3	D2	D1	D0	Note
FF	*FULL_PD*	-	-	-	*CLK3S[1]*	*CLK3S[0]*	*CLK2S*	*CLK1S*	
	0	-	-	-	1	1	0	0	Default
FE	*CLK4_DIS*	*CLK3_DIS*	*CLK2_DIS*	*CLK1_DIS*	*REF_DIS*				
	0	0	0	0	0				Default

Register definition

FULL_PD (Address FF:D7)

Power Down Control

0	Device Active (PLL ON) Enable VCXO, VREF and PLLs (default)
1	Full Power Down Disable VCXO, VREF and PLLs

Full Power Down sequence

The full power down setting is done by following sequence.

1) Change ***CLKn_DIS***(n=1,2,3,4) and ***REF_DIS*** to "1" .
2) Change ***FULL_PD*** to "1" from "0".
   The output transfers to the disabled state without glitch.

The full power down state is released by following sequence.

1) Changing ***FULL_PD*** to "0" from "1" .
2) After more than 4 ms elapse, change ***CLKn_DIS*** and ***REF_DIS*** "0" to "1".
   The output transfers to the enable state without glitch.

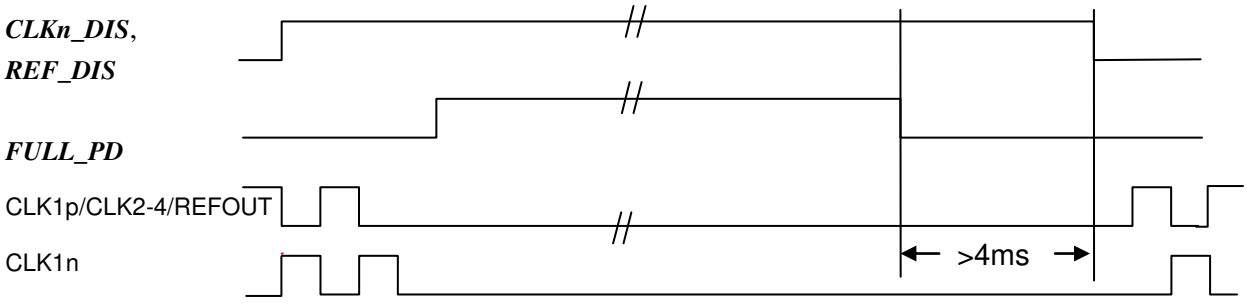


Figure.6 Full Down sequence

CLK3S[1:0] (Address FF:D3,D2)

CLK3&4 Output frequency selection

00	22.5792MHz
01	24.576MHz
10	33.8688MHz
11	36.864MHz (default)

CLK2S (Address FF:D1)

CLK2 Output frequency selection

0	108MHz. (default)
1	100.71MHz

CLK1S (Address FF:D0)

CLK1 Output frequency selection

0	148.5MHz/1.001 (default)
1	148.5MHz

CLK4_DIS (Address FE:D7)

CLK4 Output Disable

0	Enable (CLK4 Active) (default)
1	Disable(CLK4=”L”)

CLK3_DIS (Address FE:D6)

CLK3 Output Disable

0	Enable (CLK3 Active) (default)
1	Disable(CLK3=”L”)

CLK2_DIS (Address FE:D5)

CLK2 Output Disable

0	Enable (CLK2 Active) (default)
1	Disable(CLK2=”L”)

CLK1_DIS (Address FE:D4)

CLK1 Output Disable

0	Enable (CLK1 Active) (default)
1	Disable(CLK1p,CLK1n=”L”)

REF_DIS (Address FE:D3)

REFOUT Output Disable

0	Enable (REFOUT Active) (default)
1	Disable(REFOUT="L")

Clock Enable and Disable sequence

The enabling and disabling of the clock output are executed without glitch within 500 ns from the rising edge of SCL during the acknowledge operation after the corresponding byte date reception.

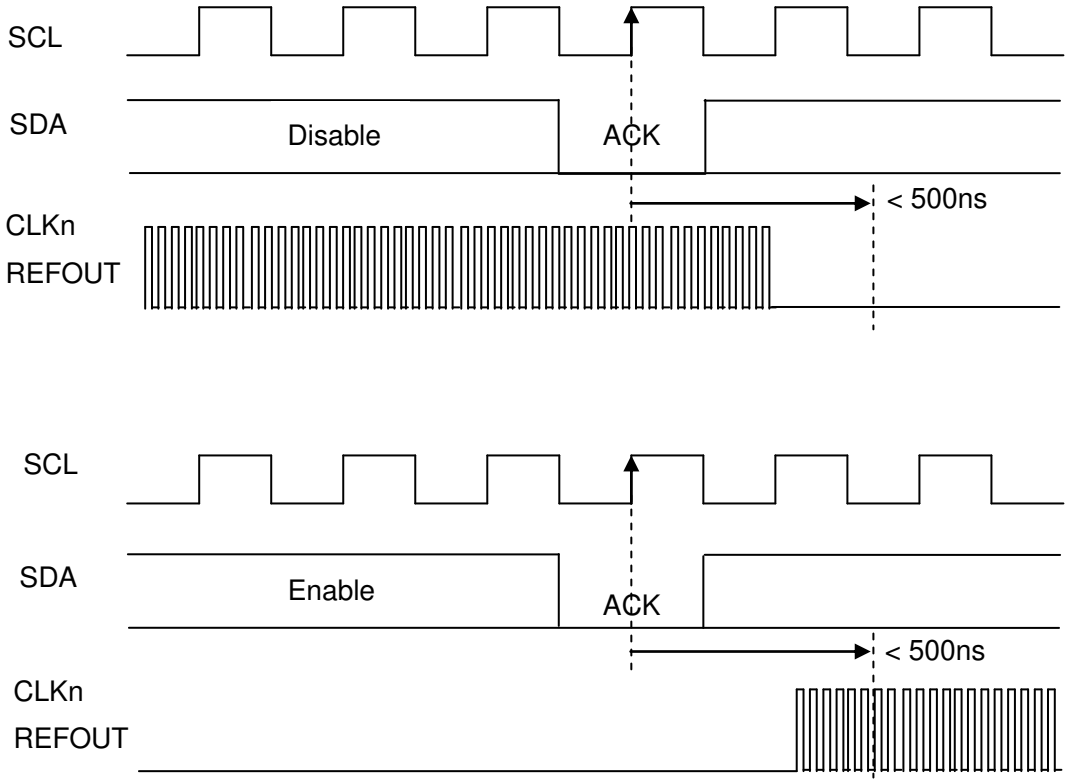


Figure.7 Output Enable and Disable sequence

Voltage Controlled Crystal Oscillator (VCXO)

The AK8136A has a voltage controlled crystal oscillator (VCXO), featuring fine frequency tuning for 27MHz of primary clock frequency by external DC voltage control. This tuning enables output clock frequency to synchronize the external clock system. VIN (Pin3) accepts DC voltage control from a processor or a system controller, and pulls the primary frequency of crystal to higher or lower. This pulling range is determined by crystal characteristic, on-chip load capacitor, and stray capacitance of PCB. The AK8136A is designed to range ±150ppm of primary frequency in AKM's authorized condition, and the typical pulling profile is shown in **Figure 8**. For details about the condition and other specific crystal application case, refer the AK8136A application note.

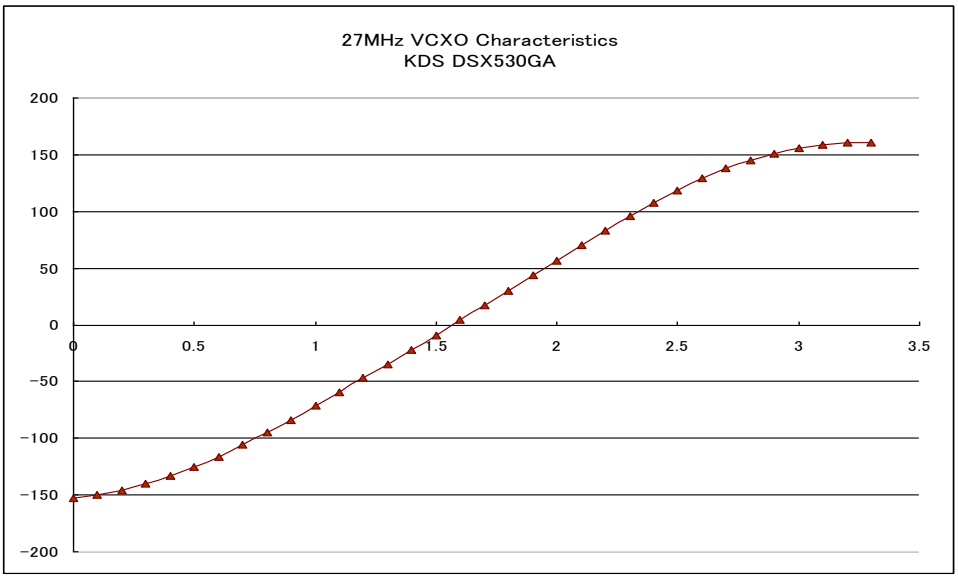


Figure 8: Typical VCXO Pulling Profile

KDS DSX530GA

Item		MIN	TYP	MAX	Unit	Remark
Nominal frequency	f0		27.000		MHz	CL=10.0pF
Equivalent resistance	R1			50	Ω	
Shunt capacitance	C0		3.0		pF	
Motional capacitance	C1		11.4		fF	
Motional inductance	L1		3.0		mH	
Drive Level			10	300	uW	

Spurious ・No spurious within 3fo±13kHz
・With in f0±500kHz the attenuation of the spurious response should be more than 3dB.

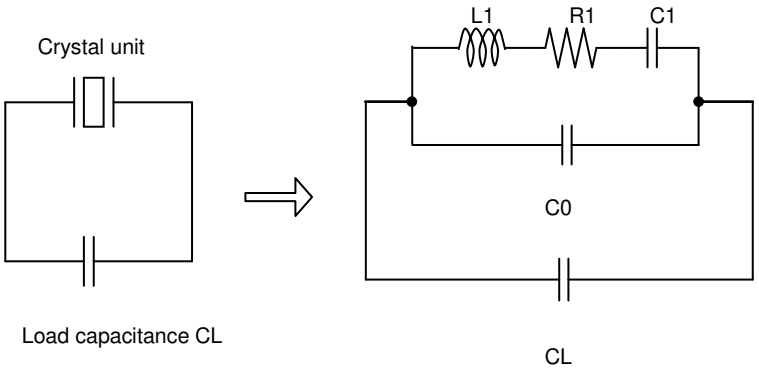
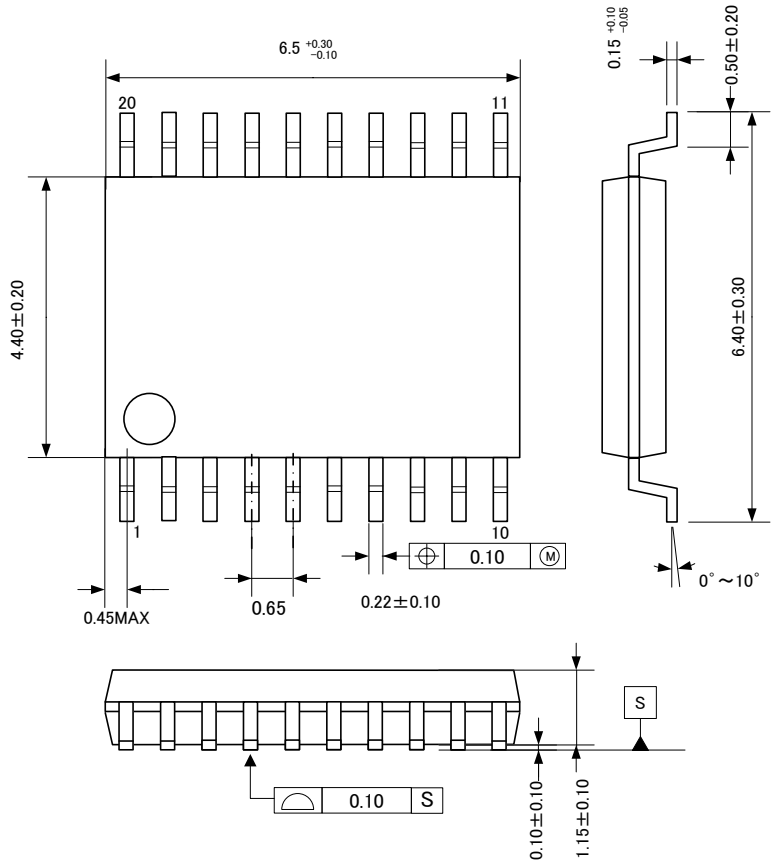
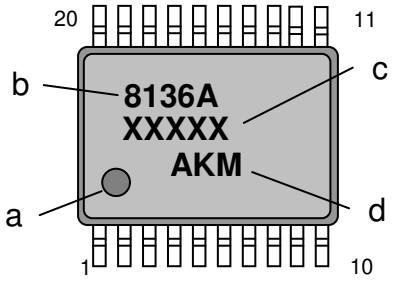


Figure.9 Equivalent parameter and load

Package Information

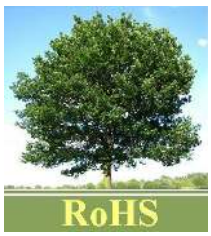


- **Marking**



a:	#1 Pin Index
b:	Part number
c:	Date code (5 digits)
d	Product Family Logo (1)

- **RoHS Compliance**



All integrated circuits form Asahi Kasei Microdevices Corporation (AKM) assembled in “lead-free” packages* are fully compliant with RoHS.

(*) RoHS compliant products from AKM are identified with “Pb free” letter indication on product label posted on the anti-shield bag and boxes.

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