

Description

The G30N02 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

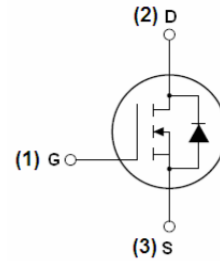
General Features

V_{DSS}	$R_{DS(ON)}$ @4.5V(Typ)	I_D
20V	10.5m Ω	30 A

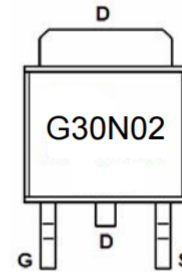
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability
- RoHS Compliant

Application

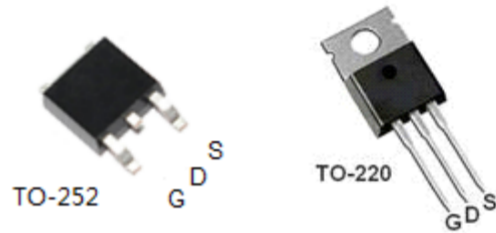
- Power switching application
- Load switching
- LED power supply



Schematic diagram



Marking and pin assignment



Ordering Information

Part Number	Marking	Case	Packaging
G30N02K	G30N02	TO-252	2500pcs/Reel
G30N02T	G30N02	TO-220	50pcs/Tube

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous	I_D	30	A
Drain Current-Continuous($T_C=100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	21	A
Pulsed Drain Current	I_{DM}	75	A
Maximum Power Dissipation	P_D	40	W
Single pulse avalanche energy ^(Note 5)	E_{AS}	150	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	3.8	$^\circ\text{C/W}$
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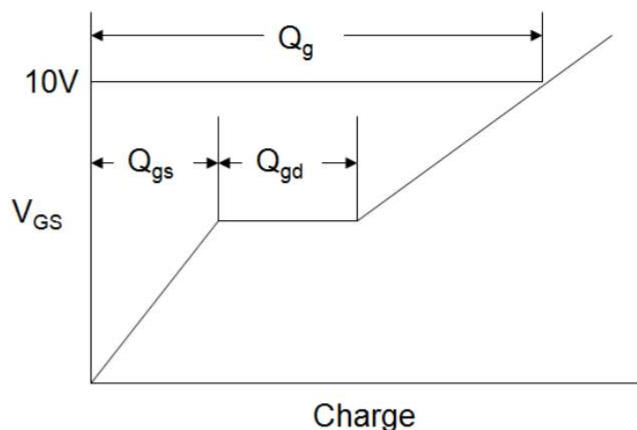
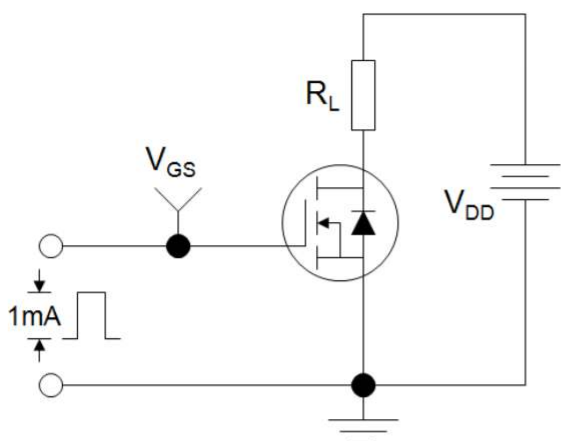
Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.7	1.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=20A$	-	10.5	13	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=20A$	10	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	900	-	PF
Output Capacitance	C_{oss}		-	162	-	PF
Reverse Transfer Capacitance	C_{rss}		-	105	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{GS}=10V, V_{DS}=10V$ $RL=0.5\Omega, R_{GEN}=3\Omega$	-	4.5	-	nS
Turn-on Rise Time	t_r		-	9.2	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	18.7	-	nS
Turn-Off Fall Time	t_f		-	3.3	-	nS
Total Gate Charge	Q_g	$V_{GS}=10V, V_{DS}=10V, I_D=20A$	-	15	-	nC
Gate-Source Charge	Q_{gs}		-	1.8	-	nC
Gate-Drain Charge	Q_{gd}		-	2.8	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=20A$	-	-	1.2	V
Diode Forward Current	I_S	-	-	-	30	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}\text{C}, I_F = 20A$ $di/dt = 100A/\mu s$ (Note 3)	-	18	-	nS
Reverse Recovery Charge	Q_{rr}		-	9.5	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

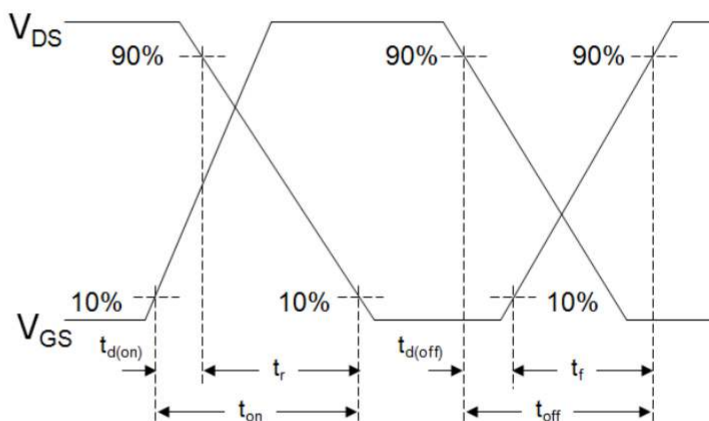
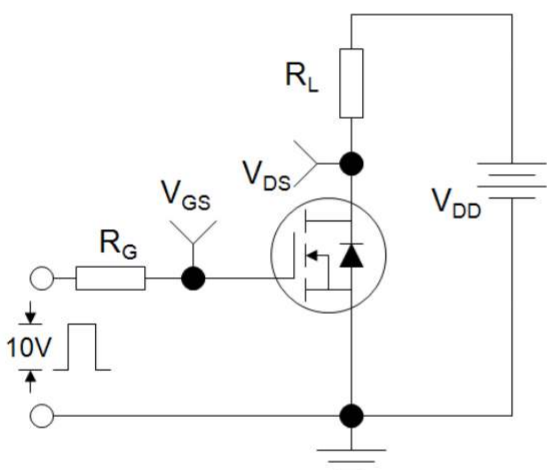
Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=10V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$

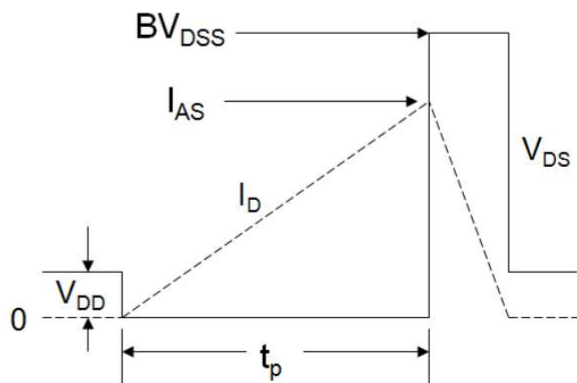
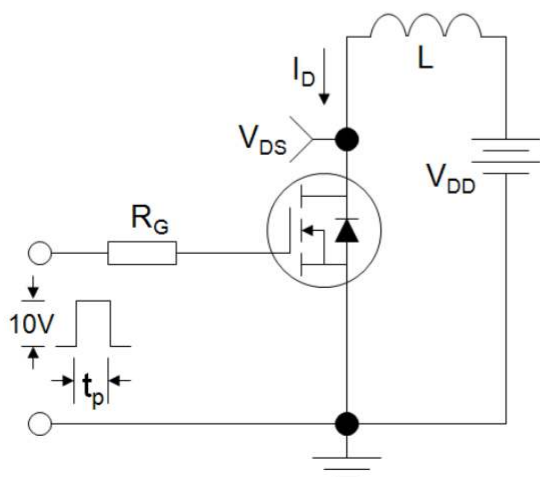
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

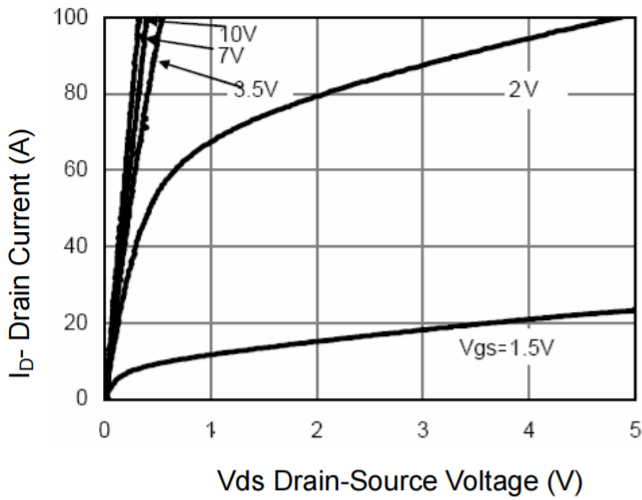


Figure 1 Output Characteristics

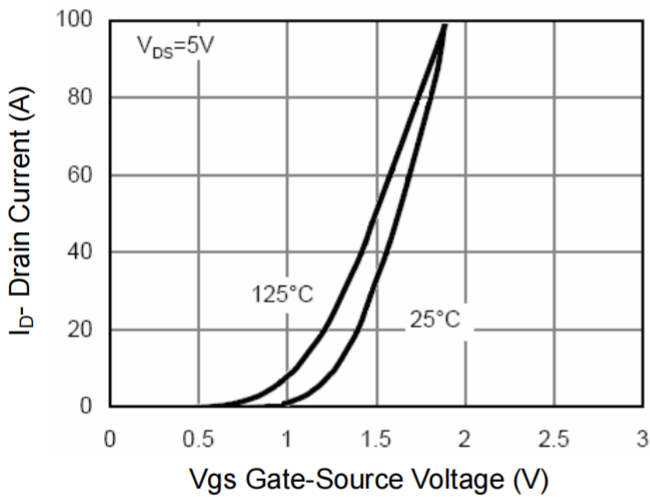


Figure 2 Transfer Characteristics

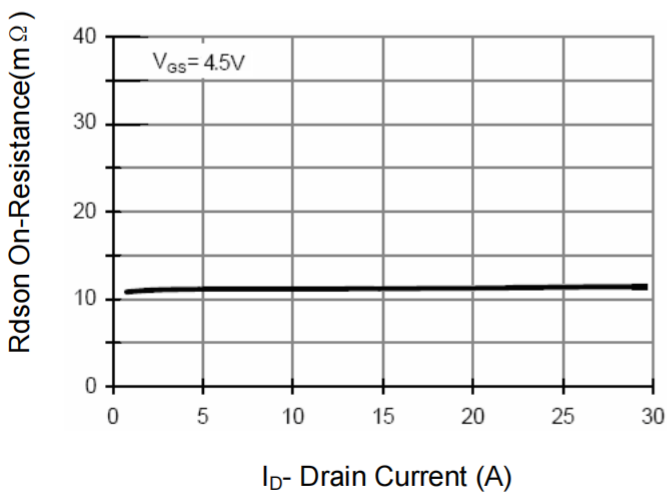


Figure 3 Rdson- Drain Current

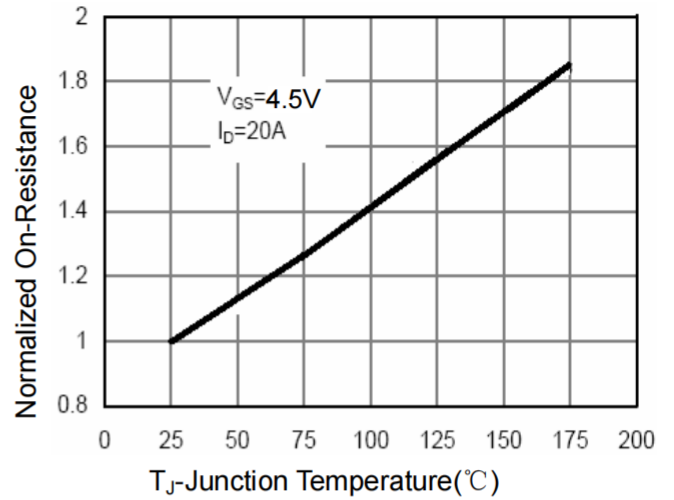


Figure 4 Rdson-Junction Temperature

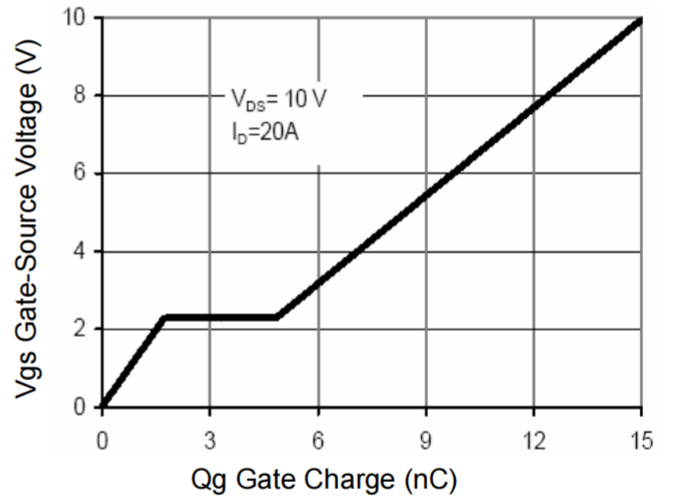


Figure 5 Gate Charge

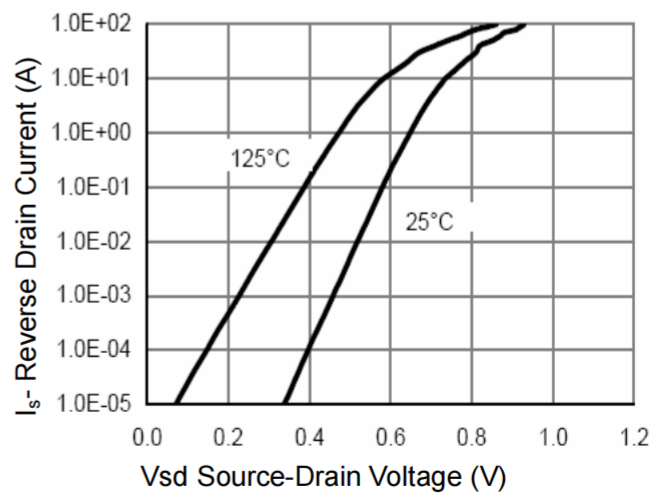


Figure 6 Source- Drain Diode Forward

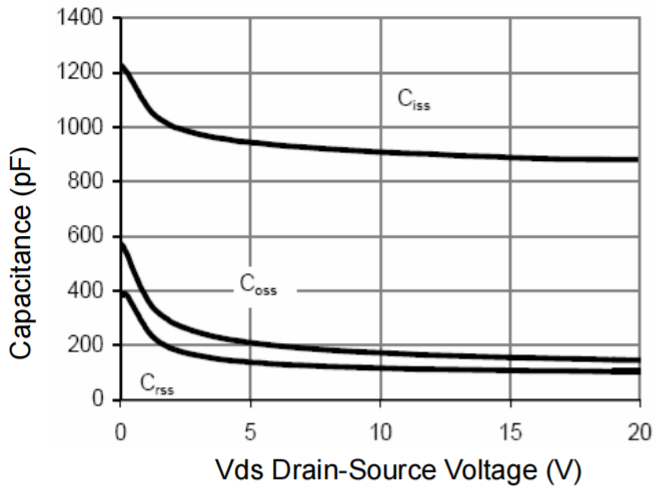


Figure 7 Capacitance vs Vds

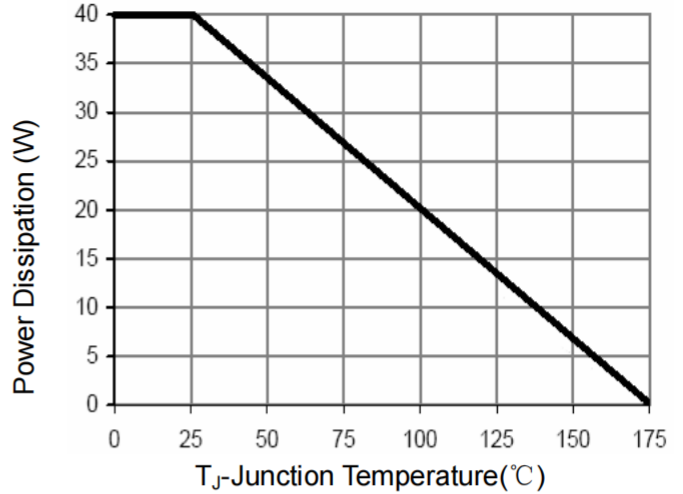


Figure 9 Power De-rating

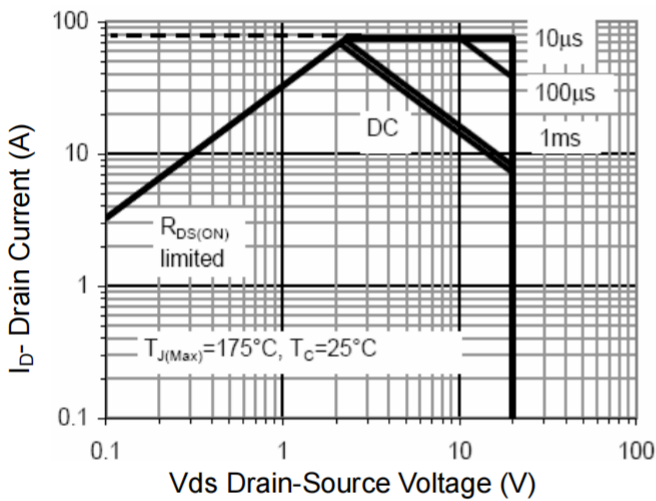


Figure 8 Safe Operation Area

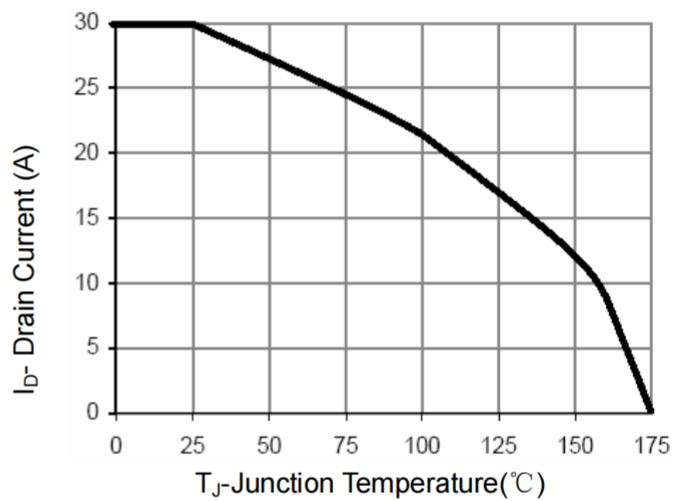


Figure 10 Current De-rating

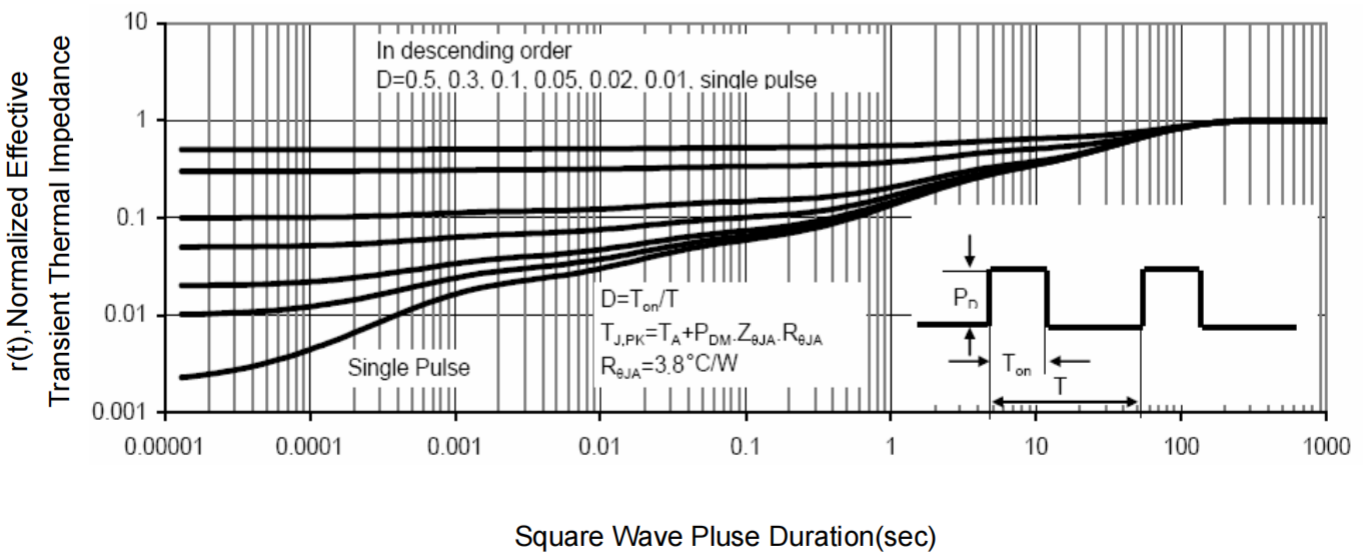
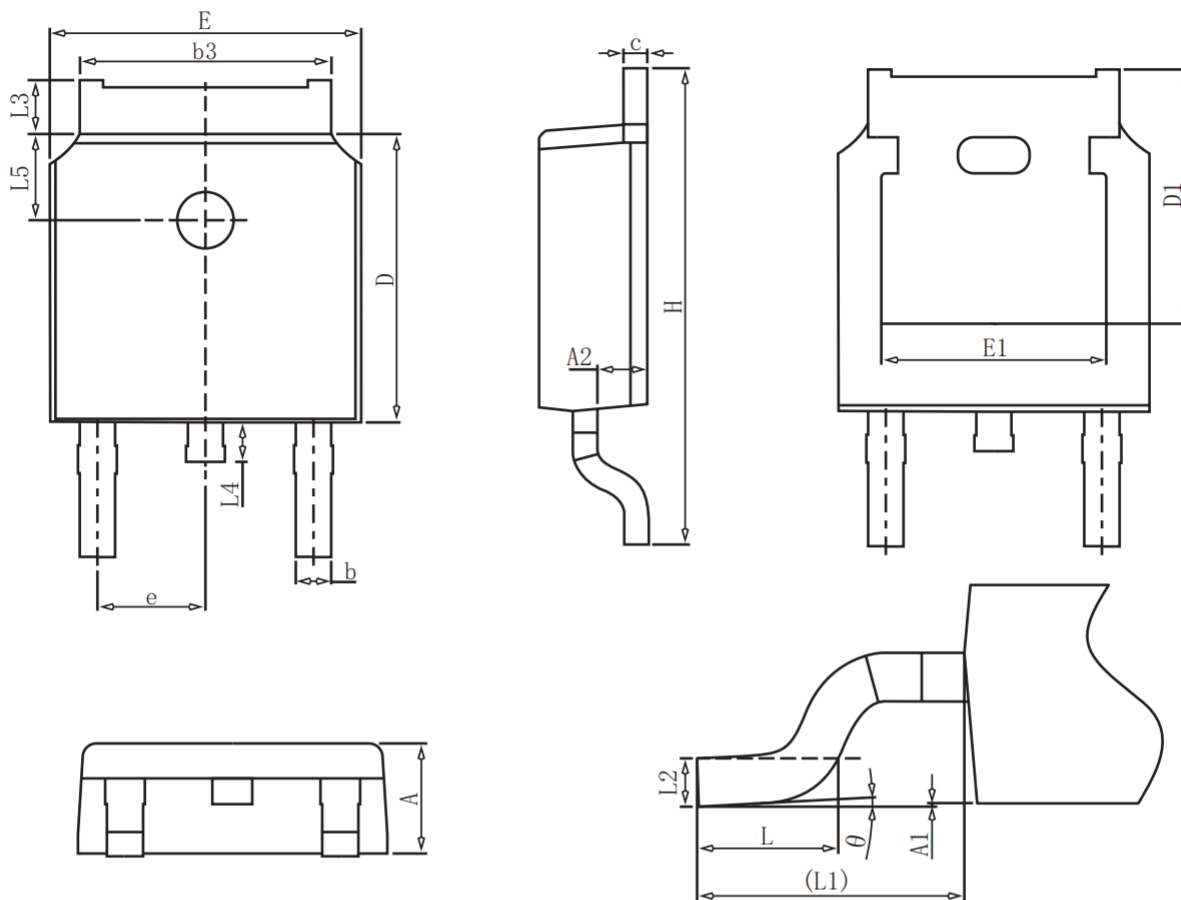


Figure 11 Normalized Maximum Transient Thermal Impedance

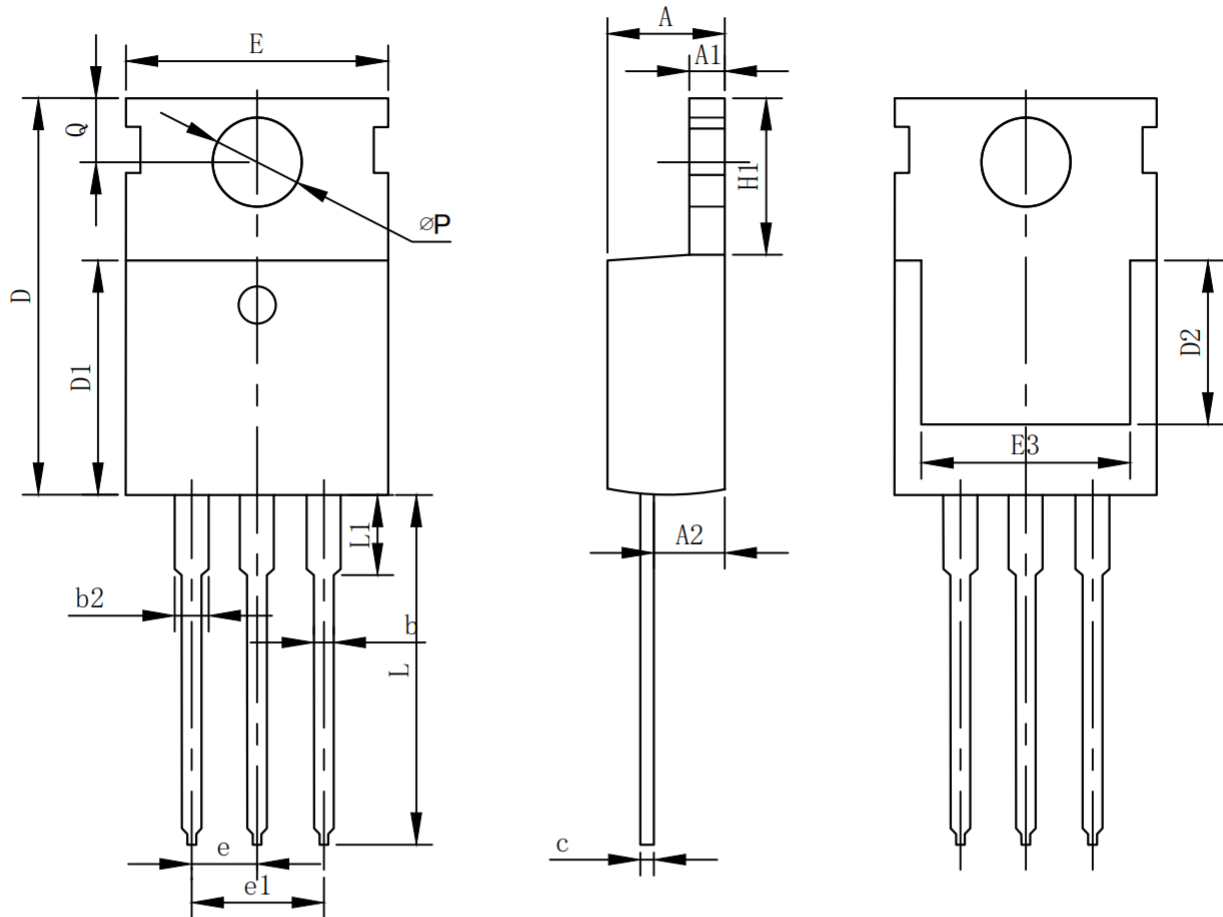
TO-252 Package information



COMMON DIMENSIONS

SYMBOL	mm		
	MIN	NOM	MAX
A	2.20	2.30	2.40
A1	0.00	-	0.20
A2	0.97	1.07	1.17
b	0.68	0.78	0.90
b3	5.20	5.33	5.50
c	0.43	0.53	0.63
D	5.98	6.10	6.22
D1	5.30REF		
E	6.40	6.60	6.80
E1	4.63	-	-
e	2.286BSC		
H	9.40	10.10	10.50
L	1.38	1.50	1.75
L1	2.90REF		
L2	0.51BSC		
L3	0.88	-	1.28
L4	0.50	-	1.00
L5	1.65	1.80	1.95
θ	0°	-	8°

TO-220 Package information



COMMON DIMENSIONS

SYMBOL	mm		
	MIN	NOM	MAX
A	4.37	4.57	4.70
A1	1.25	1.30	1.40
A2	2.20	2.40	2.60
b	0.70	0.80	0.95
b2	1.70	1.27	1.47
c	0.45	0.50	0.60
D	15.10	15.60	16.10
D1	8.80	9.10	9.40
D2	5.50	-	-
E	9.70	10.00	10.30
E3	7.00	-	-
e	2.54BSC		
e1	5.08BSC		
H1	6.25	6.50	6.85
L	12.75	13.50	13.80
L1	-	3.10	3.40
øP	3.40	3.60	3.80
Q	2.60	2.80	3.00