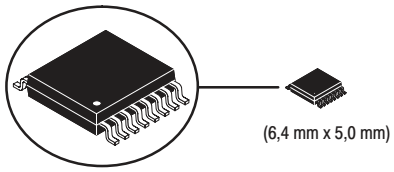


SLVS405 − OCTOBER 2001

PROGRAMMABLE FOUR-CHANNEL STEP-DOWN DC/DC CONVERTER

FEATURES

- **Four Independent 100-mA Channels Programmable Over 4-Wire Serial Port**
- **Converter Regulation Range: 7.5 V to 13.1 V in 400-mV Steps, Plus Unregulated Pass-Through Mode to Shunt VIN to any Output**
- **Internally Compensated PWM Controller and Integrated PMOS Power Switches**
- **Global and Per Channel Status Available Through Serial Port**
- **External Synchronization of PWM With System Clock**
- **Per Channel Current Limit and Global Thermal Shutdown**
- **−40°C to 85°C Ambient Temperature Range**

APPLICATIONS

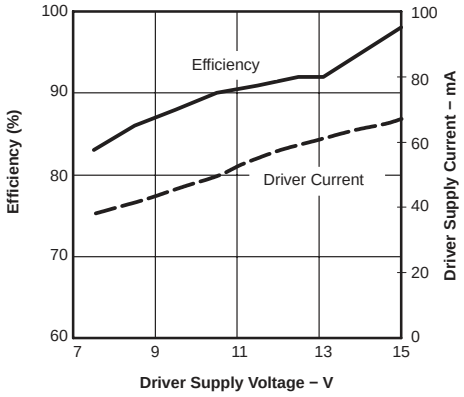
- **ADSL Central Office Line Drivers**
- **Software Line Card Provisioning**

DESCRIPTION

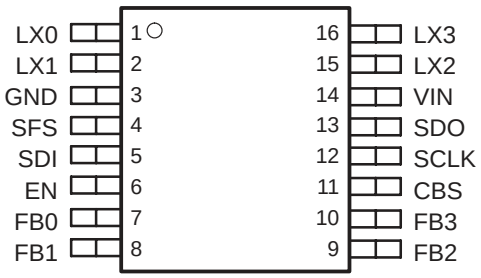
The TPS54900 four-channel step-down converter uses voltage mode PWM control to provide four independently programmable output voltages. Each regulated channel includes a high-side PMOSFET switch with a typical $r_{DS(ON)}$ of 0.8 Ω, which makes it suitable for high efficiency, low current applications. Commands sent to the TPS54900 over the four-wire serial port programs the outputs independently or globally to supply voltages from 7.5 V to 13.1 V in 0.4-V increments. When the input voltage is desired at an output, a bypass mode can be activated which fully enhances the PMOSFET switch and disables the switching circuitry of the selected channel.

The TPS54900 is an ideal companion device to power THS7102 ADSL line drivers as a part of the AC5 central office ADSL chipset. With the AC5 chipset controlling the TPS54900 output voltages, significant power savings are realized by reducing the excess supply headroom on a per line basis.

EFFICIENCY VS DRIVER SUPPLY VOLTAGE



TSSOP (PW) PACKAGE (TOP VIEW)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range‡, VIN . . . . . −0.3 V to 18 V
Input voltage range‡, EN, CBS, FB0, FB1, FB2, FB3 . . . . . −0.3 V to VIN + 0.3 V
Input voltage range‡, SCLK, SDI, SFS . . . . . −0.3 V to 5 V
Output voltage range‡, LX0, LX1, LX2, LX3 . . . . . −0.5 V to VIN + 0.3 V
Output voltage range‡, SDO . . . . . −0.3 V to 5 V
Continuous power dissipation . . . . . See Dissipation Rating Table
Operating junction temperature, T_J . . . . . −40°C to 125°C
Storage temperature range, T_{stg} . . . . . −55°C to 150°C
Lead soldering temperature, 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltages values are with respect to device GND terminal.

DISSIPATION RATING TABLE−FREE-AIR TEMPERATURES§

PACKAGE	AIR FLOW (CFM)	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PW	0	500 mW	5 mW/°C	275 mW	200 mW

§ Low-K PWB

recommended operating conditions (unless otherwise noted)

	MIN	NOM	MAX	UNITS
Supply voltage, VIN	14.25	15	16	V
Output current, LX0, LX1, LX2, LX3	20		100	mA
Synchronized PWM frequency (see Note 1)		552		kHz
Inductor	200	225	250	µH
Output capacitor		10		µF
Operating junction temperature, T_J	−40		125	°C

NOTE 1: Synchronized PWM frequency equal to one eighth of SCLK frequency.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{(qq)}$	V_I disable current	EN > V_{IH}, all outputs software disabled		1.7	2.16	mA
$I_{(q)}$	V_I quiescent current	EN pin < V_{IL}		0.7	1	mA
CUMULATIVE REGULATION						
	Regulation accuracy	Voltage codes 12.3 V, 12.7 V, 13.1 V	−2%		2%	
		Voltage codes < 12.3 V	−2.5%		2.5%	
OSCILLATOR						
$f_{(osc)}$	Free-run frequency		350	450	550	kHz
$f_{(sync)}$	Sync frequency range	$f_{(sync)}$ = SCLK / 8	550		750	kHz
	Phase stagger count	Phase difference after initialization command (see Note 2)		4		SCLK
UVLO						
$V_{(UVLO)}$	Undervoltage lockout threshold			13	13.5	V
$V_{hys(UVLO)}$	UVLO hysteresis		1.3	1.45	1.6	V

NOTE 2: Ensured by design

electrical characteristics over recommended operating conditions (unless otherwise noted) (continued)

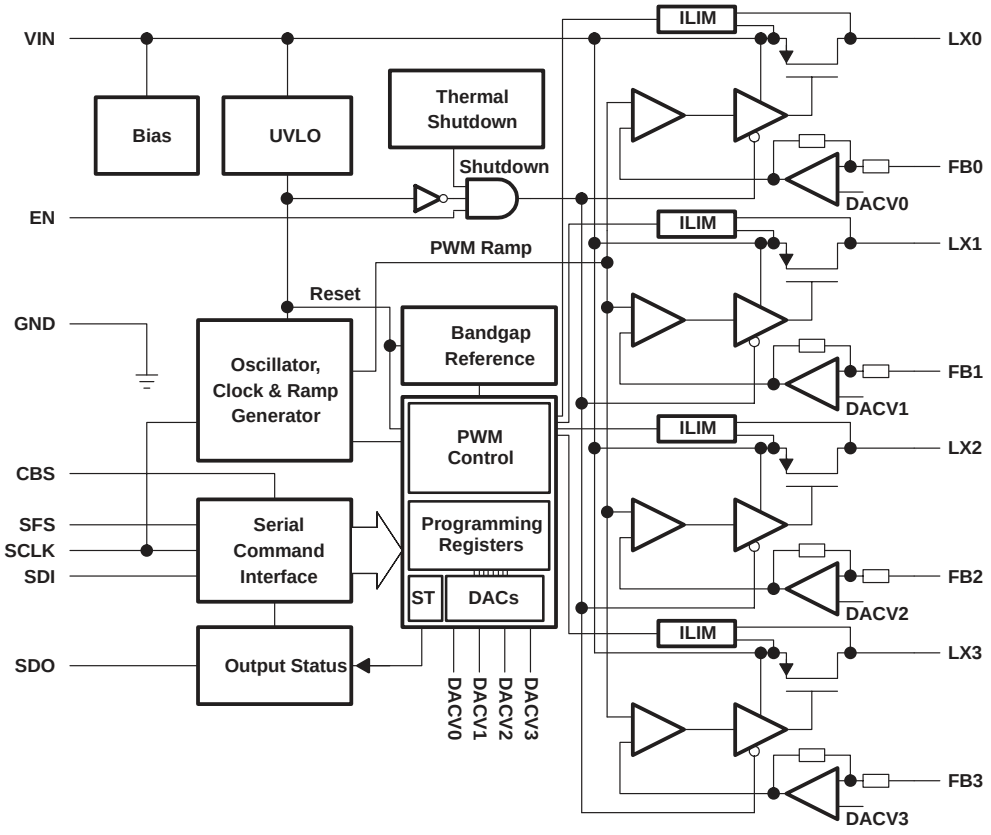
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE						
	Enable threshold		2.0			V
	Disable threshold				0.8	V
	Bypass threshold	Relative to VIN	−1.4		−0.5	V
CBS						
	Logic high threshold		2.0			V
	Logic low threshold				0.8	V
OVERCURRENT LIMIT						
$I_{(th-OCL)}$	OCL trip threshold	Channel settled after change of voltage code or EN asserted	250	450	750	mA
$t_{(OCL)}$	OCL hiccup time	$f_{(sync)}$ = 552 kHz (see Note 2)	170		360	ms
PMOS FET SWITCH						
$r_{DS(on)}$	ON resistance	Id = 0.1A		0.8	1.4	Ω
TRANSITION TIME						
$t_{d(EN)}$	Enable delay time	7.5 < V_O < 15, time from EN > V_{IH} to Channel status word = 00H		9		ms
t_{TLH}	Low−high transition time, V_O	Command from 7.5 V to bypass, VIN = 15.0 V		4		ms
t_{THL}	High−low transition time, V_O	Command from bypass to 7.5 V, 175 Ω load with VIN = 15.0 V		4		ms
THERMAL SHUTDOWN						
$T_{(OTP)}$	Over temperature trip point, T_J	Junction temperature exceeds $T_{(OTP)}$		150		°C
$T_{(hys)}$	Hysteresis temperature			10		°C
SERIAL PORT						
t_{su}	Setup time, SDIN, SFS	Inputs valid before SCLK falling edge (see Note 2)	20			ns
t_h	Hold time, SDIN, SFS	Inputs held after SCLK falling edge (see Note 2)	5			ns
$t_{c(SFS)}$	Cycle time, SFS	minimum time between commands (see Note 2)	18			SCLK
$V_{OL(SDO)}$	Output low, SDO	$I_{(sink\ SDO)}$ = 0.5 mA (see Note 2)			0.4	V
$t_{d(SCLK)}$	Delay time, SDO	SCLK rising to SDO valid (see Note 2)	0		15	ns
I_{lkg}	Off-state leakage current, SDO	SDO = 3.3 V (see Note 2)	−1		1	µA
V_{IL}	Input low voltage	See Note 2			0.7	V
V_{IH}	Input high voltage	See Note 2	2.3			V

NOTE 2: Ensured by design

Terminal Functions

TERMINAL NAME	TERMINAL NO.	PIN DESCRIPTION	FUNCTIONAL DESCRIPTION
LX0	1	Channel 0 switch output	Output to inductor and catch diode
LX1	2	Channel 1 switch output	
GND	3	Ground	Power and Analog Ground
SFS	4	Frame sync input	Read/write frame start strobe
SDI	5	Serial data in	8 bit address/16−bit data word command input
EN	6	Enable	EN < V_{IL}: Disable all channels, EN > V_{IH}: Enable activates outputs (see text)
FB0	7	Channel 0 feedback input	Feedback from L−C filter output
FB1	8	Channel 1 feedback input	
FB2	9	Channel 2 feedback input	
FB3	10	Channel 3 feedback input	
CBS	11	Channel bank select	Assigns internal channels to respond to serial address bit ADR2 = 0 when CBS < V_{IL}, or to ADR2 = 1 when CBS > V_{IH}
SCLK	12	Serial clock input	Serial clock/synchronization signal
SDO	13	Serial data out	Status data output signal, open drain
VIN	14	Input supply voltage	Chip supply and channel 0−3 switch input
LX2	15	Channel 2 switch output	Output to inductor and catch diode
LX3	16	Channel 3 switch output	

functional block diagram



detailed description

reference system/voltage divider and multiplexer

The reference system consists of a band-gap circuit, four digital to analog converter outputs (DACs), and smoothing filters. The reference system provides independent set-point voltages to the PWM control loops of each channel, and are programmed via the 4-wire serial port. Output control of the regulators is provided in 15 steps with 400-mV resolution over a range of 7.5 V to 13.1 V. The DACs can also be programmed to force the PMOSFETs into the fully *on* pass-through or bypass mode to pass the input voltage to any output.

UVLO circuit and power-up state

The undervoltage lockout (UVLO) circuit controls device operation when the input voltage is below the UVLO threshold such as during power up or power down. Hysteresis built in to the UVLO detection circuit reduces sensitivity to noise and ripple on the power supply inputs to the TPS54900. Prior to reaching the UVLO threshold, the ramp oscillator is disabled so that no switching occurs in the TPS54900, the PMOS transistors are forced into the off-state, and the registers and DACs are reset. Once the UVLO threshold is reached, the soft-start sequence begins. If the input voltage falls below the UVLO threshold after the device is programmed and operating, all four outputs are disabled, the DACs are set to zero volts, and the programming registers are reset. Subsequently returning VIN above the UVLO threshold requires reinitialization of the phase stagger and channel voltage programming

soft-start sequence and voltage transitioning

When the supply voltage exceeds the UVLO threshold, the TPS54900 is ready to be programmed via the serial interface. As each channel is programmed and enabled with a voltage code, the channel DACs begin stepping the output up from zero volts to the target voltage in 200-mV increments. If the target voltage is 15 V (i.e., pass-through mode) the DAC continues to increment in 200-mV steps between 13.1 V and the fully *on* state. When a channel is commanded to transition from one voltage level to another, the output steps up (or down) to the new level in 200-mV increments. The period between each DAC increment is approximately 87 µs when the SCLK frequency equals 4.416 MHz. This results in a maximum ramp-up time of 8 ms when stepping from 0 V to 15 V, and a maximum transition time between max and min regulation voltages (7.5 V, 13.1 V) of 4 ms. The use of small step increments provides a smooth predictable ramp and prevents inadvertent tripping of the overcurrent limit.

During this transition period, the channel status may be read via the 4-wire serial port using the read protocol. The data returned is nonzero while channel is transitioning.

oscillator, divider and sync circuit

The TPS54900 has a free-running internal ramp oscillator that operates at a nominal frequency of 450 kHz. When the 4.416-MHz SCLK signal is present, a synchronous divide-by-eight circuit provides a 552-kHz clock to synchronize the PWM ramp. The start of the ramp is coincident with every eighth rising edge of SCLK. If the TPS54900 SCLK pin is driven at a frequency lower than eight times the free-running frequency of the oscillator (f_{osc}), it may result in chaotic operation. Care should be taken to ensure that the minimum frequency at the SCLK input is 4.4 MHz.

phase stagger circuit

When two TPS54900 devices are used as a pair to operate as an 8-channel unit, the PWM ramps in the two devices can be phase staggered to reduce input ripple and bypass requirements. The initialization command forces the PWM ramp of the device with its CBS pin tied low to be staggered by four SCLK cycles compared to the device with its CBS pin forced to a logic high. Note that this command clears the voltage programming in both devices and disables the outputs. Voltage programming instructions can be issued immediately following the initialization command.

detailed description (continued)

enable (EN)

If the EN pin is held low when the TPS54900 is powered up, the oscillator starts and free-runs. Serial commands to initialize the PWM clocks and program the output levels are accepted, but the outputs are held off and do not begin regulating until the EN pin is pulled above V_{IH}.

If the TPS54900 is first programmed with outputs enabled and then EN is pulled LOW, all outputs are shut off and all DACs are reset. The EN pin does not affect the oscillator, which continues to run and maintain PWM phase stagger. The previously programmed channel voltages are also maintained in the registers. If EN is pulled above V_{IH}, the TPS54900 channels start up through the soft-start sequence and reach regulation at the previously programmed target voltages.

Bypass mode may be forced on all outputs by pulling EN above VIN – 0.5 V. When bypass mode is forced, all four channels step up to VIN in 200-mV increments.

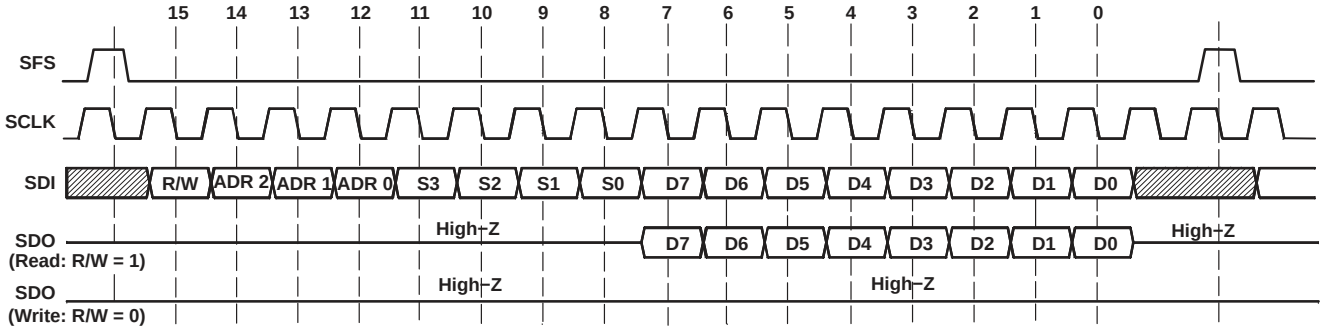
over current protection

During steady state operation, the overcurrent protection threshold is 250 mA minimum, 750 mA maximum, sampled approximately 500 ns after the start of the switching cycle. When overcurrent is sensed in the PMOSFET, the output is disabled for a *hiccup* time of 170 ms to 360 ms (SCLK = 4.416 MHz). In the *pass-through* mode, the overcurrent detection remains active and the *hiccup* behavior is unchanged.

thermal shutdown

Thermal shutdown disables the controller if the junction temperature exceeds 150°C. The hysteresis is 10°C. This shuts down off the switching circuitry and resets the soft-start circuitry. If the IC returns to normal temperature, it restarts and returns to the programmed target voltages.

serial control interface timing diagram



serial command bit assignments

SERIAL BIT		
POSITION	**NAME**	**DESCRIPTION**
15	R/W	Set to logic 1 to read from TPS54900, set to logic 0 to write to TPS54900
14	ADR2	Channel bank select, compared to logic state of CBS pin to select between two TPS54900 devices used in an 8-channel configuration
13	ADR1	Internal channel select MSB, used with ADR0 to select one of four output channels
12	ADR0	Internal channel select LSB, used with ADR1 to select one of four output channels
11	S3	Device address MSB (S3 = 1 required to address TPS54900)
10	S2	Device address bit (S2 = 1 required to address TPS54900)
9	S1	Device address bit (S1 = 1 required to address TPS54900)
8	S0	Device address LSB (S0 = 1 required to address TPS54900)
7	D7	Voltage programming MSB
6	D6	Voltage programming bit
5	D5	Voltage programming bit
4	D4	Voltage programming LSB
3	D3	Channel enable/disable (D3 = 0 enables channel(s))
2	D2	Global start
1	D1	Unassigned
0	D0	Initialize counters

valid commands

WORD	DESCRIPTION
00001111 00001001	Initialize PWM clocks with phase stagger and disable all channels
0ddd1111 vvvv0100	Turn on and regulate all channels to voltage code vvvv (see voltage programming code table)
0aaa1111 vvvv0000	Turn on and regulate channel aaa to voltage code vvvv (see voltage programming code table)
0aaa1111 dddd1000	Disable channel aaa
1aaa1111 dddddddd	Read channel status from channel aaa

NOTE: aaa: three bit channel address, 0aa: corresponds to CBS pin < V_{IL}
1aa: corresponds to CBS > V_{IH}
vvvv: voltage programming code
d: *don't care* state

voltage programming codes

VOLTAGE CODE (D4−D7)	Figure 1	VOLTAGE CODE (D4−D7)	OUTPUT VOLTAGE
0	7.5	8	10.7
1	7.9	9	11.1
2	8.3	A	11.5
3	8.7	B	11.9
4	9.1	C	12.3
5	9.5	D	12.7
6	9.9	E	13.1
7	10.3	F	Pass through mode

channel status read back codes

STATUS BYTE VALUE (D0−D7)	OUTPUT MEANING
00H	Channel settled to regulation window
Non-zero	Channel not settled or fault condition (see Note 3)

NOTE 3: Fault conditions detected include over current fault on channel addressed and over temperature fault for device (all channels)

serial interface protocol

The serial interface uses serial clock (SCLK), serial frame sync (SFS), serial data in (SDI), bank select inputs, and outputs device status on serial data out (SDO). SFS and SDI inputs are sampled on the falling edge of SCLK. An SFS pulse indicates that the bus master is ready to transmit a word, and the bit and frame counters in the TPS54900 are reset when SFS is high. The first bit (b15) of the 16-bit word is shifted in on the next falling edge of SCLK. The first eight bits of the word are denoted as the address or command, and the last eight bits are data. Refer to the table titled *Serial Command Bit Assignments*.

The command consists of three fields: the R/W bit, channel select bits ADR2−0, and for device select bits S3−S0. The R/W bit determines whether the data portion of the word is written to the TPS54900 or read from the TPS54900. The value in the channel select field determines which output channel is to receive programming data. Channel select bit ADR2 is compared to the logic level on the channel bank select input. This allows two distinct TPS54900 devices to be addressed as one logical eight-channel unit. The remaining bits ADR1, ADR0 are decoded to select one of the four on chip channels. The third part of the command is the 4-bit device select, bits S3−S0. The TPS54900 has been assigned a device ID of *F* for S3−S0. This value must be used to address TPS54900 devices.

The data field, D7−D0, is used to program output voltage levels and control TPS54900 operation.

pass through mode

The pass through mode may be used to force a channel's PMOSFETs to remain in the fully enhanced *on* state. Use of the pass through mode is desirable under several conditions. First, transmitting high peak-to-peak voltages requires maximum headroom on the line driver supply. Second, if the load current is too small, the line ranger circuit is required to operate in discontinuous mode. The output may ring in response to transient conditions. Low load current conditions may occur if the line driver is idle and the quiescent current has been reduced to conserve power. If the line must remain ready to return to normal operation, the pass through mode is appropriate. If the line is unused or can tolerate start up delays, the channel shutdown mode should be considered to conserve additional power.

channel shut down

A bit value of 1 in bit 3 is used to shut down the addressed channel. Shutting down an unused channel is recommended when power savings warrant complete power down of a line driver and start-up delays in returning to normal operation are not critical.

global program

Data bit 2 in the serial word is the *global turn-on and regulate* signal. It is used to program all outputs to the same voltage and start them up at the same time.

PWM clock initialization

Data bit 0 is used to initialize the onboard clocks. The signal to initialize the clocks is ANDed with data bit 5 and cannot be given without powering down the TPS54900 and going through a complete restart sequence.

status readback

The TPS54900 is designed to monitor its output state and recognize when it has settled into regulation at its programmed value. The open drain SDO pin reports a channel in a voltage transition or error condition (Channel Not Ready) by returning a *non-zero* data value. When SDO returns a value of 00h, the channel is in regulation.

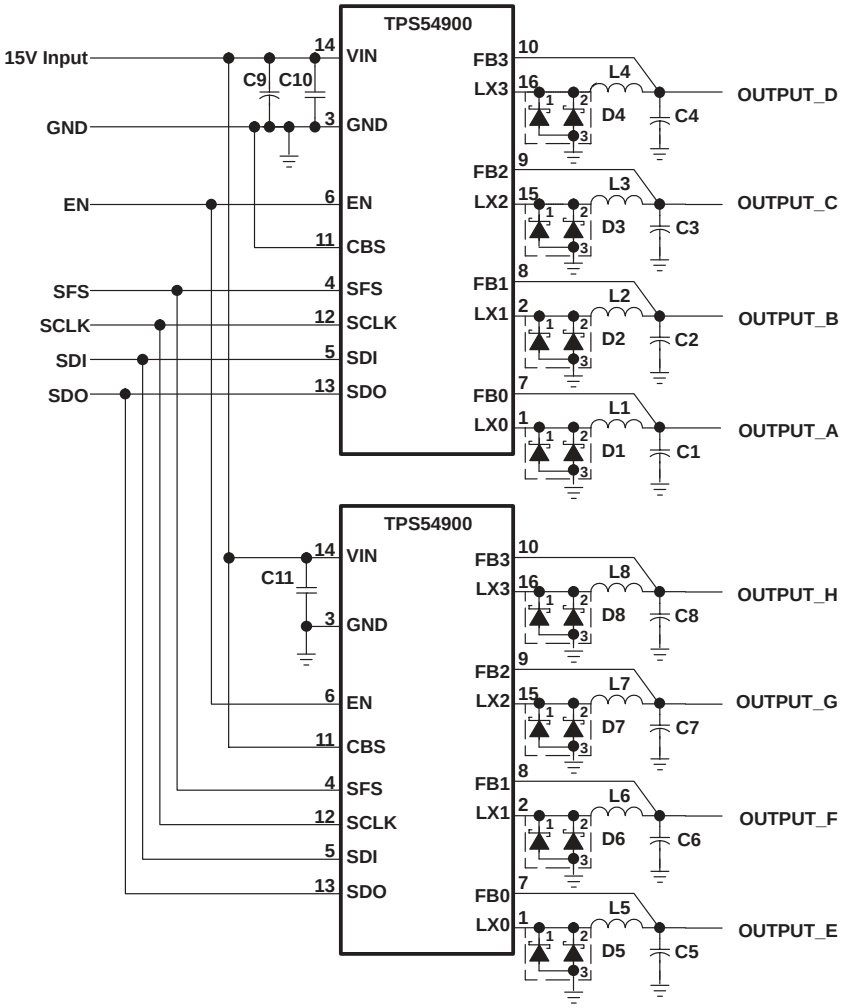
Any of the following conditions cause a *channel not ready* status to be reported:

- Channel disabled
- PWM duty factor outside expected range (i.e. 0% or 100% PW)
- Channel in overcurrent
- Channel transitioning to new target value
- Over-temperature shutdown (affects all four channels)

Noise immunity circuits in the fault detector introduce a delay in the reporting of the channel status. For instance, if a command to transition to a new target voltage is issued, the output voltage may be stable up to 250 μs before the detection circuit reports that the channel is ready. The minimum recommended status polling interval per channel is 500 μs.

APPLICATION INFORMATION

eight channel application circuit schematic



APPLICATION INFORMATION

component selection

Components were selected to maximize efficiency while maintaining acceptable area, stability, and output noise. For instance in choosing the free wheeling diodes, both junctions in the SOT−23 package are used in parallel to save up to 6 mW per channel. The recommended output filter and internal compensation were selected with the expectation of a 3.3-µH, 15-µF post filter located at the load (line driver supply input). Use of one or more ceramic capacitors in place of the 10-µF tantalum for the output filter can reduce board area at the cost of increased noise and reduced stability margin. Inductors with smaller mechanical dimensions than those from GCI or Bourns, such as the Coilcraft, reduce required board area and decrease conversion efficiency up to 4%. Use of nonshielded inductors may increase efficiency, but add risk of EMI. System level testing should be performed in qualifying component and layout decisions.

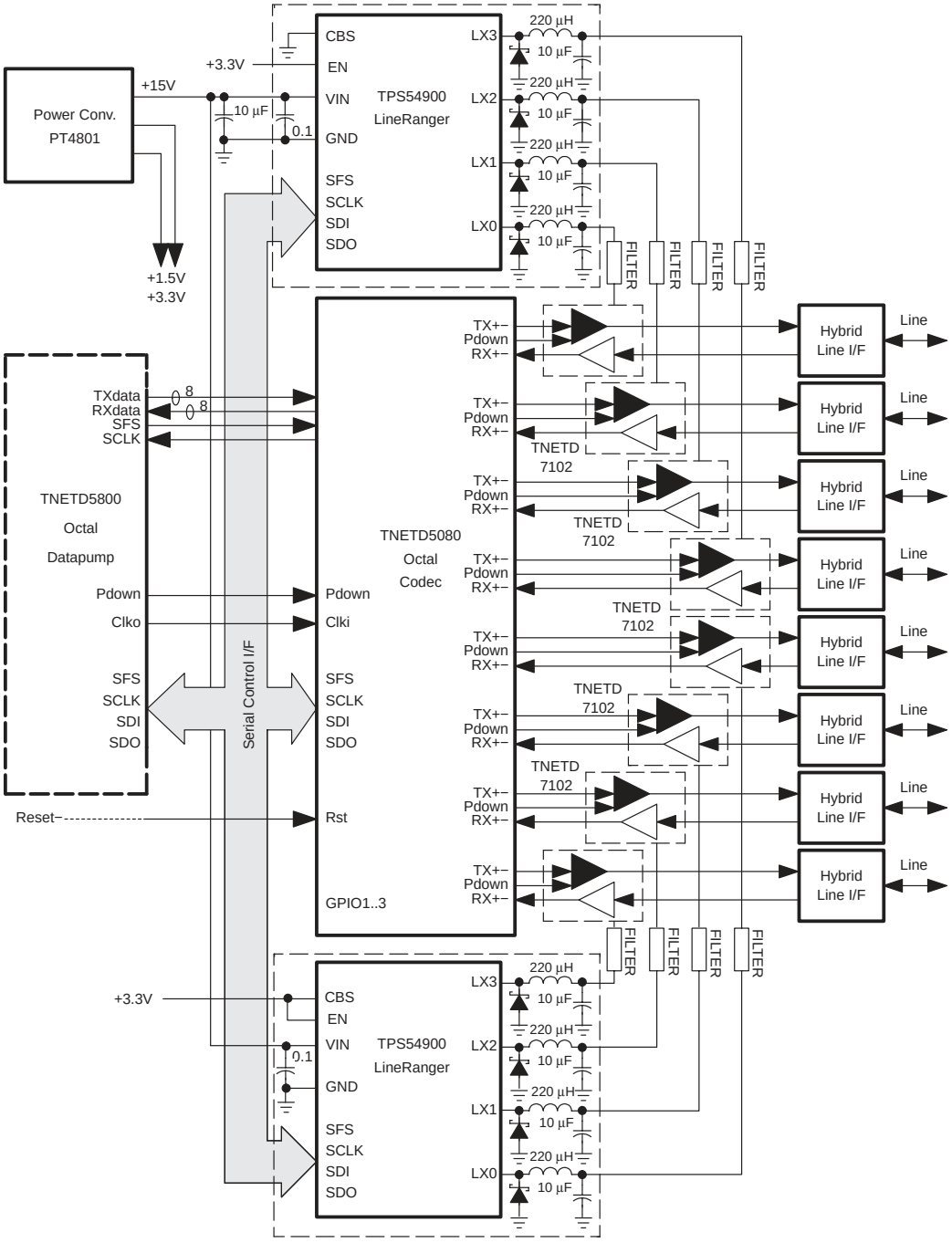
layout considerations

Two portions of the layout are critical and deserve close attention. First, the high frequency input bypass capacitors (C10 and C11 in the eight channel application circuit diagram) must be placed as close as possible and routed directly to the TPS54900 VIN and GND pins to minimize trace inductance.

Second, the free wheeling diodes (D1−8 in the eight channel application circuit diagram) must also be placed as close as possible and routed directly to the TPS54900 LX_ and GND pins. Placing the diodes on the opposite side of the board as the TPS54900, immediately opposite the TPS54900, facilitates low impedance routing of the diodes to the appropriate TPS54900 pins. The EVM layout uses this approach.

APPLICATION INFORMATION

block diagram of eight channel AC5 line card with LineRanger option



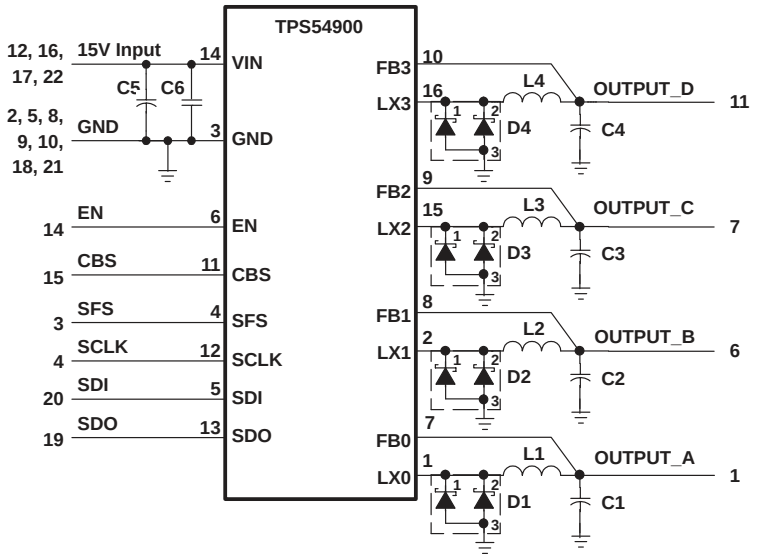
APPLICATION INFORMATION

evaluation circuit

module pin assignments

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	OUTPUT A	22	15 V Input
2	GND	21	GND
3	SFS	20	SDI
4	SCLK	19	SDO
5	GND	18	GND
6	OUTPUT B	17	15 V Input
7	OUTPUT C	16	15 V Input
8	GND	15	Channel Bank Select
9	GND	14	Enable
10	GND	13	N/C
11	OUTPUT D	12	15 V Input

application schematic



Contact Texas Instruments for additional information on external components recommendations and EVM availability.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54900PW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85		
TPS54900PWG4	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

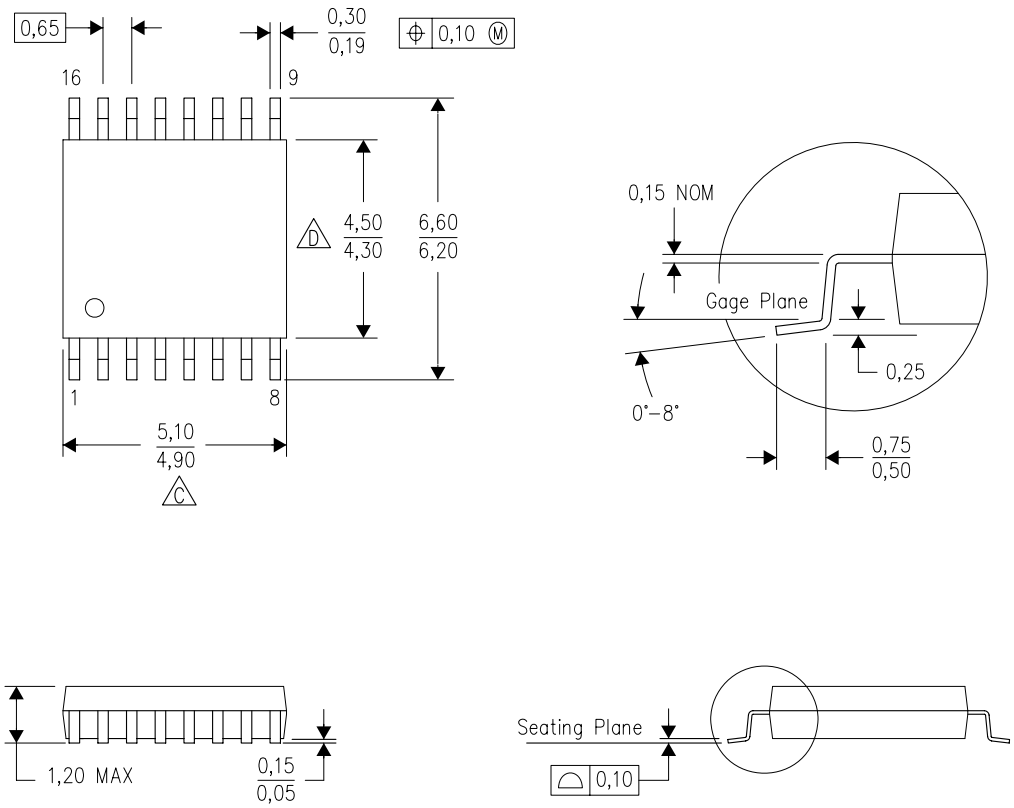
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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