

IS31AP4833

TREBLE AND BASS CONTROL WITH 3D ENHANCEMENT AUDIO POWER DRIVER

September 2021

GENERAL DESCRIPTION

The IS31AP4833 is a treble and bass control with 3D enhancement audio power driver. The IS31AP4833 provides tone (bass and treble) controls and volume control as well as a stereo audio power amplifier capable of delivering 2.8W into 4Ω with less than 10% THD with a 5V supply.

The IS31AP4833 uses flexible I2C control interface for multiple application requirements. It also features 3D sound circuitry which can be externally adjusted via a simple RC network.

The IS31AP4833 features a 13 steps tone control (-12dB ~ +12dB, 2dB/step) and a 29 steps volume control (mute, -42dB ~ +12dB, 2dB/step) for the headphone and stereo outputs. The volume and tone are controlled through an I2C compatible interface. The IS31AP4833 can get independent volume control for two channels.

IS31AP4833 is available in QFN-36 (4mm × 4mm) and TQFP-48(7mm × 7mm) package. It operates from 3.0V to 5.5V over the temperature range of -40°C to +85°C.

FEATURES

- 3.0V to 5.5V supply
- Mute control
- Treble and bass control
- Independent volume control for two channels
- Stereo input MUX
- I2C control interface
- 3D enhancement
- Thermal shutdown protection
- Click-and-pop suppression
- QFN-36(4mm × 4mm) and TQFP-48(7mm × 7mm) package

APPLICATIONS

- Cell phones, PDA, MP4, PMP
- Portable and desktop computers
- Desktops audio system
- Multimedia monitors

TYPICAL APPLICATION CIRCUIT

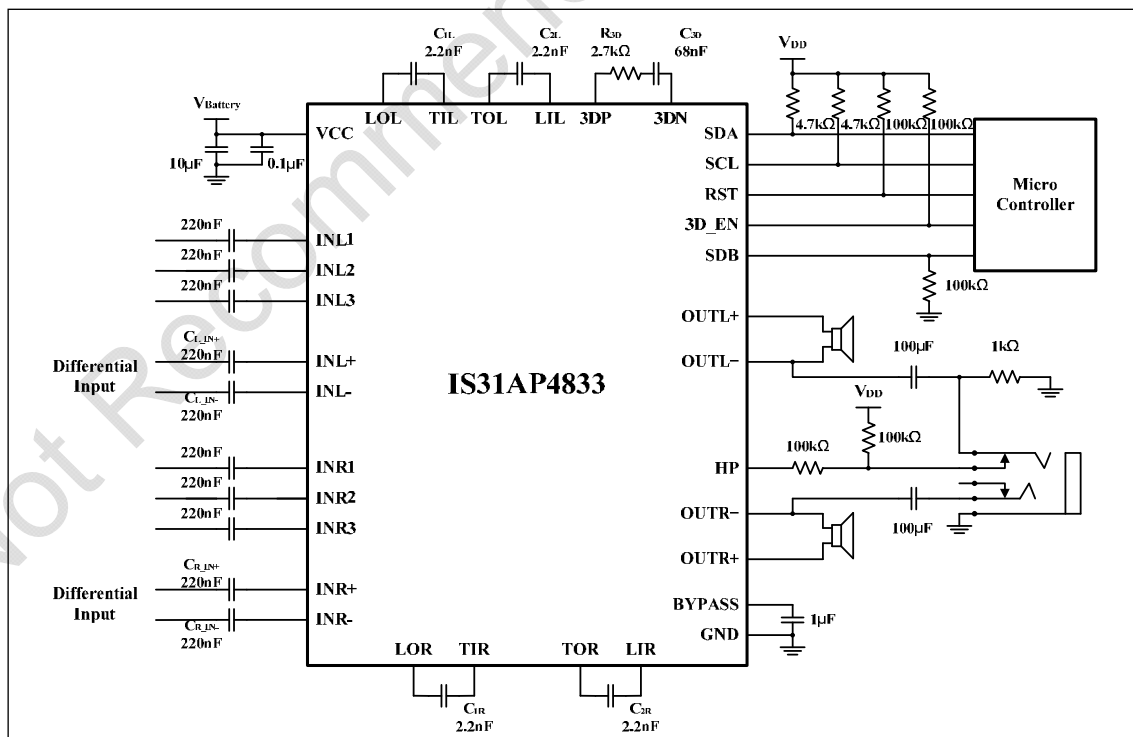


Figure 1 Typical Application Circuit

IS31AP4833

PIN CONFIGURATION

| Package | Pin Configuration (Top View) |
|---------|---|
| QFN-36 | <p>Pin Configuration (Top View) for QFN-36:</p> <ul style="list-style-type: none"> Top edge: 36 INL2, 35 INL3, 34 INL+, 33 INL-, 32 AGND, 31 INR-, 30 INR+, 29 INR3, 28 INR2 Left edge: 1 INL1, 2 LOL, 3 TIL, 4 OUTL+, 5 VCC, 6 OUTL-, 7 LIL, 8 TOL, 9 SDA Right edge: 27 INR1, 26 LOR, 25 TIR, 24 OUTR+, 23 VCC, 22 OUTR-, 21 LIR, 20 TOR, 19 SCL Bottom edge: 10 SDB, 11 BYPASS, 12 NC, 13 RST, 14 PGND, 15 HP, 16 3D_EN, 17 3DN, 18 3DP |
| TQFP-48 | <p>Pin Configuration (Top View) for TQFP-48:</p> <ul style="list-style-type: none"> Top edge: 48 INL2, 47 NC, 46 INL3, 45 INL+, 44 INL-, 43 GND, 42 GND, 41 INR-, 40 INR+, 39 INR3, 38 NC, 37 INR2 Left edge: 1 INL1, 2 NC, 3 LOL, 4 TIL, 5 OUTL+, 6 NC, 7 VCC, 8 NC, 9 OUTL-, 10 LIL, 11 TOL, 12 SDA Right edge: 36 INR1, 35 NC, 34 LOR, 33 TIR, 32 OUTR+, 31 NC, 30 VCC, 29 NC, 28 OUTR-, 27 LIR, 26 TOR, 25 SCL Bottom edge: 13 NC, 14 SDB, 15 BYPASS, 16 NC, 17 RST, 18 GND, 19 GND, 20 HP, 21 3D_EN, 22 3DN, 23 3DP, 24 NC |

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PIN DESCRIPTION

| No. | | Pin | Description |
|--------|-------------------------------|-------------|--|
| QFN-36 | TQFP-48 | | |
| 1 | 1 | INL1 | Left channel single-ended input1. |
| 2 | 3 | LOL | Left channel tone control loop out. |
| 3 | 4 | TIL | Left channel tone control in. |
| 4 | 5 | OUTL+ | Positive output of left channel. |
| 5, 23 | 7,30 | VCC | Power supply. |
| 6 | 9 | OUTL- | Negative output of left channel. |
| 7 | 10 | LIL | Left channel tone control loop in. |
| 8 | 11 | TOL | Left channel tone control out. |
| 9 | 12 | SDA | I2C serial data. |
| 10 | 14 | SDB | It will into shutdown mode when pull low. |
| 11 | 15 | BYPASS | Bypass capacitor which provides the common mode voltage. |
| 12 | 2,6,8,13,16,24,29,31,35,38,47 | NC | No connection. |
| 13 | 17 | RST | Reset chip logic and states. Active low. |
| 14,32 | 18,19,42,43 | GND | Ground. |
| 15 | 20 | HP | Detect HP insert or not. |
| 16 | 21 | 3D_EN | It will into 3D enhance mode when pull high. |
| 17 | 22 | 3DN | Negative channel 3D input. |
| 18 | 23 | 3DP | Positive channel 3D input. |
| 19 | 25 | SCL | I2C serial clock. |
| 20 | 26 | TOR | Right channel tone control out. |
| 21 | 27 | LIR | Right channel tone control loop in. |
| 22 | 28 | OUTR- | Negative output of right channel. |
| 24 | 32 | OUTR+ | Positive output of right channel. |
| 25 | 33 | TIR | Right channel tone control in. |
| 26 | 34 | LOR | Right channel tone control loop out. |
| 27 | 36 | INR1 | Right channel single-ended input1. |
| 28 | 37 | INR2 | Right channel single-ended input2. |
| 29 | 39 | INR3 | Right channel single-ended input3. |
| 30 | 40 | INR+ | Right channel positive differential input. |
| 31 | 41 | INR- | Right channel negative differential input. |
| 33 | 44 | INL- | Left channel negative differential input. |
| 34 | 45 | INL+ | Left channel positive differential input. |
| 35 | 46 | INL3 | Left channel single-ended input3. |
| 36 | 48 | INL2 | Left channel single-ended input2. |
| | | Thermal Pad | Connect to GND. |

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ORDERING INFORMATION INDUSTRIAL RANGE: -40°C TO +85°C

| Order Part No. | Package | QTY |
|---------------------|--------------------|-----------|
| IS31AP4833-QFLS2-TR | QFN-36, Lead-free | 2500/Reel |
| IS31AP4833-TQLS2 | TQFP-48, Lead-free | 250/Tray |

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- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Lumissil Microsystems is adequately protected under the circumstances

IS31AP4833

ABSOLUTE MAXIMUM RATINGS

| | |
|--|-----------------------|
| Supply voltage, V_{CC} | -0.3V ~ +6.0V |
| Voltage at any input pin | -0.3V ~ $V_{CC}+0.3V$ |
| Maximum junction temperature, T_{JMAX} | +150°C |
| Storage temperature range, T_{STG} | -65°C ~ +150°C |
| Operating temperature range, T_A | -40°C ~ +85°C |
| ESD (HBM) | ±8kV |
| ESD (CDM) | ±1kV |

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, unless otherwise noted. Typical value are $T_A = 25^\circ\text{C}$, $V_{CC} = 3.6V$.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|--------------|--------------------------------|--|------|------|------|---------------|
| V_{CC} | Supply voltage | | 3.0 | | 5.5 | V |
| I_{SD} | Shutdown current | $V_{SDB} = 0V$ | | 1 | | μA |
| | | $V_{SDB} = V_{CC}$, software shutdown | | 1 | | |
| I_{CC} | Quiescent power supply current | $V_{IN} = 0V$, $I_O = 0A$, $V_{HP} = 0V$, no load | | 6 | | mA |
| | | $V_{IN} = 0V$, $I_O = 0A$, $V_{HP} = 5V$, no load | | 4 | | |
| V_{IH_HP} | HP input high-voltage | $V_{CC} = 5.0V$ | 4.1 | | | V |
| | | $V_{CC} = 3.0V$ | 2.3 | | | |
| V_{IL_HP} | HP input low-voltage | $V_{CC} = 5.0V$ | | | 3.4 | V |
| | | $V_{CC} = 3.0V$ | | | 1.54 | |
| V_{IH} | Input high-voltage | | 1.4 | | | V |
| V_{IL} | Input low-voltage | | | | 0.4 | V |

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AC CHARACTERISTICS (Note 1)

$T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$, unless otherwise noted.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|----------|--------------------------------------|---|------|-------|------|---------------|
| Po | Output power | THD+N = 10%, f = 1kHz, $R_L = 4\Omega$, speaker | | 2.80 | | W |
| | | THD+N = 1%, f = 1kHz, $R_L = 4\Omega$, speaker | | 2.20 | | |
| | | THD+N = 10%, f = 1kHz, $R_L = 8\Omega$, speaker | | 1.75 | | |
| | | THD+N = 1%, f = 1kHz, $R_L = 8\Omega$, speaker | | 1.45 | | |
| | | THD+N = 10%, f = 1kHz, $R_L = 32\Omega$, headphone | | 0.11 | | |
| | | THD+N = 1%, f = 1kHz, $R_L = 32\Omega$, headphone | | 0.091 | | |
| THD+N | Total harmonic distortion plus noise | $P_O = 1.5\text{W}$, f = 1kHz, $R_L = 4\Omega$, speaker | | 0.069 | | % |
| | | $P_O = 0.9\text{W}$, f = 1kHz, $R_L = 8\Omega$, speaker | | 0.046 | | |
| | | $P_O = 75\text{mW}$, f = 1kHz, $R_L = 32\Omega$, headphone | | 0.022 | | |
| t_{WU} | Wake-up time from shutdown | | | 130 | | ms |
| PSRR | Power supply rejection ratio | $V_{CC} = 3.0\text{V}$, f = 217Hz, $R_L = 8\text{k}\Omega$, speaker | | -67 | | dB |
| V_{NO} | Noise | $V_{CC} = 3.0\text{V}\sim 5.0\text{V}$, $V_{IN} = 0\text{V}$, $R_L = 4\Omega$, speaker | | 60 | | μV |

DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 1)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---------------|--|-----------|------|----------|------|---------------|
| f_{SCL} | Serial-Clock frequency | | | | 400 | kHz |
| t_{BUF} | Bus free time between a STOP and a START condition | | 1.3 | | | μs |
| $t_{HD, STA}$ | Hold time (repeated) START condition | | 0.6 | | | μs |
| $t_{SU, STA}$ | Repeated START condition setup time | | 0.6 | | | μs |
| $t_{SU, STO}$ | STOP condition setup time | | 0.6 | | | μs |
| $t_{HD, DAT}$ | Data hold time | | | | 0.9 | μs |
| $t_{SU, DAT}$ | Data setup time | | 100 | | | ns |
| t_{LOW} | SCL clock low period | | 1.3 | | | μs |
| t_{HIGH} | SCL clock high period | | 0.7 | | | μs |
| t_R | Rise time of both SDA and SCL signals, receiving | (Note 2) | | 20+0.1Cb | 300 | ns |
| t_F | Fall time of both SDA and SCL signals, receiving | (Note 2) | | 20+0.1Cb | 300 | ns |

Note 1: Guaranteed by design.

Note 2: Cb = total capacitance of one bus line in pF. $I_{SINK} \leq 6\text{mA}$. t_R and t_F measured between $0.3 \times V_{CC}$ and $0.7 \times V_{CC}$.

TYPICAL PERFORMANCE CHARACTERISTICS

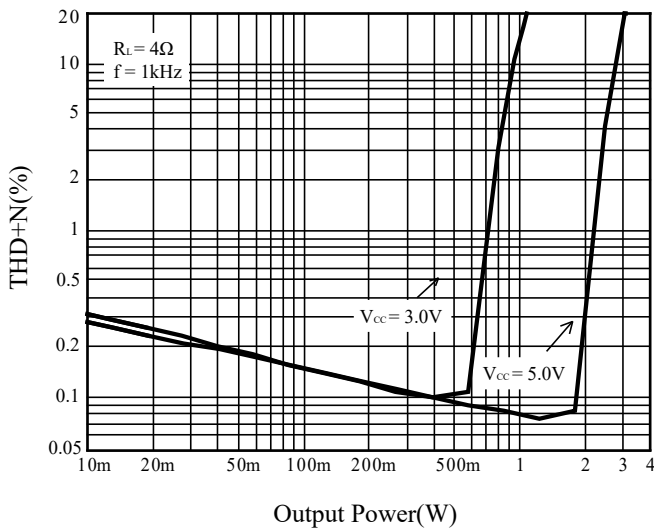


Figure 2 THD+N vs. Output Power

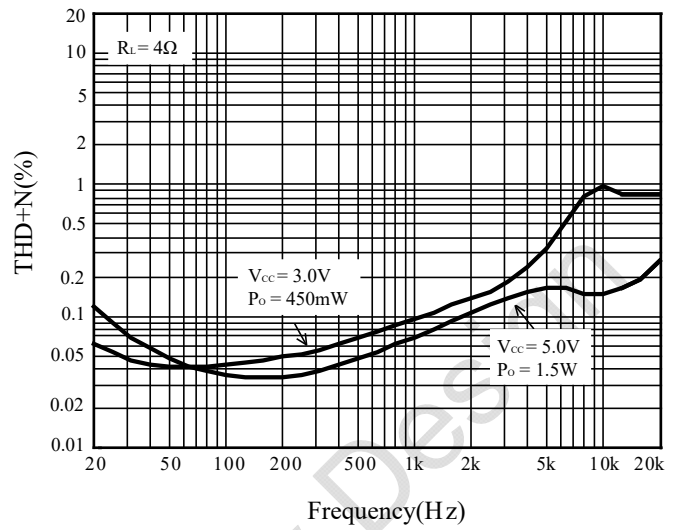


Figure 3 THD+N vs. Frequency

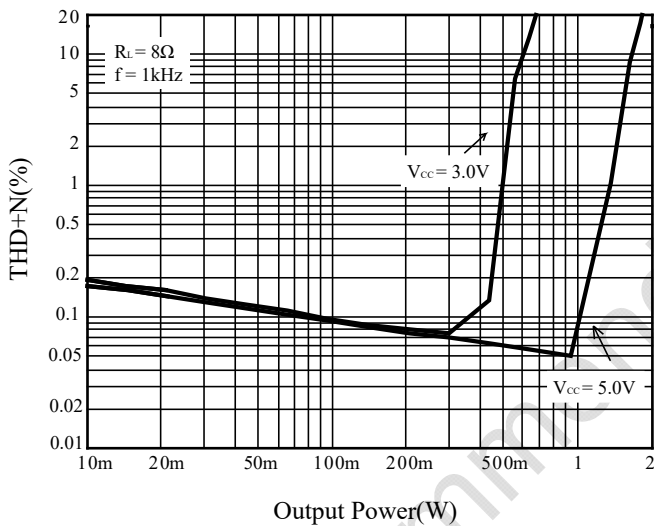


Figure 4 THD+N vs. Output Power

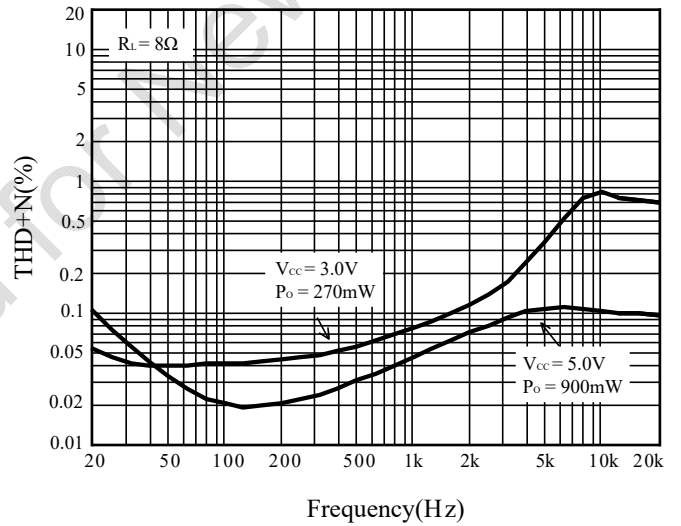


Figure 5 THD+N vs. Frequency

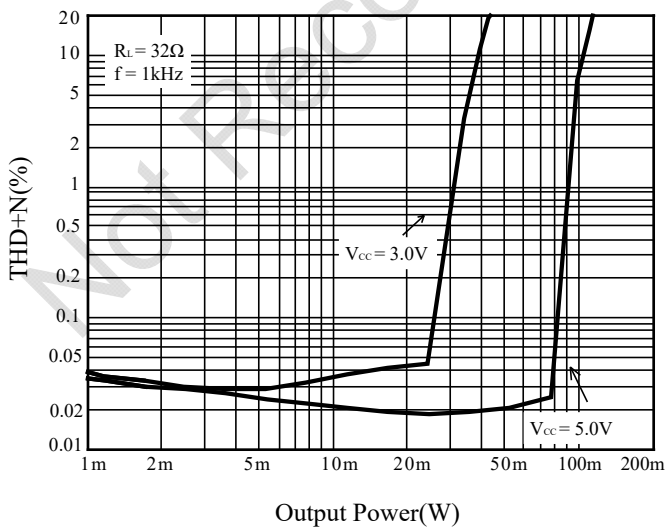


Figure 6 THD+N vs. Output Power

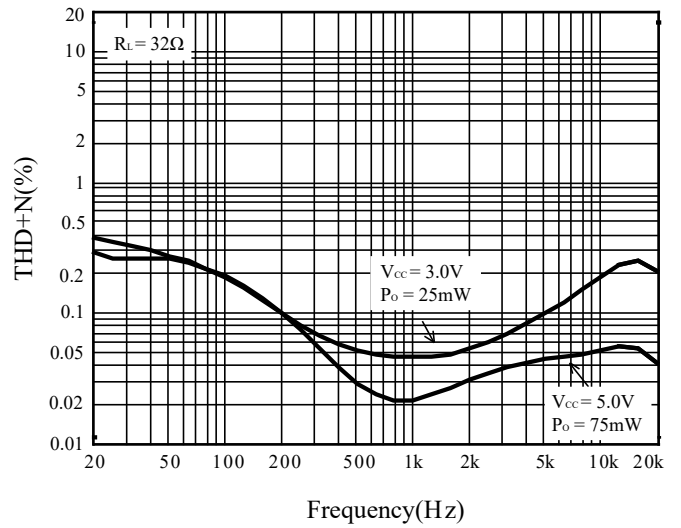


Figure 7 THD+N vs. Frequency

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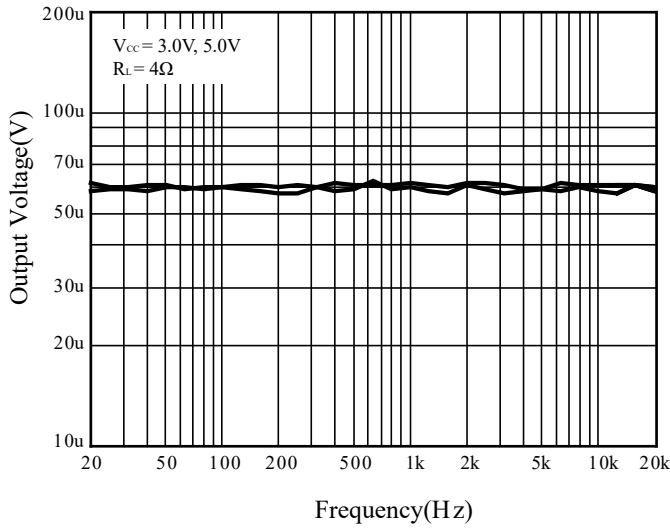


Figure 8 Noise vs. Frequency

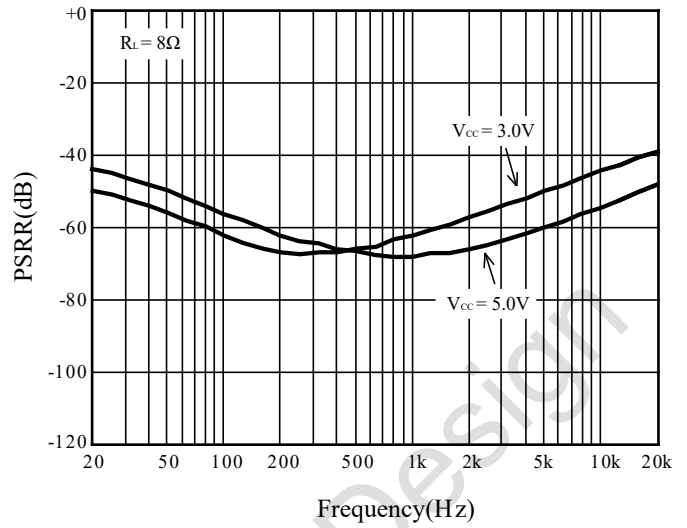


Figure 9 PSRR vs. Frequency

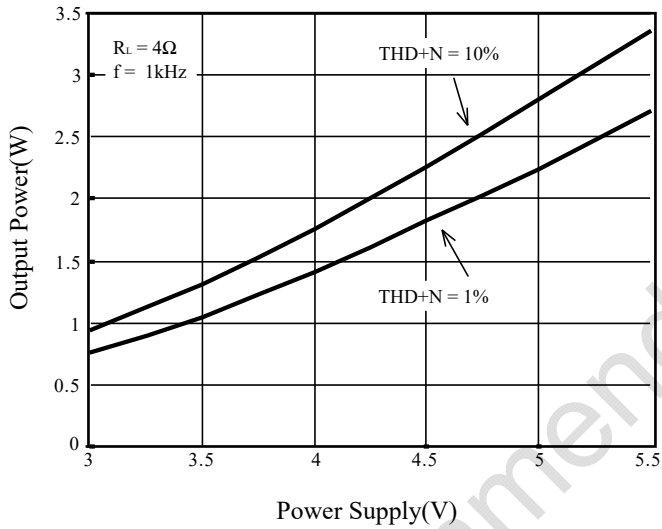


Figure 10 Output Power vs. Power Supply

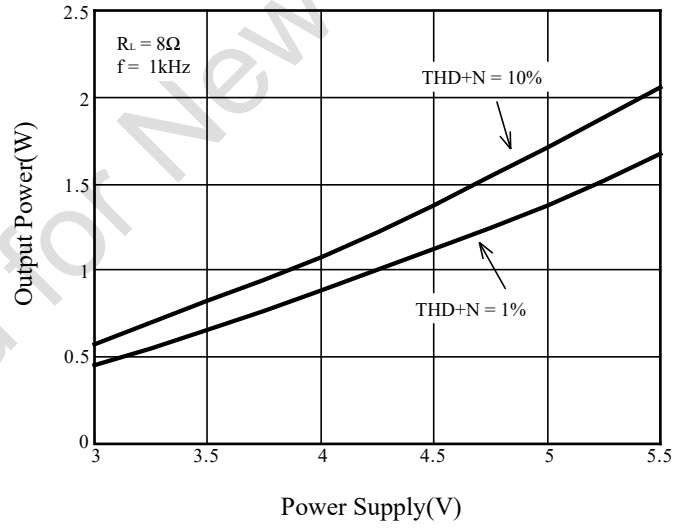


Figure 11 Output Power vs. Power Supply

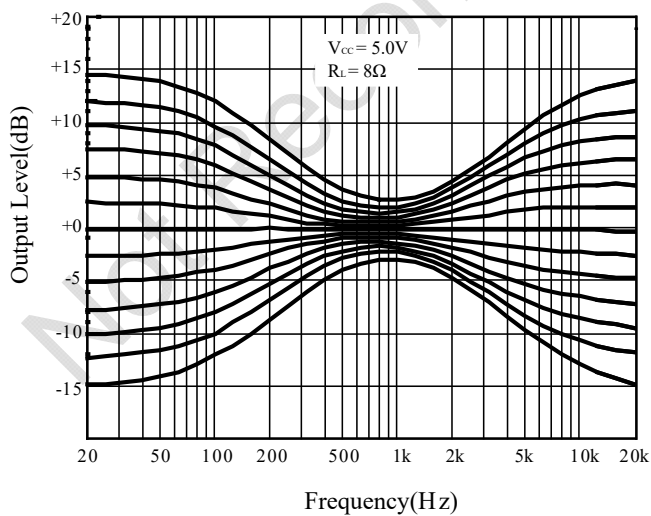
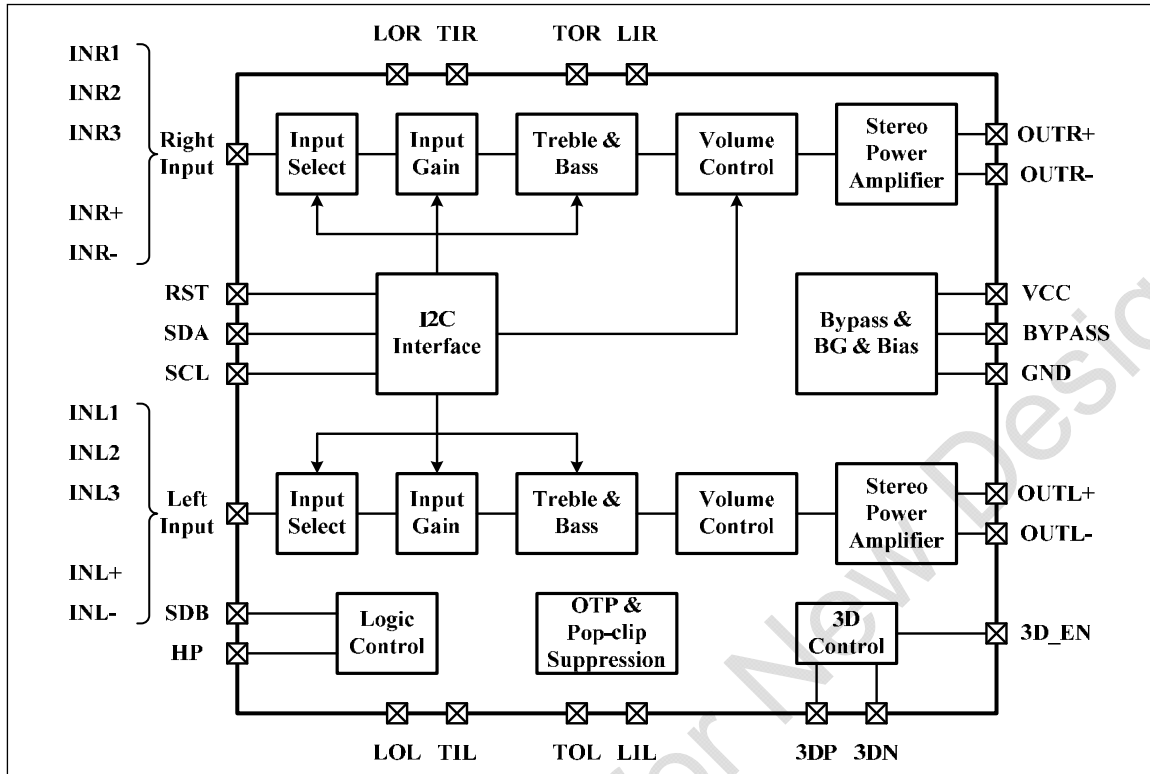


Figure 12 Bass and Treble Response vs. Frequency

IS31AP4833

FUNCTIONAL BLOCK DIAGRAM



IS31AP4833

DETAILED DESCRIPTION

I2C INTERFACE

The IS31AP4833 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31AP4833's slave address is "1000 0000". It only supports write operations.

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the IS31AP4833.

The timing diagram for the I2C is shown in Figure 13. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31AP4833's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31AP4833 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31AP4833, the register address byte is sent, most significant bit first. IS31AP4833 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31AP4833 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

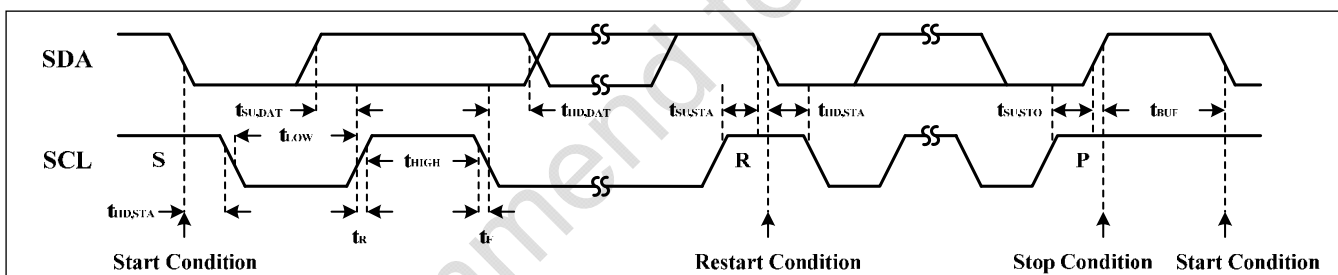


Figure 13 Interface timing

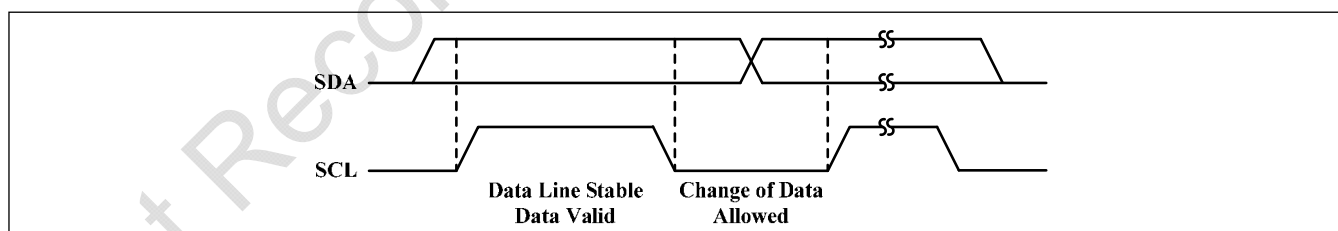


Figure 14 Bit transfer

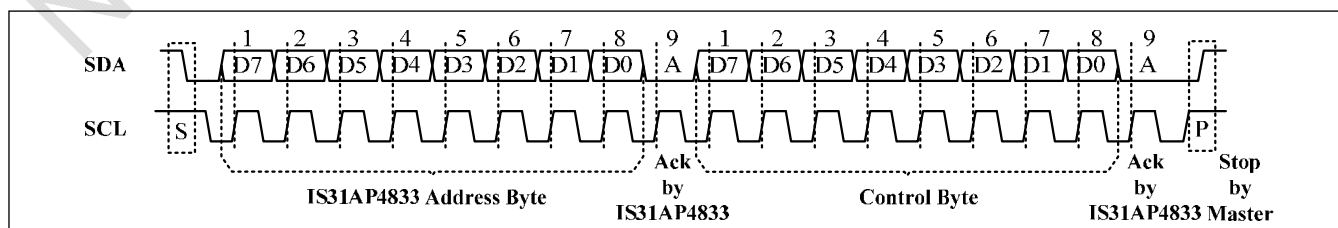


Figure 15 Writing to IS31AP4833

IS31AP4833

REGISTER DESCRIPTION

Table 1 Byte Function

| Address Bit D7:D5 | Data Bit | | | | | Function | Table | Default |
|----------------------|----------|-----|-----|-----|-----|----------------------------|-------|-----------|
| | D4 | D3 | D2 | D1 | D0 | | | |
| 000 | - | | IGS | | | Audio input gain control | 2 | 0000 0110 |
| 001 | - | BGS | | | | Bass control | 3 | 0010 0110 |
| 010 | - | TGS | | | | Treble control | 4 | 0100 0110 |
| 011 | LVS | | | | | Left channel gain control | 5 | 0111 0000 |
| 100 | RVS | | | | | Right channel gain control | 6 | 1001 0000 |
| 101 | - | | | IMS | | Audio input MUX control | 7 | 1010 0000 |
| 111 | ME | - | 3DE | SE | SSD | Operating mode control | 8 | 1110 0000 |

Table 2 Audio Input Gain Control Byte

| Bit | Address Bit | Data Bit | |
|---------|-------------|----------|-------|
| | D7:D5 | D4:D3 | D2:D0 |
| Name | 000 | - | IGS |
| Default | 000 | 00 | 110 |

Configure the input gain.

| IGS | Input Gain Select | Input Resistor |
|------------|-------------------|----------------|
| 000 | -15dB | 85kΩ |
| 001 | -12dB | 80kΩ |
| 010 | -9dB | 74kΩ |
| 011 | -6dB | 67kΩ |
| 100 | -3dB | 59kΩ |
| 101 | +0dB | 50kΩ |
| 110 | +3dB | 41kΩ |
| 111 | +6dB | 33kΩ |

Table 3 Bass Control Byte

| Bit | Address Bit | Data Bit | |
|---------|-------------|----------|-------|
| | D7:D5 | D4 | D3:D0 |
| Name | 001 | - | BGS |
| Default | 001 | 0 | 0110 |

Configure the bass gain.

| BGS | Bass Gain Select |
|------------|------------------|
| 0000 | -12dB |
| 0001 | -10dB |
| 0010 | -8dB |
| 0011 | -6dB |
| 0100 | -4dB |
| 0101 | -2dB |
| 0110 | 0dB |
| 0111 | +2dB |
| 1000 | +4dB |
| 1001 | +6dB |
| 1010 | +8dB |
| 1011 | +10dB |
| 1100 | +12dB |
| Others | Not available |

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Table 4 Treble Control Byte

| Bit | Address Bit | | Data Bit | |
|---------|-------------|--|----------|-------|
| | D7:D5 | | D4 | D3:D0 |
| Name | 010 | | - | TGS |
| Default | 010 | | 0 | 0110 |

Configure the treble gain.

| TGS | Treble Gain Select |
|------------|--------------------|
| 0000 | -12dB |
| 0001 | -10dB |
| 0010 | -8dB |
| 0011 | -6dB |
| 0100 | -4dB |
| 0101 | -2dB |
| 0110 | 0dB |
| 0111 | +2dB |
| 1000 | +4dB |
| 1001 | +6dB |
| 1010 | +8dB |
| 1011 | +10dB |
| 1100 | +12dB |
| Others | Not available |

Table 5 Left Channel Gain Control Byte

| Bit | Address Bit | | Data Bit | |
|---------|-------------|--|----------|--|
| | D7:D5 | | D4:D0 | |
| Name | 011 | | LVS | |
| Default | 011 | | 10000 | |

Configure the left channel gain (see Table 9).

| LVS | Left Volume Select |
|------------|--------------------|
| 00000 | Mute |
| 00001 | -42dB |
| 00010 | -40dB |
| 00011 | -38dB |
| | |
| 10000 | -12dB |
| | |
| 10110 | +0dB |
| 10111 | +2dB |
| | |
| 111xx | +12dB |

Table 6 Right Channel Gain Control Byte

| Bit | Address Bit | | Data Bit | |
|---------|-------------|--|----------|--|
| | D7:D5 | | D4:D0 | |
| Name | 100 | | RVS | |
| Default | 100 | | 10000 | |

Configure the right channel gain (see Table 9).

| RVS | Right Volume Select |
|------------|---------------------|
| 00000 | Mute |
| 00001 | -42dB |
| 00010 | -40dB |
| 00011 | -38dB |
| | |
| 10000 | -12dB |
| | |
| 10110 | +0dB |
| 10111 | +2dB |
| | |
| 111xx | +12dB |

Table 7 Audio Input MUX Control Byte

| Bit | Address Bit | | Data Bit | |
|---------|-------------|--|----------|-------|
| | D7:D5 | | D4:D2 | D1:D0 |
| Name | 101 | | - | IMS |
| Default | 101 | | 000 | 00 |

Single-ended or differential input selected.

| IMS | Input MUX Select |
|------------|----------------------|
| 00 | Single-ended Input 1 |
| 01 | Single-ended Input 2 |
| 10 | Single-ended Input 3 |
| 11 | Differential Input |

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Table 8 Operating Mode Control Byte

| Bit | Address Bit | Data Bit | | | | |
|---------|-------------|----------|----|-----|----|-----|
| | D7:D5 | D4 | D3 | D2 | D1 | D0 |
| Name | 111 | ME | - | 3DE | SE | SSD |
| Default | 111 | 0 | 0 | 0 | 0 | 0 |

Configure the operating mode for IS31AP4833.

SSD Shutdown Enable
 0 Operating Mode
 1 Shutdown Mode

SE Speaker Enable
 0 Speaker Enable
 1 Speaker Disable

3DE 3D Enable
 0 3D Off
 1 3D On

ME Mute Enable
 0 Mute Disable
 1 Mute Enable

Table 9 Left/Right Channel Gain Control

| Data | Gain | Data | Gain |
|-------|------|-------|------|
| 00000 | Mute | 01111 | -14 |
| 00001 | -42 | 10000 | -12 |
| 00010 | -40 | 10001 | -10 |
| 00011 | -38 | 10010 | -8 |
| 00100 | -36 | 10011 | -6 |
| 00101 | -34 | 10100 | -4 |
| 00110 | -32 | 10101 | -2 |
| 00111 | -30 | 10110 | +0 |
| 01000 | -28 | 10111 | +2 |
| 01001 | -26 | 11000 | +4 |
| 01010 | -24 | 11001 | +6 |
| 01011 | -22 | 11010 | +8 |
| 01100 | -20 | 11011 | +10 |
| 01101 | -18 | 111xx | +12 |
| 01110 | -16 | | |

IS31AP4833

APPLICATION INFORMATION

3D ENHANCEMENT

The IS31AP4833 has a 3D audio enhancement effect that helps improve the apparent stereo channel separation when, because of cabinet or equipment limitations, the left and right speakers are closer to each other than optimal.

Decreasing the resistor size will make the 3D effect more pronounced and decreasing the capacitor size will raise the cutoff frequency for the effect. A 68nF capacitor is used to reduce the effect at frequencies below 1kHz. Increasing the value of the capacitor will decrease the low cutoff frequency at which the stereo enhanced effect starts to occur as shown below

$$f_{3D} = \frac{1}{2\pi R_{3D} C_{3D}} \quad (1)$$

For example, according to the Figure 1,

$R_{3D} = 2.7k\Omega$, $C_{3D} = 68nF$

$$\text{So, } f_{3D} = \frac{1}{2\pi \times 2.7k\Omega \times 68nF} \approx 867 \text{ Hz}$$

The 3D enhancement effect enabled by setting the 3DE bit of the control byte "111x xxxx". When setting the 3DE bit to "1", 3D enhancement enabled. When setting the 3DE bit to "0", 3D enhancement disabled. Pulling the 3D_EN pin to high will enable the 3D enhancement either.

Set the 3DE bit to "1" or pull the 3D_EN pin to high will enable the 3D enhancement. Shutdown the 3D enhancement should set the 3DE bit to "0" and pull the 3D_EN pin to low.

tone CONTROL RESPONSE

Bass and treble tone controls are included in the IS31AP4833. The tone controls use two external capacitors for each stereo channel (C_{1L} , C_{2L} , C_{1R} , C_{2R}). Each has a corner frequency determined by the value of C_1 , C_2 and internal resistors in the feedback loop of the internal tone amplifier.

With $C = C_1 = C_2$, the treble turn-over frequency is nominally

$$f_{TT} = \frac{1}{2\pi \times 56k\Omega \times C} \quad (2)$$

and the bass turn-over frequency is nominally

$$f_{BT} = \frac{1}{2\pi \times 113.3k\Omega \times C} \quad (3)$$

For example, according to the Figure 1,

$C_1 = C_2 = 2.2nF$

$$\text{So, } f_{TT} = \frac{1}{2\pi \times 56k\Omega \times 2.2nF} \approx 1.3kHz$$

$$f_{BT} = \frac{1}{2\pi \times 113.3k\Omega \times 2.2nF} \approx 639 \text{ Hz}$$

The bass and treble gain can be adjusted independently by the control byte "010x xxxx" and "001x xxxx" (Table 3, 4).

GAIN SELECTION

The left/right channel gain can be adjusted by the LVS bit of the control byte "011x xxxx" and the RVS bit of the control byte "100x xxxx" (Table 5, 6).

In the speaker mode the output gain is equaled to audio input gain(IGS)+left/right channel gain(LVS/RVS)+6dB.

In the headphone mode the output gain is equaled to audio input gain(IGS)+left/right channel gain(LVS/RVS).

INPUT CAPACITORS (C_{IN})

The input capacitors (C_{IN}) and internal resistor (R_{IN}) form a high-pass filter with the corner frequency, f_c , determined in Equation (4).

$$f_c = \frac{1}{2\pi R_{IN} C_{IN}} \quad (4)$$

The value of R_{IN} is following the audio input gain (see Table 2).

For example, in figure 1,

$C_{IN} = 220nF$, the audio input gain is set to -3dB, so the $R_{IN} = 59k\Omega$,

$$\text{then, } f_c = \frac{1}{2\pi \times 59k\Omega \times 220nF} \approx 12 \text{ Hz}$$

The capacitors should have a tolerance of $\pm 10\%$ or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

MUTE FUNCTION

By setting the LVS/RVS bit to "00000" the left/right channel output will be mute independently (see Table 5, 6). The ME bit of the control byte "111x xxxx" sets the mute function for left and right channels. When the ME bit is set to "1", the left and right channels are both mute (see Table 8). When the ME bit is set to "0", the left and right channels will resume the volume before.

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INPUT SIGNAL SELECTION

IS31AP4833 can choose single-ended or differential signal for the input source. Single-ended input 1, single-ended input 2, single-ended input 3 and differential input signal can be chosen by the IMS bit of control byte "101x xxxx"(see Table 7).

HEADPHONE MODE

IS31AP4833 can also be used to drive headphone. The IC will shut off the positive output if headphone plug-in has been detected. Then the speaker will stop working and switch to the headphone mode.

SHUTDOWN MODE

Shutdown mode can either be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

SOFTWARE SHUTDOWN

By setting SSD bit of the control byte "111x xxxx" to "1", the IS31AP4833 will operate in software shutdown mode, wherein they consume only 1 μ A (Typ.) current.

HARDWARE SHUTDOWN

The chip enters hardware shutdown mode when the SDB pin is pulled low, wherein they consume only 1 μ A (Typ.) current.

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CLASSIFICATION REFLOW PROFILES

| Profile Feature | Pb-Free Assembly |
|---|----------------------------------|
| Preheat & Soak Temperature min (T _{smin}) Temperature max (T _{smax}) Time (T _{smin} to T _{smax}) (t _s) | 150°C 200°C 60-120 seconds |
| Average ramp-up rate (T _{smax} to T _p) | 3°C/second max. |
| Liquidous temperature (T _L) Time at liquidous (t _L) | 217°C 60-150 seconds |
| Peak package body temperature (T _p)* | Max 260°C |
| Time (t _p)** within 5°C of the specified classification temperature (T _c) | Max 30 seconds |
| Average ramp-down rate (T _p to T _{smax}) | 6°C/second max. |
| Time 25°C to peak temperature | 8 minutes max. |

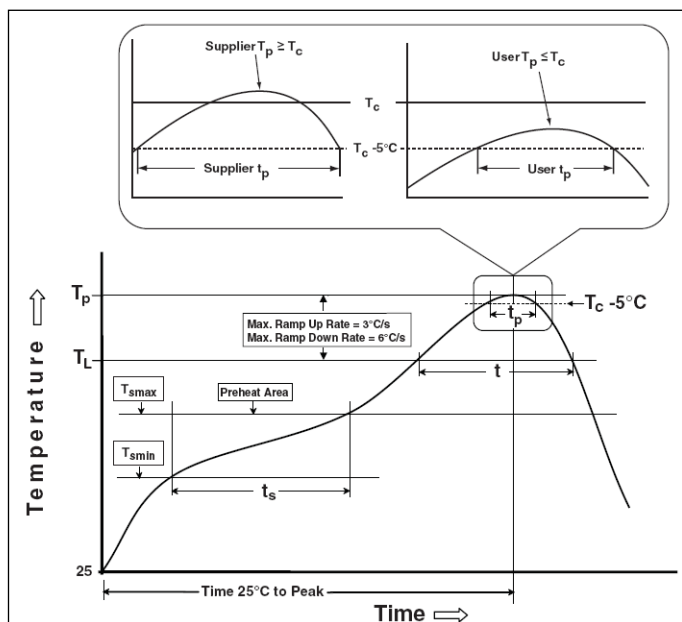
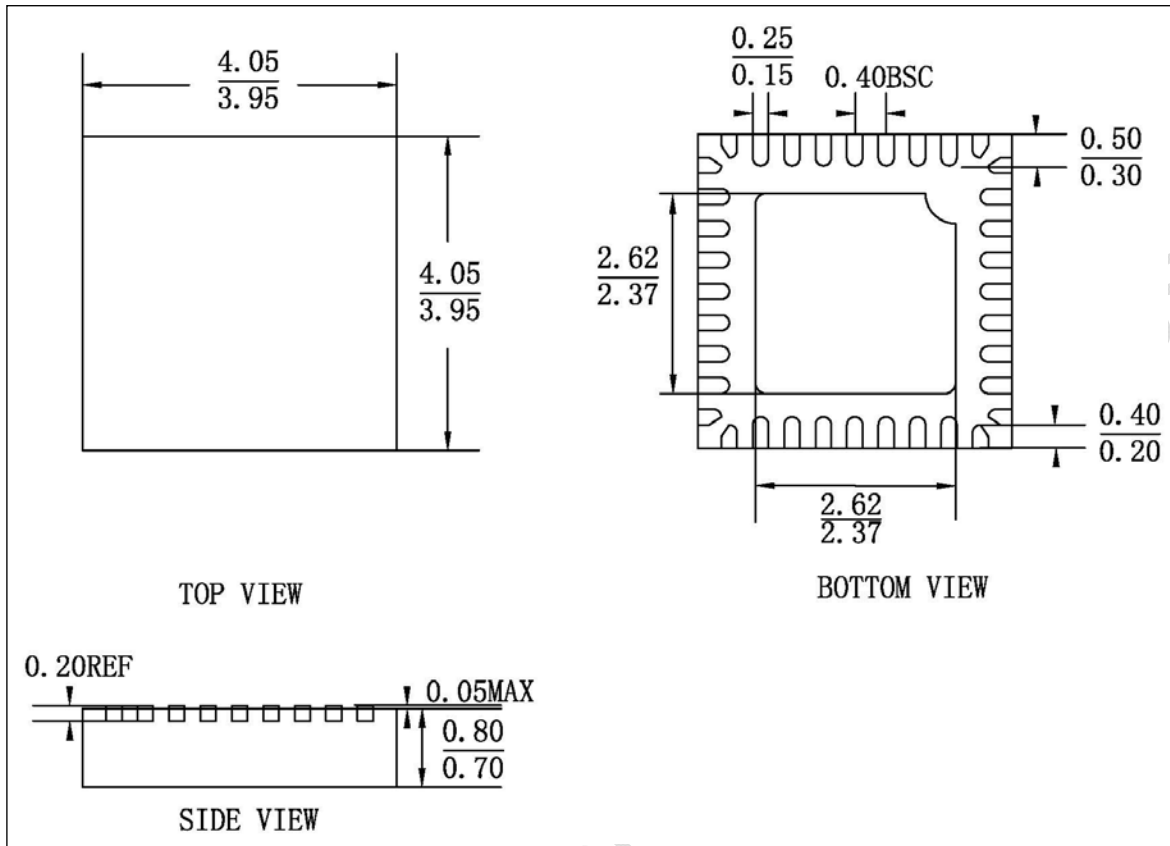


Figure 16 Classification Profile

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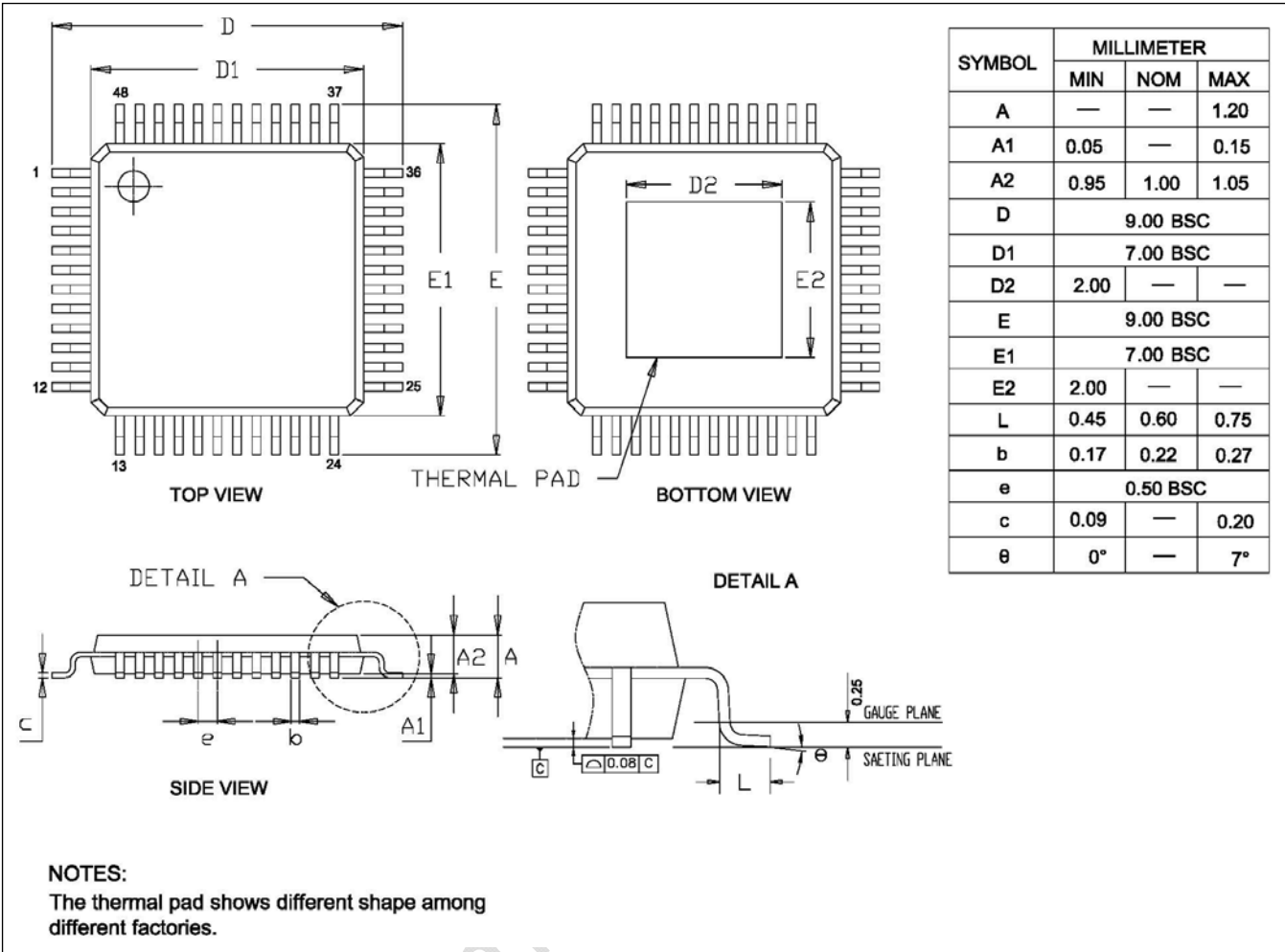
PACKAGING INFORMATION

QFN-36



IS31AP4833

TQFP-48



Note: All dimensions in millimeters unless otherwise stated.

REVISION HISTORY

| Revision | Detail Information | Date |
|----------|---------------------------------|------------|
| A | Initial release | 2012.07.31 |
| B | 1.Update POD 2.Add ESD value | 2014.03.13 |
| C | Add NRND watermark | 2021.09.07 |

Not Recommend for New Design