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Evaluating the ADP2125 Low Profile, 6 MHz, Step-Down Converter

FEATURES

500 mA, 6 MHz, synchronous, step-down dc-to-dc converter
Low profile, tiny footprint ceramic inductor and capacitors
Evaluation board assembled with 0.55 mm (maximum) height external components
Input voltage range: 2.1 V to 5.5 V
1.26 V fixed output voltage
Clock signal enable

TYPICAL APPLICATION CIRCUIT

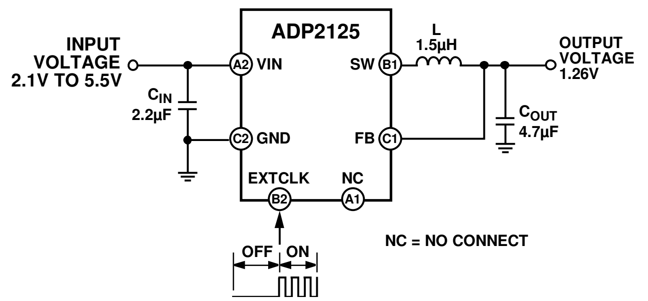

Figure 1.

GENERAL DESCRIPTION

The ADP2125 evaluation board is a complete 6 MHz (maximum), low quiescent current, synchronous buck dc-to-dc converter capable of producing up to 500 mA of output current at a fixed 1.26 V output voltage. The converter operates with an input voltage in the 2.1 V to 5.5 V range. The device uses a voltage regulating pulse-width modulation (PWM) that maintains a constant frequency with excellent stability and transient response. The evaluation board demonstrates the operation and performance of the ADP2125 as well as its compatibility with tiny ceramic components for a small area solution.

This user guide includes I/O descriptions, setup instructions, the evaluation board schematic, and the printed circuit board (PCB) layout drawings for the ADP2125 low profile step-down switching converter evaluation board.

Complete specifications for the ADP2125 are available in the ADP2125 data sheet available from Analog Devices, Inc., and should be consulted in conjunction with this user guide when using the evaluation board.

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REVISION HISTORY

12/10—Rev. 0: Rev. A

Change to Quantity column of Table 1 ... 5

10/10—Revision 0: Initial Version

EVALUATION BOARD OVERVIEW

The ADP2125 evaluation board is fully assembled and tested. The following sections describe the various connectors on the board, the proper evaluation setup, and the testing capabilities of the evaluation board.

INPUT/OUTPUT CONNECTORS

EXTCLK Test Point

This test point is used to enable or disable the converter. Connect the EXTCLK pin to GND to disable the converter. Apply a 6 MHz to 27 MHz clock signal to the EXTCLK pin to enable the converter. See the specifications table in the ADP2125 data sheet for the high and low threshold voltage levels. Do not leave this pin floating.

VOUT Test Bus

The VOUT test bus provides access to the regulated output voltage and the FB (feedback) pin of the part. A load of up to 500 mA can be applied to this bus.

VIN Test Bus

The VIN test bus connects the positive input supply voltage to the VIN pin. Connect the power supply to this bus and keep the wires as short as possible to minimize the EMI transmission.

GND Test Bus

The GND test bus is the ground connection for the part and the external components via the GND pin. Attach ground connections from external equipment to this bus.

SW Test Point

The SW test point allows access to switch node (SW pin) of the ADP2125 to monitor the switching behavior. An LC filter is connected to this pin on the board. Connect a BNC cable to measure the switching frequency to this test point.

EVALUATION SETUP

Follow these setup instructions to ensure proper operation of the ADP2125 evaluation board:

1. Connect the positive input supply to VIN.
2. Connect the input supply ground to GND.
3. Connect the desired load between VOUT and PGND. The ADP2125 can supply up to 500 mA.
4. Connect the EXTCLK pin to GND to disable the converter, or apply a 6 MHz to 27 MHz clock signal to the EXTCLK pin to enable the converter.
5. Apply a VIN between 2.1 V and 5.5 V (6.0 V absolute maximum.)

PERFORMANCE EVALUATION

The resulting oscilloscope waveforms and typical performance characteristics for the following tests are provided in the ADP2125 data sheet.

Output Accuracy

The output accuracy is verified by monitoring the output voltage at VOUT while testing both the line and load regulation.

Line Regulation

The line regulation is observed and measured by monitoring the output voltage at VOUT while varying the input voltage applied to VIN.

Load Regulation

The load regulation is observed and measured by monitoring the output voltage at VOUT while sweeping the applied load between VOUT and GND. To minimize voltage drop, use short low resistance wires, especially for heavy loads.

Efficiency

The efficiency, η, is calculated by comparing the input power to the output power.

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}$$

Output Ripple Voltage

The output voltage ripple is visible by placing an oscilloscope across the output capacitor (COUT). Set the oscilloscope to ac coupling or apply a dc offset for proper resolution.

Line Transient

Generate a high speed transient in the voltage applied to VIN and observe the behavior of the evaluation board at the SW test point and the VOUT test bus. To see the most accurate load transient waveform, place a probe directly on the output capacitor terminal with a short path to ground to limit noise and stray inductance.

Load Transient

Generate a fast transient in the current applied to VOUT and observe the behavior of the evaluation board at the SW test point and the VOUT test bus. To see the most accurate load transient waveform, place a probe directly on the output capacitor terminal with a short path to ground to limit noise and stray inductance.

Oscillator Frequency

The oscillator frequency is measured by connecting an oscilloscope to the SW test point.

Inductor Current

The inductor current is made accessible by removing one side of the inductor from its pad and connecting a current loop in series. Place an oscilloscope current probe on the loop to view the current waveform.

EVALUATION BOARD SCHEMATIC AND LAYOUT

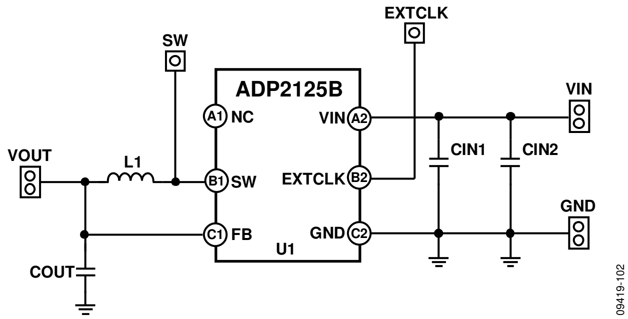

Figure 2. ADP2125 Evaluation Board Schematic

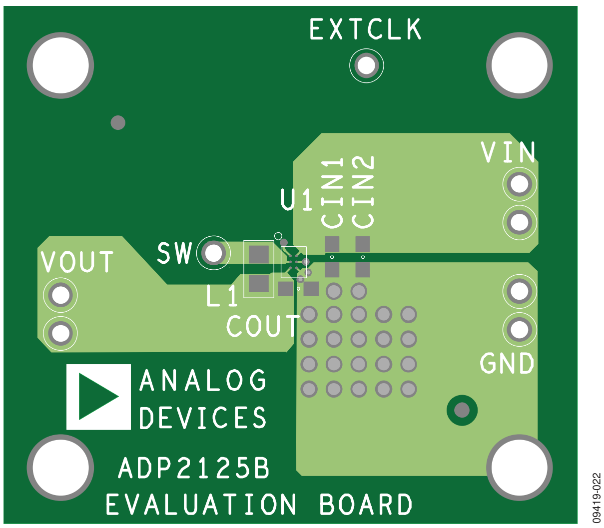

Figure 3. ADP2125 Top Layer

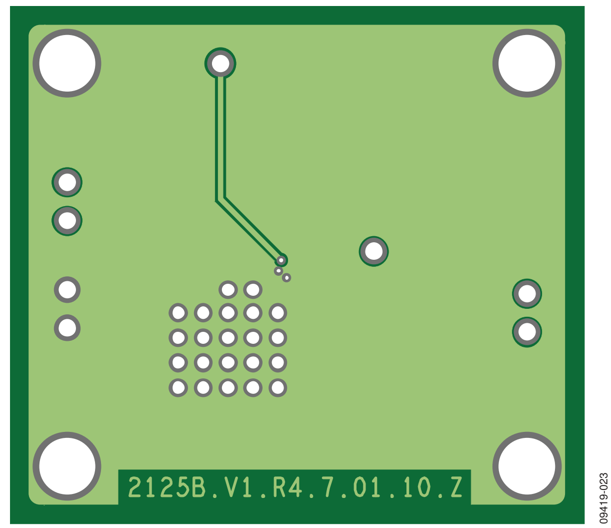

Figure 4. ADP2125 Bottom Layer

LAYOUT GUIDELINES

For high efficiency, good regulation, and stability with the ADP2125, a well-designed and manufactured PCB is essential. Use the following guidelines when designing PCBs:

- Keep the low ESR input capacitor, CIN, close to VIN and GND.
- Keep high current traces as short and as wide as possible.
- Avoid routing high impedance traces near any node connected to SW or near the inductor to prevent radiated noise injection.
- Keep the low ESR output capacitor, COUT, close to the FB and GND pins of the ADP2125. Long trace lengths from the part to the output capacitor add series inductance and may cause instability or increased ripple.

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Quantity	Reference Designator	Description	Manufacturer	Part Number
1	U1	ADP2125 low profile, 500 mA, 6 MHz, synchronous, step-down, dc-to-dc converter	Analog Devices, Inc.	ADP2125BCDZ-1.26R7
1	CIN1	Input capacitor, MLCC, 2.2 µF, 6.3 V, 0402, X5R	Murata Manufacturing Co., Ltd.	GRM155R60J225ME95D
	CIN2	Input capacitor	Open	
1	COUT	Output capacitor, MLCC, 4.7 µF, 6.3V, 0402, X5R	Murata Manufacturing Co., Ltd.	GRM155R60J475ME87D
1	L1	Inductor, 1.8 µH, 0.75 A, 0603	Murata Manufacturing Co., Ltd.	LQM18PN1R8NC0L
2	SW, EXTCLK	Headers, 0.100 in, single, straight, 1-pin	Sullins Connector Solutions	PBC01SAAN[1]
3	VOUT, VIN, GND	Headers, 0.100 in, single, straight, 2-pin	Sullins Connector Solutions	PBC02SAAN[1]

[1] Alternatively, PBC36SAAN can be purchased and cut as necessary.

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ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

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