September 1998

National Semiconductor

54AC299 • 54ACT299
8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

General Description

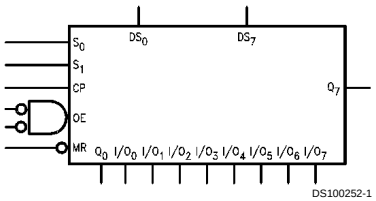
The 'AC/'ACT299 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0, Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

Features

- I_{CC} and I_{OZ} reduced by 50%
- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT299 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD)
  'AC299: 5962-88754
  'ACT299: 5962-88771

Ordering Code:

Logic Symbols



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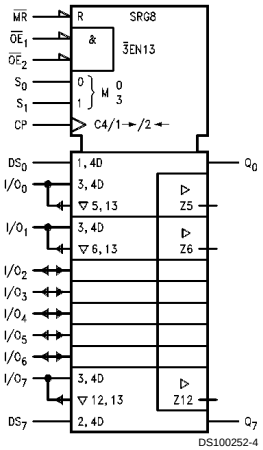
IEEE/IEC



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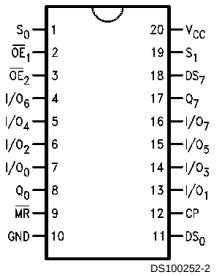
Connection Diagrams

Pin Assignment for DIP and Flatpak



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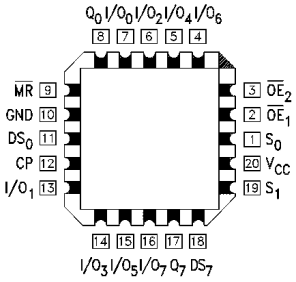
Pin Assignment for LCC



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FACT® is a registered trademark of Fairchild Semiconductor Corporation.

Connection Diagrams (Continued)

Pin Names	Description
CP	Clock Pulse Input
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I/O_0–I/O_7	Parallel Data Inputs or TRI-STATE Parallel Outputs
Q_0, Q_7	Serial Outputs

Functional Description

The 'AC/'ACT299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Truth Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

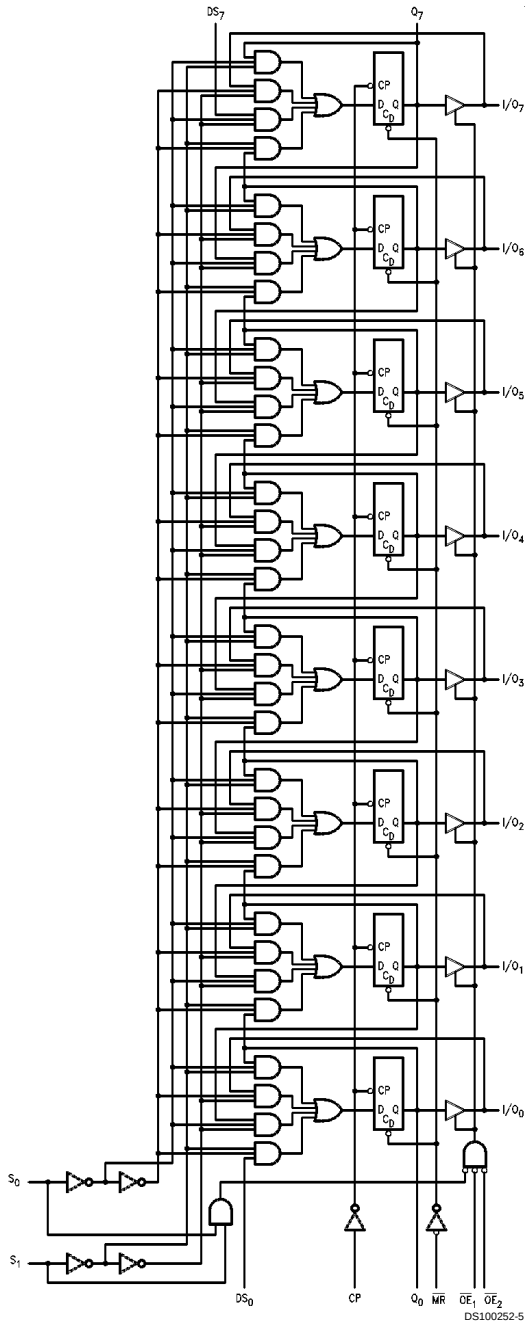
A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

Truth Table

Inputs				Response
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; Q_0–Q_7 = LOW
H	H	H	⌐	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⌐	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⌐	Shift Left, $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65˚C to +150˚C
Junction Temperature (T_J)	
CDIP	175˚C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
(Unless Otherwise Specified)	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.0V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54AC/ACT	−55˚C to +125˚C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Obviously the databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

DC Electrical Characteristics

For 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	54AC T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	3.15		
		5.5	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	1.35		
		5.5	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.9	V	I_{OUT} = −50 µA
		4.5	4.4		
		5.5	5.4		
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		3.0	2.4	V	I_{OH} = −12 mA
		4.5	3.7		I_{OH} = −24 mA
		5.5	4.7		I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.1	V	I_{OUT} = 50 µA
		4.5	0.1		
		5.5	0.1		
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		3.0	0.50	V	I_{OH} = 12 mA
		4.5	0.50		I_{OH} = 24 mA
		5.5	0.50		I_{OH} = 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V_I = V_{CC}, GND

Note 2: All outputs loaded; threshold on input associated with output under test.

DC Electrical Characteristics

For 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	54AC T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
	(Note 4)				
I_{OLD}	Minimum Dynamic	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current	5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	µA	$V_{IN} = V_{CC}$ or GND
I_{OZT}	Maximum I/O Leakage Current	5.5	±5.5	µA	V_I(OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND

Note 3: All outputs loaded; threshold on input associated with output under test.

Note 4: Maximum test duration 20 ms, one output loaded at a time.

Note 5: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Electrical Characteristics

For 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	54ACT T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0 4.5	0.8 0.8		V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level	4.5 5.5	4.4 5.4	V	I_{OUT} = −50 µA
					(Note 7) $V_{IN} = V_{IL}$ or V_{IH}
		4.5	3.70	V	I_{OH} = −24 mA
		5.5	4.70		I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.1 0.1	V	I_{OUT} = 50 µA
					(Note 7) $V_{IN} = V_{IL}$ or V_{IH}
		4.5	0.50	V	I_{OL}= 24 mA
		5.5	0.50		I_{OL}= 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	1.6	mA	$V_I = V_{CC}$ − 2.1V
	(Note 8)				
I_{OLD}	Minimum Dynamic	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current	5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	µA	$V_{IN} = V_{CC}$ or GND
I_{OZT}	Maximum I/O Leakage Current	5.5	±5.0	µA	V_I(OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND

DC Electrical Characteristics (Continued)

Note 6: I_{CC} limit for 54ACT @ 25˚C is identical to 74ACT @ 25˚C.

Note 7: All outputs loaded; thresholds on input associated with output under test.

Note 8: Maximum test duration 2.0 ms, one output loaded at a time.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	170	pF	V_{CC} = 5.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 9)	54AC T_A = −55˚C to +125˚C C_L = 50 pF		Units	Fig. No.
			Min	Max		
f_{max}	Maximum Input Frequency	3.3	70		MHz	
		5.0	80			
t_{PLH}	Propagation Delay CP to Q_0 or Q_7 (Shift Left or Right)	3.3	1.0	25.5	ns	
		5.0	1.0	17.5		
t_{PHL}	Propagation Delay CP to Q_0 or Q_7 (Shift Left or Right)	3.3	1.0	26.5	ns	
		5.0	1.0	18.0		
t_{PLH}	Propagation Delay $\overline{CP}$ to I/O_n	3.3	1.0	24.5	ns	
		5.0	1.0	17.0		
t_{PHL}	Propagation Delay $\overline{CP}$ to I/O_n	3.3	1.0	26.5	ns	
		5.0	1.0	18.5		
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7	3.3	1.0	27.0	ns	
		5.0	1.0	18.5		
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	3.3	1.0	26.5	ns	
		5.0	1.0	18.0		
t_{PZH}	Output Enable Time $\overline{OE}$ to I/O_n	3.3	1.0	22.0	ns	
		5.0	1.0	15.0		
t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n	3.3	1.0	23.5	ns	
		5.0	1.0	16.0		
t_{PHZ}	Output Disable Time $\overline{OE}$ to I/O_n	3.3	1.0	22.5	ns	
		5.0	1.0	17.0		
t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n	3.3	1.0	21.5	ns	
		5.0	1.0	16.0		

Note 9: Voltage Range 3.3 is 3.3V ±0.3V.

Voltage Range 5.0 is 5.0V ±0.5V.

AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 10)	54AC $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF Guaranteed Minimum	Units	Fig. No.
t_s	Setup Time, HIGH or LOW	3.3	9.5	ns	
	S_0 or S_1 to CP	5.0	7.0		
t_h	Hold Time, HIGH or LOW	3.3	2.0	ns	
	S_0 or S_1 to CP	5.0	2.5		
t_s	Setup Time, HIGH or LOW	3.3	6.0	ns	
	I/O_n to CP	5.0	4.0		
t_h	Hold Time, HIGH or LOW	3.3	1.5	ns	
	I/O_n to CP	5.0	2.0		
t_s	Setup Time, HIGH or LOW	3.3	7.5	ns	
	DS_0 or DS_7 to CP	5.0	5.0		
t_h	Hold Time, HIGH or LOW	3.3	1.5	ns	
	DS_0 or DS_7 to CP	5.0	1.5		
t_w	CP Pulse Width, LOW	3.3	5.5	ns	
		5.0	5.0		
t_w	$\overline{MR}$ Pulse Width, LOW	3.3	5.5	ns	
		5.0	5.0		
t_{rec}	Recovery Time	3.3	2.5	ns	
	$\overline{MR}$ to CP	5.0	2.5		

Note 10: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 11)	54ACT $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Max		
f_{max}	Maximum Input Frequency	5.0	70		MHz	
t_{PLH}	Propagation Delay CP to Q_0 or Q_7 (Shift Left or Right)	5.0	1.0	15.5	ns	
t_{PHL}	Propagation Delay CP to Q_0 or Q_7 (Shift Left or Right)	5.0	1.0	16.0	ns	
t_{PLH}	Propagation Delay CP to I/O_n	5.0	1.0	15.0	ns	
t_{PHL}	Propagation Delay CP to I/O_n	5.0	1.0	18.0	ns	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7	5.0	1.0	18.0	ns	
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	5.0	1.0	17.5	ns	

AC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V) (Note 11)	54ACT $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Max		
t_{PZH}	Output Enable Time $\overline{OE}$ to I/O_n	5.0	1.0	14.0	ns	
t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n	5.0	1.0	14.5	ns	
t_{PHZ}	Output Disable Time $\overline{OE}$ to I/O_n	5.0	1.0	14.5	ns	
t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n	5.0	1.0	14.0	ns	

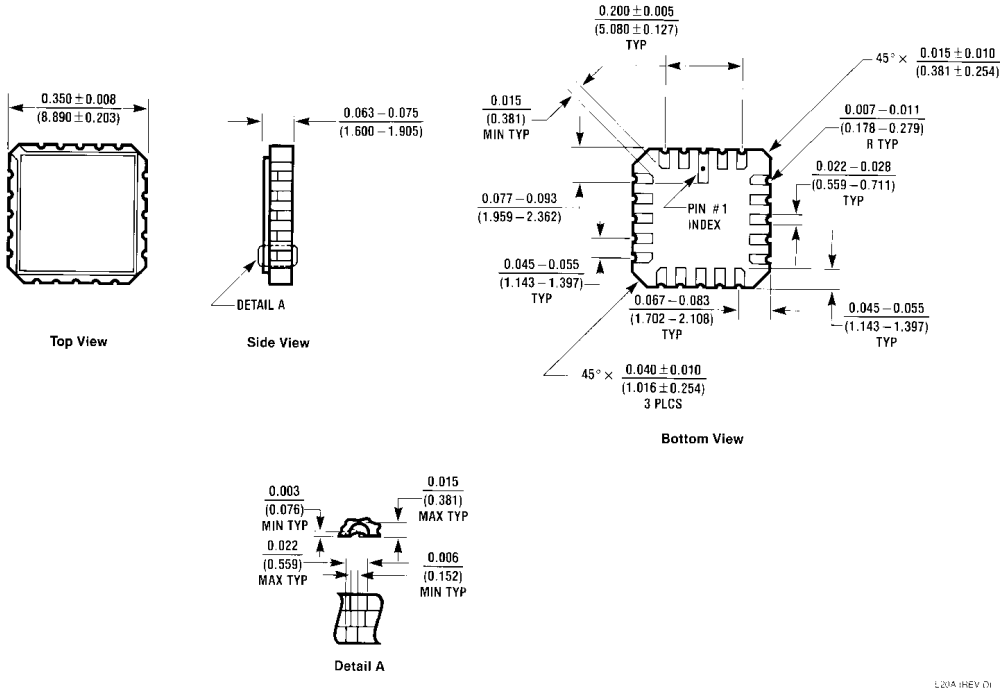
Note 11: Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

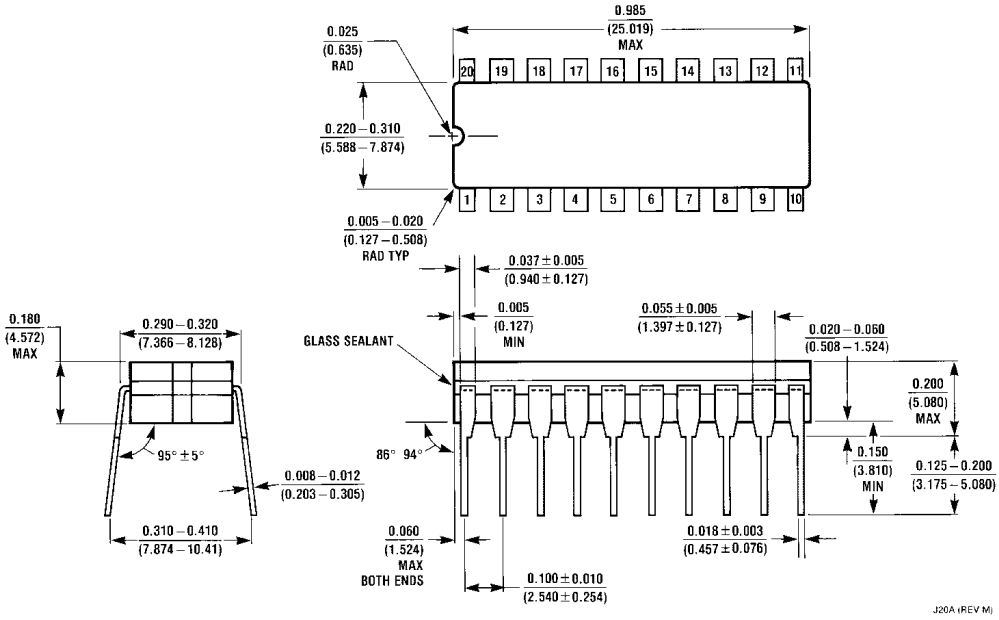
Symbol	Parameter	V_{CC} (V) (Note 12)	54ACT $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum		
t_s	Setup Time, HIGH or LOW S_0 or S_1 to CP	5.0	6.5	ns	
t_h	Hold Time, HIGH or LOW S_0 or S_1 to CP	5.0	1.5	ns	
t_s	Setup Time, HIGH or LOW I/O_n to CP	5.0	4.5	ns	
t_h	Hold Time, HIGH or LOW I/O_n to CP	5.0	1.5	ns	
t_s	Setup Time, HIGH or LOW DS_0 or DS_7 to CP	5.0	5.5	ns	
t_h	Hold Time, HIGH or LOW DS_0 or DS_7 to CP	5.0	1.5	ns	
t_w	CP Pulse Width HIGH or LOW	5.0	5.0	ns	
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	5.0	ns	
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	1.5	ns	

Note 12: Voltage Range 5.0 is 5.0V ±0.5V.

Physical Dimensions inches (millimeters) unless otherwise noted

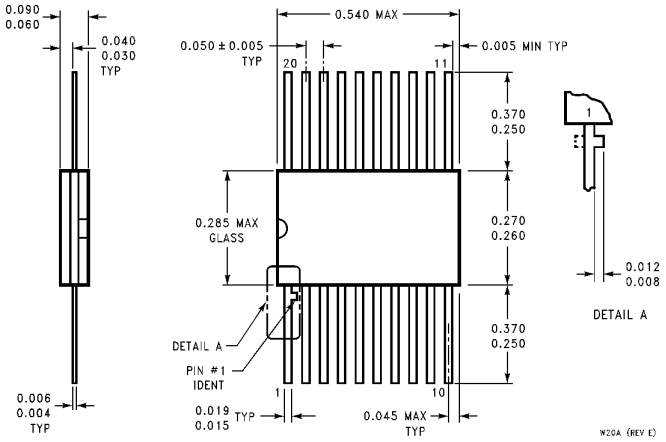


20 Terminal Ceramic Leadless Chip Carrier (LCC)
NS Package Number E20A



20 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20 Lead Ceramic FLATPAK
NS Package Number W20A

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