



## N-channel 60 V, 0.22 $\Omega$ typ., 38 A STripFET™ II Power MOSFET in a D<sup>2</sup>PAK package

Datasheet — production data

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STB45NF06T4	60 V	0.028 $\Omega$	38 A

- Typical R<sub>DS(on)</sub> = 0.022  $\Omega$
- Exceptional dv/dt capability
- 100% avalanche tested
- Standard threshold drive

### Applications

- Switching applications

### Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

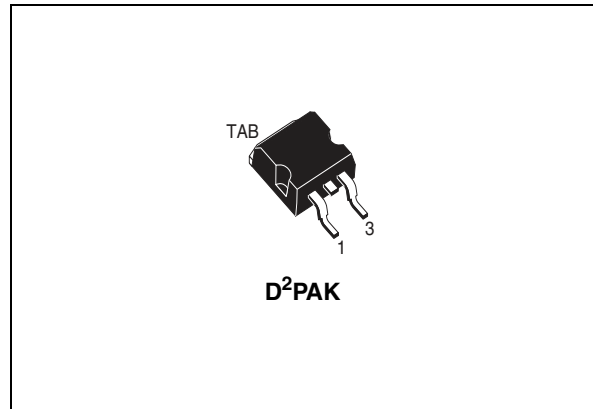


Figure 1. Internal schematic diagram

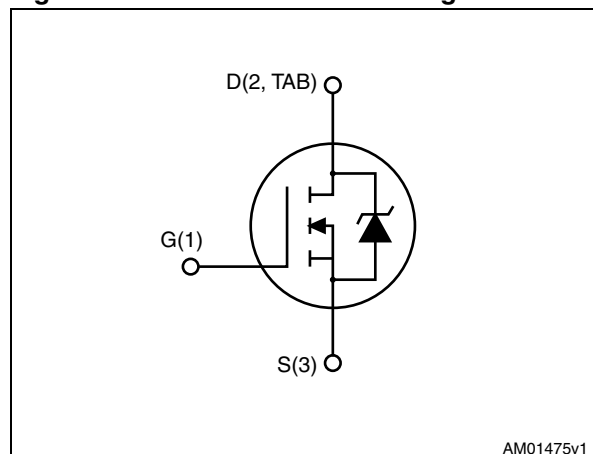


Table 1. Device summary

Order code	Marking	Package	Packaging
STB45NF06T4	B45NF06	D <sup>2</sup> PAK	Tape and reel

## Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	60	V
$V_{DGR}$	Drain-gate voltage ( $R_{GS}=20\text{ k}\Omega$ )	60	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	38	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	26	A
$I_{DM}^{(1)}$	Drain current (pulsed)	152	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	80	W
	Derating factor	0.53	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	7	V/ns
$T_{stg}$	Storage temperature	- 65 to 175	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	175	$^\circ\text{C}$

1. Pulse width limited by safe operating area

2.  $I_{SD} \leq 38\text{ A}$ ,  $di/dt \leq 300\text{ A}/\mu\text{s}$ ;  $V_{DS(\text{peak})} < V_{(BR)DSS}$ ,  $V_{DD}=80\% V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj\text{-case}}$	Thermal resistance junction-case max	1.88	$^\circ\text{C}/\text{W}$
$R_{thj\text{-amb}}^{(1)}$	Thermal resistance junction-ambient max	35	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{j\text{max}}$ )	38	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ ; $V_{DD}=50\text{ V}$ )	135	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified).

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ mA}$ , $V_{GS} = 0$	60			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 60\text{ V}$ $V_{DS} = 60\text{ V}$ , $T_C = 125\text{ °C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 19\text{ A}$		0.022	0.028	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(on)} * R_{DS(on)max}$ , $I_D = 19\text{ A}$		24		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	1730 215 63	-	pF pF pF
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 48\text{ V}$ , $I_D = 38\text{ A}$ , $V_{GS} = 10\text{ V}$	-	43 9 15	58	ns ns ns

1. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Voltage rise time	$V_{DD} = 30\text{ V}$ , $I_D = 19\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 14</a> )	-	20 100	-	ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time		-	50 20	-	ns ns
$t_{d(off)}$ $t_f$ $t_c$	Off-voltage rise time Fall time Cross-over time	$V_{clamp} = 48\text{ V}$ , $I_D = 38\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 16</a> )	-	45 42 60	-	ns ns ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		38	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		152	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 38 \text{ A}, V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 38 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	-	95		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$	-	260		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 16</a> )	-	5.5		A

1. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

2. Pulse width limited by safe operating area.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

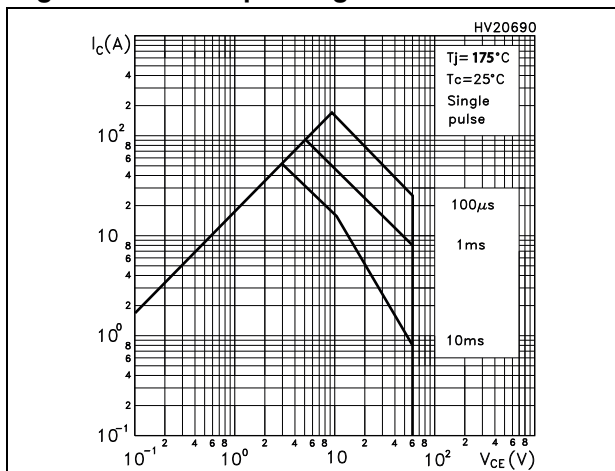


Figure 3. Thermal impedance

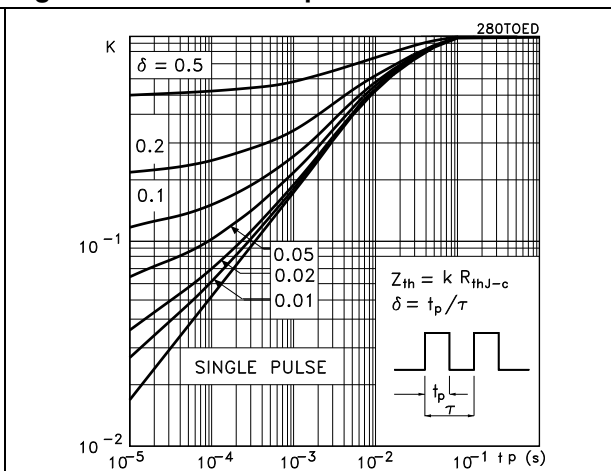


Figure 4. Output characteristics

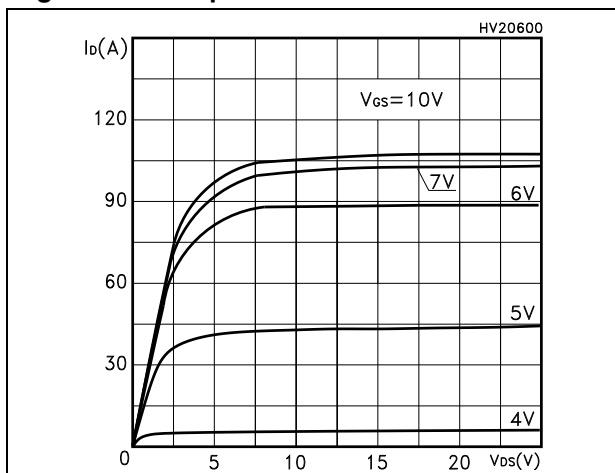


Figure 5. Transfer characteristics

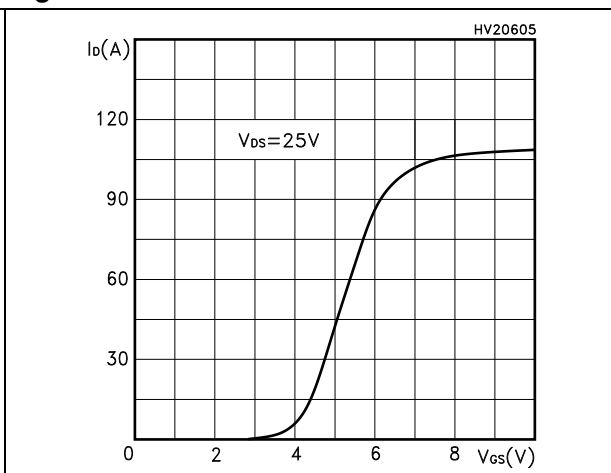


Figure 6. Transconductance

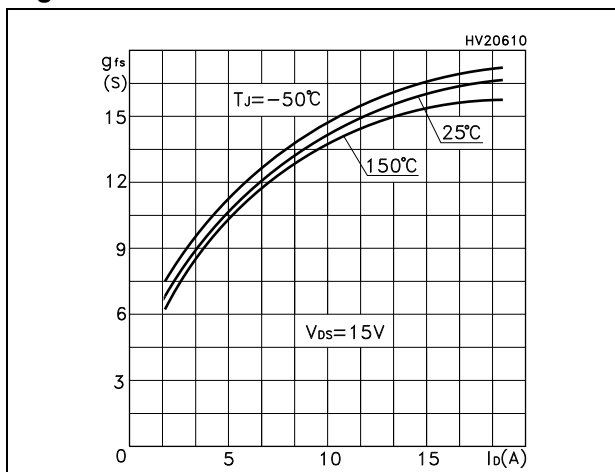


Figure 7. Static drain-source on-resistance

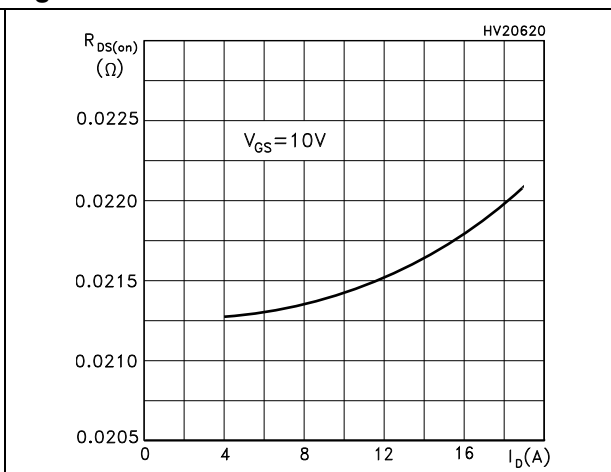


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

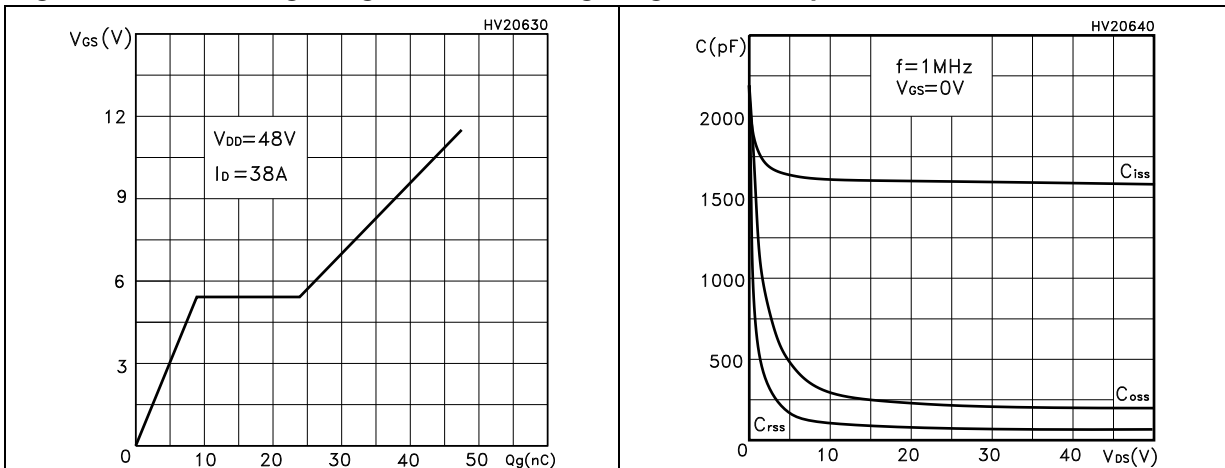


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on-resistance vs temperature

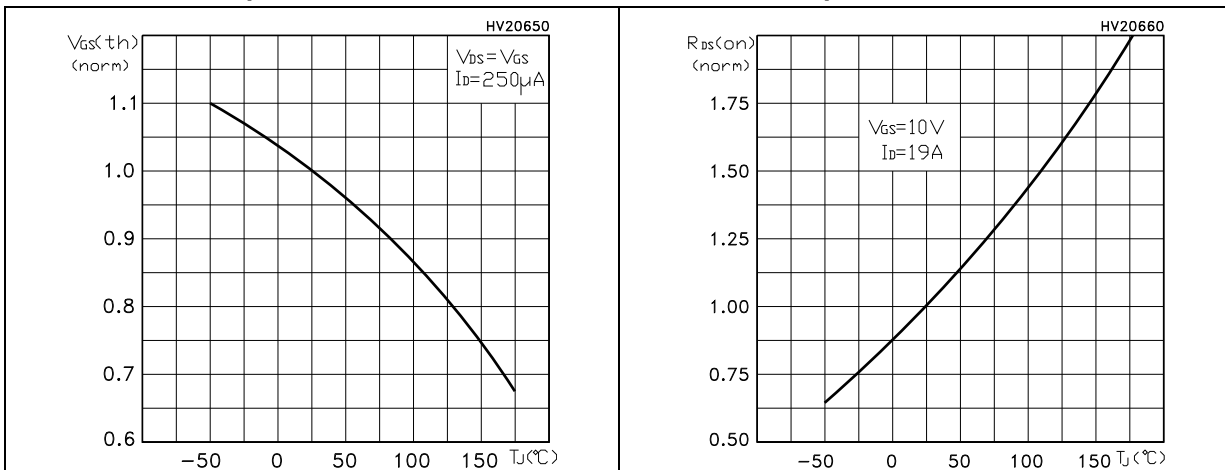
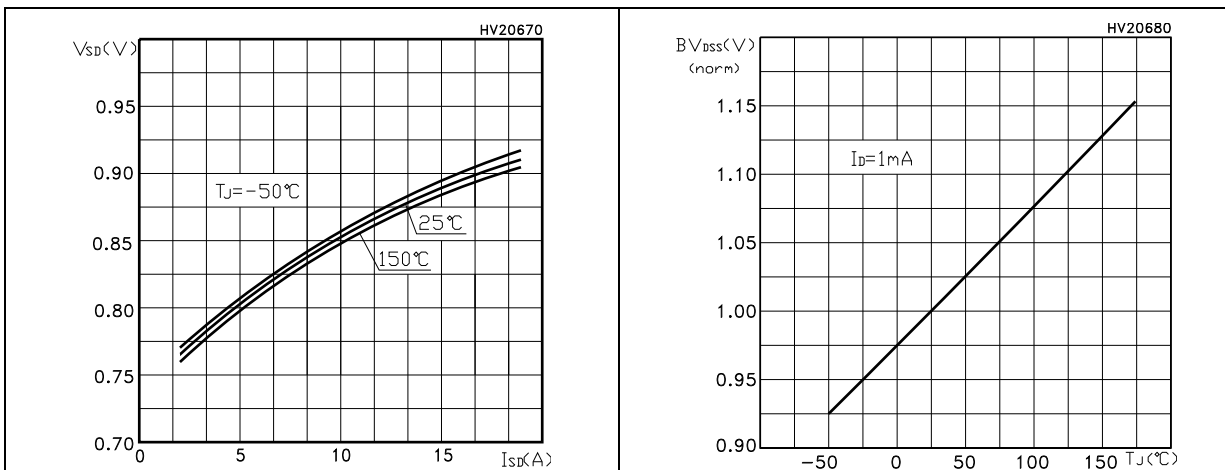
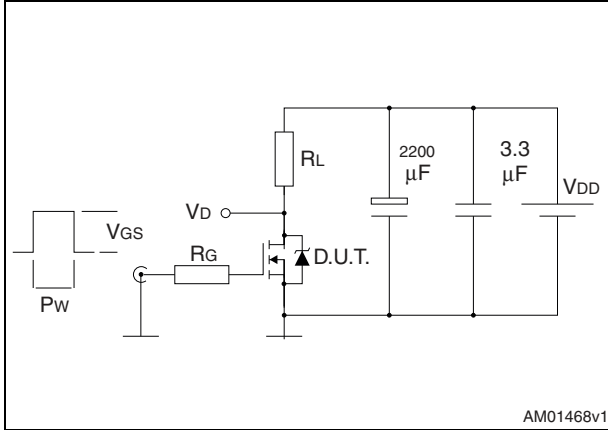


Figure 12. Source-drain diode forward characteristics Figure 13. Normalized  $B_{VDSS}$  vs temperature

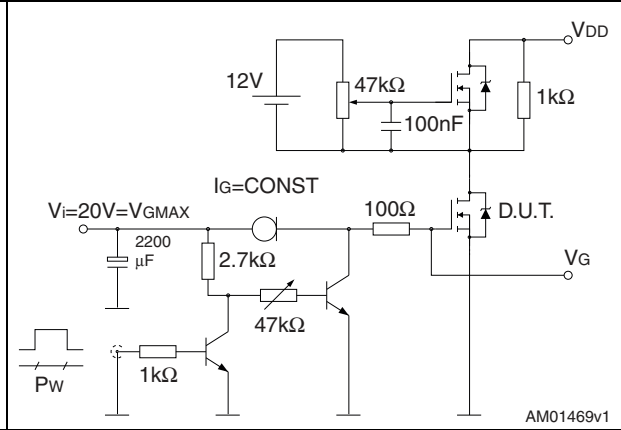


### 3 Test circuits

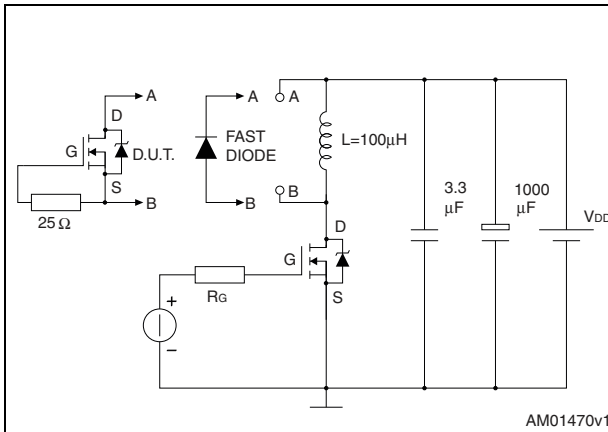
**Figure 14. Switching times test circuit for resistive load**



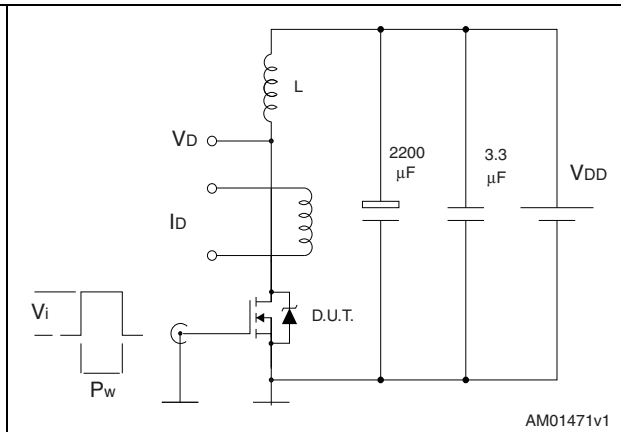
**Figure 15. Gate charge test circuit**



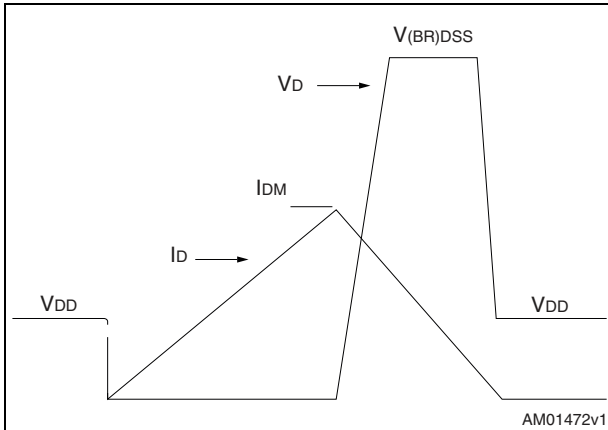
**Figure 16. Test circuit for inductive load switching and diode recovery times**



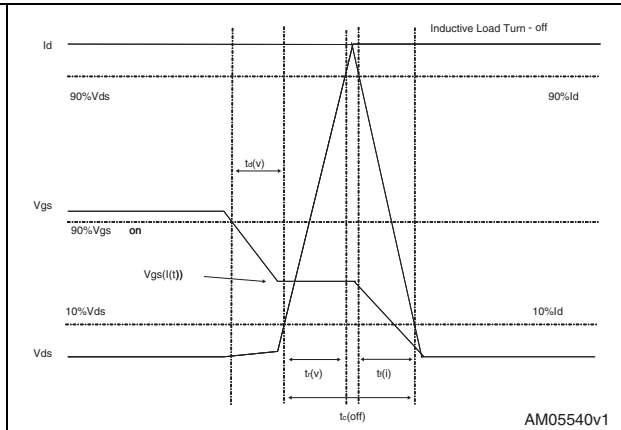
**Figure 17. Unclamped inductive load test circuit**



**Figure 18. Unclamped inductive waveform**



**Figure 19. Switching time waveform**





## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

Table 9. D<sup>2</sup>PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 20. D<sup>2</sup>PAK (TO-263) drawing

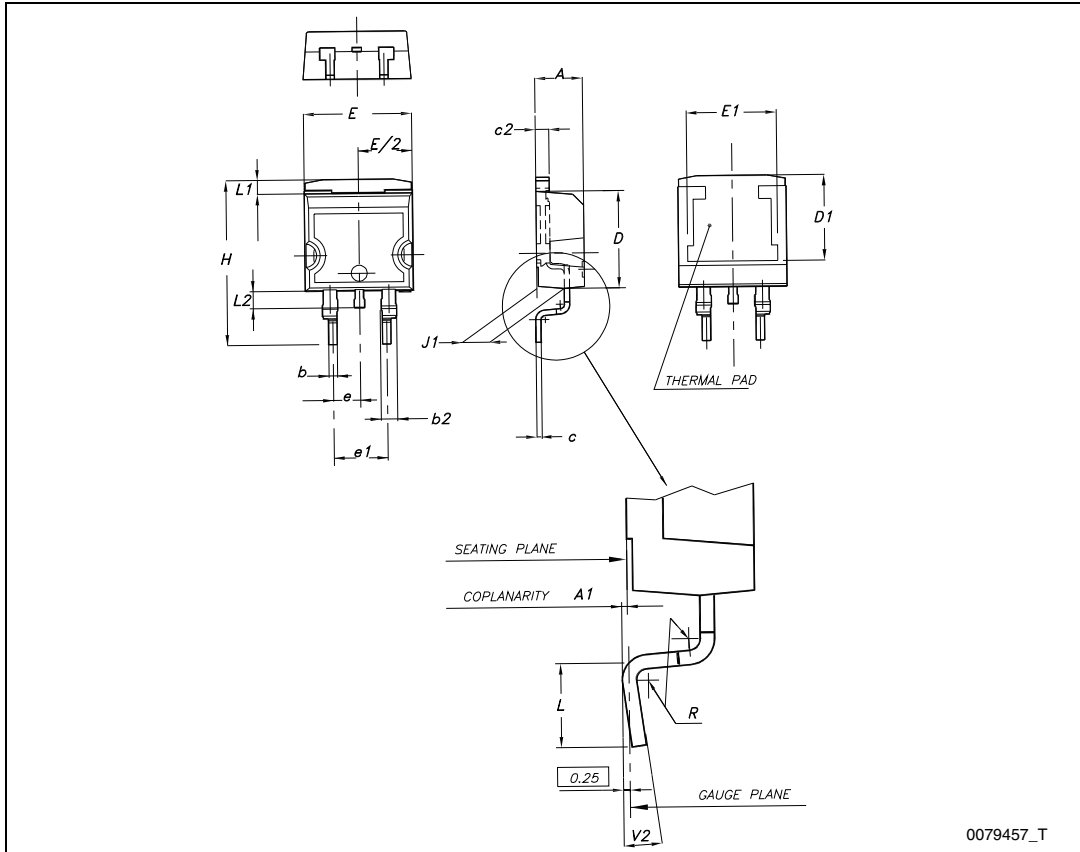
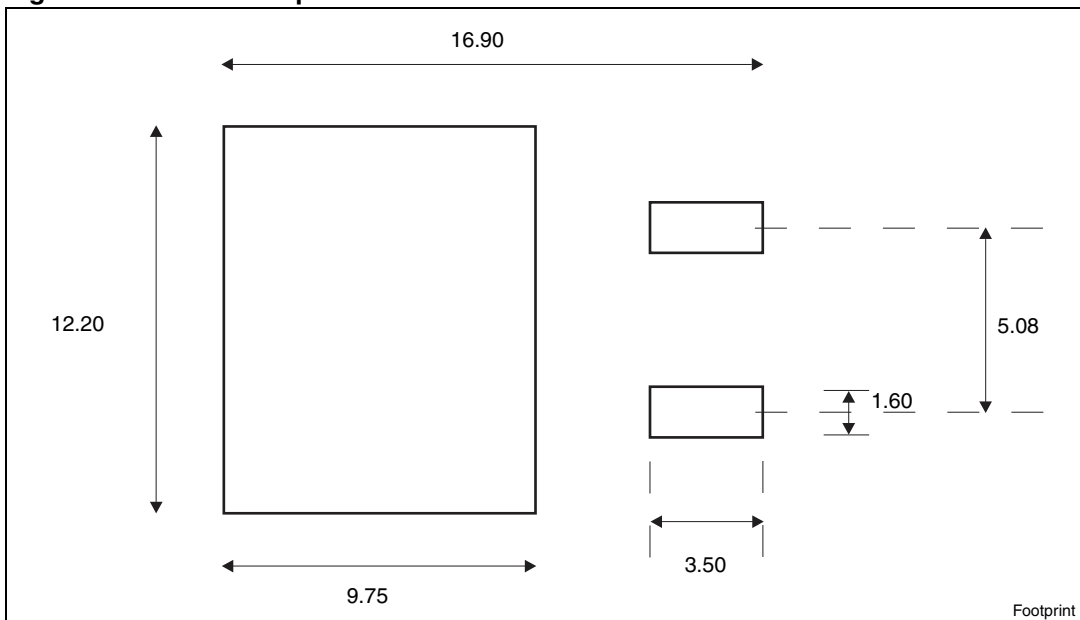


Figure 21. D<sup>2</sup>PAK footprint<sup>(a)</sup>



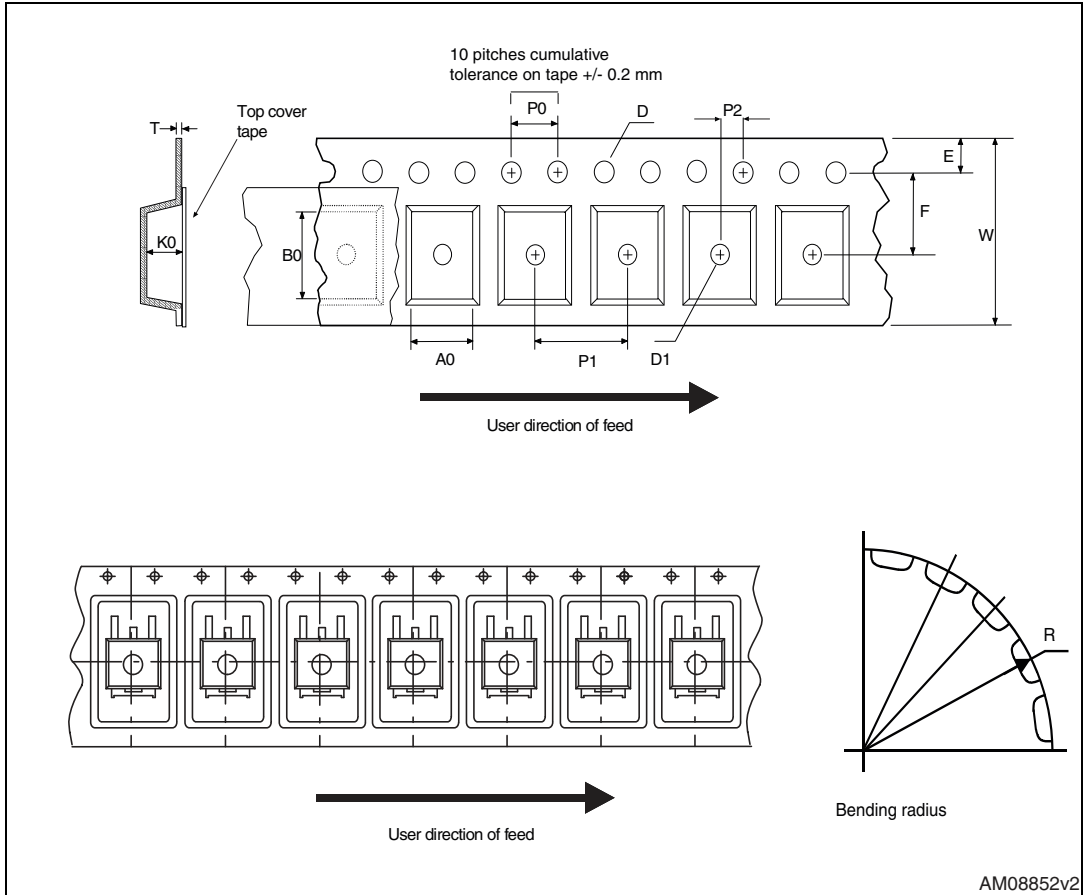
a. All dimensions are in millimeters

## 5 Packaging mechanical data

Table 10. D<sup>2</sup>PAK (TO-263) tape and reel mechanical data

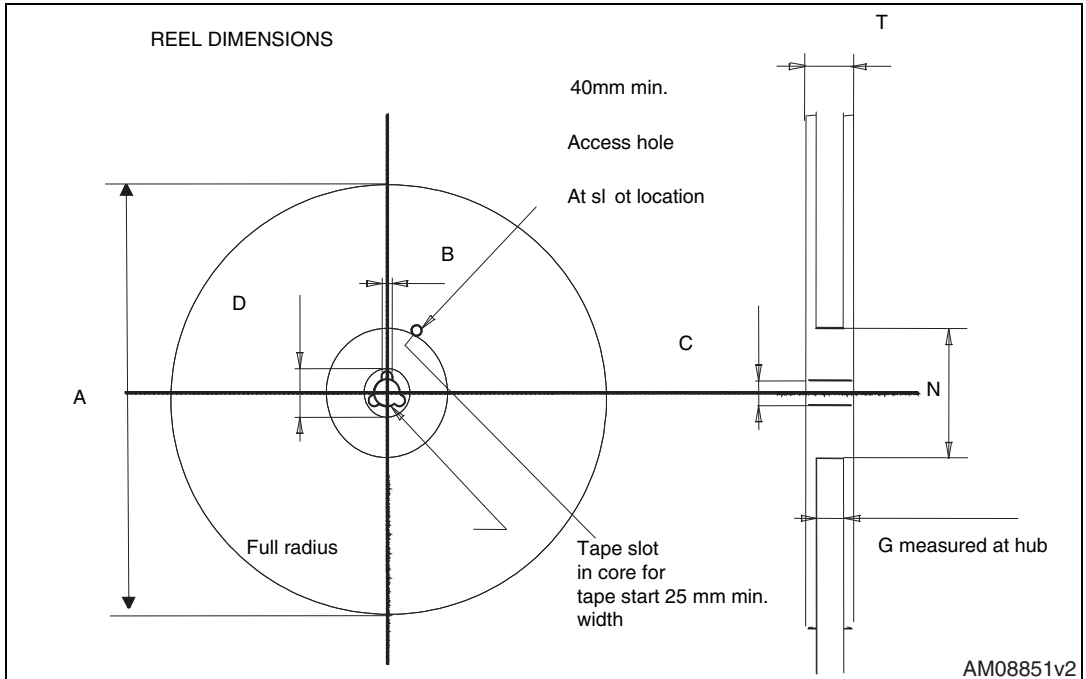
Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 22. Tape for D<sup>2</sup>PAK (TO-263) and DPAK (TO-252)



AM08852v2

Figure 23. Reel for D<sup>2</sup>PAK (TO-263) and DPAK (TO-252)



AM08851v2

## 6 Revision history

Table 11. Document revision history

Date	Revision	Changes
27-Sep-2012	1	First release.
16-Nov-2012	2	<ul style="list-style-type: none"><li>– <math>R_{thj-case}</math> has been updated in table 3</li><li>– Updated <a href="#">Section 4: Package mechanical data</a>.</li><li>– Minor text changes on cover page</li></ul>

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