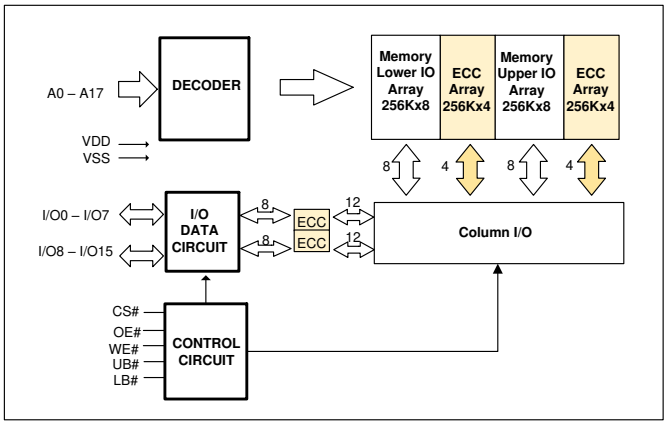
256Kx16 HIGH SPEED ASYNCHRONOUS CMOS STATIC RAM with ECC

AUGUST 2020

KEY FEATURES

- High-speed access time: 20ns
- Single power supply
  - 1.65V-2.2V VDD
- Low Standby Current:1.5mA (typical)
- Fully static operation: no clock or refresh required
- Data control
- Three state outputs
- Industrial and Automotive temperature support
- Lead-free available
- Error Detection and Correction

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The *ISSI* IS61WV25616EDALL are high-speed, low power, 4M bit static RAMs organized as 256K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology and implemented ECC function to improve reliability.

When CS# is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable (WE#) controls both writing and reading of the memory.

A data byte allows Upper Byte (UB#) and Lower Byte (LB#) access.

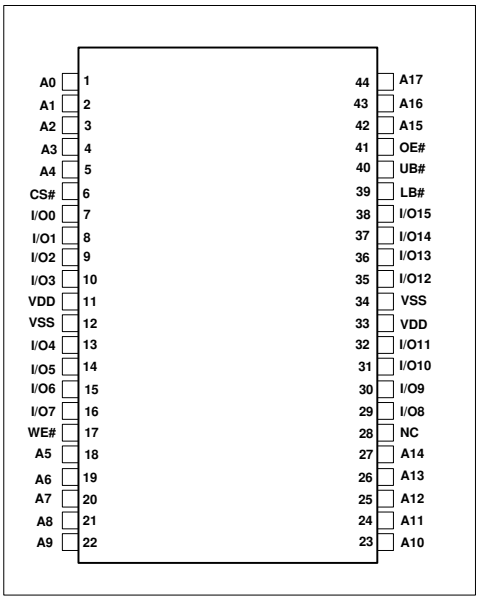
The IS61WV25616EDALL are packaged in the JEDEC standard 48-pin mini BGA (6mm x 8mm), and 44-pin TSOP (TYPE II)

PIN CONFIGURATIONS

48-Pin mini BGA(6mm x 8mm)

	1	2	3	4	5	6
A	LB#	OE#	A0	A1	A2	NC
B	I/O8	UB#	A3	A4	CS#	I/O0
C	I/O9	I/O10	A5	A6	I/O1	I/O2
D	VSS	I/O11	A17	A7	I/O3	VDD
E	VDD	I/O12	NC	A16	I/O4	VSS
F	I/O14	I/O13	A14	A15	I/O5	I/O6
G	I/O15	NC	A12	A13	WE#	I/O7
H	NC	A8	A9	A10	A11	NC

44-Pin TSOP-II



PIN DESCRIPTIONS

A0-A17	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
CS#	Chip Enable Input
OE#	Output Enable Input
WE#	Write Enable Input
LB#	Lower-byte Control (I/O0-I/O7)
UB#	Upper-byte Control (I/O8-I/O15)
NC	No Connection
VDD	Power
VSS	Ground

FUNCTION DESCRIPTION

SRAM is one of random access memories. Each byte or word has an address and can be accessed randomly. SRAM has various modes supported. Each function is described below with Truth Table.

STANDBY MODE

Device enters standby mode when deselected (CS# HIGH). The input and output pins (I/O0-15) are placed in a high impedance state. The current consumption in this mode will be ISB1, or ISB2.

WRITE MODE

Write operation issues with Chip Select (CS#) Low and Write Enable (WE#) Low. The input and output pins (I/O0-15) are in data input mode. Output buffers are closed during this time even if OE# is Low. UB# and LB# enables a byte write feature. By enabling LB# Low, data from I/O pins (I/O0 through I/O7) are written into the location specified on the address pins. And with UB# being Low, data from I/O pins (I/O8 through I/O15) are written into the location.

READ MODE

Read operation issues with Chip Select (CS#) Low and Write Enable (WE#) High. When OE# is Low, output buffer turns on to make data output. Any input to I/O pins during READ mode is not permitted. UB# and LB# enables a byte read feature. By enabling LB# Low, data from memory appears on I/O0-7. And with UB# being Low, data from memory appears on I/O8-15.

In the READ mode, output buffers can be turned off by pulling OE# High. In this mode, internal device operates as READ but I/Os are in a high impedance state. Since device is in READ mode, active current is used.

TRUTH TABLE

Mode	CS#	WE#	OE#	LB#	UB#	**I/O0-I/O7**	**I/O8-I/O15**	**VDD Current**
Not Selected	H	X	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	L	H	H	L	X	High-Z	High-Z	ICC,ICC1
	L	X	X	H	H	High-Z	High-Z	
Read	L	H	L	L	H	DOUT	High-Z	ICC,ICC1
	L	H	L	H	L	High-Z	DOUT	
	L	H	L	L	L	DOUT	DOUT	
Write	L	L	X	L	H	DIN	High-Z	ICC,ICC1
	L	L	X	H	L	High-Z	DIN	
	L	L	X	L	L	DIN	DIN	

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
Vterm	Terminal Voltage with Respect to VSS	–0.5 to V_{DD} + 0.5V	V
V_{DD}	V_{DD} Related to VSS	–0.3 to 4.0	V
tStg	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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PIN CAPACITANCE (1)

Parameter	Symbol	Test Condition	Max	Units
Input capacitance	C_{IN}	T_A = 25°C, f = 1 MHz, V_{DD} = V_{DD}(typ)	6	pF
DQ capacitance (IO0–IO15)	$C_{I/O}$		8	pF

Note:
1. These parameters are guaranteed by design and tested by a sample basis only.

OPERATING RANGE(1)

Range	Ambient Temperature	PART NUMBER	SPEED (MAX)	VDD
Commercial	0°C to +70°C	IS61WV25616EDALL	20 ns	1.65V – 2.2V
Industrial	-40°C to +85°C		20 ns	1.65V – 2.2V

Note:
1. Full device AC operation assumes a 100 µs ramp time from 0 to V_{DD}(min) and 200 µs wait time after V_{DD} stabilization.

THERMAL CHARACTERISTICS (1)

Parameter	Symbol	Rating	Units
Thermal resistance from junction to ambient (airflow = 1m/s)	$R_{\theta JA}$	TBD	°C/W
Thermal resistance from junction to pins	$R_{\theta JB}$	TBD	°C/W
Thermal resistance from junction to case	$R_{\theta JC}$	TBD	°C/W

Note:
1. These parameters are guaranteed by design and tested by a sample basis only.

AC TEST CONDITIONS (OVER THE OPERATING RANGE)

Parameter	Unit (1.65V~2.2V)
Input Pulse Level	0V to V_{DD}
Input Rise and Fall Time	1.5 ns
Output Timing Reference Level	0.9V
R1 (ohm)	13500
R2 (ohm)	10800
V_{TM} (V)	1.8V
Output Load Conditions	Refer to Figure 1 and 2

OUTPUT LOAD CONDITIONS FIGURES

FIGURE 1

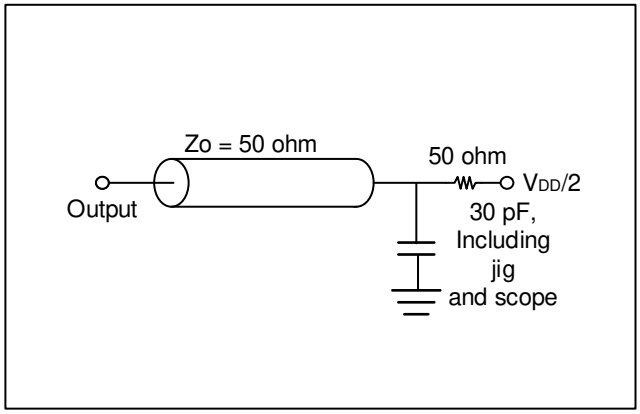
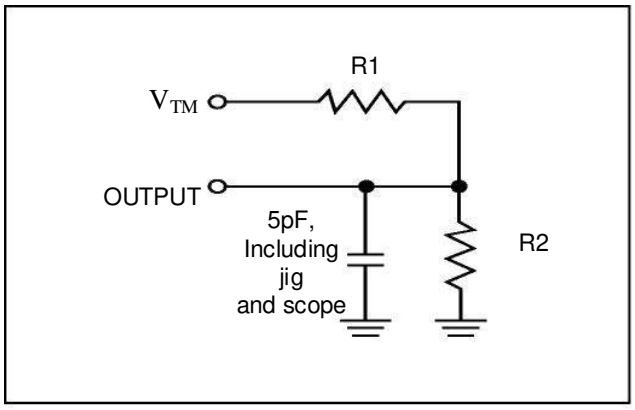


FIGURE 2



DC ELECTRICAL CHARACTERISTICS

IS61(64)WV25616EEBLL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)
VDD = 1.65V – 2.2V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	—	0.2	V
V_{IH}(1)	Input HIGH Voltage		1.4	V_{DD} + 0.2	V
V_{IL}(1)	Input LOW Voltage		–0.2	0.4	V
I_{LI}	Input Leakage	GND < V_{IN} < V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND < V_{IN} < V_{DD}, Output Disabled	–1	1	µA

Notes:
1. VILL(min) = -1.0V AC (pulse width < 20ns). Not 100% tested.
2. VIHH (max) = VDD + 1.0V AC (pulse width < 20ns). Not 100% tested.

POWER SUPPLY CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Grade	-20 Max	Unit
ICC	V_{DD} Dynamic Operating Supply Current	V_{DD} = MAX, I_{OUT} = 0 mA, f = f_{MAX}	Com.	25	mA
			Ind.	30	
			Auto.	-	
ICC1	Operating Supply Current	V_{DD} = MAX, I_{OUT} = 0 mA, f = 0	Com.	20	mA
			Ind.	25	
			Auto.	-	
ISB1	TTL Standby Current (TTL Inputs)	V_{DD} = MAX, V_{IN} = V_{IH} or V_{IL} CS# ≥ V_{IH}, f = 0	Com.	10	mA
			Ind.	15	
			Auto.	-	
ISB2	CMOS Standby Current (CMOS Inputs)	V_{DD} = MAX, CS# ≥ V_{DD} - 0.2V V_{IN} ≥ V_{DD} - 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com.	5	mA
			Ind.	6	
			Auto.	-	
			Typ. (2)	1.5	

Notes:
1. At f = fMAX, address and data inputs are cycling at the maximum frequency, f = 0 means no input line change.
2. Typical values are measured at V_{DD} = 1.8V, T_A = 25 °C and not 100% tested.

AC CHARACTERISTICS (OVER OPERATING RANGE)

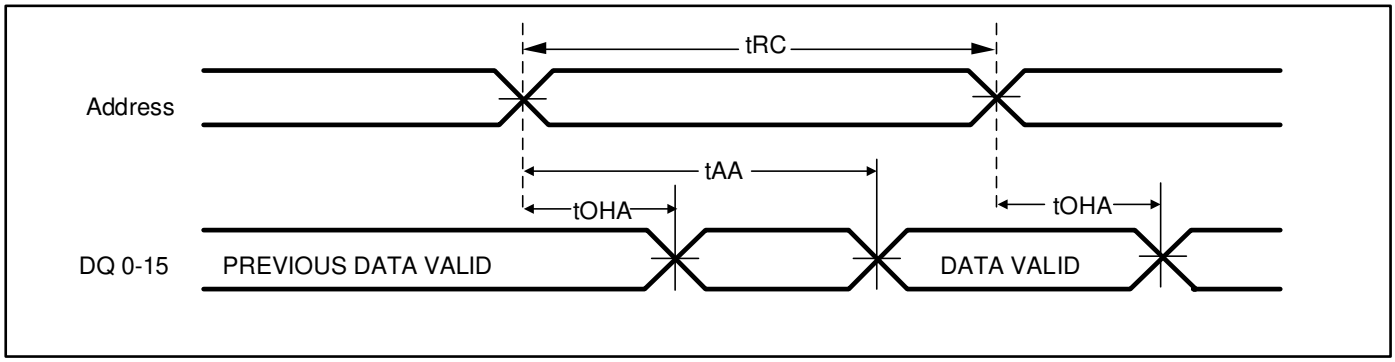
READ CYCLE AC CHARACTERISTICS

Parameter	Symbol	-20[1]		unit	notes
		Min	Max		
Read Cycle Time	tRC	20	-	ns	
Address Access Time	tAA	-	20	ns	
Output Hold Time	tOHA	2.5	-	ns	
CS# Access Time	tACE	-	20	ns	
OE# Access Time	tDOE	-	8	ns	
OE# to High-Z Output	tHZOE	0	8	ns	2
OE# to Low-Z Output	tLZOE	0	-	ns	2
CS# to High-Z Output	tHZCE	0	8	ns	2
CS# to Low-Z Output	tLZCE	3	-	ns	2
UB#, LB# Access Time	tBA	-	8	ns	
UB#, LB# to High-Z Output	tHZB	0	8	ns	2
UB#, LB# to Low-Z Output	tLZB	0	-	ns	2

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of VDD/2, and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

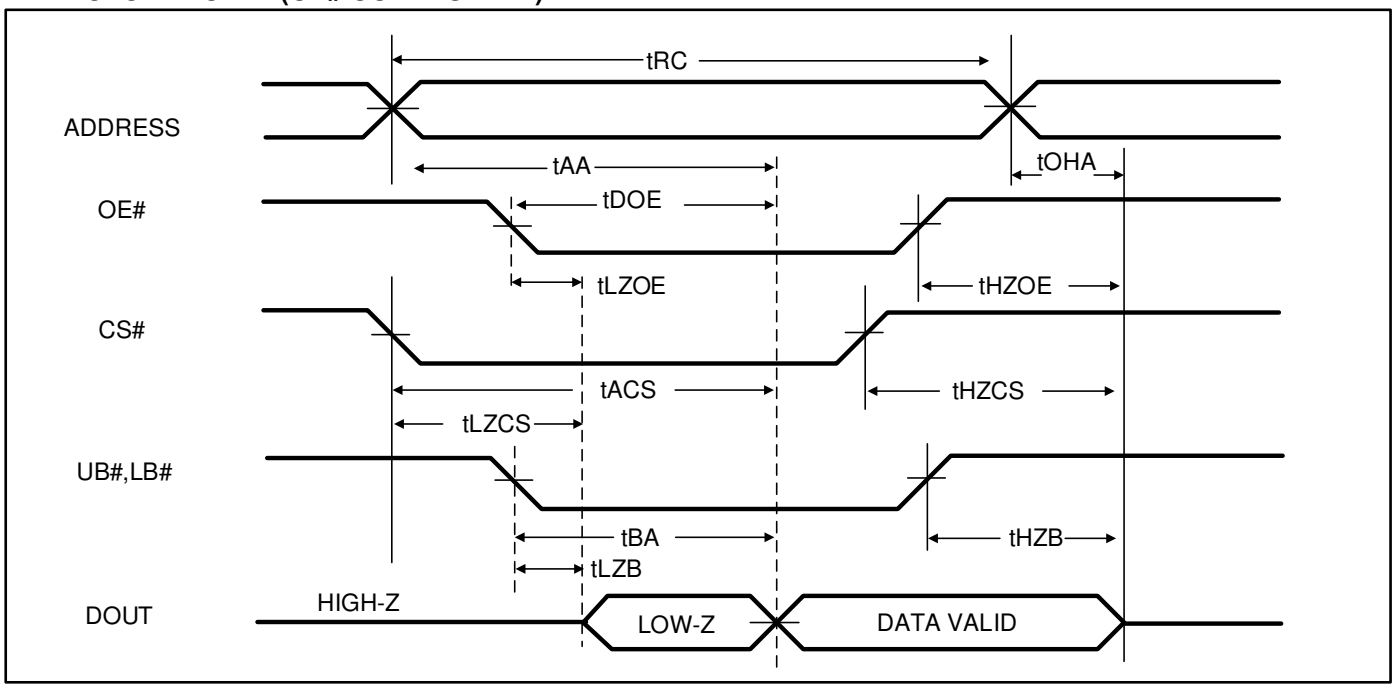
Timing Diagram

READ CYCLE NO. 1[1,2] (ADDRESS CONTROLLED , CS#, OE#, UB#, LB# = LOW, WE# = HIGH)



Note:
1. The device is continuously selected.

READ CYCLE NO. 2[1] (OE# CONTROLLED)



Notes:
1. Address is valid prior to or coincident with CS# LOW transition.

WRITE CYCLE AC CHARACTERISTICS

Parameter	Symbol	-20[1]		unit	notes
		Min	Max		
Write Cycle Time	tWC	20	-	ns	
CS# to Write End	tSCS	12	-	ns	
Address Setup Time to Write End	tAW	12	-	ns	
UB#,LB# to Write End	tPWB	12	-	ns	
Address Hold from Write End	tHA	0	-	ns	
Address Setup Time	tSA	0	-	ns	
WE# Pulse Width	tPWE1	12	-	ns	
WE# Pulse Width (OE# = LOW)	tPWE2	17	-	ns	2
Data Setup to Write End	tSD	9	-	ns	
Data Hold from Write End	tHD	0	-	ns	
WE# LOW to High-Z Output	tHZWE	-	9	ns	
WE# HIGH to Low-Z Output	tLZWE	3	-	ns	

Notes:

1 Test conditions assume signal transition times of 3 ns or less, timing reference levels of VDD/2, and output loading specified in Figure 1.

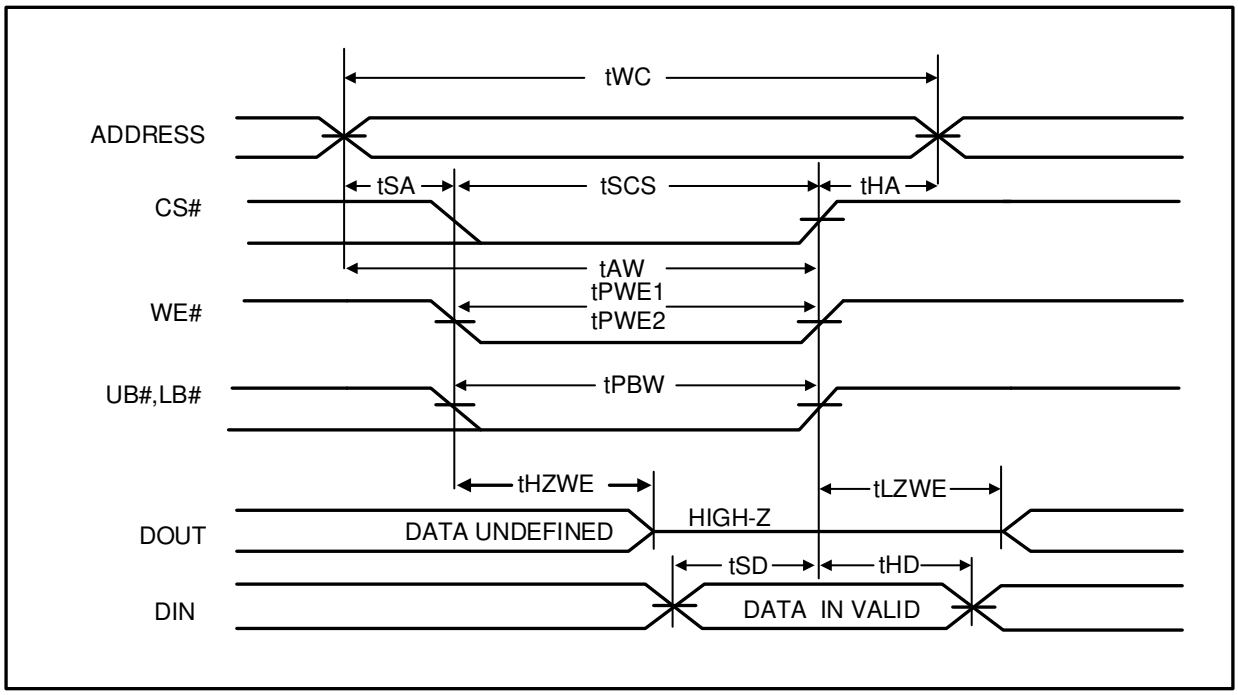
2 Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

3 The internal write time is defined by the overlap of CS# = LOW, UB# or LB# = LOW, and WE# = LOW. All signals must be in valid states to initiate a Write, but anyone can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

4 If OE# is LOW during write cycle, (WE# controlled, CS# = UB# = LB# = LOW), the minimum Write cycle time for write cycle NO.3 is the sum of tHZWE and tSD

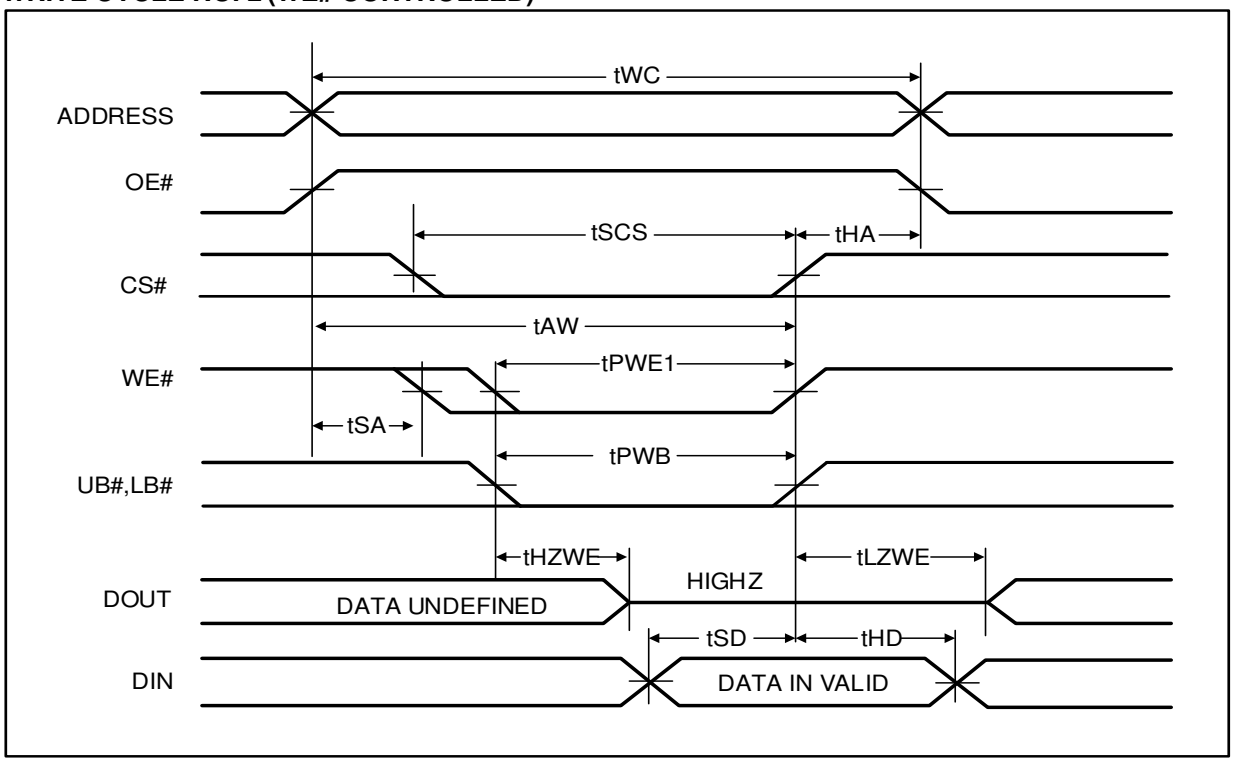
Timing Diagram

WRITE CYCLE NO. 1[1] (WE# CONTROLLED, OE# = HIGH OR LOW)

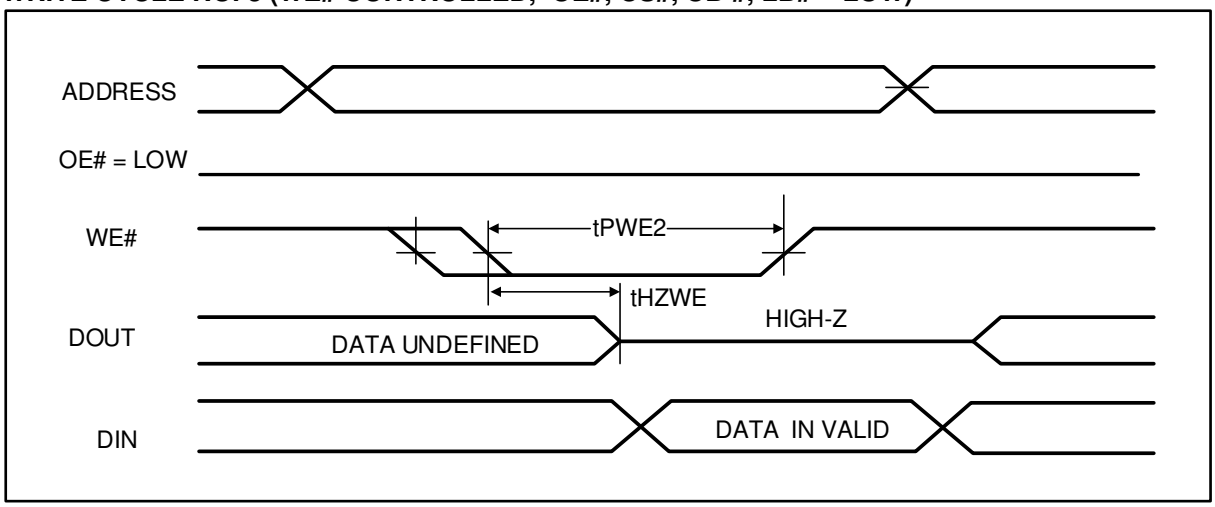


Notes:
1. tHZWE is based on the assumption when tSA=0nS after READ operation. Actual DOUT for tHZWE may not appear if OE# goes high before Write Cycle.

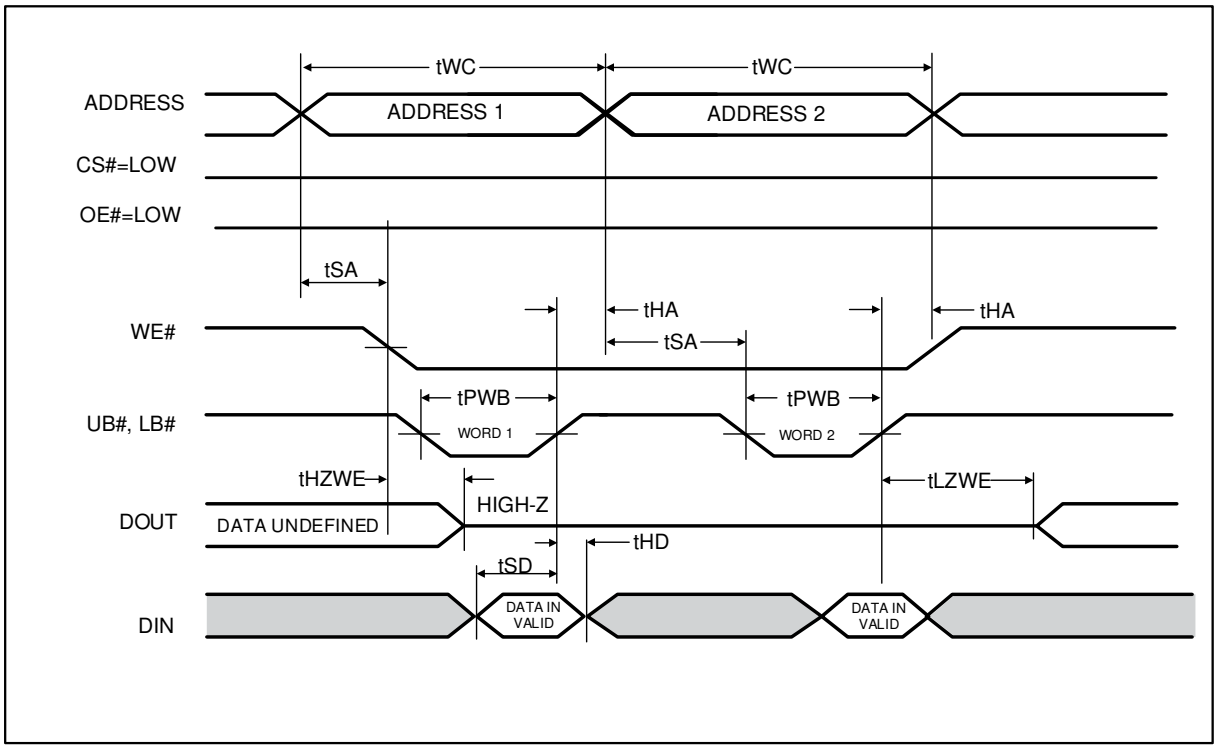
WRITE CYCLE NO. 2 (WE# CONTROLLED)



WRITE CYCLE NO. 3 (WE# CONTROLLED, OE#, CS#, UB #, LB# = LOW)



WRITE CYCLE NO. 4 (UB# & LB# Controlled)

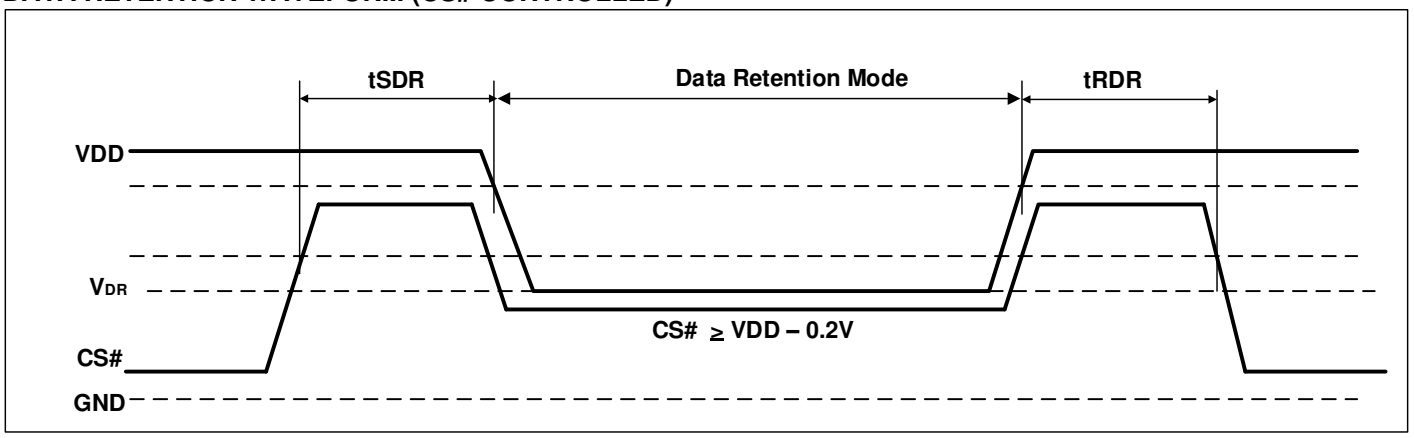


DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Test Condition	OPTION	Min.	Typ.(2)	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		1.2	-	-	V
I_{DR}	Data Retention Current	V_{DD} = MAX, CS# ≥ V_{DD} – 0.2V, V_{IN} ≥ V_{DD} - 0.2V, or V_{IN} ≤ 0.2V	Com.	-	0.5	5	mA
			Ind.	-	-	6	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	-	-	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		tRC	-	-	ns

Notes:
1. If CS# >VDD–0.2V, all other inputs including UB# and LB# must meet this condition.
2. Typical values are measured at VDD= 1.8V, TA = 25°C and not 100% tested.

DATA RETENTION WAVEFORM (CS# CONTROLLED)

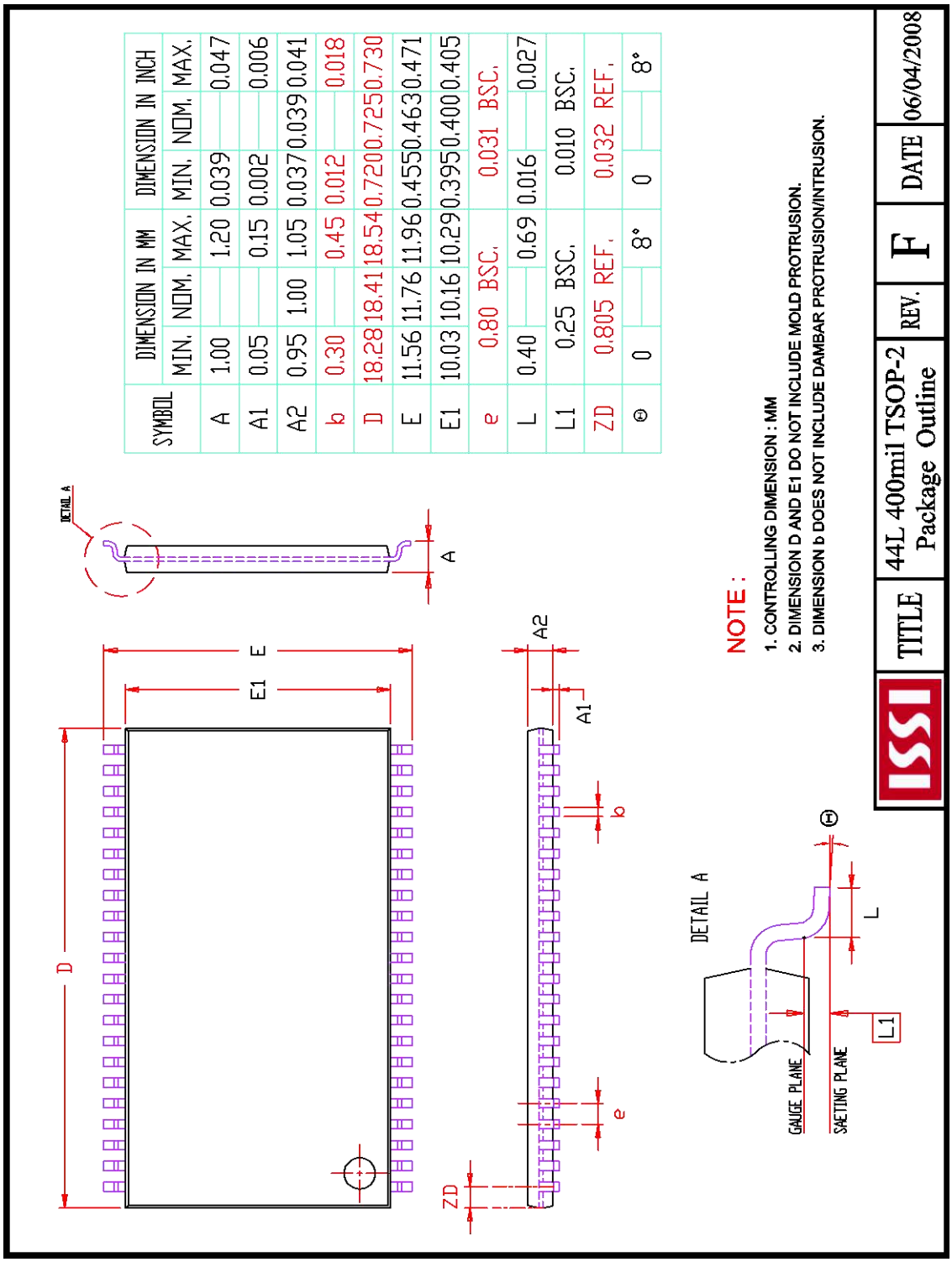


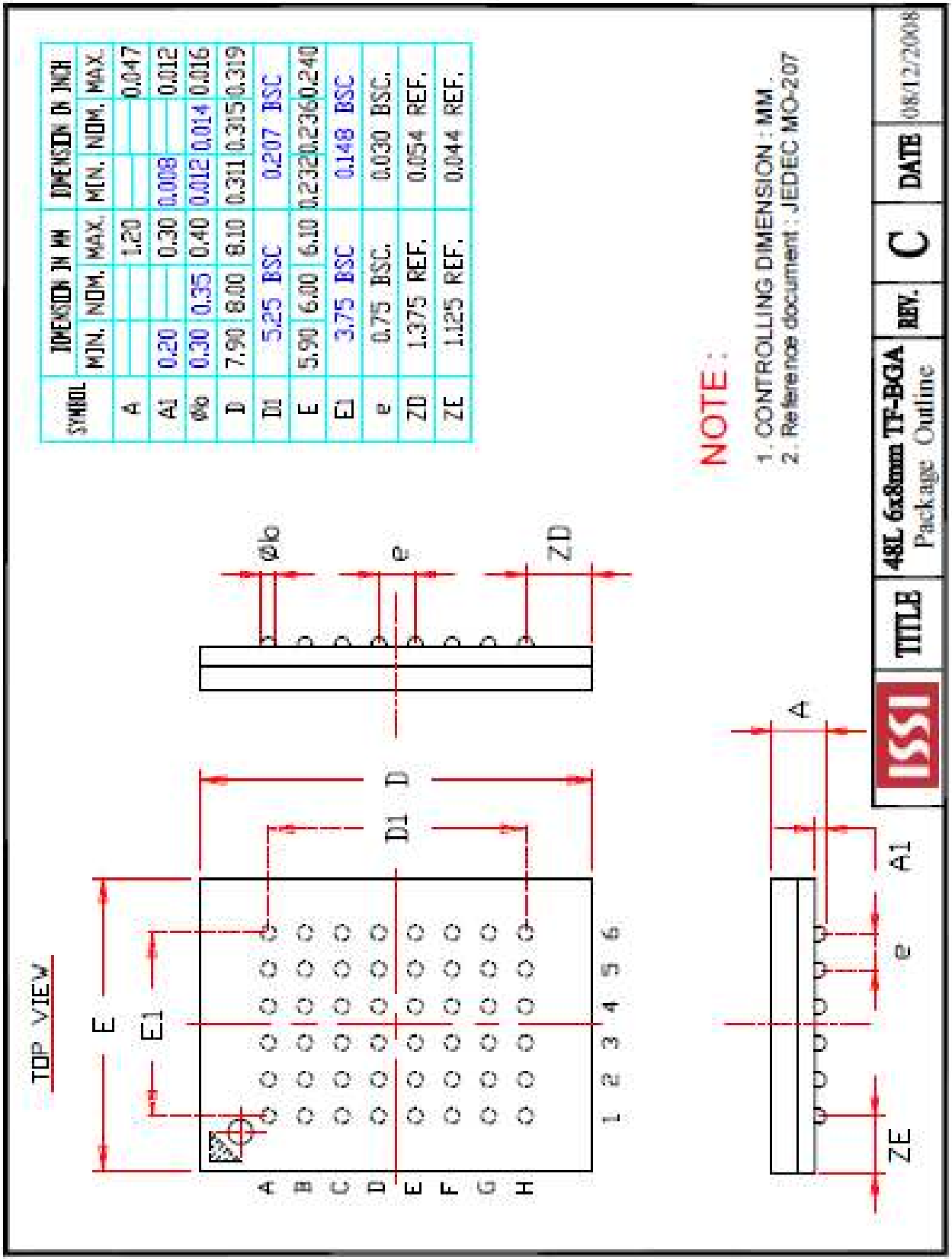
ORDERING INFORMATION

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
20	IS61WV25616EDALL-20BLI	mini BGA (6mm x 8mm), Lead-free
20	IS61WV25616EDALL-20TLI	TSOP (Type II), Lead-free

PACKAGE INFORMATION




SYMBOL
DIMENSION IN MM
DIMENSION IN INCH
MIN. NOM. MAX.
MIN. NOM. MAX.
A — — 1.20 — — 0.047
A1 0.20 — 0.30 0.008 — 0.012
ϕb 0.30 0.35 0.40 0.012 0.014 0.016
D 7.90 8.00 8.10 0.311 0.315 0.319
D1 5.25 BSC 0.207 BSC
E 5.90 6.00 6.10 0.232 0.236 0.240
E1 3.75 BSC 0.148 BSC
e 0.75 BSC. 0.030 BSC.
ZD 1.375 REF. 0.054 REF.
ZE 1.125 REF. 0.044 REF.
NOTE:
1. CONTROLLING DIMENSION : MM.
2. Reference document : JEDEC MO-207
TITLE
48L 6x8mm TF-BGA
Package Outline
REV.
C
DATE
08/12/2008
TOP VIEW
E
E1
D
D1
ϕb
e
ZD
A
A1
ZE
1 2 3 4 5 6
A B C D E F G H