64 Analog Input Telemetry Controller for Space

Description

The LX7730 is a spacecraft telemetry manager that is radiation-hardened by design and works with either a space FPGA controller such as RTG4, RTAX-S/SL, and RT PolarFire, or a space MCU such as SAMRH71F20, SAMV71Q21RT, and SAM3X8ERT.

The LX7730 contains a 64 universal input multiplexer that can be configured for a mix of differential and/or single ended sensor inputs. The internal programmable current source can be directed to any of the 64 universal inputs. The universal inputs can be acquired by the internal 12-bit ADC at a sample rate up to 13kHz. The universal inputs also function as variable bi-level inputs with the threshold set by an internal 8-bit DAC. There is an additional 10-bit current DAC with complementary outputs. Finally, there are 8 fixed threshold bi-level inputs with logic outputs.

The LX7730 is register programmable with 17 addressable 8-bit registers. Two options are available for communication with the host system controller. First there is an 8-bit parallel bus with 5 address bits, a parity bit, and a read/write bit that can communicate at a speed of up to 25Mword/s. The second option is a pair of 12.5Mbit/s SPI interfaces that support redundant communication to two different hosts.

The LX7730 has enable registers that allow most of the device to be shut down to reduce power consumption, and supports cold sparing on its signal pins. The dielectric isolated process is failsafe.

The LX7730LMFQ offers lower guaranteed operating and standby supply currents than the LX7730MFQ, as shown in the Electrical Characteristics. Operation is identical in all other respects. All other references to LX7730 in this data sheet apply to the LX7730LMFQ, LX7730MFQ, and LX7730LMMF.

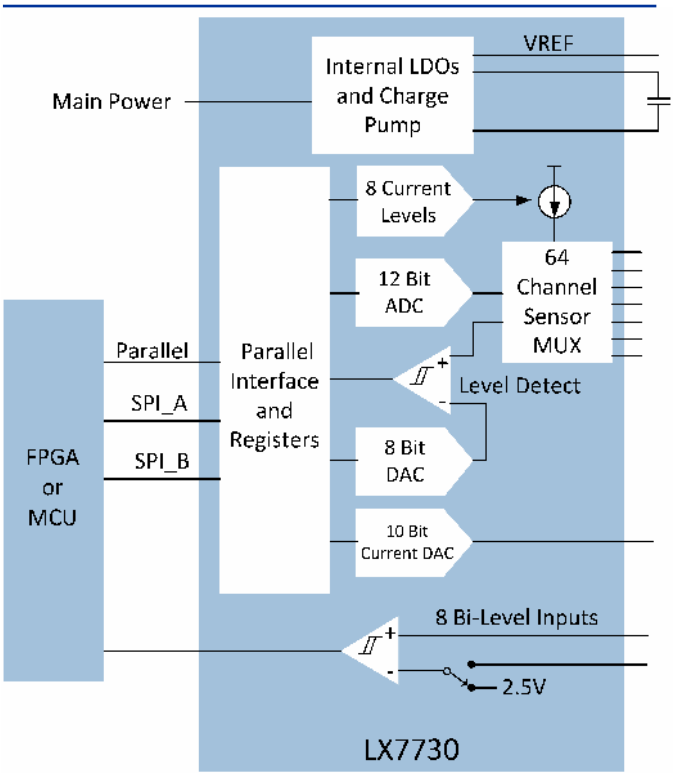
The LX7730(L)MFQ is packaged in a 132-pin hermetic ceramic quad flat pack. The LX7730LMMF is packaged in a lead-free 208 pin non-hermetic plastic quad flat pack. Both parts operate over a 55°C to 125°C temperature range, and are radiation tolerant to 100krad(Si) TID and 50krad(Si) ELDRs, as well as single event effects.

Features

- 64 channel analog input multiplexer
- Break-Before-Make switching
- 13ksps 12-bit ADC
- 1% precision 5V voltage reference
- 3% precision adjustable current source
- Threshold monitoring
- 8 bi-level analog inputs and logic outputs
- 8 additional bi-level inputs from the multiplexer
- 10-bit DAC
- Parallel interface or dual SPI interface
- Radiation tolerant: 100krad(Si) TID, 50krad(Si) ELDRS, SEL immune up to 87MeV.cm²/mg and 125°C (fluence of 10^8 particles/cm²)

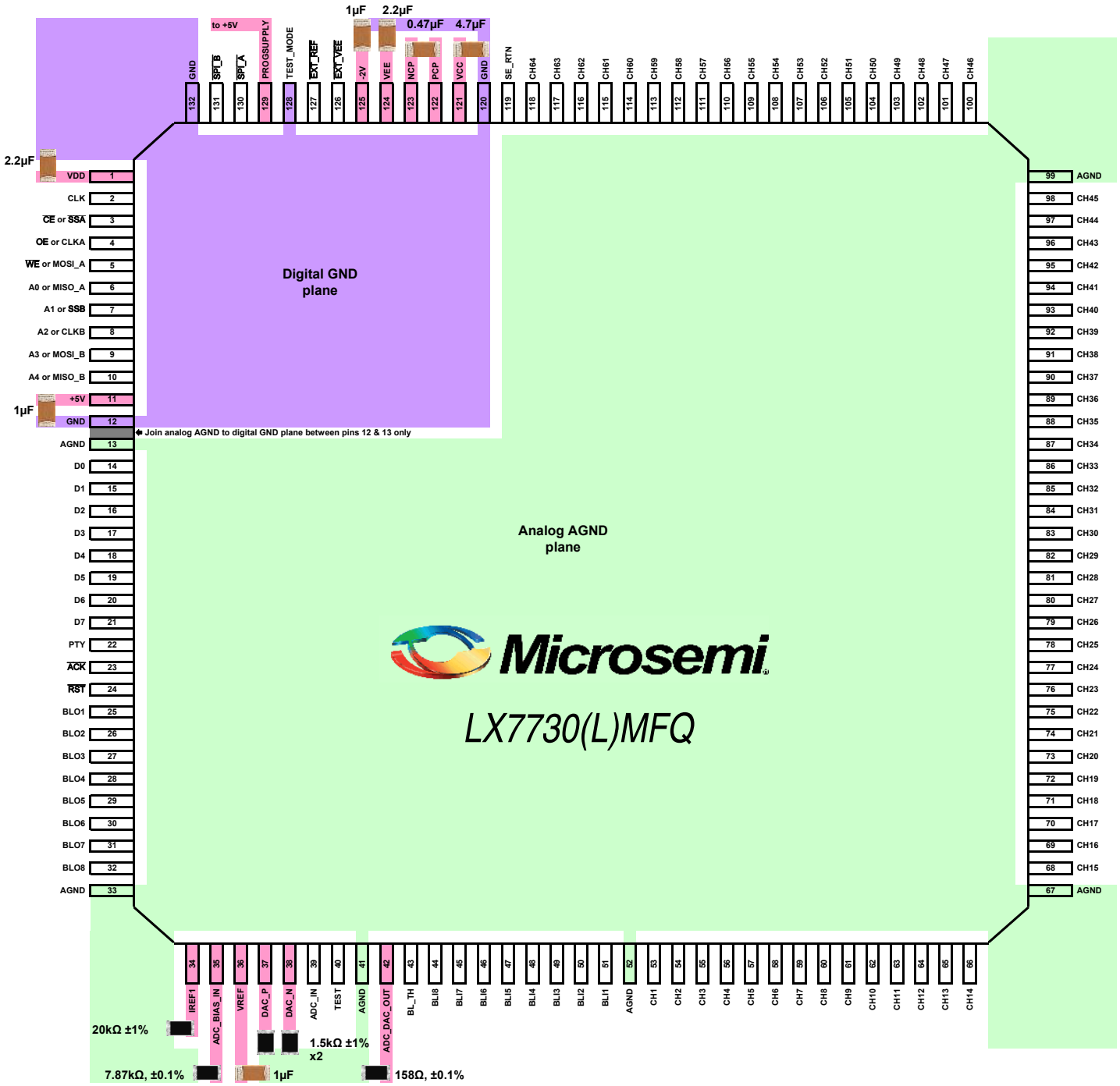
Applications

- Spacecraft health monitoring
- Attitude control
- Payload equipment



Typical Telemetry System

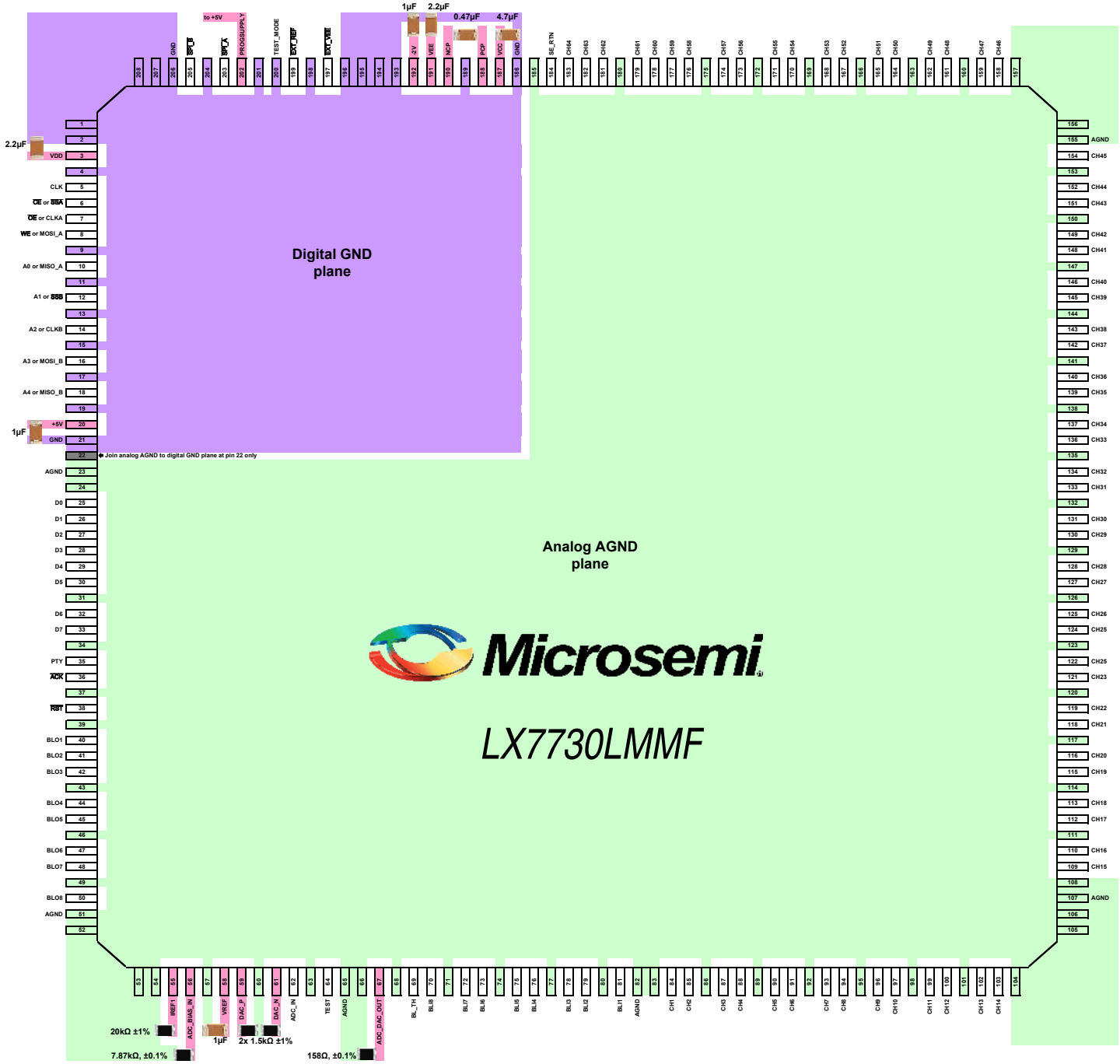
1 CQFP-132 Pin Configuration and Pinout with Recommended Layout



2 Ordering Information

Operating Temperature	Package Type	Package	Part Number	SMD Number	Flow	Shipping Type
-55°C to 125°C	Hermetic Ceramic	CQFP 132L	LX7730MFQ-V	SMD5962-1721901VXC	QML-V	Tray
			LX7730MFQ-Q	SMD5962-1721901QXC	QML-Q	
			LX7730LMFQ-EV	TBD	MIL-PRF-38535 Class V	
			LX7730LMFQ-EQ	TBD	MIL-PRF-38535 Class Q	
	Ceramic		LX7730MFQ-ES	-	Engineering Samples	
	Plastic	QFP 208L	LX7730LMMF	-	JEDEC	

3 QFP-208 Pin Configuration and Pinout with Recommended Layout



Note 1. The layout examples show split planes for SGND and MGND. Separate SGND and MGND planes can be used

Note 2. Capacitors are shown as  . Resistors are shown as 

Note 3. The QFP has many unused pins, shown as un-named pins. These pins are not bonded internally. The layout example connects these pins to one or the other of the ground planes to assist with connectivity

Note 4. The pin marked TEST (CQFP pin 40, QFP pin 64) is a factory test pin which must be left open

4 CQFP-132-pin Numbering and Pin Descriptions

132L	Name	Pin Type	Pin Function	Description
1	VDD	Power	I/O Supply	Connect to the external logic controller's (FPGA, MCU) I/O power supply (2.25V to 5.5V) to set the I/O logic level for all logic I/Os. Bypass close to the pin with a 2.2µF capacitor to GND
2	CLK	Logic Input (1MΩ to GND)	ADC Clock	Connect a 125kHz to 500kHz clock to operate the ADC logic
3	$\overline{CE}$, or $\overline{SSA}$	Logic Input (1MΩ to VDD)	Chip Enable Slave Select A	Active low chip enable for the parallel interface ($\overline{SPI\_A}$ = $\overline{SPI\_B}$ = 1) Active low slave select for SPI channel A interface ($\overline{SPI\_A}$ = 0, $\overline{SPI\_B}$ = 1)
4	$\overline{OE}$, or CLKA	Logic Input (1MΩ to VDD)	Output Enable Clock A	Active low output enable (read) for the parallel interface ($\overline{SPI\_A}$ = $\overline{SPI\_B}$ = 1) Clock input for SPI channel A interface ($\overline{SPI\_A}$ = 0, $\overline{SPI\_B}$ = 1)
5	$\overline{WE}$, or MOSI_A	Logic Input (1MΩ to VDD)	Write Enable MOSI A	Active low write enable for the parallel interface ($\overline{SPI\_A}$ = $\overline{SPI\_B}$ = 1) Data input for SPI channel A interface ($\overline{SPI\_A}$ = 0, $\overline{SPI\_B}$ = 1)
6	A0, or MISO_A	Logic I/O (1MΩ to GND)	Address A0 MISO A	Register address bit A0 (LSB) for the parallel interface ($\overline{SPI\_A}$ = $\overline{SPI\_B}$ = 1) Data output for SPI channel A interface ($\overline{SPI\_A}$ = 0, $\overline{SPI\_B}$ = 1)
7	A1, or $\overline{SSB}$	Logic Input (1MΩ to VDD)	Address A1 Slave Select B	Register address bit A1 for the parallel interface ($\overline{SPI\_A}$ = $\overline{SPI\_B}$ = 1) Active low slave select for SPI channel B interface ($\overline{SPI\_A}$ = 1, $\overline{SPI\_B}$ = 0)
8	A2, or CLKB	Logic Input (1MΩ to GND)	Address A2 Clock B	Register address bit A2 for the parallel interface ($\overline{SPI\_A}$ = $\overline{SPI\_B}$ = 1) Clock input for SPI channel B interface ($\overline{SPI\_A}$ = 1, $\overline{SPI\_B}$ = 0)
9	A3, or MOSI_B	Logic Input (1MΩ to GND)	Address A3 MOSI B	Register address bit A3 for the parallel interface ($\overline{SPI\_A}$ = $\overline{SPI\_B}$ = 1) Data input for SPI channel B interface ($\overline{SPI\_A}$ = 1, $\overline{SPI\_B}$ = 0)
10	A4, or MISO_B	Logic I/O (1MΩ to GND)	Address A4 MISO B	Register address bit A4 (MSB) for the parallel interface ($\overline{SPI\_A}$ = $\overline{SPI\_B}$ = 1) Data output for SPI channel B interface ($\overline{SPI\_A}$ = 1, $\overline{SPI\_B}$ = 0)
11	+5V	Power	Internal +5V Supply	Bypass close to the pin with a 1µF capacitor to GND. Optionally overdrive pin with an external 5.5V ±0.25V supply which shuts down the internal regulator
12	GND	Ground	Digital and Power Ground	All GND pins 12, 120, and 132 must be used, connected together via a plane or split-plane on the PCB, and used for connection and termination of digital and power external components. Only join GND here at pin 12 to AGND at pin 13 as a star point
13	AGND	Ground	Analog Ground	All AGND pins 13, 33, 41, 52, 67, and 99 must be used, connected together via a plane or split-plane on the PCB, and used for termination of analog signals only. Only join AGND here at pin 13 to GND at pin 12 as a star point
14 - 21	D0 - D7	Logic I/O (1MΩ to GND)	Data Bus	Data bus D0 (LSB) to D7 (MSB) for the parallel interface
22	PTY	Logic I/O (1MΩ to GND)	Data Bus Parity	Even parity bit for the parallel interface combined address (A0 - A4), data (D0 - D7) bits, and the PTY signal. A write parity error sets the $\overline{ACK}$ output high
23	$\overline{ACK}$	Logic Output	Data Bus Write Acknowledge	Data write acknowledge output for the serial and parallel interfaces. $\overline{ACK}$ is active low to validate data (indicate no parity error) for serial or parallel writes to LX7730
24	$\overline{RESET}$	Logic I/O	System Reset	Active low input resets the LX7730 internal settings to the POR state. An optional capacitor to GND extends the internal reset time
25 - 28	BLO1 - BLO4	Logic Outputs	Bi-Level Outputs 1 to 4	Output of fixed threshold bi-level monitor (comparator) input BLI1, BLI2, BLI3 and BLI4 at pins 51, 50, 49, and 48 respectively
29	BLO5	Logic Output	Bi-Level Output 5	Output of fixed threshold bi-level monitor (comparator) input BLI5 at pin 47 When the LX7730 is in reset state (either $\overline{RESET}$ pin 24 held active low, or Master Reset register 0 contains 0x6A) then output is instead VCC LVD status, Power Status Register 2 bit D2 (Table 18 on page 33)
30	BLO6	Logic Output	Bi-Level Output 6	Output of fixed threshold bi-level monitor (comparator) input BLI6 at pin 46 When the LX7730 is in reset state (either $\overline{RESET}$ pin 24 held active low, or Master Reset register 0 contains 0x6A) then output is instead VEE LVD status, Power Status Register 2 bit D1 (Table 18 on page 33)
31	BLO7	Logic Output	Bi-Level Output 7	Output of fixed threshold bi-level monitor (comparator) input BLI7 at pin 45 When the LX7730 is in reset state (either $\overline{RESET}$ pin 24 held active low, or Master Reset register 0 contains 0x6A) then output is instead +5V LVD status, Power Status Register 2 bit D0 (Table 18 on page 33)
32	BLO8	Logic Output	Bi-Level Output 8	Output of fixed threshold bi-level monitor (comparator) input BLI8 at pin 44 When the LX7730 is in reset state (either $\overline{RESET}$ pin 24 held active low, or Master Reset register 0 contains 0x6A) then output is instead Power On Enable status, which is high when the internal logic is ready after power-up
33	AGND	Ground	Analog Ground	All AGND pins 13, 33, 41, 52, 67, and 99 must be used, connected together via a plane or split-plane on the PCB, and used for termination of analog signals only. Only join AGND to GND at pins 12 and 13

132L	Name	Pin Type	Pin Function	Description
34	IREF1	Analog Input	Current Reference Bias Resistor	Connect a 20kΩ ±1% resistor from IREF1 to AGND pin 33 to set the internal reference current. Minimize the track length from the resistor to pin 34, and route a direct track to AGND pin 33. The voltage at IREF1 is 1.6V
35	ADC_ BIAS_IN	Analog Input	ADC Bias Resistor	Connect a 7.87kΩ, ±0.1% resistor from ADC_BIAS_IN to AGND pin 33 to set the internal precision current reference for the ADC. Minimize the track length to pin 35, and route a direct track to AGND pin 33. The voltage at ADC_BIAS_IN is 1.6V
36	VREF	Analog I/O	Internal VREF Output External VREF Input	To use the internal +5V ±1% reference voltage, connect a 1µF capacitor from VREF to AGND pin 33 and tie $\overline{\text{EXT\_REF}}$ pin 127 to +5V. To use an external reference voltage up to 5.5V, connect the external reference to VREF, and tie $\overline{\text{EXT\_REF}}$ pin 127 to either GND or AGND
37	DAC_P	Analog Output	10-Bit Current DAC (+) Output	Positive output for the 10-bit current DAC. The code range 0x000 to 0x3FF in the 10-bit DAC registers 14 and 15 (Table 30 on page 46) sources an increasing output current from 0 to 2mA. Terminate DAC_P with a resistor ≤1.5kΩ to AGND to develop a nominal output voltage ≤3V maximum at code 0x3FF. To assign the DAC_P output alternatively to internal use as the current source for the analog input multiplexer, set Current Mux Level register 5 bit D7 = 0 (Table 21 on page 38) and leave DAC_P open
38	DAC_N	Analog Output	10-Bit Current DAC (-) Output	Negative output for the 10-bit current DAC. The code range 0x000 to 0x3FF in the 10-bit DAC registers 14 and 15 (Table 30 on page 46) sources a decreasing output current from 2 to 0mA. Terminate DAC_N with a resistor ≤1.5kΩ to AGND to develop a nominal output voltage ≤3V maximum at code 0x000. If the 10-bit DAC is to be assigned to internal use as the current source for the analog input multiplexer (Current Mux Level register 5 bit D7 = 0), terminate DAC_N to either GND or AGND
39	ADC_IN	Analog I/O	AFE Output ADC Input	Optionally connect a redundant ADC here to monitor the final output from the complete AFE multiplexer-gain-filter system. Alternatively, to assert a unipolar input signal with 0 to 2V range directly to the ADC, disable the AFE by setting ADC Control register bit D0 = 1 (Table 24 on page 40)
40	TEST	Factory Use	Test	Internally bonded test node. Leave this pin floating
41	AGND	Ground	Analog Ground	All AGND pins 13, 33, 41, 52, 67, and 99 must be used, connected together via a plane or split-plane on the PCB, and used for termination of analog signals only. Only join AGND to GND at pins 12 and 13
42	ADC_ DAC_ OUT	Analog Input	DAC bias resistor	Connect a 158Ω, ±0.1% resistor from ADC_ DAC_OUT to AGND pin 41 to provide the precision load for the ADC's current output DAC. Minimize the track length to pin 42, and route a direct track to AGND pin 41. The voltage at ADC_DAC_OUT ranges from 1V minimum to 2V maximum during an ADC conversion, and returns to 0V at the end of the conversion
43	BL_TH	Analog Input	Bi-Level (-) external threshold input	Optional external negative (-) threshold voltage for the fixed threshold bi-level monitors (comparators) BL1 to BLI8 To use an external reference voltage between 0.1V and 4.9V on BL_TH, set bit B7 in the Bi-Level Bank register 12 (Table 28 on page 44) To use the internal 2.5V ±50mV threshold, clear bit B7 in the Bi-Level Bank register 12, and connect the BL_TH pin to either GND or AGND
44 - 51	BLI8 - BLI1	Analog Inputs	Bi-Level (+) inputs 8 to 1	Fixed threshold bi-level monitor (comparator) positive (+) inputs 8 to 1 which are compared against either an internal 2.5V ±50mV threshold, or an external voltage between 0.1V and 4.9V on the BL_TH pin 43
52	AGND	Ground	Analog Ground	All AGND pins 13, 33, 41, 52, 67, and 99 must be used, connected together via a plane or split-plane on the PCB, and used for termination of analog signals only. Only join AGND to GND at pins 12 and 13
53 - 66	CH1 - CH14	Analog I/Os	ADC Inputs, Current Source	Sensor/signal acquisition inputs up to ±10V, selectable current source output
67	AGND	Ground	Analog Ground	All AGND pins 13, 33, 41, 52, 67, and 99 must be used, connected together via a plane or split-plane on the PCB, and used for termination of analog signals only. Only join AGND to GND at pins 12 and 13
68-98	CH15 - CH45	Analog I/Os	ADC Inputs, Current Source	Sensor/signal acquisition inputs up to ±10V, selectable current source output
99	AGND	Ground	Analog Ground	All AGND pins 13, 33, 41, 52, 67, and 99 must be used, connected together via a plane or split-plane on the PCB, and used for termination of analog signals only. Only join AGND to GND at pins 12 and 13
100 - 118	CH46 - CH64	Analog I/Os	ADC Inputs, Current Source	Sensor/signal acquisition inputs up to ±10V, selectable current source output

132L	Name	Pin Type	Pin Function	Description
119	SE_RTN	Analog Input	Sensor Return	Common return for single ended sensor/signal inputs. Typically connected to AGND, or a remote signal ground in the range ±10V for differential sensor/signal inputs. Tie to AGND if unused
120	GND	Ground	Digital and Power Ground	All GND pins 12, 120, and 132 must be used, connected together via a plane or split-plane on the PCB, and used for connection and termination of digital and power external components. Only join GND to AGND at pins 12 and 13
121	VCC	Power	Input Supply	Connect to the main power supply (11.4V to 16V). Bypass close to the pin with a 4.7µF capacitor to GND
122	PCP	Output	Charge Pump Flying Capacitor non-inverting	Flying capacitor positive node for the internal VEE inverting charge pump. If the internal VEE charge pump is used ($\overline{EXT\_VEE}$ pin 126 tied to +5V), connect a 0.47µF capacitor between this pin and the NCP pin. PCP swings between GND and VCC. If an external VEE supply is used ($\overline{EXT\_VEE}$ pin 126 tied to either GND or AGND), leave PCP open
123	NCP	Output	Charge Pump Flying Capacitor inverting	Flying capacitor negative node for the internal VEE inverting charge pump. If the internal VEE charge pump is used ($\overline{EXT\_VEE}$ pin 126 tied to +5V), connect a 0.47µF capacitor between this pin and the PCP pin. NCP swings between GND and VEE. If an external VEE supply is used ($\overline{EXT\_VEE}$ pin 126 tied to either GND or AGND), leave NCP open
124	VEE	Power	-10V to -16V Supply	If the internal inverting charge pump is used to generate VEE ($\overline{EXT\_VEE}$ pin 126 tied to +5V), bypass close to the pin with a 2.2µF capacitor to GND (not AGND) If an external VEE supply is used ($\overline{EXT\_VEE}$ pin 126 tied to GND), connect to an external voltage in the range -10V to -16V, and bypass close to the pin with a 2.2µF capacitor to either GND or AGND
125	-2V	Power	Internal -2V Supply	Bypass close to the pin with a 1µF capacitor to GND
126	$\overline{EXT\_VEE}$	Logic Input (1MΩ to +5V)	VEE Select	To use the internal inverting charge pump to generate VEE, tie $\overline{EXT\_VEE}$ to +5V. To use an external negative supply on VEE pin 124, tie $\overline{EXT\_VEE}$ to either GND or AGND
127	$\overline{EXT\_REF}$	Logic Input (1MΩ to +5V)	VREF Select	To use the internal +5V ±1% reference voltage, tie $\overline{EXT\_REF}$ to +5V. To use an external reference voltage on VREF pin 36, tie $\overline{EXT\_REF}$ to either GND or AGND
128	$\overline{TEST\_MODE}$	Factory Use	Test	Internally bonded test node. Connect to either GND or AGND
129	PROG SUPPLY	Factory Use	Test	Internally bonded test node. Connect to +5V pin 11
130	$\overline{SPI\_A}$	Logic Input (1MΩ to VDD)	SPI Interface A Enable	A falling edge on the $\overline{SPI\_A}$ input selects the SPI channel A interface and de-selects both the parallel interface and the SPI channel B interface. The SPI channel A interface remains selected while active low, or until a falling edge on the $\overline{SPI\_B}$ input over-rides and selects the SPI channel B interface instead. Select the parallel interface instead of one of the SPI channels by taking both the $\overline{SPI\_A}$ and $\overline{SPI\_B}$ inputs high
131	$\overline{SPI\_B}$	Logic Input (1MΩ to VDD)	SPI Interface B Enable	A falling edge on the $\overline{SPI\_B}$ input selects the SPI channel B interface and de-selects both the parallel interface and the SPI channel A interface. The SPI channel B interface remains selected while active low, or until a falling edge on the $\overline{SPI\_A}$ input over-rides and selects the SPI channel A interface instead. Select the parallel interface instead of one of the SPI channels by taking both the $\overline{SPI\_A}$ and $\overline{SPI\_B}$ inputs high
132	GND	Ground	Digital and Power Ground	All GND pins 12, 120, and 132 must be used, connected together via a plane or split-plane on the PCB, and used for connection and termination of digital and power external components. Only join GND to AGND at pins 12 and 13

5 QFP-208 Pin Numbering and Pin Descriptions

208L	Name	Pin Type	Pin Function	Description
3	VDD	Power	I/O Supply	Connect to the external logic controller's (FPGA, MCU) I/O power supply (2.25V to 5.5V) to set the I/O logic level for all logic I/Os. Bypass close to the pin with a 2.2µF capacitor to GND
5	CLK	Logic Input (1MΩ to GND)	ADC Clock	Connect a 125kHz to 500kHz clock to operate the ADC logic
6	$\overline{CE}$, or $\overline{SSA}$	Logic Input (1MΩ to VDD)	Chip Enable Slave Select A	Active low chip enable for the parallel interface ($\overline{SPI\_A}$ = $\overline{SPI\_B}$ = 1) Active low slave select for SPI channel A interface ($\overline{SPI\_A}$ = 0, $\overline{SPI\_B}$ = 1)
7	$\overline{OE}$, or CLKA	Logic Input (1MΩ to VDD)	Output Enable Clock A	Active low output enable (read) for the parallel interface ($\overline{SPI\_A}$ = $\overline{SPI\_B}$ = 1) Clock input for SPI channel A interface ($\overline{SPI\_A}$ = 0, $\overline{SPI\_B}$ = 1)
8	$\overline{WE}$, or MOSI_A	Logic Input (1MΩ to VDD)	Write Enable MOSI A	Active low write enable for the parallel interface ($\overline{SPI\_A}$ = $\overline{SPI\_B}$ = 1) Data input for SPI channel A interface ($\overline{SPI\_A}$ = 0, $\overline{SPI\_B}$ = 1)
10	A0, or MISO_A	Logic I/O (1MΩ to GND)	Address A0 MISO A	Register address bit A0 (LSB) for the parallel interface ($\overline{SPI\_A}$ = $\overline{SPI\_B}$ = 1) Data output for SPI channel A interface ($\overline{SPI\_A}$ = 0, $\overline{SPI\_B}$ = 1)
12	A1, or $\overline{SSB}$	Logic Input (1MΩ to VDD)	Address A1 Slave Select B	Register address bit A1 for the parallel interface ($\overline{SPI\_A}$ = $\overline{SPI\_B}$ = 1) Active low slave select for SPI channel B interface ($\overline{SPI\_A}$ = 1, $\overline{SPI\_B}$ = 0)
14	A2, or CLKB	Logic Input (1MΩ to GND)	Address A2 Clock B	Register address bit A2 for the parallel interface ($\overline{SPI\_A}$ = $\overline{SPI\_B}$ = 1) Clock input for SPI channel B interface ($\overline{SPI\_A}$ = 1, $\overline{SPI\_B}$ = 0)
16	A3, or MOSI_B	Logic Input (1MΩ to GND)	Address A3 MOSI B	Register address bit A3 for the parallel interface ($\overline{SPI\_A}$ = $\overline{SPI\_B}$ = 1) Data input for SPI channel B interface ($\overline{SPI\_A}$ = 1, $\overline{SPI\_B}$ = 0)
18	A4, or MISO_B	Logic I/O (1MΩ to GND)	Address A4 MISO B	Register address bit A4 (MSB) for the parallel interface ($\overline{SPI\_A}$ = $\overline{SPI\_B}$ = 1) Data output for SPI channel B interface ($\overline{SPI\_A}$ = 1, $\overline{SPI\_B}$ = 0)
20	+5V	Power	Internal +5V Supply	Bypass close to the pin with a 1µF capacitor to GND. Optionally overdrive pin with an external 5.5V ±0.25V supply which shuts down the internal regulator
21	GND	Ground	Digital and Power Ground	All GND pins 21, 186, and 206 must be used, connected together via a plane or split-plane on the PCB, and used for connection and termination of digital and power external components. Only join GND here at pin 21 to AGND at pin 23 as a star point
23	AGND	Ground	Analog Ground	All AGND pins 23, 51, 65, 82, 107, and 155 must be used, connected together via a plane or split-plane on the PCB, and used for termination of analog signals only. Only join AGND here at pin 23 to GND at pin 21 as a star point
25 - 30, 32, 33	D0 - D7	Logic I/O (1MΩ to GND)	Data Bus	Data bus D0 (LSB) to D7 (MSB) for the parallel interface
35	PTY	Logic I/O (1MΩ to GND)	Data Bus Parity	Even parity bit for the parallel interface combined address (A0 - A4), data (D0 - D7) bits, and the PTY signal. A write parity error sets the $\overline{ACK}$ output high
36	$\overline{ACK}$	Logic Output	Data Bus Write Acknowledge	Data write acknowledge output for the serial and parallel interfaces. $\overline{ACK}$ is active low to validate data (indicate no parity error) for serial or parallel writes to LX7730
38	$\overline{RESET}$	Logic I/O	System Reset	Active low input resets the LX7730 internal settings to the POR state. An optional capacitor to GND extends the internal reset time
40 - 42, 44	BLO1 - BLO4	Logic Outputs	Bi-Level Outputs 1 to 4	Output of fixed threshold bi-level monitor (comparator) input BLI1, BLI2, BLI3 and BLI4 at pins 81, 79, 78, and 76 respectively
45	BLO5	Logic Output	Bi-Level Output 5	Output of fixed threshold bi-level monitor (comparator) input BLI5 at pin 75 When the LX7730 is in reset state (either $\overline{RESET}$ pin 24 held active low, or Master Reset register 0 contains 0x6A) then output is instead VCC LVD status, Power Status Register 2 bit D2 (Table 18 on page 33)
47	BLO6	Logic Output	Bi-Level Output 6	Output of fixed threshold bi-level monitor (comparator) input BLI6 at pin 73 When the LX7730 is in reset state (either $\overline{RESET}$ pin 24 held active low, or Master Reset register 0 contains 0x6A) then output is instead VEE LVD status, Power Status Register 2 bit D1 (Table 18 on page 33)
48	BLO7	Logic Output	Bi-Level Output 7	Output of fixed threshold bi-level monitor (comparator) input BLI7 at pin 72 When the LX7730 is in reset state (either $\overline{RESET}$ pin 24 held active low, or Master Reset register 0 contains 0x6A) then output is instead +5V LVD status, Power Status Register 2 bit D0 (Table 18 on page 33)
50	BLO8	Logic Output	Bi-Level Output 8	Output of fixed threshold bi-level monitor (comparator) input BLI8 at pin 70 When the LX7730 is in reset state (either $\overline{RESET}$ pin 24 held active low, or Master Reset register 0 contains 0x6A) then output is instead Power On Enable status, which is high when the internal logic is ready after power-up
51	AGND	Ground	Analog Ground	All AGND pins 23, 51, 65, 82, 107, and 155 must be used, connected together via a plane or split-plane on the PCB, and used for termination of analog signals only. Only join AGND to GND at pins 21 and 23

208L	Name	Pin Type	Pin Function	Description
55	IREF1	Analog Input	Current Reference Bias Resistor	Connect a 20kΩ ±1% resistor from IREF1 to AGND pin 51 to set the internal reference current. Minimize the track length from the resistor to pin 55, and route a direct track to AGND pin 51. The voltage at IREF1 is 1.6V
56	ADC_ BIAS_IN	Analog Input	ADC Bias Resistor	Connect a 7.87kΩ, ±0.1% resistor from ADC_BIAS_IN to AGND pin 51 to set the internal precision current reference for the ADC. Minimize the track length to pin 56, and route a direct track to AGND pin 51. The voltage at ADC_BIAS_IN is 1.6V
58	VREF	Analog I/O	Internal VREF Output External VREF Input	To use the internal +5V ±1% reference voltage, connect a 1µF capacitor from VREF to AGND pin 51 and tie $\overline{\text{EXT\_REF}}$ pin 199 to +5V. To use an external reference voltage up to 5.5V, connect the external reference to VREF, and tie $\overline{\text{EXT\_REF}}$ pin 199 to either GND or AGND
59	DAC_P	Analog Output	10-Bit Current DAC (+) Output	Positive output for the 10-bit current DAC. The code range 0x000 to 0x3FF in the 10-bit DAC registers 14 and 15 (Table 30 on page 46) sources an increasing output current from 0 to 2mA. Terminate DAC_P with a resistor ≤1.5kΩ to AGND to develop a nominal output voltage ≤3V maximum at code 0x3FF. To assign the DAC_P output alternatively to internal use as the current source for the analog input multiplexer, set Current Mux Level register 5 bit D7 = 0 (Table 21 on page 38) and leave DAC_P open
61	DAC_N	Analog Output	10-Bit Current DAC (-) Output	Negative output for the 10-bit current DAC. The code range 0x000 to 0x3FF in the 10-bit DAC registers 14 and 15 (Table 30 on page 46) sources a decreasing output current from 2 to 0mA. Terminate DAC_N with a resistor ≤1.5kΩ to AGND to develop a nominal output voltage ≤3V maximum at code 0x000. If the 10-bit DAC is to be assigned to internal use as the current source for the analog input multiplexer (Current Mux Level register 5 bit D7 = 0), terminate DAC_N to either GND or AGND
62	ADC_IN	Analog I/O	AFE Output ADC Input	Optionally connect a redundant ADC here to monitor the final output from the complete AFE multiplexer-gain-filter system. Alternatively, to assert a unipolar input signal with 0 to 2V range directly to the ADC, disable the AFE by setting ADC Control register bit D0 = 1 (Table 24 on page 40)
64	TEST	Factory Use	Test	Internally bonded test node. Leave this pin floating
65	AGND	Ground	Analog Ground	All AGND pins 23, 51, 65, 82, 107, and 155 must be used, connected together via a plane or split-plane on the PCB, and used for termination of analog signals only. Only join AGND to GND at pins 21 and 23
67	ADC_ DAC_ OUT	Analog Input	DAC bias resistor	Connect a 158Ω, ±0.1% resistor from ADC_ DAC_OUT to AGND pin 65 to provide the precision load for the ADC's current output DAC. Minimize the track length to pin 67, and route a direct track to AGND pin 65. The voltage at ADC_DAC_OUT ranges from 1V minimum to 2V maximum during an ADC conversion, and returns to 0V at the end of the conversion
69	BL_TH	Analog Input	Bi-Level (-) external threshold input	Optional external negative (-) threshold voltage for the fixed threshold bi-level monitors (comparators) BL1 to BLI8 To use an external reference voltage between 0.1V and 4.9V on BL_TH, set bit B7 in the Bi-Level Bank register 12 (Table 28 on page 44) To use the internal 2.5V ±50mV threshold, clear bit B7 in the Bi-Level Bank register 12, and connect the BL_TH pin to either GND or AGND
70, 72, 73, 75, 76, 78, 79, 81	BLI8 - BLI1	Analog Inputs	Bi-Level (+) inputs 8 to 1	Fixed threshold bi-level monitor (comparator) positive (+) inputs 8 to 1 which are compared against either an internal 2.5V ±50mV threshold, or an external voltage between 0.1V and 4.9V on the BL_TH pin 69
82	AGND	Ground	Analog Ground	All AGND pins 23, 51, 65, 82, 107, and 155 must be used, connected together via a plane or split-plane on the PCB, and used for termination of analog signals only. Only join AGND to GND at pins 21 and 23
84, 85, 87, 88, 90, 91, 93, 94, 96, 97, 99, 100, 102, 103	CH1 - CH14	Analog I/Os	ADC Inputs, Current Source	Sensor/signal acquisition inputs up to ±10V, selectable current source output
107	AGND	Ground	Analog Ground	All AGND pins 23, 51, 65, 82, 107, and 155 must be used, connected together via a plane or split-plane on the PCB, and used for termination of analog signals only. Only join AGND to GND at pins 21 and 23

208L	Name	Pin Type	Pin Function	Description
109, 110, 112, 113, 115, 116, 118, 119, 121, 122, 124, 125, 127, 128, 130, 131, 133, 134, 136, 137, 139, 140, 142, 143, 145, 146, 148, 149, 151, 152, 154	CH15 - CH45	Analog I/Os	ADC Inputs, Current Source	Sensor/signal acquisition inputs up to ±10V, selectable current source output
155	AGND	Ground	Analog Ground	All AGND pins 23, 51, 65, 82, 107, and 155 must be used, connected together via a plane or split-plane on the PCB, and used for termination of analog signals only. Only join AGND to GND at pins 21 and 23
158, 159, 161, 162, 164, 165, 167, 168, 170, 171, 173, 174, 176, 177, 178, 179, 181, 182, 183	CH46 - CH64	Analog I/Os	ADC Inputs, Current Source	Sensor/signal acquisition inputs up to ±10V, selectable current source output
184	SE_RTN	Analog Input	Sensor Return	Common return for single ended sensor/signal inputs. Typically connected to AGND, or a remote signal ground in the range ±10V for differential sensor/signal inputs. Tie to AGND if unused
186	GND	Ground	Digital and Power Ground	All GND pins 21, 186, and 206 must be used, connected together via a plane or split-plane on the PCB, and used for connection and termination of digital and power external components. Only join GND to AGND at pins 21 and 23
187	VCC	Power	Input Supply	Connect to the main power supply (11.4V to 16V). Bypass close to the pin with a 4.7µF capacitor to GND
188	PCP	Output	Charge Pump Flying Capacitor non-inverting	Flying capacitor positive node for the internal VEE inverting charge pump. If the internal VEE charge pump is used ($\overline{\text{EXT\_VEE}}$ pin 197 tied to +5V), connect a 0.47µF capacitor between this pin and the NCP pin. PCP swings between GND and VCC. If an external VEE supply is used ($\overline{\text{EXT\_VEE}}$ pin 197 tied to either GND or AGND), leave PCP open
190	NCP	Output	Charge Pump Flying Capacitor inverting	Flying capacitor negative node for the internal VEE inverting charge pump. If the internal VEE charge pump is used ($\overline{\text{EXT\_VEE}}$ pin 197 tied to +5V), connect a 0.47µF capacitor between this pin and the PCP pin. NCP swings between GND and VEE. If an external VEE supply is used ($\overline{\text{EXT\_VEE}}$ pin 197 tied to either GND or AGND), leave NCP open
191	VEE	Power	-10V to -16V Supply	If the internal inverting charge pump is used to generate VEE ($\overline{\text{EXT\_VEE}}$ pin 197 tied to +5V), bypass close to the pin with a 2.2µF capacitor to GND (not AGND) If an external VEE supply is used ($\overline{\text{EXT\_VEE}}$ pin 197 tied to GND), connect to an external voltage in the range -10V to -16V, and bypass close to the pin with a 2.2µF capacitor to either GND or AGND
192	-2V	Power	Internal -2V Supply	Bypass close to the pin with a 1µF capacitor to GND
197	$\overline{\text{EXT\_VEE}}$	Logic Input (1MΩ to +5V)	VEE Select	To use the internal inverting charge pump to generate VEE, tie $\overline{\text{EXT\_VEE}}$ to +5V. To use an external negative supply on VEE pin 191, tie $\overline{\text{EXT\_VEE}}$ to either GND or AGND
199	$\overline{\text{EXT\_REF}}$	Logic Input (1MΩ to +5V)	VREF Select	To use the internal +5V ±1% reference voltage, tie $\overline{\text{EXT\_ REF}}$ to +5V. To use an external reference voltage on VREF pin 58, tie $\overline{\text{EXT\_ REF}}$ to either GND or AGND

208L	Name	Pin Type	Pin Function	Description
200	TEST_MODE	Factory Use	Test	Internally bonded test node. Connect to either GND or AGND
202	PROG SUPPLY	Factory Use	Test	Internally bonded test node. Connect to +5V pin 11
203	$\overline{\text{SPI\_A}}$	Logic Input (1MΩ to VDD)	SPI Interface A Enable	A falling edge on the $\overline{\text{SPI\_A}}$ input selects the SPI channel A interface and de-selects both the parallel interface and the SPI channel B interface. The SPI channel A interface remains selected while active low, or until a falling edge on the $\overline{\text{SPI\_B}}$ input over-rides and selects the SPI channel B interface instead. Select the parallel interface instead of one of the SPI channels by taking both the $\overline{\text{SPI\_A}}$ and $\overline{\text{SPI\_B}}$ inputs high
205	$\overline{\text{SPI\_B}}$	Logic Input (1MΩ to VDD)	SPI Interface B Enable	A falling edge on the $\overline{\text{SPI\_B}}$ input selects the SPI channel B interface and de-selects both the parallel interface and the SPI channel A interface. The SPI channel B interface remains selected while active low, or until a falling edge on the $\overline{\text{SPI\_A}}$ input over-rides and selects the SPI channel A interface instead. Select the parallel interface instead of one of the SPI channels by taking both the $\overline{\text{SPI\_A}}$ and $\overline{\text{SPI\_B}}$ inputs high
206	GND	Ground	Digital and Power Ground	All GND pins 21, 186, and 206 must be used, connected together via a plane or split-plane on the PCB, and used for connection and termination of digital and power external components. Only join GND to AGND at pins 21 and 23

Note: Pin numbers not shown in the table above are not bonded internally.

6 Absolute Maximum Ratings

Note: Stresses above those listed in “ABSOLUTE MAXIMUM RATINGS”, may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Parameter	Min	Max	Units
Main Power (VCC) to GND	-0.5	20	V
Logic Supply Voltage (VDD) to GND	-0.5	7	V
+5V (current internally limited)	-0.5	7	V
VEE (current internally limited)	-20	+0.5	V
FPGA or MCU system controller interface (pins 2 - pin 32) to GND	-0.5	7	V
Sensor Inputs (CH1 - CH64, SE_RTN) to GND (VCC = GND)	-20	20	V
Sensor Inputs (CH1 - CH64, SE_RTN) to GND (VCC = 11.4V to 16V)	-20	VCC + 2.5V	V
Bi-Level Inputs (BLI1 to 8) to GND	-10	10	V
Input clamp currents		5	mA
ADC_IN, DAC_N, DAC_P, $\overline{\text{RESET}}$, VREF, BL_TH, IREF1 to GND	-0.5	7	V
Operating Junction Temperature	-55	150	°C
Storage Junction Temperature	-65	160	°C
ESD Susceptibility (HBM, ML_STD883, Method 3015.7) Host system controller interface pins 2 to 10, 14 to 32, 126 to 128, 130, 131 Power pins 1, 11, 121 to 125, 129		1000	V
ESD Susceptibility (HBM, ML_STD883, Method 3015.7) Analog channel inputs CH1 to CH64 and BLI1 to BLI8 bi-level inputs		500	V
Peak Lead Solder Temperature (10 seconds)		260 (+0, -5)	°C

7 Operating Ratings

Note: Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics.

Parameter	Min	Max	Units
VCC	11.4	16	V
VDD	2.25	5.5	V
VEE (when externally applied)	-16	-10	V
+5V (current internally limited)	4.5	5.5	V
FPGA or MCU system controller Interface to GND	0	5.5	V
Sensor Inputs (CH1 - CH64, SE_RTN) to GND	-10	10	V
Bi-Level Inputs (BLI1 to BLI8) to GND	0	8	V
Input Clamp Currents		Fault condition ≤ 3	mA
ADC_IN, DAC_N, DAC_P, $\overline{\text{RESET}}$, VREF, BL_TH, IREF1 to GND	0	5.5	V
Current from Reference Voltage (VREF pin)	0	10	mA

8 Thermal Properties

Note: The θ_{JC} numbers assume no forced airflow. Junction temperature is calculated using $T_J = T_C + (PD \times \theta_{JC})$. In particular, θ_{JC} is a function of the PCB construction. The stated number below is for a four-layer board in accordance with JESD-51 (JEDEC).

Package	Thermal Resistance	Typ	Units
CQFP-132	θ_{JC}	10	°C/W
QFP-208		6.5	

9 Heatsink Recommendations

The top or the base of the plastic package can be used as the heat conducting surface. It is recommended to use the base of the ceramic package as the surface for conducting heat from the package. The metal package top is attached to the package body at the top of relatively thin cavity walls, and so has a much higher thermal resistance from the die than the base of the package. The leads can be formed to mount the part upside down if necessary. It is recommended to apply a thermal interface material between either package and its heat dissipater. The heat dissipater can be copper layers within a multilayer circuit board to spread heat laterally across the board, or a direct mounted dissipation element.

10 Electrical Characteristics

The following specifications apply over the operating ambient temperature of -55°C ≤ T_A ≤ 125°C except where otherwise noted with the following test conditions: VCC = 15V, VDD = 3.3V; R_{IREF} = 20kΩ ±1%; $R_{ADC\_BIAS\_IN}$ = 7.87kΩ ±0.1%; $R_{ADC\_DAC\_OUT}$ = 158Ω ±0.1%; $\overline{EXT\_VEE}$ open, $\overline{EXT\_REF}$ open; CH1 and CH2 are selected with CH2 grounded; CLK = 500kHz. Register 7 = b'001010xx' setting 10kHz anti-alias filtering. Typical parameters refer to T_J = 25°C. Positive currents flow into pins. Specifications apply to both LX7730 and LX7730L unless otherwise stated.

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
Internally Regulated Voltages						
V_{VEE}	VEE voltage	VCC - |VEE|	1.5	2.6	3	V
V_{+5V_NOM}	+5V voltage		4.75	5.00	5.25	V
V_{REF_NOM}	VREF voltage		4.95	5.00	5.05	V
V_{IREF}	IREF pin voltage	R_{IREF} = 20kΩ	1.568	1.600	1.632	V
Analog MUX						
$V_{CH\#\_DIFF}$	Differential Range	CH# to CH#, or CH# to SE_RTN	0		5	V
$V_{CH\#\_COMM}$	Common Mode Range	With V_{CH1} - V_{CH2} = 5V	-5		5	V
$V_{CH\#\_CLP\_P}$	Voltage Clamp (power applied)	Clamp Current = 1mA (into pin) (1)	VCC	16	17	V
		Clamp Current = 1mA (out of pin)	-23	-20	-16	
$V_{CH\#\_CLP}$	Voltage Clamp (VCC=VEE = 0)	Clamp Current = 1mA (into pin)	16	20	23	V
		Clamp Current = 1mA (out of pin)	-23	-20	-16	
All to V_{CH1}	CH# to CH# Isolation	CH1 and SE_RTN selected; CH2 to CH64 each with series 2kΩ to a 10kHz common source, CH1 with 2kΩ to GND. SE_RTN to GND		60		dB
V_{ADC_IN}	Settling Time	Including dead time			10	µs
$I_{CH\#\_BIAS}$	Bias Current	VCH1= -5V to 5V	-200	0	200	nA
$I_{CH\#\_LEAK}$	Leakage Current	VCH1= -5V to 5V; IC powered off	-200	0	200	nA
ISE_RTN	Bias Current	VSE_RTN= -5V to 5V	-200	0	200	nA
ISE_RTN	Leakage Current	VSE_RTN= -5V to 5V; IC powered off	-200	0	200	nA
Programmable Current Source						
$I_{CH\#\_FSC}$	Full scale current	Register 5 Use_IDAC bit D7 = 0, Register 5 Double bit D3 = 0	1880	1940	2000	µA
$I_{CH\#\_IN}$	Integral nonlinearity		-7.5	0	7.5	
$I_{CH\#\_DN}$	Differential nonlinearity		-7.5	0	7.5	
$I_{CH\#\_FSC\_DW}$	Full scale current	Register 5 Use_IDAC bit D7 = 0, Register 5 Double bit D3 = 1	3710	3830	3950	
$I_{CH\#\_IN\_DW}$	Integral nonlinearity		-15	0	15	
$I_{CH\#\_DN\_DW}$	Differential nonlinearity		-15	0	15	
$I_{CH\#\_DAC31}$	10-bit DAC = code 31	Register 5 Use_IDAC bit D7 = 1	290	300	310	
$I_{CH\#\_IN\_DAC}$	Integral nonlinearity 10-bit DAC codes 0 to 31	Register 5 Use_IDAC bit D7 = 1 Using {DAC_D9 : DAC_D0} codes in the Register 14 & 15 set from b'00000000 00' to b'00000111 11' (0 to 31)	-2	0	2	
$I_{CH\#\_DN\_DAC}$	Differential nonlinearity 10-bit DAC codes 0 to 31		-2	0	2	
Adjustable threshold Bi-Level MUX and 8-Bit DAC						
V_{DAC8_MAX}	Threshold DAC Max Output	Using code value of 255/255	4.95	5.00	5.05	V
V_{DAC8_LSB}	Threshold DAC LSB Weight			19.5		mV
V_{DAC8_IL}	DAC Integral Linearity	Using codes 20 to 240, best fit straight line	-1		1	LSB
V_{DAC8_OFF}	Offset error		-10		10	mV
V_{DAC8_DL}	DAC Differential Linearity		-0.75		0.75	LSB
$V_{CMP\#\_HYS}$	Hysteresis	Rising threshold = DAC output Falling threshold = (DAC output - $V_{CMP\#\_HYS}$)	75	112	150	mV
10-Bit Current DAC						
I_{DAC10_PFS}	DAC_P output full scale		-2.06	-2.00	-1.94	mA
I_{DAC10_NFS}	DAC_N output full scale			0		mA
I_{DAC10_LSB}	LSB Weight			-1.953		µA
I_{DAC10_IN}	Integral Nonlinearity		-5	0	5	LSB
I_{DAC_DN}	Differential Nonlinearity		-0.5	0	0.5	LSB
V_{DAC10_PN}	Compliance Range		0		3	V
T_{DAC10_SET}	Settling			0.2	1	µs

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
Instrumentation Amplifier with gain control (measured at ADC_IN)						
V_{IA_OFFSET}	Calculated by interpolation	Register 7 = b'00101000' (gain = 0.4, 10kHz); referenced to input; -55°C, 25°C	-2	13	25	mV
		Register 7 = b'00101000' (gain = 0.4, 10kHz); referenced to input; 125°C	-2	13	30	
		Register 7 = b'00101001' (gain = 2, 10kHz); referenced to input; -55°C, 25°C	-3	0	3	
		Register 7 = b'00101001' (gain = 2, 10kHz); referenced to input ;125°C	-3	0	4	
		Register 7 = b'00101010' (gain = 10, 10kHz); referenced to input; -55°C, 25°C	-3	0	3	
		Register 7 = b'00101010' (gain = 10, 10kHz); referenced to input; 125°C	-3	0	3	
V_{IA_GAIN}	$Gain = \frac{Vo2 - Vo1}{Vi2 - Vi1}$	Register 7 = b'00101000' (gain = 0.4, 10kHz)	0.398	0.400	0.402	$\frac{Vout}{Vin}$
		Register 7 = b'00101001' (gain = 2, 10kHz)	1.992	1.998	2.004	
		Register 7 = b'00101010' (gain = 10, 10kHz)	9.965	9.995	10.025	
T_{IA_RISE}	Output Step Rise Time 10% to 90%; Vo = 2Vpp	Register 7 = b'00101000' (gain = 0.4, 10kHz)	120	210	333	µs
		Register 7 = b'00101001' (gain = 2, 10kHz)	31	52	105	
		Register 7 = b'00101010' (gain = 10, 10kHz)	31	52	105	
P_{1_IA}	Pole frequency	Register 7 = b'000000xx' (400Hz)	360	600	1000	Hz
P_{2_IA}	Pole frequency	Register 7 = b'000101xx' (2kHz)	1.4	2.8	3.8	kHz
P_{3_IA}	Pole frequency	Register 7 = b'001010xx' (10kHz)	8.8	13.5	18.2	kHz
12-Bit Analog-to-Digital Converter (input at ADC_IN)						
V_{ADC_LR}	Linear Range	Input applied to ADC_IN	0		2.0	V
V_{ADC_FSE}	Full scale error	Best fit curve applied to full range	-2.5	0	2.5	%
V_{ADC_OFFSET}	Offset Error		-10	0	10	mV
V_{ADC_IN}	Integral nonlinearity	-55°C, 25°C	-6	0	6	LSB
		125°C	-7	0	7	
V_{ADC_DN}	Differential nonlinearity		-1	0	3	
I_{ADC_LEAK}	Leakage current	Register 7 = b'01000000' (analog front end is disabled); ADC not converting	-0.2	0	0.2	µA
t_{CONV}	Conversion Time	Cycles of CLK pin, guaranteed by design		13		clocks
t_{ACQU}	Acquisition Time			25		
t_{SAMP}	Sample Period			38		
Fixed Threshold Bi-Level Inputs						
$V_{BLI\#\_THRES}$	Threshold (Rising Voltage)	Internal reference	2.45	2.50	2.55	V
		With external 2.50V reference	2.45	2.50	2.55	
$V_{BLI\#\_HYS}$	Hysteresis	Rising threshold = $V_{BLI\#\_THRES}$ Falling threshold = ($V_{BLI\#\ THRES}$ - $V_{BLI\#\ HYS}$)	60	120	180	mV
$V_{BLI\#\_CLP\_P}$	Voltage Clamp (power applied)	Clamp Current = 1mA into pin	15	20	23	V
		Clamp Current = -1mA out of pin	-23	-20	-15	
$V_{BLI\#\_CLP}$	Voltage Clamp (power removed)	Clamp Current = 1mA into pin	15	20	23	V
		Clamp Current = -1mA out of pin	-23	-20	-15	
$I_{BLI\#\_BIAS}$	Bias Current	V_{BLI1} = 0V to 5V	-0.2	0	1.5	µA
$I_{BLI\#\_LEAK}$	Leakage Current	V_{BLI1} = 0V to 5V; IC powered off	-0.2	0	1.5	µA
$t_{BLI\#}$	Propagation Delay	High to low transition	0.3	0.8	1.3	µs
		Low to high transition	0.8	2.1	3.4	
V_{BL_TH}	BL_TH pin Voltage Range		0.1		4.9	V
I_{BL_TH}	Threshold pin Leakage	V_{BL_TH} = 0V to 5V	-0.2	0	2.0	µA

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
Logic Levels for FPGA or MCU System Controller Interface (pins 2 - pin 32) I/Os						
V_{EXT_VEE}, V_{EXT_VREF}	Program pins	Threshold Voltage	2.0	2.5	3.0	V
V_{LOG_IN}	Input Logic Threshold	Threshold Voltage	35	50	65	%VDD
V_{LOG_OUT}	Logic Output Levels	High Logic Level (4mA source)	VDD-0.3		VDD	V
		Low Logic Level (4mA sink)	0		0.3	
I_{LOG_IN}	Input currents	$\overline{SPI\_A}$, $\overline{SPI\_B}$: V_{LOG_IN} = 3.3V	-2	0	2	µA
		$\overline{SPI\_A}$, $\overline{SPI\_B}$: V_{LOG_IN} = 0V	-10	-4	-1.5	
		CQFP-32 pins 2, 6, 8 to 10, 14 to 21, 22 and QFP-208 pins 5, 10, 14, 16, 18, 25 to 30, 32, 33, 35. I/O as input, V_{LOG_IN} = 3.3V	1.5	4	10	
		CQFP-32 pins 2, 6, 8 to 10, 14 to 21, 22 and QFP-208 pins 5, 10, 14, 16, 18, 25 to 30, 32, 33, 35. I/O as input, V_{LOG_IN} = 0V	-2	0	2	
		CQFP-32 pins 3 to 5, 7 and QFP-208 pins 6, 7, 8 12. I/O as input, V_{LOG_IN} = 3.3V	-2	0	2	
		CQFP-32 pins 3 to 5, 7 and QFP-208 pins 6, 7, 8 12. I/O as input, V_{LOG_IN} = 0V	-10	-4	-1.5	
		$\overline{EXT\_VREF}$ or $\overline{EXT\_VEE}$ = 5V	-2	0	2	
		$\overline{EXT\_VREF}$ or $\overline{EXT\_VEE}$ = 0V	-12	-6	-1.5	
		$\overline{RESET}$ with power on enabled: V_{LOG_IN} = 3.3V	1.5	4	10	
		$\overline{RESET}$ with power on enabled: V_{LOG_IN} = 0V	-150	-66	-33	
Operating Current						
I_{VCC} (LX7730L)	VCC Operating Current	Register 1 = b'11011111'. All blocks enabled Register 7 = b'00xxxx00'. Gain = 0.4, CH1 = 0V. Internal VEE ($\overline{EXT\_VEE}$ pin tied to +5V)	38	61	78	mA
		Register 1 = b'11011111'. All blocks enabled Register 7 = b'00xxxx00'. Gain = 0.4 External VEE = -12V ($\overline{EXT\_VEE}$ pin tied to GND)		54	71	
I_{VCC} (LX7730)		Register 1 = b'11011111'. All blocks enabled Register 7 = b'00xxxx00'. Gain = 0.4, CH1 = 0V. Internal VEE ($\overline{EXT\_VEE}$ pin tied to +5V)	38	70	85	
See Section 12.1.3 on page 17 for power saving options						
I_{VCC} (LX7730L)	VCC Standby Current	Register 1 = b'0xxxxxxx'	2	4	6.75	mA
I_{VCC} (LX7730)					7.00	
I_{VEE}	VEE Current	Using external VEE source Positive current out of pin	-2	-4.7	-7.0	mA
I_{VDD}	VDD Current	All digital I/O pins static		0.9		mA
Under Voltage Detection						
V_{VCC}	VCC UVLO	Voltage rising; 200mV hysteresis	9.5	10	10.5	V
V_{VEE}	VEE UVLO	Voltage falling; 200mV hysteresis	-8.2	-8.0	-7.5	V
V_{+5V}	+5V UVLO	Voltage rising; 200mV hysteresis	3.9	4.15	4.4	V

(1)Voltage Clamp (power applied) 1mA into pin will clamp to the VCC supply

11 System Outline

The LX7730 circuitry comprises:

- A power supply and voltage reference (Section 12 on page 16)
- A reset circuit (Section 13 on page 19)
- Bi-level discrete monitors (BDM) comprising 16 comparators for monitoring analog inputs (Section 14 on page 20)
  - 8 comparators monitor a combination of the 64 analog inputs, and provide outputs via an internal register
  - 8 comparators monitor 8 dedicated analog input pins, and provide outputs on 8 dedicated digital output pins
- A 12-bit analog signal monitor (ASM) with programmable gain and filtering for a mix of up to 64 single-ended or 32 differential inputs (Section 15 on page 24)
- Two DACs for current-driving sensors and other purposes (Section 16 on page 28)
- Multiple digital interfaces (one parallel, two serial) to the system controller, with registers for configuration, operation, and monitoring (Section 17 on page 29)

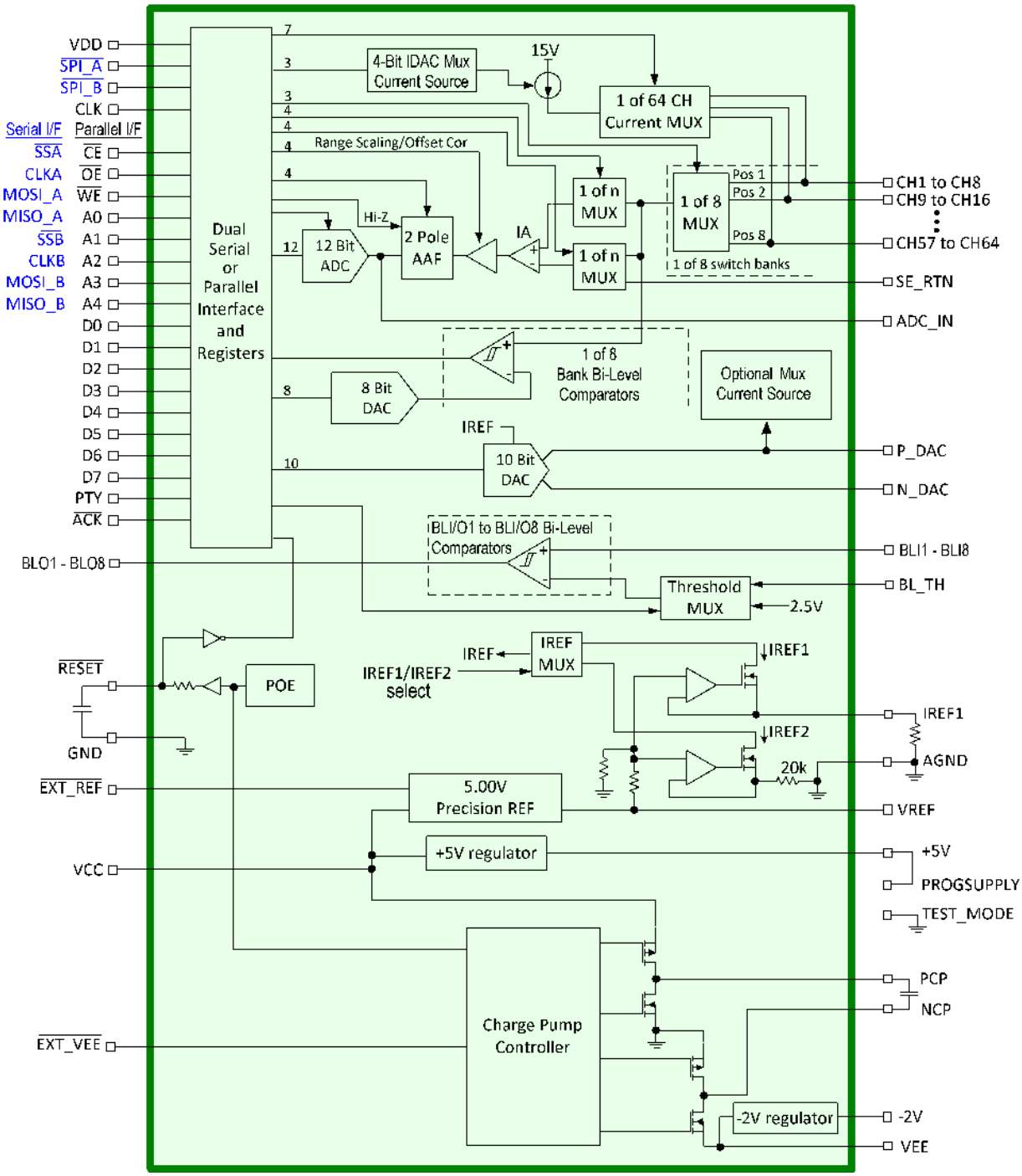


Figure 1. Block Diagram

12 Power Supplies, Bias Resistors, and Voltage Reference

12.1 Power Supply Configurations and Decoupling

The main input supply to the LX7730 is a single +11.4V to 16V supply, VCC, with a typical standby current of 4mA, and a typical operating current dependent on features enabled. A separate supply, VDD, drives the logic I/O and sets the I/O thresholds and voltages. On-chip power management (Figure 2) provides the following additional rails from VCC:

- A linear regulator provides a +5V ±0.25V supply from VCC, with the internal circuitry drawing 30mA typical current
- An inverting charge pump generates an unregulated negative supply, VEE, from VCC
  - An external -16V to -10V supply at 5mA typical may be used instead
- A linear regulator provides a -2V supply from VEE for internal biasing
- A precision +5V ±1% voltage reference
  - An external voltage reference (typically 5V or 5.12V) may be used instead

Figure 2 below and Table 6 on page 19 outline the power supply connections and provide decoupling capacitor recommendations, presuming low inductance capacitors such as MLCCs are used. Capacitance values can be reduced for supplies with tracking under a few inches to a bulk capacitor. Do not reduce the values for C4 and C5 in Figure 2.

See Table 6 on page 19 for details on the 3 resistors $R_{ADC\_BIAS\_IN}$, $R_{ADC\_DAC\_OUT}$, and R_{IREF1}. See section 0 on page 45 for details on the 10-bit DAC resistors on the DAC_P and DAC_N outputs.

The LX7730 won't be damaged by any of the permutations of VDD and/or VCC being down, with or without logic signals being applied up to 7V abs max. However, the LX7730's internal registers and operations are automatically reset by failure of either VCC or VDD, and data readback (serial or parallel) with return logic low and writes will be ignored as cold-spare behavior. If the host system detects a VCC and/or VDD failure, then after restoring the rail(s), the LX7730 should be re-configured as it would be for a normal cold start.

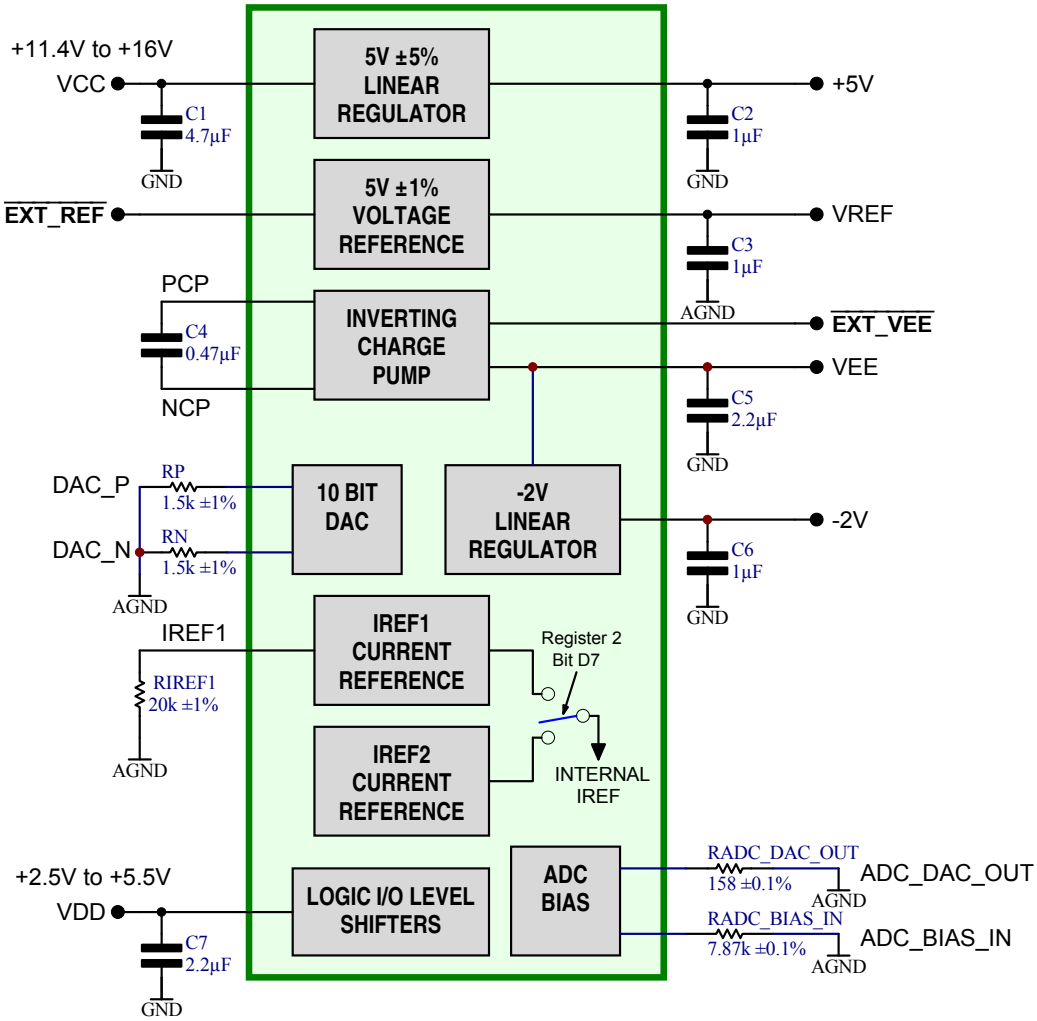


Figure 2. Power Supplies, Bias Resistors, and Voltage Reference

Table 1. Power Supplies Configuration and Decoupling Capacitors

Supply Pin	Voltage Range	Notes	Capacitor	Ground
VCC	11.4V to 16V	Main LX7730 supply	4.7µF	GND
+5V	4.5V to 5.5V	Internal +5V linear regulator from VCC used	1µF	GND
	5.25V to 6.0V	External +5.5V ±0.25V supply used, auto-disabling the internal regulator		
VREF	4.95V to 5.05V	Internal +5V ±1% reference voltage used ($\overline{\text{EXT\_REF}}$ pin tied to +5V)	1µF	AGND
	0V to 5.5V	External 5V or 5.12V reference voltage used ($\overline{\text{EXT\_REF}}$ pin tied to GND)	As required	
VDD	2.25V to 5.5V	External FPGA or MCU controller's I/O power supply	2.2µF	GND
VEE	-VCC to -10V	Internal inverting charge pump from VCC used ($\overline{\text{EXT\_VEE}}$ pin tied to +5V). Flying capacitor between PCP pin 122 and NCP pin 123 is 0.47µF	2.2µF	GND
	-16V to -10V	External VEE supply used ($\overline{\text{EXT\_VEE}}$ pin tied to GND)		AGND
-2V	-2V typical	Internal -2V linear regulator from VEE	1µF	GND

12.1.1 VCC Options

The LX7730 is typically operated from a system 12V or 15V nominal supply. A 12V nominal supply is recommended for monitoring and measuring signals on CH1 to CH64 up to ±8V, to minimize power consumption. A 15V nominal supply is recommended for monitoring and measuring signals over the full ±10V range. Note that the input voltage limit for the 8 bi-level comparators BLI1 to BL8 is ±8V maximum, independent of VCC.

If it is necessary to meet ECSS-E-ST-50-14C's fault voltage tolerance (V_{rft}) specification of ±17.5V for the CH1 to CH64 analog inputs when power is applied, then select VCC in the range 15V to 16V. The LX7730's fault voltage tolerance exceeds ±17.5V when powered down. See section 15.4 on page 28 for details of alternative protection approaches.

12.1.2 VEE Options

The main negative supply, VEE, is generated by an internal charge pump by default. This charge pump can be disabled to allow an external -16V to -10V supply to be used instead (Table 2).

Table 2. VEE Supply Methods

VEE Supply Method	$\overline{\text{EXT\_VEE}}$ pin	GND pin	Capacitor Between PCP pin and NCP pin (C4 in Figure 2)	Capacitor on VEE pin (C5 in Figure 2)
VEE internally generated by inverting charge pump from VCC	+5V	GND	0.47µF	2.2µF to GND
VEE externally supplied (-16V to -10V) directly to VEE pin	GND or AGND	GND or AGND	Not fitted. Leave PCP and NCP pins open	2.2µF to AGND

12.1.3 Power Saving Options

The internal 5V linear regulator accounts for about 30mA of the current draw from the VCC pin. The regulator itself contributes 210mW to 300mW to the dissipation from a 12V to 15V VCC supply by dropping 7V to 10V. This consumption can be removed by driving the 5V pin 11 with an external 5.5V ±0.25V supply, for example by a local buck regulator from the 12V to 15V VCC supply. The external supply is toleranced as 5.5V ±0.25V to as to be above the internal 5V linear regulator's 5.25V upper specification, and still below the 6V maximum pin rating. Maintaining a higher voltage disables the internal 5V linear regulator, which remains available as seamless backup should the external 5.5V supply suffer short term brownouts or even fail. If the external 5.5V supply is not derived from VCC, ensure that the 5.5V supply is never more than a Schottky diode drop higher than VCC.

Table 3 shows the trade-offs between VCC supply current, ADC INL, and ADC sample rate by adjusting the bias resistor on the ADC_BIAS_IN pin, the frequency of the ADC clock on CLK pin, and the ADC input voltage range used. Note that while the values given are worst case data taken from characterization, they are not production tested and therefore are not guaranteed.

Table 4 on page 18 shows the typical VCC supply current savings when various internal circuit blocks are disabled, and summarizes the functions affected and not affected.

Table 5 on page 19 provides typical current consumption for various power supply choices with ADC operating at 12.5ksps as follows:

- ADC input of 200mV at ADC_IN. Register 1 = 0xA1 (ADC on, analog front end off). Register 7 = 0x40
- ADC input of 200mV at CH1. Register 1 = 0xDF (ADC and complete analog front end on). Register 7 = 0x00 or 0x02

Some internal stages in the instrumentation amplifier, filter, and ADC use resistive loadings, so current consumption rises with signal amplitude at ADC_IN. The different signal amplitudes in Table 5 for gains of 0.4 and 10 highlights this effect.

The LX7730 settings used for the measurements in Table 5 are:

- VDD = 5V
- CLK = 500kHz, R_{IREF1} = 20kΩ, $R_{ADC\_BIAS\_IN}$ = 7.87kΩ, and $R_{ADC\_DAC\_OUT}$ = 158Ω
- Current Mux register 5 = 0x80, 10-bit DAC register 14 and 15 = 0x00 and 0x00 to disable both current DACs
- Current Source, Bank-Bi-Level, 10-Bit DAC, and BLI/BLO Bi-Level disabled in register 1
- Signal Conditioning Amplifier register 7 = 0x00 for gain = 0.4, 0x02 for gain = 10
- ADC Control register = 0x10 to configure the ADC to be auto-sampling at its fastest rate

Table 3. Operating Current Reduction by ADC Bias Reduction

$R_{ADC\_BIAS\_IN}$	$R_{ADC\_DAC\_OUT}$	CLK	Max Sample Rate	Input range V_{ADC_IN}	INL Max	I_{VCC}
7.87kΩ ±0.1%	158Ω ±0.1%	500kHz	13ksps	0V to 2V	±7 LSB	Factory tested specification
				0.2V to 1.8V	±4.5 LSB	No change in operating current
				0.4V to 1.6V	±3.25 LSB	
		250kHz	6.5ksps	0V to 2V	±8 LSB	
				0.2V to 1.8V	±4.5 LSB	
				0.4V to 1.6V	±3.25 LSB	
15kΩ ±0.1%	301Ω ±0.1%	250kHz	6.5ksps	0V to 2V	±8 LSB	7.1mA to 8.3mA reduction in operating current
				0.2V to 1.8V	±4.5 LSB	
				0.4V to 1.6V	±3 LSB	
30kΩ ±0.1%	604Ω ±0.1%	250kHz	6.5ksps	0V to 2V	±8.5 LSB	11.3mA to 12.2mA reduction in operating current
				0.2V to 1.8V	±5.75 LSB	
				0.4V to 1.6V	±4 LSB	
		125kHz	3.25ksps	0V to 2V	±8.75 LSB	
				0.2V to 1.8V	±4.5 LSB	
				0.4V to 1.6V	±3.25 LSB	

Table 4. Typical Analog Block Operating Currents and Wakeup Times

LX7730 Internal Block	Functions Available with Block Disabled	Enable/Disable Register	Typical Block Current (VCC = 15V)	Typical Wakeup Time (VCC = 15V)
CH1-CH64 Multiplexer & Instrumentation Amplifier with gain of 10	BLI1-8 bi-level comparators. ADC can acquire an external 2V full-scale signal on ADC_IN	Function Enable register 1 bits D3 & D6 (Table 17)	11 mA (ADC_IN = 0V)	4 µs
CH1-CH64 Multiplexer & Instrumentation Amplifier with gain of 2 or 0.4				464 µs
Multiplexer Current Source @ 2mA	All ADC acquisition system including multiplexer bi-level comparators, but excluding both current source types	Function Enable register 1 bit D5 (Table 17)	2 mA	1.4 µs
Bank Bi-Level Comparators	BLI1-8 bi-level comparators. ADC acquisition system except multiplexer bi-level comparators	Function Enable register 1 bit D4 (Table 17)	1 mA	-
Instrumentation Amplifier	BLI1-8 bi-level comparators. Multiplexer bi-level comparators. ADC can acquire a 2V full-scale signal on ADC_IN	Function Enable register 1 bit D3 (Table 17)	1 mA (ADC_IN = 0V)	40 µs
10-Bit DAC Current Source	All ADC acquisition system including multiplexer bi-level comparators. Alternate current source available via Current Mux Level register 5 (Table 21 on page 38)	Function Enable register 1 bit D2 (Table 17)	2 mA	44 µs
BLI1-8 Bi-Level Comparators	All ADC acquisition system including multiplexer bi-level comparators	Function Enable register 1 bit D1 (Table 17)	1 mA	1.8 µs
ADC	Acquisition system analog front end including multiplexer bi-level comparators. Output of analog front end is available at ADC_IN for acquisition by external ADC	Function Enable register 1 bit D0 (Table 17)	16 mA	7.2 µs

Table 5. Consumption for Various Power Supply Choices and ADC Operating Modes

VCC	VEE	+5V	I_{VCC}	I_{VEE}	$I_{+5.5V}$	ADC Mode
12.0V	Internal charge pump	Internal 5V linear regulator operating from VCC	29 mA	-	-	ADC_IN used (note 1)
			58 mA			CH1 used with gain = 0.4 (note 2)
			69 mA			CH1 used with gain = 10 (note 3)
15.0V			30 mA			ADC_IN used (note 1)
			61 mA			CH1 used with gain = 0.4 (note 2)
			72 mA			CH1 used with gain = 10 (note 3)
12.0V	External -12.0V		26 mA	2.1 mA	-	ADC_IN used (note 1)
			52 mA	4.7 mA		CH1 used with gain = 0.4 (note 2)
			63 mA	5.0 mA		CH1 used with gain = 10 (note 3)
15.0V			26 mA	2.2 mA		ADC_IN used (note 1)
			54 mA	4.9 mA		CH1 used with gain = 0.4 (note 2)
			64 mA	5.1 mA		CH1 used with gain = 10 (note 3)
12.0V	Internal charge pump	External 5.5V	6 mA	-	25 mA	ADC_IN used (note 1)
			29 mA		24 mA	CH1 used with gain = 0.4 (note 2)
			30 mA		40 mA	CH1 used with gain = 10 (note 3)
	External -12.0V		3 mA	2.2 mA	23 mA	ADC_IN used (note 1)
			24 mA	4.9 mA	29 mA	CH1 used with gain = 0.4 (note 2)
			24 mA	5.2 mA	39 mA	CH1 used with gain = 10 (note 3)

(1) 200mV signal at ADC_IN
(2) 80mV signal at ADC_IN
(3) 2V signal at ADC_IN

12.2 Bias Resistors

Table 6 lists the 3 bias resistors required for standard ADC operation (CLK = 500kHz). See Table 3 on page 18 for other options for ADC_BIAS_IN and ADC_DAC_OUT values. Minimize the track length from each resistor to its pin, and route a direct track from the other end of each resistor to the nearest AGND pin. Pages 3 and 2 show example layouts.

Table 6. Bias Resistors

Resistor Function	Resistance to AGND	Voltage Across Resistor	Resistor Dissipation
IREF1	20kΩ ±1%	1.6V static	0.13mW
ADC_BIAS_IN	7.87kΩ ±0.1%	1.6V static	0.33mW
ADC_DAC_OUT	158Ω ±0.1%	From 1V to 2V during an ADC conversion, otherwise 0V	25mW peak

13 Reset Pin and Power-On Reset

13.1 Reset Circuit

The LX7730's internal reset circuit (Figure 3 on page 20) uses a Power On Enable block to monitor the level of the +5V supply. The POE signal is low initially, pulling the $\overline{\text{RESET}}$ pin low through a 50k resistor. The logic level at the $\overline{\text{RESET}}$ pin is inverted to provide an internal RESET signal, which resets internal registers and user interfaces. The POE signal goes high once the +5V supply has stabilized, pulling the $\overline{\text{RESET}}$ pin high through the 50k resistor, releasing the reset condition. The LX7730 can also be reset using the Master Reset register 0 (Table 16 on page 33). Note that most system blocks are enabled on reset. Unwanted blocks may be disabled via the Function Enable register 1 (Table 17 on page 34).

An optional external capacitor from the $\overline{\text{RESET}}$ pin to GND provides further noise immunity. 1nF is recommended to provide a nominal 35µs delay.

$$\text{DELAY} = 35 \times C_{\text{RESET}}\ \mu s \text{ where } C_{\text{RESET}} \text{ is in nF}$$

Equation 1. $\overline{\text{RESET}}$ Pin Capacitor Delay

Once the LX7730 is out of reset and operating normally, the $\overline{\text{RESET}}$ pin remains pulled high internally through the 50kΩ resistor. This may be over-ridden by an external active low $\overline{\text{RESET}}$ pulse from a system controller, for example. An open-drain/collector output, a tri-stateable output, or a push-pull output through a series diode (anode to $\overline{\text{RESET}}$ pin) may be used. If a push-pull logic signal is used to drive the $\overline{\text{RESET}}$ pin directly, then this also over-rides the LX7730's Power On Enable signal. In this case the $\overline{\text{RESET}}$ pin must be pulsed low after power-up to ensure that the LX7730's logic is reset.

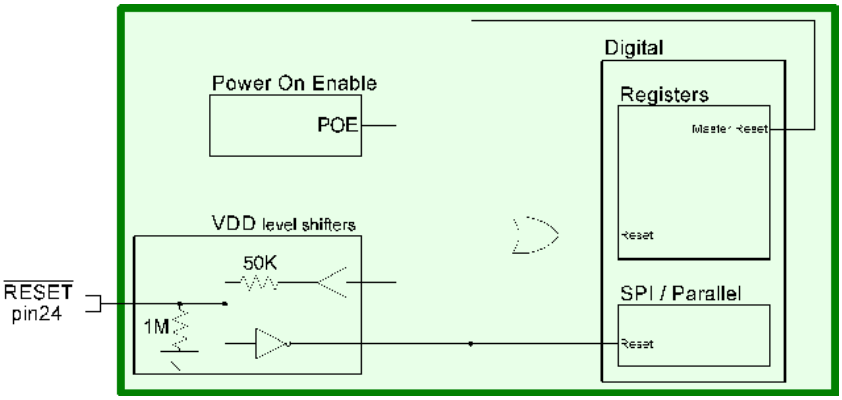


Figure 3. LX7730's Internal Reset Block Diagram

The LX7730 can also be put into the reset state by writing 0x6A to the Master Reset register 0 (Table 16 on page 33). Toggling the $\overline{\text{RESET}}$ pin low then high clears the Master Reset register 0 to 0x00 as part of the reset process.

14 Bi-level Discrete Monitors (BDM)

14.1 BDM Summary

There is a total of 16 voltage comparators available to detect changes on single ended signals:

- The 8 BLI/BLO bi-level comparators use dedicated input pins BLI1 to BLI8 and output pins BLO1 to BLO8
- The 8 bank bi-level comparators' inputs connect to a configurable combination of the 64 analog inputs CH1 to CH64 (see block diagram Figure 6 on page 22, and section 15 on page 24). The bank comparator outputs appear in the Bank Bi-Level Comparators Output Status register 13 (Table 29 on page 44).

Both sets of comparators are enabled by default on POR and after a reset. The BLI/BLO bi-level comparators may be disabled (to save power) by clearing Function Enable register 1 bit D1 = 0 (Table 9 on page 34). The bank bi-level comparators may be disabled by clearing bit D4 = 0 in the same register. Table 4 on page 18 shows typical analog block operating currents and wakeup times.

14.2 BLI/BLO Fixed Threshold Bi-Level Comparators

The 8 BLI/BLO bi-level comparator non-inverting inputs share a common trip threshold (Figure 5 on page 21). By default on POR or after a reset, the rising voltage threshold is 2.5V ±50mV, and the hysteresis is 120mV ±60mV on falling edges. Alternatively, an external trip threshold in the range 0.1V to 4.9V may be applied to the BL_TH pin, and this voltage is selected by setting B7 in the Bank Bi-Level register 12 (Table 28 on page 44).

The 4 BLO outputs BLO5 to BLO8 have an alternate system monitoring function when the LX7730 is in reset state (Table 7 below). The LX7730 is in reset state when either $\overline{\text{RESET}}$ pin 24 held active low (section 13 on page 19), or Master Reset register 0 (Table 16 on page 33) contains 0x6A.

Table 7. BLO1 to BLO8 Output System Monitoring Functions In Reset State

Output	Function when the LX7730 is in reset state
BLO1 - BLO4	Outputs of fixed threshold bi-level comparator inputs BL1, BL2, BL3 and BL4, using the default 2.5V threshold
BLO5	VCC LVD status, Power Status Register 2 bit D2 (Table 18 on page 33)
BLO6	VEE LVD status, Power Status Register 2 bit D1 (Table 18 on page 33)
BLO7	+5V LVD status, Power Status Register 2 bit D0 (Table 18 on page 33)
BLO8	Power On Enable status, which is high when the internal logic is ready after power-up

The input voltage limit for the 8 bi-level comparators BLI1 to BL8 is +8V maximum, +10V absolute maximum, independent of VCC. To protect these inputs beyond +8V, an external clamp circuit can be used (Figure 4 below). Over-voltage capability is limited by component power ratings. At ±17.5V, R1 dissipates 24mW/61mW, the Zener 15mW/2mW.

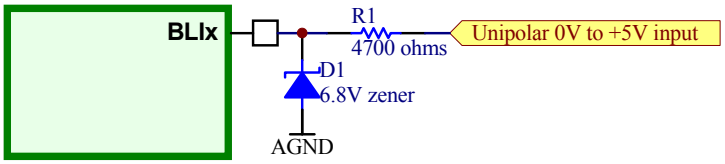


Figure 4. Bank Bi-Level Comparator Input Over-Voltage Clamp

The input protection clamps at each BLI input operate between the input and GND. The small (<1.5µA) leakage current drawn by a clamp provides a weak pulldown to each input, so an open BLI input will produce a corresponding low BLO output, presuming no noise coupling or other EMI effects at the input.

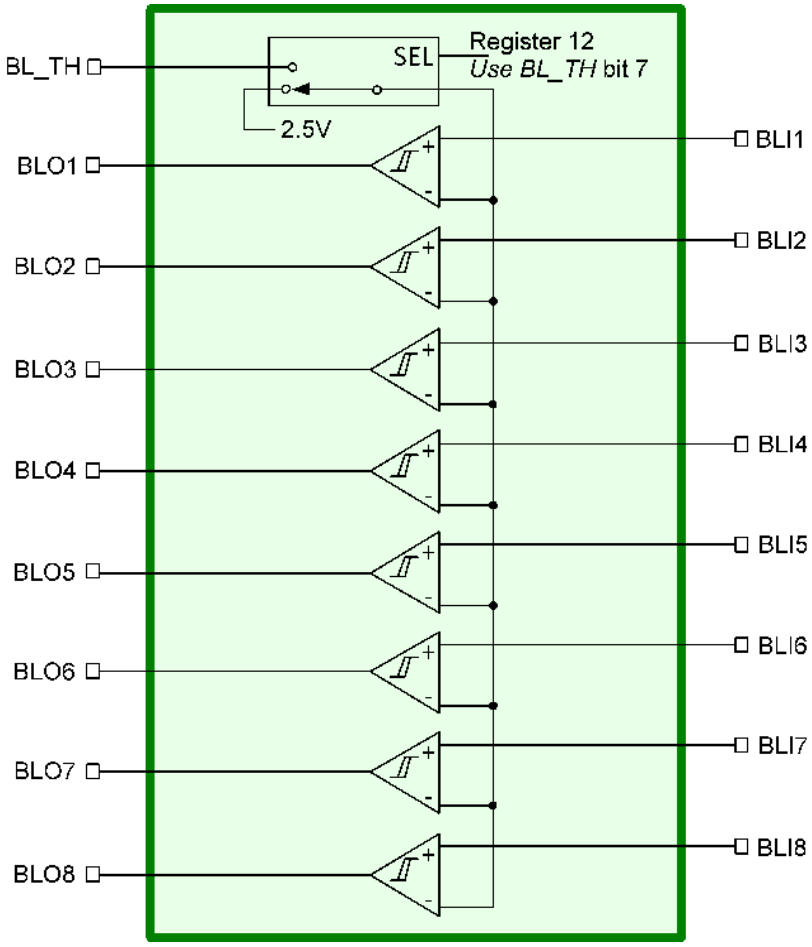


Figure 5. BLI-BLO Bi-Level Comparators Block Diagram

14.3 Bank Bi-Level Comparators

The 8 bank bi-level comparator non-inverting inputs share a common trip threshold set in the range 0 to 5V. This is set by an 8-bit DAC controlled by the 8-Bit Bank Bi-Level Comparators Threshold DAC register (Table 26 on page 42). The bank bi-level comparator outputs are available in the Bank Bi-Level Comparators Output Status register 13 (Table 29 on page 44). The bank bi-level comparators are sampled during the clock cycle that register 13 is read.

The bank bi-level comparator non-inverting inputs connect to 8 of the 64 analog inputs CH1 to CH64, which are also the inputs to the analog signal monitor (section 15 on page 24). The multiplexers for CH1 to CH64 are controlled by either the bank bi-level comparator circuitry or by the analog signal monitor. Either way, the bank bi-level comparators always receive 8 different inputs from CH1 to CH64.

14.3.1 Bank Bi-Level Comparators Control the Bank Input Multiplexers

The Bank Bi-Level Comparators Input Selection register 12 (Table 28 on page 44) selects which bank of 8 inputs are routed to the non-inverting inputs of the bank bi-level comparators, when register 12's En Sw bit D3 = 1. The register selects one of eight groups of consecutive inputs to be routed to the comparators. The groups are CH1 to CH8, CH9 - CH16, CH17 - CH24, CH25 - CH32, CH33 - CH40, CH41 - CH48, CH49 - CH56, and CH57 - CH64.

Figure 6 on page 22 shows a block diagram of bank bi-level comparators operating with register 12's En Sw bit D3 = 1. Here, the 8 bank multiplexers are controlled by a common 3-bit selection input.

The analog signal monitor can acquire single ended or differential signals from any combination of the eight inputs pre-selected by the setting in register 12.

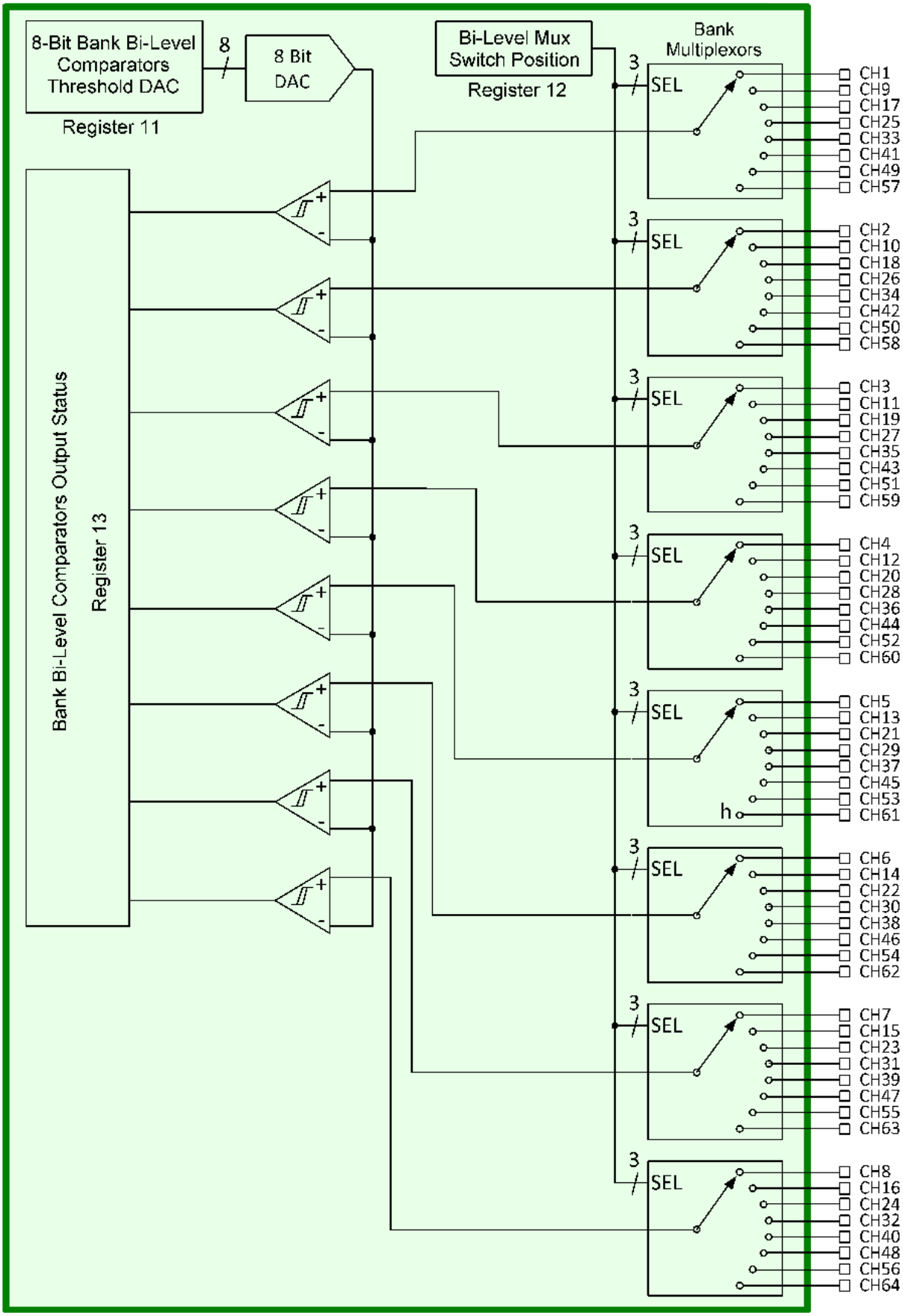


Figure 6. Bank Bi-Level Comparators Block Diagram

14.3.2 Analog Signal Monitor (ASM) Controls the Bank Input Multiplexers

When Bank Bi-Level Comparators Input Selection register 12's En Sw bit D3 = 0, the bank bi-level comparators are connected to inputs selected by Mux Channel Select registers 3 and 4 (Table 19 on page 36, Table 20 on page 37). In this mode, the 8 bank multiplexers are controlled individually, not by a common 3-bit selection input as in the case for Figure 6. Since the output of each of the 8 bank multiplexers routes to a bank bi-level comparator input, it is necessary to follow the ASM multiplexer input selection logic to determine the bank bi-level comparator inputs.

The Non-Inverting Mux Channel Select register 3 (Table 19 on page 36) selects which of the inputs CH1 to CH64 is routed by the analog multiplexer to the non-inverting input of the instrumentation amplifier. This selected input also routes to one of the bank bi-level comparators. The 3 bits [BD2:BD0] in register 3 select a multiplexer bank, and therefore selects which bank bi-level comparator the input is routed to also. Table 8 below identifies the bank bi-level comparator defined by Table 19.

Table 8: Bank Allocated by Register 3 for the Instrumentation Amplifier's Non-Inverting Input

Register Description	Register Address	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Non-Inverting Mux Channel Select register	**3 0x03**	**-**	**-**	**BD2**	**BD1**	**BD0**	**PD2**	**PD1**	**PD0**
Bank 1 selected. Register 3 selects input for bank comparator 1	3 0x03	x	x	0	0	0	x	x	x
Bank 2 selected. Register 3 selects input for bank comparator 2				0	0	1	x	x	x
Bank 3 selected. Register 3 selects input for bank comparator 3				0	1	0	x	x	x
Bank 4 selected. Register 3 selects input for bank comparator 4				0	1	1	x	x	x
Bank 5 selected. Register 3 selects input for bank comparator 5				1	0	0	x	x	x
Bank 6 selected. Register 3 selects input for bank comparator 6				1	0	1	x	x	x
Bank 7 selected. Register 3 selects input for bank comparator 7				1	1	0	x	x	x
Bank 8 selected. Register 3 selects input for bank comparator 8				1	1	1	x	x	x

The Inverting Mux Channel Select register 4 (Table 20 on page 37) selects which of the inputs CH1 to CH64 is routed by the analog multiplexer to the inverting input of the instrumentation amplifier. The 3 bits [BD2:BD0] in register 4 select a multiplexer bank, and therefore selects which comparator. As before, Table 9 below identifies the bank bi-level comparator defined by Table 20.

Table 9: Bank Allocated by Register 4 for the Instrumentation Amplifier's Non-Inverting Input

Register Description	Register Address	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Inverting Mux Channel Select register	**4 0x04**	**-**	**Use SE_RTN**	**BD2**	**BD1**	**BD0**	**PD2**	**PD1**	**PD0**
Bank 1 selected. Register 4 selects input for bank comparator 1	4 0x04	x	x	0	0	0	x	x	x
Bank 2 selected. Register 4 selects input for bank comparator 2				0	0	1	x	x	x
Bank 3 selected. Register 4 selects input for bank comparator 3				0	1	0	x	x	x
Bank 4 selected. Register 4 selects input for bank comparator 4				0	1	1	x	x	x
Bank 5 selected. Register 4 selects input for bank comparator 5				1	0	0	x	x	x
Bank 6 selected. Register 4 selects input for bank comparator 6				1	0	1	x	x	x
Bank 7 selected. Register 4 selects input for bank comparator 7				1	1	0	x	x	x
Bank 8 selected. Register 4 selects input for bank comparator 8				1	1	1	x	x	x

The remaining 6 or 7 bank bi-level comparators not assigned to a bank by register 3 and register 4 are routed to the inputs shown in Table 10 below. There will be 7 unassigned comparators if register 3 and register 4 select the same bank.

Table 10: Bank Bi-Level Comparator Inputs for Banks Not Assigned by Register 3 and Register 4

Unassigned Bank	Multiplexer Channel Routed to Bank Bi-Level Comparator
Bank 1	CH1
Bank 2	CH2
Bank 3	CH3
Bank 4	CH4
Bank 5	CH5
Bank 6	CH6
Bank 7	CH7
Bank 8	CH8

When the analog signal monitor is configured to acquire a single ended signal, then the inverting input of the instrumentation amplifier is normally either connected to GND or to the SE_RTN pin. In this case, register 4 isn't needed to select an input channel, and can used simply to select an input to one of the bank bi-level comparators.

15 12-bit Analog Signal Monitor (ASM)

The analog signal acquisition system comprises the following blocks (Figure 7):

- A 64-input multiplexer organized as 8 banks of 8-input multiplexers. A combination of up to 64 single-ended or 32 differential inputs from 64 package pins CH1 to CH64 are selectable
  - Differential signals in the range -5V to +5V are constrained that non-inverting and inverting input pairs must be connected to different banks. See section 15.1.1 on page 25 for details and a routing example
  - Positive-going single-ended signals in the range 0 to +5V can be used on any of the 64 inputs, and referred to either the internal GND or the SE_RTN pin. See section 15.1.2 on page 26 for details and a routing example
  - Negative-going single-ended signals in the range -5V to 0V are treated as differential signals, with the signal connected to the inverting input pin and the non-inverting input pin connected to the signal ground (AGND). See section 15.1.3 on page 27 for details and a routing example
- The 8 multiplexer bank outputs are also routed to the non-inverting inputs of the 8 bank voltage comparators, as discussed in section 14.3 on page 21
- One of two internal programmable current sources may be enabled and routed to any selected input to drive passive sensors, as discussed in section 16 on page 28
- An instrumentation amplifier with a choice of three fixed gain settings (x0.4, x2, or x10) to prescale single ended and differential input signals with ranges of 5V, 1V, or 200mV
- A 2-pole anti alias filter with a choice of three fixed pole settings (10kHz, 2kHz, or 400Hz)
- a 12-bit ADC with a 0V to 2V input range, with input accessible directly at the ADC_IN pin
  - The ADC input can be acquired by an external ADC for redundancy by monitoring ADC_IN
  - The ADC input can be driven directly via an external signal path when the anti-alias filter is put into Hi-Z using the Filter Off bit D6 in the Signal Conditioning Amplifier register 7 (Table 23 on page 39)

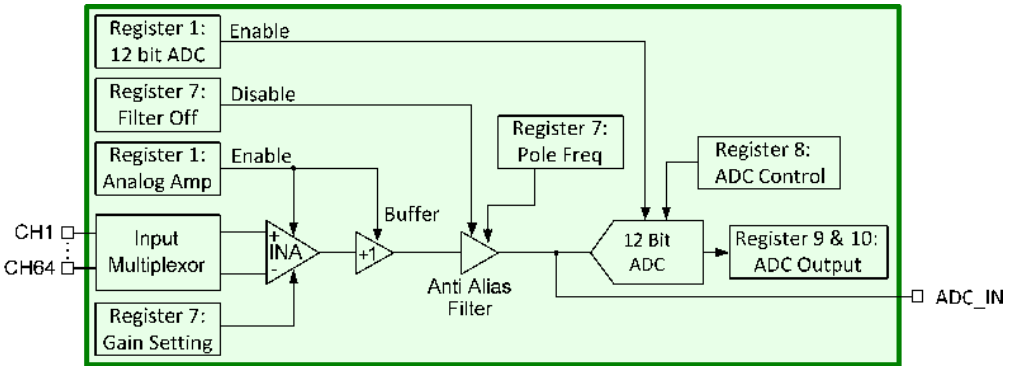


Figure 7. Analog Signal Monitor (ASM) Signal Chain

Various blocks in the analog signal acquisition system can be disabled to save power if they are not used through the Function Enable register (Table 9 on page 34). This is discussed in section 12.1.3 on page 17. Table 4 on page 18 shows typical analog block operating currents and wakeup times.

15.1 Configuring the Instrumentation Amplifier's Input Multiplexers

The input multiplexer selects an input for the instrumentation amplifier's non-inverting and inverting inputs. The ADC processes a unipolar voltage with a fixed range 0 to 2V, so the voltage at the instrumentation amplifier's non-inverting input is expected to be more positive than or equal to the voltage at the inverting input.

Figure 8 on page 25 shows the structure of the instrumentation amplifier multiplexers. The input channels CH1 to CH64 connect to 8 bank multiplexers. The eight bank multiplexer outputs route to a further multiplexer each for the non-inverting and inverting inputs.

The 8 bank multiplexers for CH1 to CH64 are controlled by either the analog signal monitor or by the bank bi-level comparator circuitry according to the setting of the En Sw bit D3 in the Bank Bi-Level register 12 (Table 28 on page 44). When Bank Bi-Level Comparators Input Selection register 12's En Sw bit D3 = 0, the bank bi-level comparators are connected to inputs selected by Mux Channel Select registers 3 and 4 (Table 19 on page 36, Table 20 on page 37). See section 14.3.1 on page 21 for details of inputs selected when the bank bi-level comparators manage the bank multiplexers.

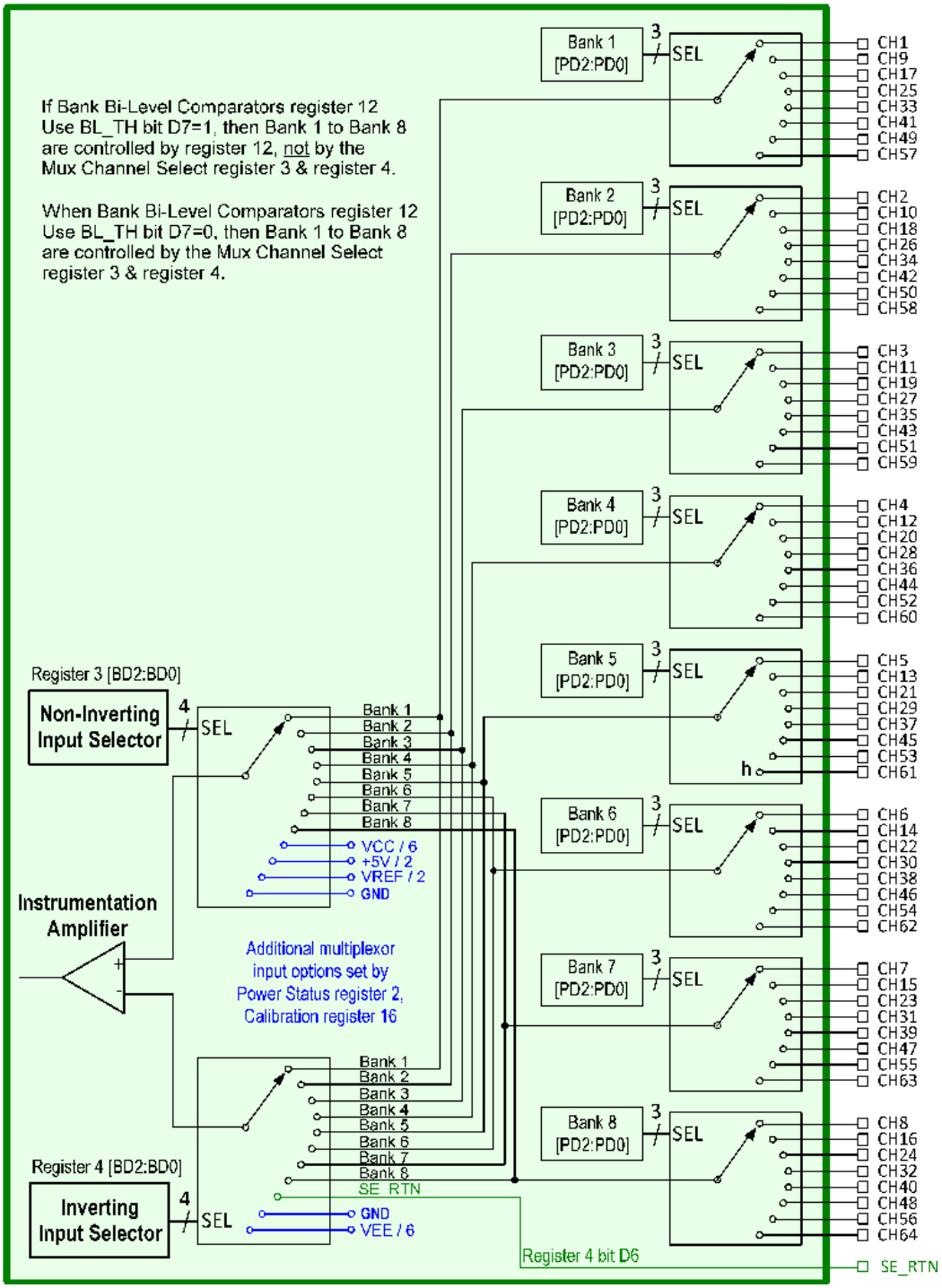


Figure 8. Instrumentation Amplifier Multiplexer Block Diagram

15.1.1 MULTIPLEXOR CONFIGURATION FOR DIFFERENTIAL SIGNALS

To acquire a differential signal in the range -5V to +5V, use the Mux Channel Select registers 3 and 4 (Table 19 on page 36, Table 20 on page 37) to select the non-inverting and inverting inputs respectively. Figure 9 on page 26 shows an example of the signal routings for a differential signal. Note that SE_RTN can be selected for a differential inverting input, freeing up a CH input for use an extra positive-going single-ended signal input.

The instrumentation amplifier expects the voltage at the non-inverting input to be more positive than the voltage at the inverting input, to provide a positive-going, unipolar voltage at its output in the range 0V to 2V for the ADC input. If the differential input signal polarity is reversed, the output of the instrumentation amplifier will clamp at 0V. The ADC result will be at or around 0x000 (depending on signal amplitude and offset errors). If the polarity of a differential signal to be acquired is unknown, measure it twice and swap the inputs between conversions. The correct result is the highest value.

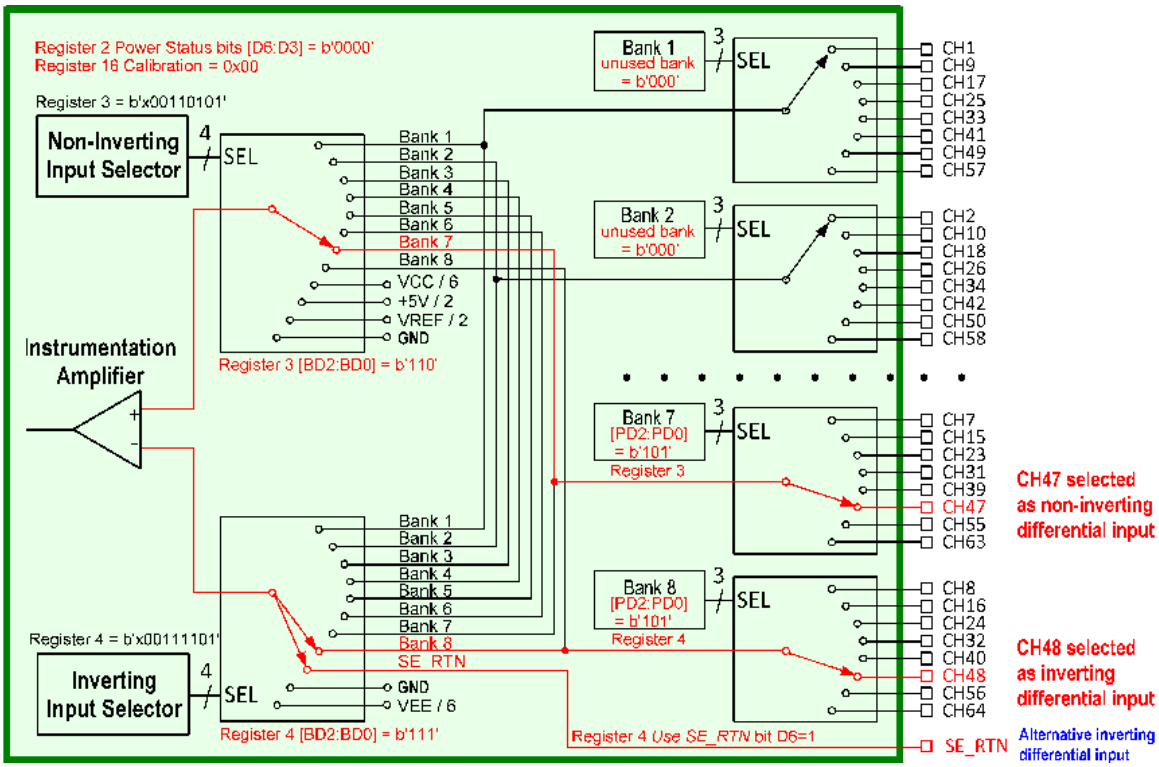


Figure 9. Example Selection of a Differential Input for Analog-to-Digital Conversion

15.1.2 MULTIPLEXOR CONFIGURATION FOR SINGLE-ENDED SIGNALS (POSITIVE-GOING)

To acquire a positive-going single-ended signal in the range 0V to 5V, configure the Non-Inverting Mux Channel Select register 3 (Table 19 on page 36) to select the non-inverting input. The inverting input can be connected to either internal AGND, or to an external GND via the SE_RTN pin. The selection of SE_RTN is made by the Inverting Mux Channel Select register (Table 20 on page 37). The selection of internal GND is made by the I GND bit D1 in the Calibration register (Table 32 on page 48). Figure 10 below shows an example of the signal routings for a positive-going single-ended signal.

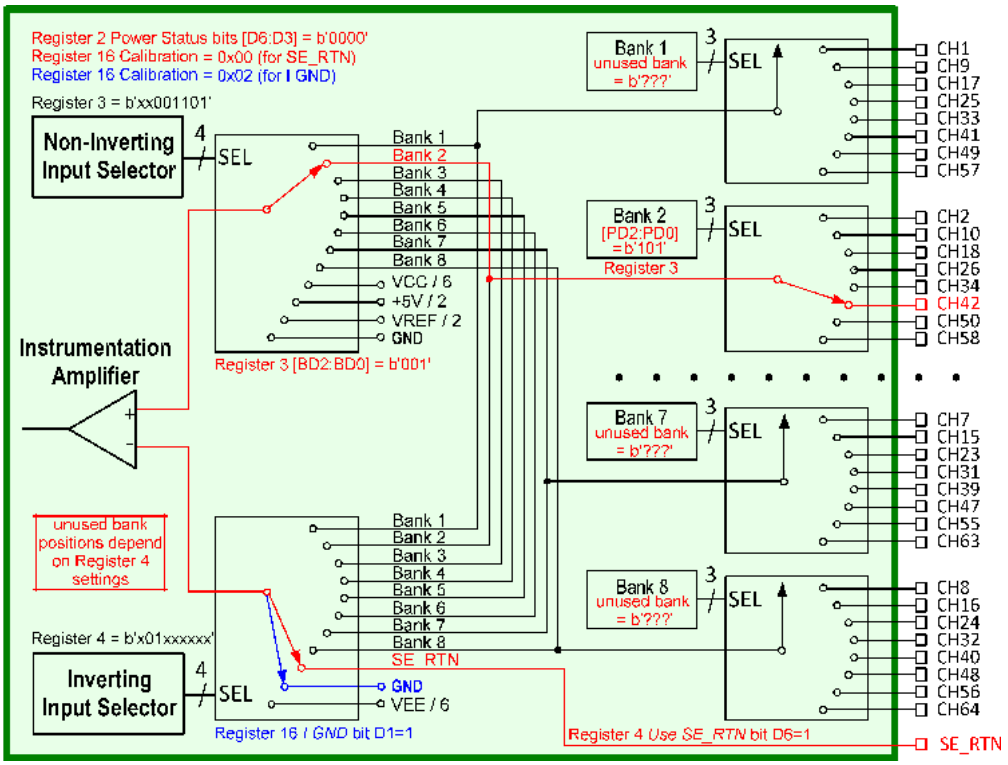


Figure 10. Example Selection of a Positive-Going Single-Ended Input for Analog-to-Digital Conversion

15.1.3 MULTIPLEXOR CONFIGURATION FOR SINGLE-ENDED SIGNALS (NEGATIVE-GOING)

Negative-going single-ended signals in the range -5V to 0V are treated as differential signals, with the non-inverting input externally connected to 0V, and the inverting input connected to the signal. The external GND connection is necessary because the non-inverting input cannot be connected to AGND internally or to the SE_RTN pin, unlike the inverting input.

Use the Mux Channel Select registers 3 and 4 (Table 19 on page 36, Table 20 on page 37) to select the non-inverting and inverting inputs respectively. Figure 11 below shows an example of the signal routings for one or more negative-going single-ended signals. In this example, CH1 is selected as the GND input, and is wired to AGND on the PCB. With the choice of CH1 made, any of the channel inputs in Bank 2 to Bank 8 may be selected for acquisition of negative-going single-ended signals. The remaining 7 inputs in Bank 1 are available for positive-going single-ended signals or differential signals as discussed in sections 15.1.2 and 15.1.1 respectively.

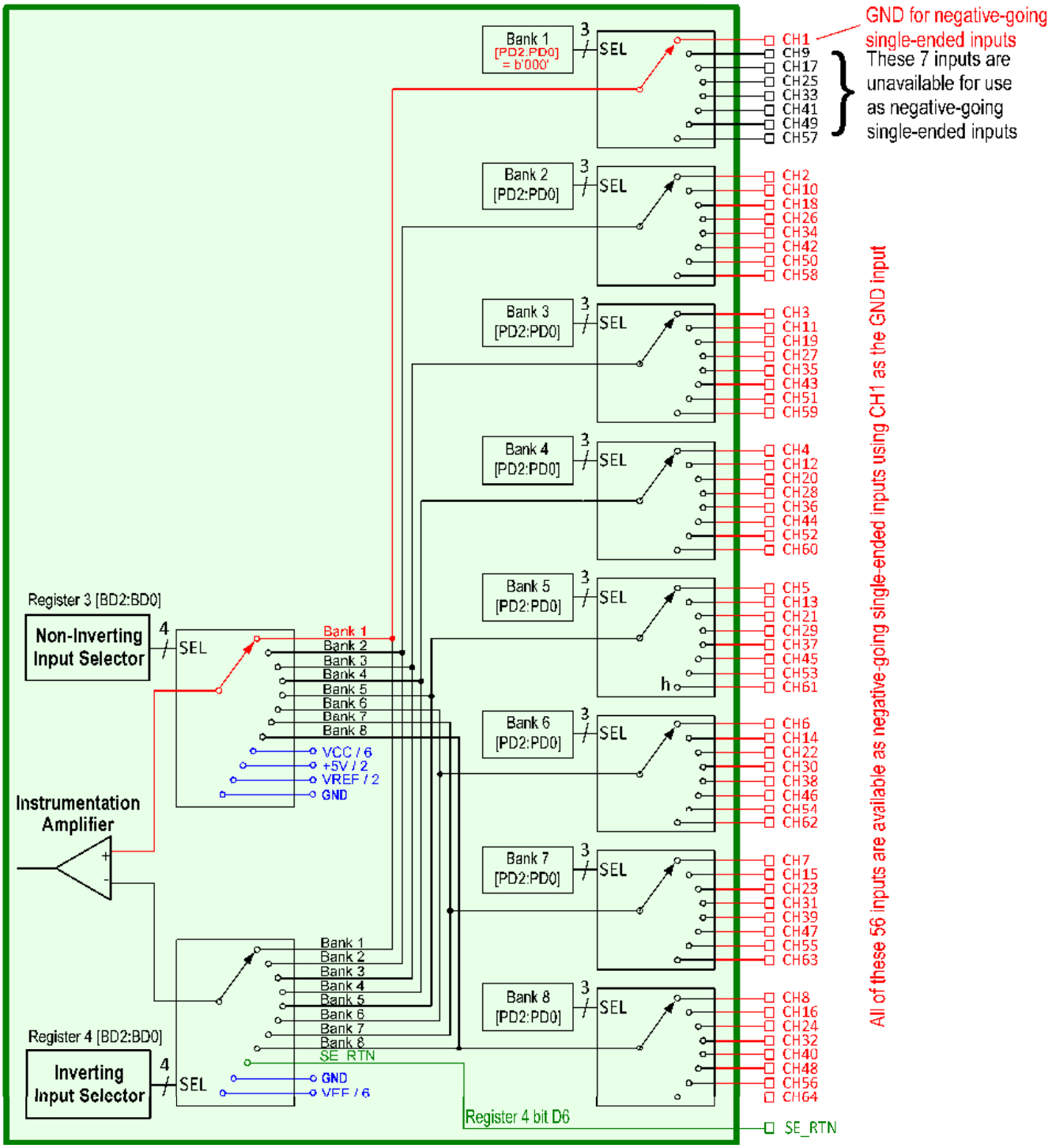


Figure 11. Example Selection of Negative-Going Single-Ended Inputs for Analog-to-Digital Conversion

15.2 Configuring the Instrumentation Amplifier and Anti Alias Filters

The instrumentation amplifier and anti alias filters are controlled by the Signal Conditioning Amplifier register 7 (Table 23 on page 39). The amplifier has a typical rise time (2V step, 10% to 90%) of 52µs with a gain of 10 or 2, and 210µs with a gain of 0.4. Allow settling time when switching between signals for acquisition.

15.3 Configuring the 12 Bit ADC

The ADC is a 12-bit SAR taking its acquisition timing from a 125kHz to 500kHz (typically 500kHz) clock at the CLK pin. See Table 3 on page 18 for details how operating current and INL can be reduced by adjusting the ADC's bias, input voltage range, and CLK frequency. The ADC is controlled by the ADC Control register 8 (Table 24 on page 40). See section 19.9 on page 40 for details of ADC internal timing and operation, plus configuration and control details.

15.4 CH1 to CH64 Input Over-Voltage Protection

The LX7730 is designed for cold redundancy, and the ADC inputs CH1 to CH64 can take ±20V with the LX7730 powered off (VCC=0V). This passes the ECSS-E-ST-50-14C's fault voltage tolerance (V_{rft}) specification of ±17.5V.

With the LX7730 powered on (VCC=12V or 15V usually), positive inputs start to clamp to VCC at about 1V above VCC, and this current must be maintained at no more than 3mA continuous, 5mA peak. Negative inputs can still go to -20V with VCC applied. An over-voltage of up to 1.5V above VCC is fine, as the input current is kept under 3mA continuous. To meet V_{rft} = ±17.5V input protection when powered up, either use VCC=16V or apply a series resistor to each input to be protected, with suitable value to limit the fault current to under 3mA. For inputs more than 1.5V above VCC, each input clamp appears as a resistance in the range 325Ω to 850Ω is series with 1.5V. For example, use 270Ω series resistance with VCC=15V ±5%. To divert input fault currents into GND instead of VCC, use an external clamp circuit (Figure 12). Over-voltage capability is limited by component power ratings. At ±17.5V, R1 dissipates 25mW, the Zener's 60mW/3mW.

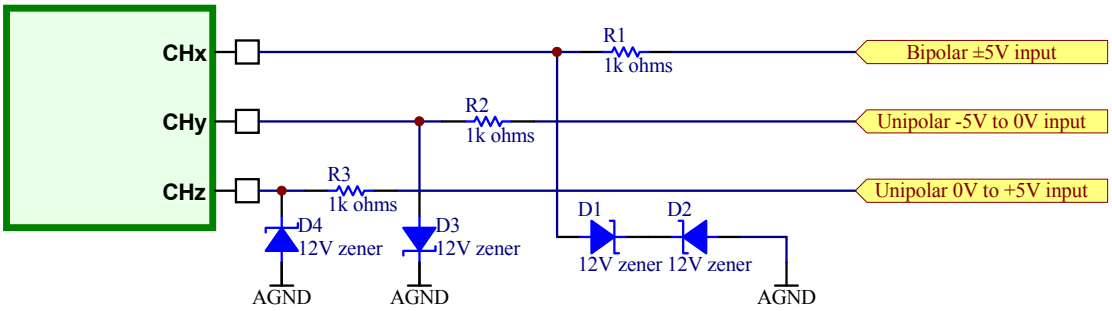


Figure 12. Channel Input Over-Voltage Clamp Circuits

16 Current Source DACs

The LX7730 includes two DACs intended for setting sensor source currents and generating general purpose output currents or voltages:

- A 4-bit DAC that can only be used to set a current source in the nominal range 242.5µA to 3830µA which drives a selected multiplexer input for passive sensor stimulation
- A 10-bit DAC that can either:
  - Drive a selected multiplexer input with a current source with 31 steps in the nominal range 9.7µA to 300µA (in place of the 4-bit DAC), or
  - Drive the DAC_P and DAC_N pins as a complementary output DAC with 1023 steps up to nominal full-scale outputs of 0 to 2mA and 2 to 0mA respectively. The output currents are typically converted to voltages with external resistors, with a maximum output compliance range of 0 to 3V. A 1.5kΩ resistor to AGND is recommended (as shown in the recommended layout in Section 1 on page 2 for DAC outputs used. This value provides a nominal 3V maximum at 2mA full scale. Output glitches on DAC code changes can be smoothed with a 1nF or higher capacitance fitted in parallel with each resistor. If one of the DAC outputs is not used, the resistor can be replaced by a direct connection to AGND.

16.1 Configuring the 4-Bit DAC

The 4-bit DAC is powered on or off by the Current Source Disable bit D5 in the Function Enable register 1 (Table 17 on page 34). The Current Mux Level register 5 (Table 21 on page 38) configures the 4-bit DAC. See Section 19.6 on page 37 for details. Note that the 4-bit DAC is disabled by default on reset, to avoid driving an inappropriate input.

16.2 Configuring the 10-Bit DAC

The 10-bit DAC is powered on or off by the 10-Bit DAC bit D2 in the Function Enable register 1 (Table 17 on page 34). See Section 0 on page 45 for configuration details in either of the two modes outlined above. Note that to update the DAC, the DAC LSB register 15 is written first. When the DAC MSB register 14 is written, the two LSBs in the DAC LSB register 15 are combined with the eight bits just stored in the DAC MSB register 14. This 10-bit word is used immediately to update the 10-bit DAC.

17 Digital Interfaces

The LX7730 includes a 25Mword/s parallel interface and two 12.5Mbit/s serial interfaces. All interfaces address the LX7730's full set of 32 internal registers (Table 15 on page 32). Only one interface can be active at a time, selected by the $\overline{SPI\_A}$ and $\overline{SPI\_B}$ input pins. The parallel interface is selected when $\overline{SPI\_A}$ = $\overline{SPI\_B}$ = 1. One of the serial interfaces is selected by the falling edge of either $\overline{SPI\_A}$ or $\overline{SPI\_B}$, regardless of the level of the other signal (Table 11). In this way, each serial interface offers full redundancy against a dead connection (stuck in any state) from the other serial interface.

$\overline{SPI\_B}$	$\overline{SPI\_A}$	Interface Selection
1	1	Parallel
0 or 1	1↓0	SPI_A selected; current parallel or serial transmission aborted
0↑1	0	SPI_A remains selected
1	0	
1↓0	0 or 1	SPI_B selected; current parallel or serial transmission aborted
0	0↑1	SPI_B remains selected
0	1	

Table 11. Parallel and Serial Interface Selection Logic

17.1 Using the Parallel Interface

The parallel interface is selected by setting the inputs $\overline{SPI\_A}$ = 1 and $\overline{SPI\_B}$ = 1. The parallel interface uses 5 register address pins A0 to A4, the 8 data pins D0 to D7, an active-low chip enable pin $\overline{CE}$ for reading and writing registers, and an active-low write enable pin $\overline{WE}$ for writing registers. The PTY and ACK pins provide mandatory data validation for every write (Table 12 on page 29). The LX7730 performs an even parity check on the 14-bit combination of the 5 address signals A0 to A4, the 8 data signals, and PTY itself. Parity is correct if there are an even number of 1s in this 14-bit word.

When the parallel bus is idle, the chip enable $\overline{CE}$, output enable $\overline{OE}$, and write enable $\overline{WE}$ are inactive high. Multiple devices may share the same address and data bus by providing individual $\overline{CE}$ and $\overline{OE}$ lines for each device.

Pin Name	Direction	Description	Function for Read	Function for Write
$\overline{CE}$	Input	Active low chip enable	Low	Low
$\overline{OE}$	Input	Active low output enable for read	Low	High
$\overline{WE}$	Input	Active low write enable	High	Low
A0 - A4	Input	Register address bit A0 (LSB) to A4 (MSB)	Register to read	Register to write
D0 - D7	I/O	Data byte D0 (LSB) to D7 (MSB)	Data from LX7730	Data to LX7730
PTY	I/O	Even parity bit (even number of 1s) for the combined address (A0 - A4), data (D0 - D7) bits, and the PTY signal. A write parity error sets the $\overline{ACK}$ output high	Parity bit from LX7730	Parity bit to LX7730
$\overline{ACK}$	Output	Data write acknowledge output. $\overline{ACK}$ is active low to validate a data write to LX7730 (indicate no parity error)	-	Parity $\overline{pass}$/fail

Table 12. Parallel Interface Selected by [$\overline{SPI\_A}$ = 1 and $\overline{SPI\_B}$ = 1]

17.1.1 Writing the LX7730 through the Parallel Interface

To write data to a register, $\overline{OE}$ remains high. In any desired sequence take $\overline{CE}$ low and set the desired register address A0 - A4, data byte D0 - D7, and parity bit PTY. Within 20ns of these signals stabilizing, the $\overline{ACK}$ output will go low to indicate that the parity check has passed. Pulse $\overline{WE}$ low for at least 15ns to latch the data into the register addressed (Figure 13). If the $\overline{ACK}$ output is high (parity error) when $\overline{WE}$ is pulsed low, then the data will not be latched into the LX7730. When writing multiple registers in a sequence, leave $\overline{CE}$ low for the duration of the repeated writes.

17.1.2 Reading the LX7730 through the Parallel Interface

To read data from a register, $\overline{WE}$ remains high. In any desired sequence take $\overline{CE}$ low and set the desired register address A0 - A4 to be read. 10ns minimum after these signals stabilizing, pulse $\overline{OE}$ low for at least 30ns to transfer the register's data to the data pins D0 - D7 (Figure 13). The data byte and parity bit will be valid within 10ns. When reading multiple registers in a sequence, leave $\overline{CE}$ low for the duration of the repeated reads.

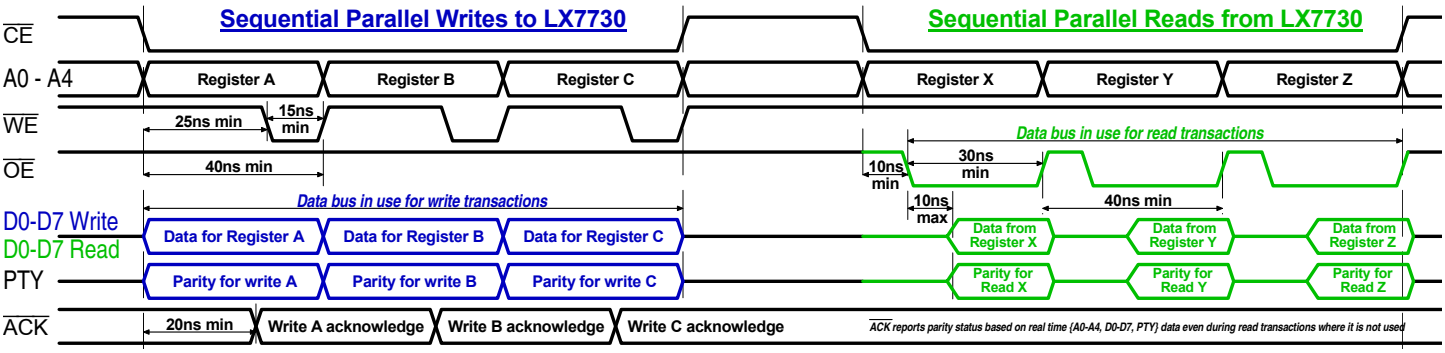


Figure 13. Parallel Data Timing for Successive Parallel Data Reads and Successive Parallel Data Writes

17.2 Using the Serial Interfaces

Serial interface A is selected by setting the inputs SPI_A = 0 and SPI_B = 1 (Table 14 below). Serial interface B is selected by setting the inputs SPI_A = 1 and SPI_B = 0 (Table 14 on page 31). The serial interface packs a R/$\overline{W}$ bit, the 5 register address bits A4 to A0, the 8 data bits D7 to D0, and a parity bit P into a 15-bit word in that order. The parity bit provides mandatory data validation for every write. The LX7730 performs an even parity check on this 15-bit word. Parity is correct if there are an even number of 1s in the word. Figure 14 shows the serial write timing diagram.

Note that an SPI transaction must be exactly 15 bits long between $\overline{SSA}$ or $\overline{SSB}$ falling at the start of the transaction and rising again at the end. The serial interface does not simply retain and process the last 15 bits of a transmission. Instead, the LX7730 decodes each transmission on the fly, and so arbitrary length transmissions cannot be accepted.

Figure 15 and Figure 16 show the serial read timing. Use an 80ns minimum CLKA and CLKB period (12.5MHz), with 32ns minimum high time and 10ns minimum low time. Setup/hold time on MOSI is 10ns/0ns before/after the rising edge of CLKx reaches logic 1. Data is valid on MISO 10ns after the falling edge of CLKx reaches logic 0, and should be sampled on the subsequent rising edge of CLKx.

Multiple devices may share the same serial B bus by providing individual $\overline{SPI\_B}$ lines for each device, and routing the $\overline{SSB}$, CLKB, MOSI_B, MISO_B as common signals to all devices. All device $\overline{SPI\_A}$ inputs remain high. When the bus is idle, all individual $\overline{SPI\_B}$ inputs and $\overline{SSB}$ are high. To access a target device using a shared SPI_B port:

1. Set $\overline{SPI\_B}$ = 0 for the target device to select it. The other $\overline{SPI\_B}$ inputs remain high
2. After a minimum 10ns, set $\overline{SSB}$ = 0
3. Execute the read or write sequence per Figure 14, Figure 15, and Figure 16
4. Set $\overline{SSB}$ = 1
5. To execute another read or write sequence on the same device, continue to step 2 ensuring $\overline{SSB}$ = 1 for ≥40ns
6. Otherwise, set $\overline{SPI\_B}$ = 1 so now the shared bus is in idle mode with all $\overline{SSB}$ and individual $\overline{SPI\_B}$ inputs high

Allowing multiple devices to share the same serial A bus is also possible, but is more complicated because the bus idle mode described above ($\overline{SPI\_A}$ = $\overline{SPI\_B}$ = 1) is also selecting the parallel interface, which shares control lines with the serial A bus. Contact factory for configuration details if sharing serial A bus is required.

Pin Name	SPI channel A interface selected by [$\overline{SPI\_A}$ = 0 and $\overline{SPI\_B}$ = 1]
$\overline{SSA}$	Active low slave select
CLKA	Clock input
MOSI_A	Data input
MISO_A	Data output
$\overline{ACK}$	Data write acknowledge output. $\overline{ACK}$ is active low to validate each data write to LX7730 (indicate no parity error). Parity is correct if there are an even number of 1s in the 15-bit data transmission, including the parity bit. $\overline{ACK}$ remains valid until the next falling edge of $\overline{SSA}$

Table 13. SPI Channel A Interface Selected by [$\overline{SPI\_A}$ = 0 and $\overline{SPI\_B}$ = 1]

Pin Name	SPI channel B interface selected by [$\overline{SPI\_A}$ = 1 and $\overline{SPI\_B}$ = 0]
$\overline{SSB}$	Active low slave select
CLKB	Clock input
MOSI_B	Data input
MISO_B	Data output
$\overline{ACK}$	Data write acknowledge output. $\overline{ACK}$ is active low to validate each data write to LX7730 (indicate no parity error). Parity is correct if there are an even number of 1s in the 15-bit data transmission, including the parity bit. $\overline{ACK}$ remains valid until the next falling edge of $\overline{SSB}$

Table 14. SPI Channel B Interface Selected by [$\overline{SPI\_A}$ = 1 and $\overline{SPI\_B}$ = 0]

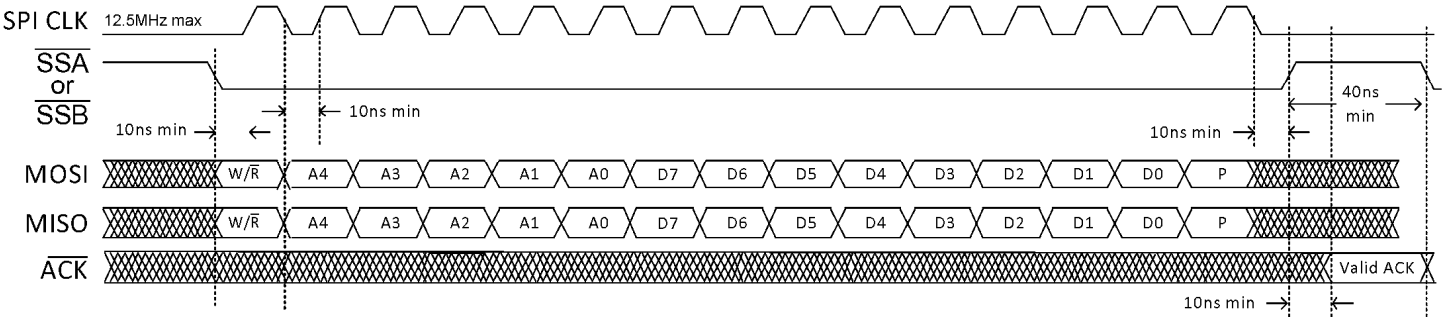


Figure 14. Serial Data Write Timing Diagram

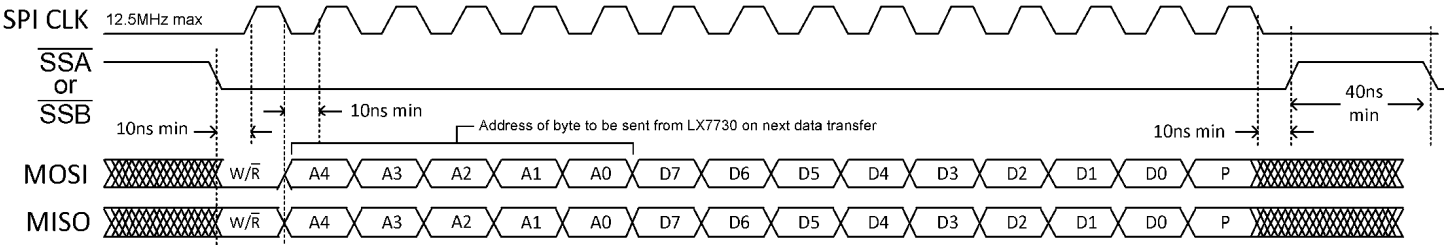


Figure 15. Serial Data Read Timing Diagram

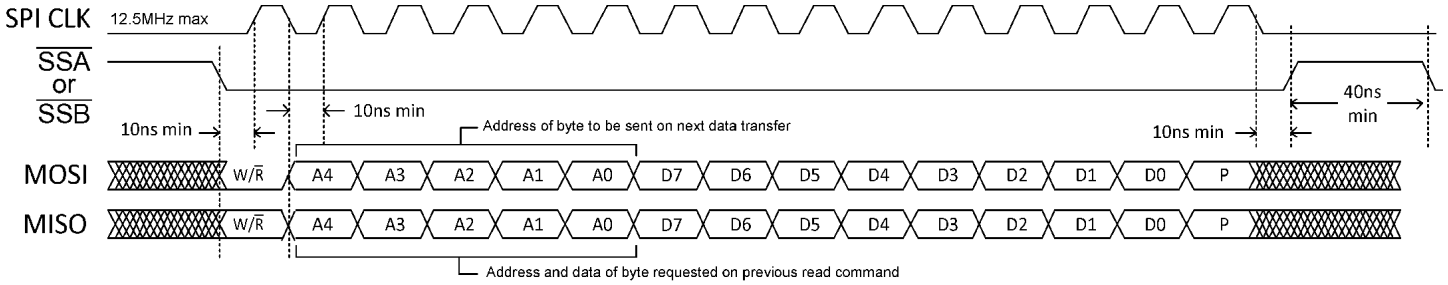


Figure 16. Serial Data Read Timing Diagram

18 Register Map

Register	Function	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Normal Operation Registers									
0 (0x00)	**Master Reset**	0x6A: reset mode. Any other value: normal operation							
1 (0x01)	**Function Enable**	Chip Enable	Sensor Mux	Current Source Disable	Bank Bi-Level	Analog Amplifiers	10-Bit DAC	BLI/BLO Bi-Level	12-Bit ADC
2 (0x02)	**Power Status**	Use IREF2	Monitor VCC	Monitor VEE	Monitor +5V	Monitor VREF	VCC LVD	VEE LVD	+5V LVD
3 (0x03)	**Non- Inverting Mux Channel**	-	-	Select Bank [BD2:BD0]			Select Position [PD2:PD0]		
4 (0x04)	**Inverting Mux Channel**	-	Use SE_RTN	Select Bank [BD2:BD0]			Select Position [PD2:PD0]		
5 (0x05)	**Current Mux Level**	Use IDAC	-	-	-	Double	Set Current		
6 (0x06)	**Current Mux Channel**	-	-	Select Channel					
7 (0x07)	**Signal Conditioning Amplifier**	-	Filter Off	2nd Pole Frequency		1st Pole Frequency		Amplifier Gain	
8 (0x08)	**ADC Control**	Auto Sample Rate Position [S2:S0]			Auto Conv	Data Ready	Busy	Start Conv	ADC_IN = HiZ
9 (0x09)	**ADC Result MSB**	ADC Result MSB [ADC_D11:ADC_D4]							
10 (0x0A)	**ADC Result LSB**	0	0	0	0	ADC Result LSB [ADC_D3:ADC_D0]			
11 (0x0B)	**8-Bit Bank Bi-Level Comparators Threshold DAC**	Threshold DAC [BI_D7:BI_D0]							
12 (0x0C)	**8-Bit Bank Bi-Level Comparators Input Selection**	Use BL_TH	-	-	-	EN BL Sw Pos	Select Banks Switch Position		
13 (0x0D)	**8-Bit Bank Bi-Level Comparators Output Status**	Comp-arator 7	Comp-arator 6	Comp-arator 5	Comp-arator 4	Comp-arator 3	Comp-arator 2	Comp-arator 1	Comp-arator 0
14 (0x0E)	**10-Bit DAC MSB**	DAC Setting MSB [DAC_D9:DAC_D2]							
15 (0x0F)	**10-Bit DAC LSB**	0	0	0	0	0	0	DAC_D1	DAC_D0
16 (0x10)	**Calibration**	IA Short	-	-	Cont Check	NP TEST	-	I GND	0
Trim Adjustment and Factory Calibration Registers									
17 (0x11)	**OTP**	-	-	-	-	-	-	OTP out select	OTP in select
18 (0x12)	**Trim 18**	cmux[2:0]			vref[4:0]				
19 (0x13)	**Trim 19**	vbgtc[3:0]				offs[3:0]			
20 (0x14)	**Trim 20**	vbg[4:0]					vtoi[4:2]		
21 (0x15)	**Trim 21**	vtoi[1:0]		osc[3:0]				ADCvtoi[4:3]	
22 (0x16)	**Trim 22**	ADCvtoi[2:0]			-	-	-	-	-
23 (0x17)	**Trim 23**	Io_dis	-	-	-	-	-	-	-
24 (0x18)	**Trim 24 (unused)**	-	-	-	-	-	-	-	-
25 (0x19)	**Trim 25 (unused)**	-	-	-	-	-	-	-	-
Unimplemented Registers									
26 (0x1A)	**Writes to these addresses are not stored and reads return 0x00**	0	0	0	0	0	0	0	0
27 (0x1B)		0	0	0	0	0	0	0	0
28 (0x1C)		0	0	0	0	0	0	0	0
29 (0x1D)		0	0	0	0	0	0	0	0
30 (0x1E)		0	0	0	0	0	0	0	0
31 (0x1F)		0	0	0	0	0	0	0	0

Note 1: Unused bits marked "-" are implemented but not used, and may be written and read with any values.
Note 2: Unused bits marked "0" are unimplemented. Writes are ignored, and the bits read back as 0.

Table 15. Register Map

19 Register Descriptions

19.1 Register address 0: Master Reset

When the Master Reset register 0 contains 0x6A, the LX7730 is in reset mode which sets all other registers to the power on reset (POR) state. Writes to the other registers are ignored in reset mode.

Toggling the $\overline{\text{RESET}}$ pin low then high also releases reset mode by clearing the Master Reset register 0 to 0x00.
See Section 13 on page 19 for operation of the $\overline{\text{RESET}}$ pin.

To perform a reset, first write 0x6A to Master Reset register 0. Then over-write any other value (such as 0xFF) to Master Reset register 0 to restore normal operation and allow register write access.

If Master Reset register 0 is maintained with value 0xFF (or any value except 0x6A or 0x00), then the LX7730's fundamental operational status can be checked by reading this register back:

- If Master Reset register 0 = 0xFF, then the LX7730 has not been reset by either the $\overline{\text{RESET}}$ pin being toggled or a power failure
- If Master Reset register 0 = 0x00, then either the LX7730 has been reset by some circumstance, or the power is currently down
  - If the Function Enable register 1 (Table 17 on page 34) reads back as 0xFF (the default after a reset event), then the LX7730 has been reset by some circumstance, and the power is up
  - If the Function Enable register 1 reads back as 0x00, then it is likely that the LX7730's power is currently down and so the system interface isn't working

Table 16: Register 0: Master Reset

Register Description	Register Address	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Reset LX7730 to Power-On Reset state	**0 0x00**	0	1	1	0	1	0	1	0
Set LX7730 for normal operation		Any value except b'01101010' (0x6A)							
Default register setting on POR or $\overline{\text{RESET}}$		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

19.2 Register address 1: Function Enable

The Function Enable register 1 provides the option to disable internal blocks for power saving; See Table 4 on page 18 for typical block operating currents and wakeup times. Clearing the Chip Enable bit D7 = 0 puts the LX7730 into standby mode with typical VCC consumption of 4mA.

Table 17. Register 1: Function Enable

Register Description	Register Address	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Function Enable register	**1 0x01**	**Chip Enable**	**Sensor Mux**	**Current Source Disable**	**Bank Bi-Level**	**Analog Ampli-fiers**	**10-Bit DAC**	**BLI/BLO Bi-Level**	**12-Bit ADC**
Default register setting on POR or RESET		**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
12-Bit ADC powered down The CH1-CH64 inputs, instrumentation amplifier, anti-alias filter, multiplexer bank bi-level comparators, BLI/BLO bi-level comparator inputs are unaffected. Output of analog front end is available at the ADC_IN pin for acquisition by external ADC	1 0x01	1	x	x	x	x	x	x	0
12-Bit ADC enabled									1
BLI/BLO Bi-Level Comparators powered down BLI1-8 are Hi-Z. The multiplexer bank bi-level comparators are unaffected		1	x	x	x	x	x	0	x
BLI/BLO Bi-Level Comparators enabled								1	
10-bit DAC powered down DAC_P & DAC_N outputs are Hi-Z		1	x	x	x	x	0	x	x
10-bit DAC enabled							1		
Instrumentation Amplifier powered down The instrumentation amplifier driving the anti-alias filter is powered down, so multiplexer inputs will not reach the ADC. The multiplexer bank bi-level comparators are not affected. The ADC can acquire an external signal on the ADC_IN pin after powering down the anti-alias filter by setting Signal Conditioning Amplifier register 7-bit D6 (Table 23 on page 39)		1	x	x	x	0	x	x	x
Instrumentation Amplifier enabled						1			
Bank Bi-Level Comparators powered down The multiplexer bank bi-level comparators are disabled. CH1-CH64 inputs, ADC, BLI/BLO bi-level comparator are unaffected	1 0x01	1	x	x	0	x	x	x	x
Bank Bi-Level Comparators enabled			1		1				
Multiplexer Current Source enabled The current source is selected and configured by the Current Mux Level register 5 (Table 21 on page 38). The current source is directed to the input channel CH1 to CH64 selected by the Current Mux Channel Selection register 6 (Table 22 on page 39)		1	x	0	x	x	x	x	x
Multiplexer Current Source powered down The 10-bit DAC may still be used to drive its DAC_P & DAC_N outputs if enabled by setting bit D2 = 1 and clearing bit D7 = 0 in the Current Mux Level register 5 (Table 21 on page 38)				1					
CH1-CH64 Multiplexer powered down (disabling Multiplexer Bank Bi-Level Comparators also) CH1-CH64 inputs are Hi-Z. The BLI/BLO bi-level comparator inputs are unaffected		1	0	x	x (0 saves power)	x	x	x	x
CH1-CH64 Multiplexer enabled			1		x				
Standby mode Digital interface is operational. CH1-CH64 & BLI1-BLI8 inputs, and DAC_N & DAC_P outputs are Hi-Z		0	x	x	x	x	x	x	x
Operating mode The LX7730 is in normal operation, with optional analog blocks disabled per the [D6-D0] settings. Typical wakeup time from sleep mode is 333µs		1	Select which analog blocks are operational. See Table 4 on page 18 and Table 5 on page 19 for typical block operating currents and wakeup times						

19.3 Register address 2: Power Status

The Power Status register 2 provides the option to check for a LVD condition or to monitor the power rails. There is also a bit for selection of the redundant IREF pin.

The Monitor VCC, Monitor VEE, Monitor +5V, and Monitor VREF bits [D6:D3] can be used to route one of these 4 power supply voltages, with attenuation, directly to the ADC. This over-rides the settings of both the Non-Inverting Mux Channel Select register 3 (Table 19 on page 36) and the Inverting Mux Channel Select register 4 (Table 20 on page 37).

When selecting Monitor VREF, note that when VREF is also being used as the reference for the ADC, then the ADC result will be ratiometric. After setting the signal conditioning amplifier gain to 0.4 (Table 23 on page 39), the Monitor VREF signal will appear at the ADC input as (0.4 x VREF/2). Since the internal reference to the ADC is (0.4 x VREF = 2V), the ADC conversion will always appear as nominally half-scale (0x800). In this case, VREF must be monitored relative to a known external voltage such as VCC.

The Calibration register 16 (Table 33 on page 48) offers more over-rides to the instrumentation amplifier inputs. However, bits [D6:D3] in register 2 below have priority over Calibration register settings.

Table 18: Register 2: Power Status

Register Description		Register Address	Register Data							
			D7	D6	D5	D4	D3	D2	D1	D0
Power Status register		**2 0x02**	**Use IREF2**	**Monitor VCC**	**Monitor VEE**	**Monitor +5V**	**Monitor VREF**	**VCC LVD**	**VEE LVD**	**+5V LVD**
Default register setting on POR or RESET			**0**	**0**	**0**	**0**	**0**	**x**	**x**	**0**
+5V rail is more positive than +4.15V LVD threshold		2 0x02	x	x	x	x	x	x	x	0
+5V rail is more negative than +3.95V LVD threshold										1
VEE rail is more negative than -8.2V LVD threshold			x	x	x	x	x	x	0	x
VEE rail is more positive than -8V LVD threshold									1	
VCC rail is more positive than +10V LVD threshold			x	x	x	x	x	0	x	x
VCC rail is more negative than +9.8V LVD threshold								1		
Instrumentation amplifier's non-inverting input voltage is over-ridden to be:	**Instrumentation amplifier's inverting input voltage is over-ridden to be:**		**x**	**Bits [D6:D3] over-ride the settings of the Non-Inverting and Inverting Mux Channel Select registers 3 and 4**				**x**	**x**	**x**
No action when [D6:D3] = b'0000'			x	0	0	0	0	x	x	x
VREF pin divided by 2	AGND		x	0	0	0	1	x	x	x
+5V pin divided by 2	AGND		x	0	0	1	x	x	x	x
AGND	VEE pin divided by 6		x	0	1	x	x	x	x	x
VCC pin divided by 6	AGND		x	1	x	x	x	x	x	x
Internal reference current is set by a 20kΩ ±1% resistor from IREF1 pin to AGND			0	x	x	x	x	x	x	x
Internal reference current is set by an internal resistor, IREF2, instead of any resistor at IREF1 pin			1							

19.4 Register address 3: Non-Inverting Mux Channel Select

The Non-Inverting Mux Channel Select register 3 selects which of the inputs CH1 to CH64 is routed by the analog multiplexer to the non-inverting input of the instrumentation amplifier.

The [BD2:BD0] and [PD2:PD0] bits select an input channel. The 3 bits [BD2:BD0] select a multiplexer bank, and the 3 bits [PD2:PD0] select a multiplexer position. The bank and position select corresponds to channel number CH1-CH64 according to the following equation:

$$CHANNEL = [BD2 : BD0] + (8 \times [PD2 : PD0]) + 1$$

Equation 2. Multiplexer Input Channel Selection

The setting in this register is ignored (over-ridden) by any of the following settings:

- One or more of the 4-bits [D6:D3] in the Power Status register 2 is set. These settings monitor the VREF, +5V, VEE, and VCC rails. See Table 18 above
- Either or both of the 2 bits D4 and D3 in the Calibration register 16 is set. These settings are used for testing and calibration. See Table 33 on page 48

Table 19: Register 3: Non-Inverting Mux Channel Select

Register Description	Register Address	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Non-Inverting Mux Channel Select register	**3**	**-**	**-**	**BD2**	**BD1**	**BD0**	**PD2**	**PD1**	**PD0**
Default register setting on POR or RESET	**0x03**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
The instrumentation amplifier's non-inverting input is routed from one of channel CH1-CH64 selected by the equation: `CHANNEL = [BD2 : BD0] + (8 × [PD2 : PD0]) + 1`	3 0x03	x	x	BD2	BD1	BD0	PD2	PD1	PD0
Selected channel is [0] + (8 X [0]) + 1 = CH1				**0**	**0**	**0**	**0**	**0**	**0**
Selected channel is [1] + (8 X [0]) + 1 = CH2				0	0	1	0	0	0
Selected channel is [2] + (8 X [0]) + 1 = CH3				0	1	0	0	0	0
Selected channel is [3] + (8 X [0]) + 1 = CH4				0	1	1	0	0	0
Selected channel is [4] + (8 X [0]) + 1 = CH5				1	0	0	0	0	0
Selected channel is [5] + (8 X [0]) + 1 = CH6				1	0	1	0	0	0
Selected channel is [6] + (8 X [0]) + 1 = CH7				1	1	0	0	0	0
Selected channel is [7] + (8 X [0]) + 1 = CH8				1	1	1	0	0	0
Selected channel is [0] + (8 X [1]) + 1 = CH9				**0**	**0**	**0**	**0**	**0**	**1**
... and so on ...		x	x	*... and so on ...*					
Selected channel is [7] + (8 X [6]) + 1 = CH56				**1**	**1**	**1**	**1**	**1**	**0**
Selected channel is [0] + (8 X [7]) + 1 = CH57				0	0	0	1	1	1
Selected channel is [1] + (8 X [7]) + 1 = CH58				0	0	1	1	1	1
Selected channel is [2] + (8 X [7]) + 1 = CH59				0	1	0	1	1	1
Selected channel is [3] + (8 X [7]) + 1 = CH60				0	1	1	1	1	1
Selected channel is [4] + (8 X [7]) + 1 = CH61				1	0	0	1	1	1
Selected channel is [5] + (8 X [7]) + 1 = CH62				1	0	1	1	1	1
Selected channel is [6] + (8 X [7]) + 1 = CH63				1	1	0	1	1	1
Selected channel is [7] + (8 X [7]) + 1 = CH64				**1**	**1**	**1**	**1**	**1**	**1**
Unused register bits. Values written are stored and read back		0/1	0/1	x	x	x	x	x	x

19.5 Register address 4: Inverting Mux Channel Select

The Inverting Mux Channel Select register 4 selects which of one the inputs CH1 to CH64 or the SE_RTN pin is routed by the analog multiplexer to the inverting input of the instrumentation amplifier.

If the Use SE_RTN bit D6 is 0, then the [BD2:BD0] and [PD2:PD0] bits select an input channel. The 3 bits [BD2:BD0] select a multiplexer bank, and the 3 bits [PD2:PD0] select a multiplexer position. The bank and position select corresponds to channel number CH1-CH64 according to the following expression:

$$CHANNEL = [BD2 : BD0] + (8 \times [PD2 : PD0]) + 1$$

Equation 3. Multiplexer Input Channel Selection

If the Use SE_RTN bit D6 is 1, then the [BD2:BD0] and [PD2:PD0] bits are ignored, and the inverting input of the instrumentation amplifier is connected to the voltage on the SE_RTN pin. The SE_RTN pin allows a remote ground point that is common to multiple single ended inputs to be used as a signal reference without sacrificing one of the 64 multiplexer inputs.

The setting in this register is ignored (over-ridden) by any of the following settings:

- One of more of the 4-bits [D6:D3] in the Power Status register 2 is set. These settings monitor the VREF, +5V, VEE, and VCC rails. See Table 18 on page 35
- Either or both of the 2 bits D7 and D4 in the Calibration register 16 is set. These settings are used for testing and calibration. See Table 33 on page 48
- Setting the D1 bit in the Calibration register 16 causes the inverting input of the instrumentation amplifier to be connected to AGND. This provides a convenient ground connection for local single ended inputs without using the SE_RTN pin. See Table 32 on page 48

Table 20: Register 4: Inverting Mux Channel Select

Register Description	Register Address	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Inverting Mux Channel Select register	**4 0x05**	**-**	**Use SE_RTN**	**BD2**	**BD1**	**BD0**	**PD2**	**PD1**	**PD0**
Default register setting on POR or RESET		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
The instrumentation amplifier's inverting input is routed from one of channel CH1-CH64 selected by the equation: $CHANNEL = [BD2 : BD0] + (8 \times [PD2 : PD0]) + 1$		x	0	BD2	BD1	BD0	PD2	PD1	PD0
Selected channel is [0] + (8 X [0]) + 1 = CH1				**0**	**0**	**0**	**0**	**0**	**0**
Selected channel is [1] + (8 X [0]) + 1 = CH2				0	0	1	0	0	0
Selected channel is [2] + (8 X [0]) + 1 = CH3				0	1	0	0	0	0
Selected channel is [3] + (8 X [0]) + 1 = CH4				0	1	1	0	0	0
Selected channel is [4] + (8 X [0]) + 1 = CH5				1	0	0	0	0	0
Selected channel is [5] + (8 X [0]) + 1 = CH6				1	0	1	0	0	0
Selected channel is [6] + (8 X [0]) + 1 = CH7				1	1	0	0	0	0
Selected channel is [7] + (8 X [0]) + 1 = CH8				1	1	1	0	0	0
Selected channel is [0] + (8 X [1]) + 1 = CH9				**0**	**0**	**0**	**0**	**0**	**1**
... and so on ...	4 0x04	x	0	*... and so on ...*					
Selected channel is [7] + (8 X [6]) + 1 = CH56				**1**	**1**	**1**	**1**	**1**	**0**
Selected channel is [0] + (8 X [7]) + 1 = CH57				0	0	0	1	1	1
Selected channel is [1] + (8 X [7]) + 1 = CH58				0	0	1	1	1	1
Selected channel is [2] + (8 X [7]) + 1 = CH59				0	1	0	1	1	1
Selected channel is [3] + (8 X [7]) + 1 = CH60				0	1	1	1	1	1
Selected channel is [4] + (8 X [7]) + 1 = CH61				1	0	0	1	1	1
Selected channel is [5] + (8 X [7]) + 1 = CH62				1	0	1	1	1	1
Selected channel is [6] + (8 X [7]) + 1 = CH63				1	1	0	1	1	1
Selected channel is [7] + (8 X [7]) + 1 = CH64				**1**	**1**	**1**	**1**	**1**	**1**
The instrumentation amplifier's inverting input is routed from the SE_RTN pin		X	1	x	x	x	x	x	x
Unused register bit. Value written is stored and reads back		0/1	x	x	x	x	x	x	x

19.6 Register address 5: Current Mux Level

The Current Mux Level register 5 sets the current in the 4-bit IDAC multiplexer current source. The Double bit D3 selects between low and high ranges. When the Double bit D3 = 1, the current set by bits [D2:D0] is doubled. From the Electrical Characteristics table, the current (including tolerances for both full scale current and DAC INL) follows the expressions in Equation 4 below:

Double bit D3 = 0: $Multiplexor\ Current = \{([D2 : D0] + 1) / 8 \times (1940\mu A \pm 60\mu A)\} \pm 7.5\mu A$

Double bit D3 = 1: $Multiplexor\ Current = \{([D2 : D0] + 1) / 8 \times (3830\mu A \pm 120\mu A)\} \pm 15\mu A$

Equation 4. 4-bit IDAC Multiplexer Current Source Transfer Characteristic

Example 1: Double bit D3 = 0, [D2:D0] = 011

$Multiplexor\ Current = \{([3] + 1) / 8 \times (1940\mu A \pm 60\mu A)\} \pm 7.5\mu A = 970\mu A \pm 30\mu A \pm 7.5\mu A = 970\mu A \pm 37.5\mu A$

Example 2: Double bit D3 = 1, [D2:D0] = 001

$Multiplexor\ Current = \{([1] + 1) / 8 \times (3830\mu A \pm 120\mu A)\} \pm 15\mu A = 957.5\mu A \pm 30\mu A \pm 15\mu A = 957.5\mu A \pm 45\mu A$

Table 21 on page 38 shows the programmed current (with tolerances) for all 16 options, in the order of increasing current.

The 10-bit DAC may be used as the input channel multiplexer instead of the IDAC by setting Use IDAC bit D7 = 1 (Table 21 on page 38). When assigned as the internal multiplexer current source, the 10-bit DAC is configured as 5-bit programmable current source in the range 0 to 300µA. See Table 31 on page 47 for 10-bit DAC configuration in this mode.

When Use IDAC bit D7 = 0, the 10-bit DAC is available as a general-purpose DAC, with complementary outputs on the DAC_P output pin and the DAC_N output pin. See Table 30 on page 46 for 10-bit DAC configuration in this mode.

Table 21: Register 5: Current Mux Level

Register Description	Register Address	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Current Mux Level register	**5**	**Use IDAC**	**-**	**-**	**-**	**Double**	**D2**	**D1**	**D0**
Default register setting on POR or RESET	**0x05**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Use IDAC in low range. Current is ({D3:D0} + 1) / 8 x 242.5µA	5 0x05	0	x	x	x	0	D2	D1	D0
Use IDAC in high range. Current is ({D3:D0} + 1) / 8 x 478.75µA						1			
IDAC (low range) current is set to 242.5µA ±15µA (±6.2%)		0				0	0	0	0
IDAC (high range) current is set to 478.75µA ±30µA (±6.3%)						1	0	0	0
IDAC (low range) current is set to 485µA ±22.5µA (±4.6%)						0	0	0	1
IDAC (low range) current is set to 727.5µA ±30µA (±4.1%)						0	0	1	0
IDAC (high range) current is set to 957.5µA ±45µA (±4.7%)						1	0	0	1
IDAC (low range) current is set to 970µA ±37.5µA (±3.9%)						0	0	1	1
IDAC (low range) current is set to 1212.5µA ±45µA (±3.7%)						0	1	0	0
IDAC (high range) current is set to 1436.25µA ±60µA (±4.2%)						1	0	1	0
IDAC (low range) current is set to 1455µA ±52.5µA (±3.6%)						0	1	0	1
IDAC (low range) current is set to 1697.5µA ±60µA (±3.5%)						0	1	1	0
IDAC (high range) current is set to 1915µA ±75µA (±3.9%)						1	0	1	1
IDAC (low range) current is set to 1940µA ±60µA (±3.1%)						0	1	1	1
IDAC (high range) current is set to 2393.75µA ±90µA (±3.8%)						1	1	0	0
IDAC (high range) current is set to 2872.5µA ±105µA (±3.7%)						1	1	0	1
IDAC (high range) current is set to 3351.25µA ±120µA (±3.6%)						1	1	1	0
IDAC (high range) current is set to 3830µA ±135µA (±3.5%)						1	1	1	1
Unused register bits. Values written are stored and read back		x	0/1	0/1	0/1	x	x	x	x
Use the 10-bit DAC as the programmable current source to the input channel multiplexer instead of the IDAC. The 10-bit DAC is configured by registers 14 and 15 (Table 30 on page 46)		1	x	x	x	x	x	x	x

19.7 Register address 6: Current Mux Channel Selection

The Current Mux Select register 6 selects which one of the 64 input channels CH1-CH64 that the selected multiplexer current source is routed to.

To apply a current source to an input channel:

- First select which input channel that the selected multiplexer current source is routed to using the Current Mux Select register 6 (Table 22 on page 39)
- Enable the current source circuitry by clearing Current Source Disable bit D5 = 0 in the Function Enable register 1 (Table 17 on page 18)
- Configure the Current Mux Level register 5 (Table 21 above)
  - To use the 4-bit IDAC current source, clear Use IDAC bit D7 = 0, and select the desired current level with the remaining bits
  - To use the 10-bit DAC as the multiplexer current source instead of the IDAC, set Use IDAC bit D7 = 1, and select the desired multiplexer current level using the 10-bit DAC registers 14 and 15 (Table 31 on page 47)

To disable current sourcing to any multiplexer input channel, either:

- Disable the current source circuitry by setting Current Source Disable bit D5 = 1 in the Function Enable register 1 (Table 17 on page 18), or
- Set the programmed multiplexer source current to 0µA by
  - Selecting the 10-bit DAC as the multiplexer current source by writing 0x80 to the Current Mux Level register 5 (Table 21 above), and
  - Setting the 10-bit DAC current to 0µA by first writing 0x00 to the 10-bit DAC LSB register 15, and then writing 0x00 to the 10-bit DAC MSB register 14 (Table 31 on page 47)

Table 22: Register 6: Current Mux Channel Selection

Register Description	Register Address	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Current Mux Channel register	**6**	**-**	**-**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default register setting on POR or RESET	**0x06**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Selected channel for current source is CH1-CH64 is [D5:D0] + 1	6 0x06	-	-	D5	D4	D3	D2	D1	D0
Selected channel for current source is CH1		x	x	0	0	0	0	0	0
Selected channel for current source is CH2				0	0	0	0	0	1
Selected channel for current source is CH3				0	0	0	0	1	0
... and so on ...				*... and so on ...*					
Selected channel for current source is CH62				1	1	1	1	0	1
Selected channel for current source is CH63				1	1	1	1	1	0
Selected channel for current source is CH64				1	1	1	1	1	1
Unused register bits. Values written are stored and read back		0/1	0/1	x	x	x	x	x	x

19.8 Register address 7: Signal Conditioning Amplifier

The Signal Conditioning Amplifier register 7 controls a programmable gain amplifier and a pair of cascaded single pole low pass anti-alias filters. These stages sit in the signal chain between the instrumentation amplifier output and the ADC input.

The signal conditioning amplifier is enabled by setting Filter Off bit D6 = 0, in which case the amplifier's output (which is the final input to the ADC) appears at the ADC_IN pin. The signal at ADC_IN can be monitored by external circuitry if desired, such as by a second ADC for redundancy.

To use the ADC directly without any of the analog front end (multiplexer, current source, instrumentation amplifier, gain, filters), disable the signal conditioning amplifier by setting Filter Off bit D6 = 1. This configures the final amplifier's output to Hi-Z, allowing the ADC_IN pin to be driven by an external 0V to 2V input voltage.

The two 1-pole anti-alias filters are independent. They can be set to the same or different cutoff frequencies depending on the response desired.

Table 23: Register 7: Signal Conditioning Amplifier

Register Description	Register Address	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Signal Conditioning Amplifier register	**7 0x07**	**-**	**Filter Off**	**2nd Pole Frequency**		**1st Pole Frequency**		**Amplifier Gain**	
Default register setting on POR or RESET		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Signal conditioning amplifier gain is 0.4 A 5V signal at the multiplexer covers the 2V ADC input range	7 0x07	x	0	x	x	x	x	0	0
Signal conditioning amplifier gain is 2 A 1V signal at the multiplexer covers the 2V ADC input range		x	0	x	x	x	x	0	1
Signal conditioning amplifier gain is 10		x	0	x	x	x	x	1	0
A 200mV signal at the multiplexer covers the 2V ADC input range		x	0	x	x	x	x	1	1
1st single pole low pass anti-alias filter cutoff frequency is 400Hz		x	0	x	x	0	0	x	x
1st single pole low pass anti-alias filter cutoff frequency is 2kHz		x	0	x	x	0	1	x	x
1st single pole low pass anti-alias filter cutoff frequency is 10kHz		x	0	x	x	1	0	x	x
Factory test setting. Do not use		x	0	x	x	1	1	x	x
2nd single pole low pass anti-alias filter cutoff frequency is 400Hz		x	0	0	0	x	x	x	x
2nd single pole low pass anti-alias filter cutoff frequency is 2kHz		x	0	0	1	x	x	x	x
2nd single pole low pass anti-alias filter cutoff frequency is 10kHz		x	0	1	0	x	x	x	x
Factory test setting. Do not use		x	0	1	1	x	x	x	x
Analog front end is enabled and drives the ADC_IN pin as an output with the final signal that is available to be acquired by the internal ADC		x	0	x	x	x	x	x	x
Analog front end is disabled. The ADC_IN pin is an input. Apply an external 0V to 2V input voltage at the ADC_IN pin for ADC acquisition		x	1	x	x	x	x	x	x
Unused register bit. Value written is stored and read back		0/1	x	x	x	x	x	x	x

19.9 Register address 8: ADC Control

The ADC Control register 8 initiates a single ADC conversion or configures auto-conversion, and allows conversion status to be monitored (Table 24). Note that the Data Ready bit D3 is simply the inverse of the Busy bit D2.

The ADC Control register 8 comprises:

- Four latched bits D7 to D4 that are written by the user to configure single- or auto-conversion,
- Two status bits D3 and D2 that change with timing of the ADC's state machine, and
- The Start Conv bit D1 which operates as both a user command to start an ADC conversion on write, and a status bit controlled by the ADC's state machine on read

Table 24: Register 8: ADC Control

Register Description	Register Address	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
ADC Control register	**8 0x08**	**Auto Sample Rate [S2:S0]**			**Auto Conv**	**Data Ready**	**Busy**	**Start Conv**	**0**
Default register setting on POR or $\overline{\text{RESET}}$		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Leave this bit cleared to 0 to enable the gain and filter stages	8 0x08	x	x	x	x	x	x	x	0
Start a single-shot ADC conversion		x	x	x	0	x	x	1	0
Read status: the ADC is performing a single-shot conversion		x	x	x	0	0	1	x	0
Read status: the ADC is not performing a conversion. The most recent conversion result is available in the ADC Result MSB and LSB registers 9 and 10 (Table 25 on page 42)						1	0		
Read status: the ADC has performing a continuous conversion		Auto Sample Rate			1	0	1	x	0
Read status: the ADC has finished a continuous conversion and is waiting to start another conversion						1	0		
Stop ADC auto-conversions at the end of the current conversion		x	x	x	0	x	x	0	0
Start ADC auto-conversions at sample rate set by [S2:S0]		Set rate			1	x	x	0	0
ADC sample rate = CLK / 40, so 12500 conversions/s at CLK = 500kHz		0	0	0					
ADC sample rate = CLK / 95, so 5263 conversions/s at CLK = 500kHz		0	0	1					
ADC sample rate = CLK / 205, so 2439 conversions/s at CLK = 500kHz		0	1	0					
ADC sample rate = CLK / 425, so 1176 conversions/s at CLK = 500kHz		0	1	1					
ADC sample rate = CLK / 865, so 578 conversions/s at CLK = 500kHz		1	0	0					
ADC sample rate = CLK / 1745, so 286 conversions/s at CLK = 500kHz		1	0	1					
ADC sample rate = CLK / 3505, so 142 conversions/s at CLK = 500kHz		1	1	0					
ADC sample rate = CLK / 7025, so 71 conversions/s at CLK = 500kHz		1	1	1					

The ADC's state machine timing is shown in Figure 17 below. A conversion is initiated by writing ADC Control register 8 setting either the Start Conv bit D1=1 for a single conversion, or the Auto Conv bit D4=1 for continuous conversions. The conversion starts on the subsequent rising edge of CLK.

The ADC_DAC_OUT pin is the output of the ADC's internal SAR DAC. This pin should not be loaded in production (just fitted with $R_{ADC\_DAC\_OUT}$ per Table 3 on page 18), but provides a useful output for debugging ADC operation.

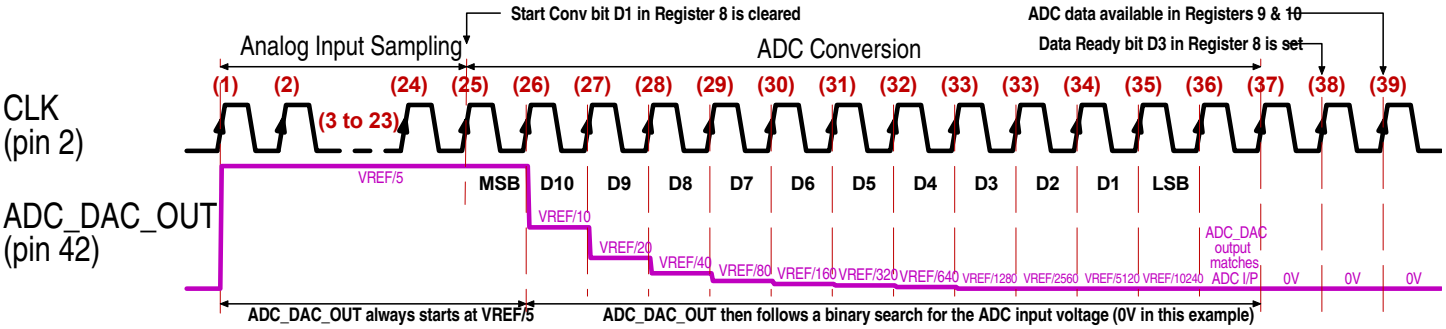


Figure 17. ADC Conversion Timing

The ADC samples the input for 25 CLK periods, and then converts the sampled value for the next 12 CLK periods. The Data Ready bit is set by the rising edge of the 38th CLK, and the ADC result is valid in the ADC Result MSB and LSB registers 9 and 10 (Table 25 on page 42) after the 39th CLK rising edge. Until the 39th CLK rising edge, ADC Result MSB and LSB registers 9 and 10 retain the result of the previous acquisition.

Some notes to consider when planning acquisition timing:

- The ADC's state machine operates from the CLK pin (125kHz to 500kHz). The lower limit of 125kHz is not a hard limit, but an issue of increasing INL due to leakage in the sample/hold capacitor. See Table 3 on page 18 for details. ADC analog performance (offset and gain error, INL, DNL) is guaranteed in the Electrical Characteristics table at 500kHz
- CLK is typically operated continuously, but it may be halted in either low or high state between conversions
  - At the earliest, halt CLK after its 39th rising edge (leaving CLK high) or subsequent falling edge (leaving CLK low) in the case of a single conversion
- ADC Control register 8 can be written with CLK halted, and CLK started when desired
  - After writing ADC Control register 8 with a Start Conv or Auto Conv command, a read of ADC Control register 8 before the first subsequent rising edge of CLK will cause the Start Conv command or Auto Conv to be cancelled
- The rising edge of the 25th CLK is the instant that the sample/hold aperture closes and the analog input is stored
  - Start Conv bit D1 in ADC Control register 8 is also cleared by the 25th CLK rising edge
  - The input multiplexor and current source can be switched to another input any time after the 25th CLK rising edge without affecting the conversion underway. This allows 14 CLKs (28µs with a 500kHz CLK) settling time for the next ADC input selection
- For fastest sequential acquisitions, write ADC Control register 8 with a Start Conv command during the 39th CLK period. The current ADC result will be available for the first 38 CLK periods of this new conversion, and so can read from ADC Result MSB and LSB resisters 9 and 10 after starting the new conversion
- The ADC state machine is reset by the Power On Enable block (Section 13.1 on page 19) on power-up. It is not, however, reset by either the $\overline{\text{RESET}}$ pin or via the Master Reset register 0. If the LX7720 is reset this way after power up, any ADC conversion underway will continue through completion. If the external ADC CLK source is halted by this reset event, be aware that up to 38 CLK periods will be required to complete this ADC conversion before a new one can be initiated.

19.9.1 Single-Shot ADC Conversion

To start a single conversion, set the Start Conv bit D1 by writing ADC Control register 8 with 0x02.

- In parallel interface mode, the Start Conv command is recognized by the ADC state machine at the falling edge of $\overline{\text{WE}}$
- In SPI mode, the Start Conv command is recognized at the rising edge of $\overline{\text{SSA}}$ or $\overline{\text{SSB}}$

The Start Conv command is latched into the ADC state machine by the next rising edge of CLK (Figure 18). If ADC Control register 8 is read before the next rising edge of CLK, then the Start Conv command is cancelled. If ADC activity is to be monitored by polling ADC Control register 8, be sure to either monitor CLK or wait at least a CLK period between starting a conversion and reading register 8.

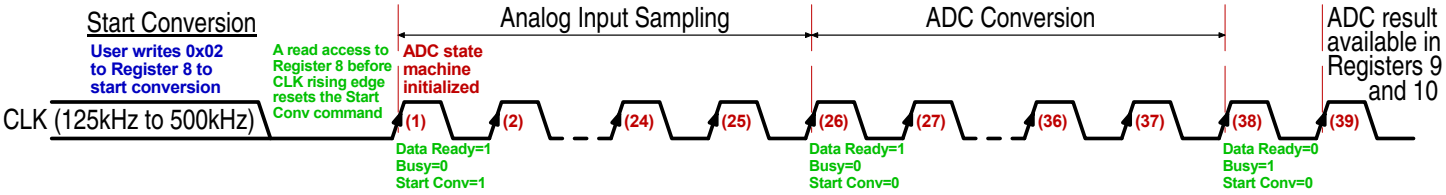


Figure 18. Single Conversion Timing

ADC Control register 8 bits D3 to D1 are not implemented as latched interface register bits, but represent real-time states within the ADC's state machine. The asynchronous nature of read and write access to ADC Control register 8 with respect to the ADC's state machine gives rise to small differences between behaviors when controlled by the parallel or a serial interface.

ADC Control register 8 Start Conv bit D1 is cleared the ADC's state machine on the 25th rising edge of CLK after writing ADC Control register 8 with 0x02. ADC Control register 8 Data Ready bit D3 and Busy bit D2 are toggled by the ADC's state machine on the 38th rising edge of CLK (Figure 18).

Since the status change of bits D3 to D1 are asynchronous to register reads through the parallel or serial interface, changes may occur mid-read. With the serial interface, this will appear as a parity error. A re-read will provide the correct status. With the parallel interface, the data bus and parity bit during a read ($\overline{\text{OE}}$ = 0) will show any bit changes transparently during the read.

19.9.2 CONTINUOUS (AUTO) ADC CONVERSIONS

To start continuous conversions, set the Auto Conv bit D4 by writing ADC Control register 8 with a value from 0x10 to 0xF0 according to the sample rate desired (Table 24). The bits S2 to S0 in ADC Control register 8 select the sample rate. ADC continuous conversions are stored in the ADC Result MSB and LSB registers 9 and 10 until the next conversion is ready, and then overwritten. The sample rate follows Equation 5 below. Table 24 shows sample rates for 500kHz CLK.

$$\text{ADC sample rate} = \frac{\text{CLK}}{40 + \left(55 \times \left[2^{[S2\,:\,S0]} - 1\right]\right)} \text{ ADC conversions per second}$$

Equation 5. ADC Auto Sample Rate

19.10 Register addresses 9 and 10: ADC Result MSB and LSB

The ADC result MSB register 9 contains the 8 MSBs [ADC _D11: ADC _D4], and the ADC result LSB register 10 contains the 4 LSBs [ADC _D3: ADC _D0] for the last completed 12-bit ADC conversion [ADC _D11: ADC _D0]. The 4 unused bits in the ADC result LSB register always return 0s. The ADC characteristics follow the expressions in Equation 6 below:

$$\text{Voltage at ADC\_IN} = \frac{[\text{ADC\_D11 : ADC\_D0}] \times 2}{4096} \text{ V} \quad \text{or} \quad [\text{ADC\_D11 : ADC\_D0}] = (\text{Voltage at ADC\_IN}) \times 2048$$

Equation 6. ADC Characteristics

Table 25: Register 9 and 10: ADC Result MSB and LSB

Register Description	Register Address	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
ADC Result MSB register	9	ADC _D11	ADC _D10	ADC _D9	ADC _D8	ADC _D7	ADC _D6	ADC _D5	ADC _D4
Default register setting on POR or RESET	0x09	0	0	0	0	0	0	0	0
ADC Result LSB register	10	0	0	0	0	ADC _D3	ADC _D2	ADC _D1	ADC _D0
Default register setting on POR or RESET	0x0A	0	0	0	0	0	0	0	0

19.11 Register address 11: 8-Bit Bank Bi-Level Comparators Threshold DAC

The 8-Bit Bank Bi-Level Comparators Threshold DAC register sets the 8-bit DAC setting the rising-voltage threshold for the inverting inputs to the 8 bank bi-level comparators (See Table 26 and Table 27 on page 43, Figure 6 on page 22). The bank bi-level comparators are 8 comparators whose non-inverting inputs connect to a selection of the internal multiplexer outputs, and whose outputs are available in a register. The comparators have built in hysteresis, making the falling-voltage threshold for the inverting inputs typically 112mV lower than the voltage set by this DAC.

Table 26: Register 11: 8-Bit Bank Bi-Level Comparators Threshold DAC

Register Description		Register Address	Register Data							
			D7	D6	D5	D4	D3	D2	D1	D0
8-Bit Bank Bi-Level Comparators Threshold DAC register		11	BI _D7	BI _D6	BI _D5	BI _D4	BI _D3	BI _D2	BI _D1	BI _D0
Default register setting on POR or RESET		0x0B	0	0	0	0	0	0	0	0
0x00 (0): DAC output is typically 0V	DAC output precision is not guaranteed in the range 0x00 to 0x13	11 0x0B	0	0	0	0	0	0	0	0
0x01 (1): DAC output is typically 0.02V			0	0	0	0	0	0	0	1
... up to ...			... up to ...							
0x12 (18): DAC output is typically 0.35V			0	0	0	1	0	0	1	0
0x13 (19): DAC output is typically 0.37V			0	0	0	1	0	0	1	1
0x14 (20): DAC output is 0.392V typical (0.359V - 0.426V)			0	0	0	1	0	1	0	0
0x15 (21): DAC output is 0.412V typical (0.378V - 0.446V)			0	0	0	1	0	1	0	1
0x16 (22): DAC output is 0.431V typical (0.398V - 0.465V)			0	0	0	1	0	1	1	0
... up to ...			... up to ...							
0xEE (238): DAC output is 4.667V typical (4.591V - 4.743V)			1	1	1	0	1	1	1	0
0xEF (239): DAC output is 4.686V typical (4.61V - 4.763V)			1	1	1	0	1	1	1	1
0xF0 (240): DAC output is 4.706V typical (4.629V - 4.783V)			1	1	1	1	0	0	0	0
0xF1 (241): DAC output is typically 4.73V	DAC output precision is not guaranteed in the range 0xF1-0xFF		1	1	1	1	0	0	0	1
0xF2 (242): DAC output is typically 4.75V			1	1	1	1	0	0	1	0
... up to ...			... up to ...							
0xFE (254): DAC output is typically 4.98V			1	1	1	1	1	1	1	0
0xFF (255): DAC output is typically 5V			1	1	1	1	1	1	1	1

The bank bi-level comparator non-inverting inputs are configured by register 12 (Table 28 on page 44), and the outputs are available in register 13 (Table 29 on page 44).

There is also an independent set of 8 bi-level comparators called the BLI/BLO comparators whose non-inverting inputs connect to the 8 pins BLI1 to BLI8, and whose outputs connect to the 8 pins BLO1 to BLO8. See section 14.2 on page 20.

The DAC is implemented as a voltage output R-2R ladder. If the Bank bi-level comparators are not used, setting the DAC to 0x00 (which is the condition after a reset) saves a little power.

The DAC is specified for linearity over the code range 0x14 to 0xF0 (20 to 240), which corresponds to an DAC output voltage range of 0.4V to 4.7V. The DAC output voltage over this range follows the expression in Equation 7 below. This includes the ±1% full scale error, the ±1 LSB INL, and the ±10mV offset error). The expression is also valid for values outside this code range, but the precision may be worse.

$$\text{Bi-Level DAC Output} = \frac{\left(\frac{5 \times 256}{255} \pm 1\%\right) \times \left(\{BL\_D7 : BL\_D0\} \pm 1\right)}{256} \pm 0.010\ \text{V}$$

which simplifies to:

$$\text{Bi-Level DAC Output} = \frac{\{BL\_D7 : BL\_D0\} \pm 1}{51 \pm 1\%} \pm 0.010\ \text{V}$$

Equation 7. 8-Bit Bank Bi-Level Comparators Threshold DAC Transfer Characteristic

Design Example

Desired DAC voltage is 3V. Using Table 27 on page 43, the DAC [BL_D7:BL_D0] setting for 3.0V typical is 0x99, or 153. With that value, the tolerances can be calculated:

$$\text{Bi-Level DAC Output (max)} = \frac{\{153\} + 1}{51 \times 0.99} + 0.010\ \text{V} = 3.06\text{V}$$

$$\text{Bi-Level DAC Output (min)} = \frac{\{153\} - 1}{51 \times 1.01} - 0.010\ \text{V} = 2.94\text{V}$$

Table 27. 8-Bit Bank Bi-Level Comparators Threshold DAC Typical Outputs

Code	DAC Output	Code	DAC Output	Code	DAC Output	Code	DAC Output	Code	DAC Output	Code	DAC Output	Code	DAC Output	Code	DAC Output
0x00	0.00V	0x20	0.63V	0x40	1.25V	0x60	1.88V	0x80	2.51V	0xA0	3.14V	0xC0	3.76V	0xE0	4.39V
0x01	0.02V	0x21	0.65V	0x41	1.27V	0x61	1.90V	0x81	2.53V	0xA1	3.16V	0xC1	3.78V	0xE1	4.41V
0x02	0.04V	0x22	0.67V	0x42	1.29V	0x62	1.92V	0x82	2.55V	0xA2	3.18V	0xC2	3.80V	0xE2	4.43V
0x03	0.06V	0x23	0.69V	0x43	1.31V	0x63	1.94V	0x83	2.57V	0xA3	3.20V	0xC3	3.82V	0xE3	4.45V
0x04	0.08V	0x24	0.71V	0x44	1.33V	0x64	1.96V	0x84	2.59V	0xA4	3.22V	0xC4	3.84V	0xE4	4.47V
0x05	0.10V	0x25	0.73V	0x45	1.35V	0x65	1.98V	0x85	2.61V	0xA5	3.24V	0xC5	3.86V	0xE5	4.49V
0x06	0.12V	0x26	0.75V	0x46	1.37V	0x66	2.00V	0x86	2.63V	0xA6	3.25V	0xC6	3.88V	0xE6	4.51V
0x07	0.14V	0x27	0.76V	0x47	1.39V	0x67	2.02V	0x87	2.65V	0xA7	3.27V	0xC7	3.90V	0xE7	4.53V
0x08	0.16V	0x28	0.78V	0x48	1.41V	0x68	2.04V	0x88	2.67V	0xA8	3.29V	0xC8	3.92V	0xE8	4.55V
0x09	0.18V	0x29	0.80V	0x49	1.43V	0x69	2.06V	0x89	2.69V	0xA9	3.31V	0xC9	3.94V	0xE9	4.57V
0x0A	0.20V	0x2A	0.82V	0x4A	1.45V	0x6A	2.08V	0x8A	2.71V	0xAA	3.33V	0xCA	3.96V	0xEA	4.59V
0x0B	0.22V	0x2B	0.84V	0x4B	1.47V	0x6B	2.10V	0x8B	2.73V	0xAB	3.35V	0xCB	3.98V	0xEB	4.61V
0x0C	0.24V	0x2C	0.86V	0x4C	1.49V	0x6C	2.12V	0x8C	2.75V	0xAC	3.37V	0xCC	4.00V	0xEC	4.63V
0x0D	0.25V	0x2D	0.88V	0x4D	1.51V	0x6D	2.14V	0x8D	2.76V	0xAD	3.39V	0xCD	4.02V	0xED	4.65V
0x0E	0.27V	0x2E	0.90V	0x4E	1.53V	0x6E	2.16V	0x8E	2.78V	0xAE	3.41V	0xCE	4.04V	0xEE	4.67V
0x0F	0.29V	0x2F	0.92V	0x4F	1.55V	0x6F	2.18V	0x8F	2.80V	0xAF	3.43V	0xCF	4.06V	0xEF	4.69V
0x10	0.31V	0x30	0.94V	0x50	1.57V	0x70	2.20V	0x90	2.82V	0xB0	3.45V	0xD0	4.08V	0xF0	4.71V
0x11	0.33V	0x31	0.96V	0x51	1.59V	0x71	2.22V	0x91	2.84V	0xB1	3.47V	0xD1	4.10V	0xF1	4.73V
0x12	0.35V	0x32	0.98V	0x52	1.61V	0x72	2.24V	0x92	2.86V	0xB2	3.49V	0xD2	4.12V	0xF2	4.75V
0x13	0.37V	0x33	1.00V	0x53	1.63V	0x73	2.25V	0x93	2.88V	0xB3	3.51V	0xD3	4.14V	0xF3	4.76V
0x14	0.39V	0x34	1.02V	0x54	1.65V	0x74	2.27V	0x94	2.90V	0xB4	3.53V	0xD4	4.16V	0xF4	4.78V
0x15	0.41V	0x35	1.04V	0x55	1.67V	0x75	2.29V	0x95	2.92V	0xB5	3.55V	0xD5	4.18V	0xF5	4.80V
0x16	0.43V	0x36	1.06V	0x56	1.69V	0x76	2.31V	0x96	2.94V	0xB6	3.57V	0xD6	4.20V	0xF6	4.82V
0x17	0.45V	0x37	1.08V	0x57	1.71V	0x77	2.33V	0x97	2.96V	0xB7	3.59V	0xD7	4.22V	0xF7	4.84V
0x18	0.47V	0x38	1.10V	0x58	1.73V	0x78	2.35V	0x98	2.98V	0xB8	3.61V	0xD8	4.24V	0xF8	4.86V
0x19	0.49V	0x39	1.12V	0x59	1.75V	0x79	2.37V	0x99	3.00V	0xB9	3.63V	0xD9	4.25V	0xF9	4.88V
0x1A	0.51V	0x3A	1.14V	0x5A	1.76V	0x7A	2.39V	0x9A	3.02V	0xBA	3.65V	0xDA	4.27V	0xFA	4.90V
0x1B	0.53V	0x3B	1.16V	0x5B	1.78V	0x7B	2.41V	0x9B	3.04V	0xBB	3.67V	0xDB	4.29V	0xFB	4.92V
0x1C	0.55V	0x3C	1.18V	0x5C	1.80V	0x7C	2.43V	0x9C	3.06V	0xBC	3.69V	0xDC	4.31V	0xFC	4.94V
0x1D	0.57V	0x3D	1.20V	0x5D	1.82V	0x7D	2.45V	0x9D	3.08V	0xBD	3.71V	0xDD	4.33V	0xFD	4.96V
0x1E	0.59V	0x3E	1.22V	0x5E	1.84V	0x7E	2.47V	0x9E	3.10V	0xBE	3.73V	0xDE	4.35V	0xFE	4.98V
0x1F	0.61V	0x3F	1.24V	0x5F	1.86V	0x7F	2.49V	0x9F	3.12V	0xBF	3.75V	0xDF	4.37V	0xFF	5.00V

19.12 Register address 12: Bank Bi-Level Comparators Input Selection

The Bank Bi-Level Comparators Input Selection register 12 selects which bank of 8 inputs are routed to the non-inverting inputs of the bank bi-level comparators, when En Sw bit D3 = 1. Figure 6 on page 22 is a block diagram of bank bi-level comparators operating with En Sw bit D3 = 1.

When En Sw bit D3 = 0, the bank bi-level comparators are connected to inputs controlled by Mux Channel Select registers 3 and 4 (Table 19 on page 36, Table 20 on page 37). See section 14.3.2 on page 23 for details how the comparators are connected to the inputs CH1 to CH64 in this mode.

The comparator inverting inputs are connected to a common threshold voltage set by an 8-bit DAC configured by register 11 (Table 26 on page 42). The bank bi-level comparator outputs are available in register 13 (Table 29 on page 44).

The Use BL-TH bit D7 selects the reference voltage (inverting input trip threshold) for the independent BLI/BLO bi-level comparators, whose non-inverting inputs connect to pins BLI1 to BLI8, and whose outputs connect to pins BLO1 to BLO8.

Table 28: Register 12: Bank Bi-Level Comparators Input Selection

Register Description	Register Address	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Bank Bi-Level Comparators Input Selection register	**12 0x0C**	**Use BL_TH**	**-**	**-**	**-**	**Bi-Level Mux Switch Position**			
						En Sw	**D2**	**D1**	**D0**
Default register setting on POR or RESET		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bank bi-level comparators input selection set by the Mux Channel Select registers 3 & 4 (Table 19 on page 36, Table 20 on page 37)	12 0x0C	x	x	x	x	0	x	x	x
Analog multiplexer inputs CH1 - CH8 to the bank comparators		x	x	x	x	1	0	0	0
Analog multiplexer inputs CH9 - CH16 to the bank comparators		x	x	x	x	1	0	0	1
Analog multiplexer inputs CH17 - CH24 to the bank comparators		x	x	x	x	1	0	1	0
Analog multiplexer inputs CH25 - CH32 to the bank comparators		x	x	x	x	1	0	1	1
Analog multiplexer inputs CH33 - CH40 to the bank comparators		x	x	x	x	1	1	0	0
Analog multiplexer inputs CH41 - CH48 to the bank comparators		x	x	x	x	1	1	0	1
Analog multiplexer inputs CH49 - CH56 to the bank comparators		x	x	x	x	1	1	1	0
Analog multiplexer inputs CH57 - CH64 to the bank comparators		x	x	x	x	1	1	1	1
Unused register bits. Values written are stored and read back		x	0/1	0/1	0/1	x	x	x	x
BLI/BLO comparators use an internal 2.5V ±50mV reference		0	x	x	x	x	x	x	x
BLI/BLO comparators use external reference on the BL_TH pin		1	x	x	x	x	x	x	x

19.13 Register address 13: Bank Bi-Level Comparators Output Status

The Bank Bi-Level Comparators Output Status register 13 provides the outputs of the 8 bank bi-level comparators selected by the 4 LSBs {D3:D0} in register 12 (Table 28 above). A comparator output is high when its associated input is higher than the common threshold voltage set by an 8-bit DAC configured by register 11 (Table 26 on page 42).

Table 29: Register 13: Bank Bi-Level Comparators Output Status

Register Description	Register Address	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Bank Bi-Level Comparators Output Status register	**13 0x0D**	**Selected Bank Bi-Level Comparators Outputs**							
Default register setting on POR or RESET		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Register 12 = 0xX0 to 0xX7. Bank comparators input selection set by the Mux Channel Select registers 3 & 4	13 0x0D	See Table 19 on page 36, Table 20 on page 37							
Register 12 = 0xX8: Bank comparators cover CH1 - CH8		CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
Register 12 = 0xX9: Bank comparators cover CH9 - CH16		CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9
Register 12 = 0xXA: Bank comparators cover CH17 - CH24		CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17
Register 12 = 0xXB: Bank comparators cover CH25 - CH32		CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25
Register 12 = 0xXC: Bank comparators cover CH33 - CH40		CH40	CH39	CH38	CH37	CH36	CH53	CH34	CH33
Register 12 = 0xXD: Bank comparators cover CH41 - CH48		CH48	CH47	CH46	CH45	CH44	CH43	CH42	CH41
Register 12 = 0xXE: Bank comparators cover CH49 - CH56		CH56	CH55	CH54	CH53	CH52	CH51	CH50	CH49
Register 12 = 0xXF: Bank comparators cover CH57 - CH64		CH64	CH63	CH62	CH61	CH60	CH59	CH58	CH57

19.14 Register address 14 and 15: 10-Bit DAC MSB and LSB

The 10-bit DAC MSB register 14 contains the eight MSBs, and the 10-Bit DAC LSB register 15 contains the two LSBs for the 10-bit current DAC.

To update the DAC, the DAC LSB register 15 is written first. DAC LSB register 15 only stores the two LSBs, [D1:D0]. The remaining 6 bits [D7:D2] are ignored, and read back from the register as 0s. When the DAC MSB register 14 is written, the two LSBs in the DAC LSB register 15 are combined with the eight bits just stored in the DAC MSB register 14. This 10-bit word is used immediately to update the 10-bit DAC. The structure is shown in Figure 19 below.

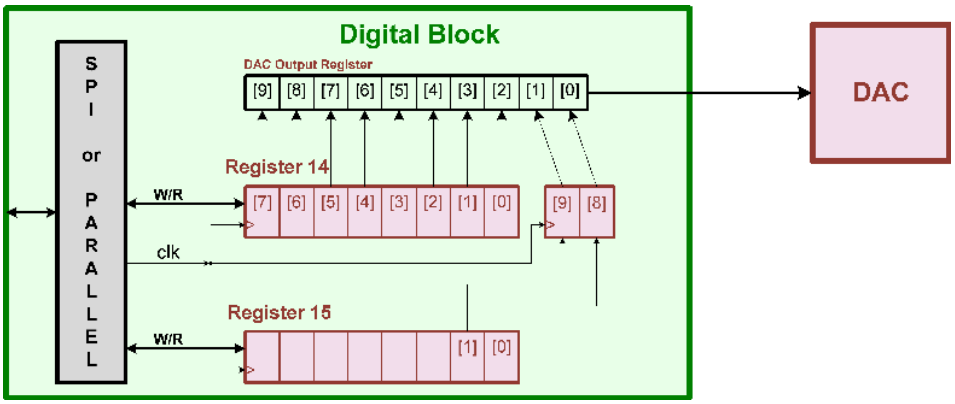


Figure 19. Register 14 and Register 15 Mapping to DAC Output Register

The 10-bit DAC is assigned to one of three modes of operation:

- Powered down, by clearing Function Enable register 1 bit D2 = 0 (Table 17 on page 34)
- Assigned as a general-purpose complementary current output 10-bit DAC, in the range 0 to 2mA routed to the DAC_P output pin and the DAC_N output pin
- Assigned as the internal multiplexer 5-bit current source, in the range 0 to 300µA

To use the 10-bit DAC as a general purpose DAC:

- Clear the Current Mux Level register 5 Use IDAC bit D7 = 0 (Table 21 on page 38). This selects the 4-bit IDAC current source as the multiplexer current source, and frees the 10-bit DAC
- The code range 0 to 1023 in the 10-bit DAC registers 14 and 15 (Table 30 below) sources an increasing output current from 0 to 2mA at the DAC_P output pin, and a decreasing output current from 2 to 0mA at the DAC_N output pin
- Terminate both the DAC_P output pin and the DAC_N output pin with resistors ≤1.5kΩ to AGND to develop nominal output voltages ≤3V maximum at code 0x3FF and 0x000 respectively

From the Electrical Characteristics table, the DAC_P and DAC_N currents (including full scale current tolerance of 0.06mA and DAC INL of 5 LSBs) follow Equation 8, where R_{IREF1} = 20kΩ ±1% resistor from the IREF1 pin to AGND:

$$DAC\_P = \frac{(2 \pm 0.06) \times \{DAC\_D9 : DAC\_D0\}}{1024} \pm \frac{5 \times 2.06}{1024}\ mA = \frac{(2 \pm 0.06) \times \{DAC\_D9 : DAC\_D0\}}{1024} \pm 0.010\ mA$$

$$DAC\_N = (2 \pm 0.06) \times \left(1 - \frac{\{DAC\_D9 : DAC\_D0\}}{1024}\right) \pm 0.010\ mA$$

Equation 8. 10-bit DAC Transfer Characteristic for Output Pins DAC_P and DAC_N

Example 1: [DAC_D9:DAC_D0] = b'01000000 00' = 256

$$DAC\_P = \frac{(2 \pm 0.06) \times \{256\}}{1024} \pm 0.010\ mA = 0.5mA \pm 0.025mA = 0.475mA\ to\ 0.525mA$$

$$DAC\_N = (2 \pm 0.06) \times \left(1 - \frac{\{256\}}{1024}\right) \pm 0.010\ mA = 1.5mA \pm 0.055mA = 1.445mA\ to\ 1.555mA$$

Example 2: [DAC_D9:DAC_D0] = b'11000000 00' = 768

$$DAC\_P = \frac{(2 \pm 0.06) \times \{768\}}{1024} \pm 0.010\ mA = 1.5mA \pm 0.055mA = 1.445mA\ to\ 1.555mA$$

$$DAC\_N = (2 \pm 0.06) \times \left(1 - \frac{\{768\}}{1024}\right) \pm 0.010\ mA = 0.5mA \pm 0.025mA = 0.475mA\ to\ 0.525mA$$

Table 30: Register addresses 14 and 15: 10-Bit DAC (driving the DAC_P pin and the DAC_N pin)

Register Description	Register Address	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
10-Bit DAC MSB register	14	DAC _D9	DAC _D8	DAC _D7	DAC _D6	DAC _D5	DAC _D4	DAC _D3	DAC _D2
Default register setting on POR or $\overline{\text{RESET}}$	0x0E	0	0	0	0	0	0	0	0
10-Bit DAC LSB register	15	0	0	0	0	0	0	DAC _D1	DAC _D0
Default register setting on POR or $\overline{\text{RESET}}$	0x0F	0	0	0	0	0	0	0	0
$DAC\_P = \frac{2 \times \{DAC\_D9 : DAC\_D0\}}{1024}\ mA$ $DAC\_N = 2 \times \left(1 - \frac{\{DAC\_D9 : DAC\_D0\}}{1024}\right) mA$	14 0x0E and 15 0x0F	Current Mux Level register 5 Use IDAC bit D7 = 0 (Table 21 on page 38), making the DAC available with complementary outputs DAC_P and DAC_N. Terminate the DAC_P pin and the DAC_N pin each with a resistor ≤1.5kΩ to AGND to develop complementary nominal output voltages ≤3V							
DAC_P = 0mA, DAC_N = 2mA ±3%		Reg.14 = 0x00. Reg.15 = 0x00. {DAC_D9 : DAC_D0} = b'00000000 00' = 0							
DAC_P = 0.002mA, DAC_N = 1.998mA		Reg.14 = 0x00. Reg.15 = 0x01. {DAC_D9 : DAC_D0} = b'00000000 01' = 1							
... up to ...		... up to ...							
DAC_P = 1.996mA, DAC_N = 0.004mA		Reg.14 = 0xFF. Reg.15 = 0x02. {DAC_D9 : DAC_D0} = b'11111111 10' = 1022							
DAC_P = 1.998mA, DAC_N = 0.002mA		Reg.14 = 0xFF. Reg.15 = 0x03. {DAC_D9 : DAC_D0} = b'11111111 11' = 1023							

To use the 10-bit DAC for internal use as a 5-bit current source for the analog input multiplexer:

- Set the Current Mux Level register 5 Use IDAC bit D7 = 1 (Table 21 on page 38). This de-selects the 4-bit IDAC current source as the multiplexer current source, and allocates the 10-bit DAC instead
- The code range 0 to 31 in the 10-bit DAC registers 14 and 15 (Table 31 on page 47) sources an output current from 0 to 300µA to the analog input multiplexer
- Leave the DAC_P pin open, and terminate the DAC_N pin to either GND or AGND

From the Electrical Characteristics table, the multiplexer source current (including full scale current tolerance of 10µA and DAC INL of 2µA) follows Equation 9 below, where R_{IREF1} = 20kΩ ±1% resistor from the IREF1 pin to AGND:

$$Mux\_Current = \left(\{DAC\_D9 : DAC\_D0\} \times \frac{300 \pm 10}{31}\right) \pm 2\ \mu A$$

Equation 9. 10-bit DAC Transfer Characteristic For 5-bit Current Source

Example 1: [DAC_D9:DAC_D0] = b'00000010 00' = 8

$$Mux\_Current = \left(\{8\} \times \frac{300 \pm 10}{31}\right) \pm 2\ \mu A = 77.42\mu A \pm 4.58\mu A$$

Example 2: [DAC_D9:DAC_D0] = b'00000110 00' = 24

$$Mux\_Current = \left(24\} \times \frac{300 \pm 10}{31}\right) \pm 2\ \mu A = 232.26\mu A \pm 9.74\mu A$$

Table 31: Register addresses 14 and 15: 10-Bit DAC (as internal multiplexer current source)

Register Description	Register Address	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
10-Bit DAC MSB register	14 0x0E	DAC _D9	DAC _D8	DAC _D7	DAC _D6	DAC _D5	DAC _D4	DAC _D3	DAC _D2
Default register setting on POR or $\overline{\text{RESET}}$		0	0	0	0	0	0	0	0
10-Bit DAC LSB register		0	0	0	0	0	0	DAC _D1	DAC _D0
Default register setting on POR or $\overline{\text{RESET}}$		0	0	0	0	0	0	0	0
Only use {DAC_D9 : DAC_D0} codes in the range b'00000000 00' to b'00000111 11' (0 to 31)		Current Mux Level register 5 Use IDAC bit D7 = 1 (Table 21 on page 38), assigning the DAC_P output to internal use as the current source for the analog input multiplexer. Leave the DAC_P pin open, and connect the DAC_N pin to either GND or AGND							
Mux_Current = 0µA	14 0x0E and 15 0x0F	Reg.14 = 0x00. Reg.15 = 0x00. {DAC_D9 : DAC_D0} = b'00000000 00' = 0							
Mux_Current is set to 9.7µA ±2.3µA (±24%)		Reg.14 = 0x00. Reg.15 = 0x01. {DAC_D9 : DAC_D0} = b'00000000 01' = 1							
Mux_Current is set to 19.4µA ±2.6µA (±13.7%)		Reg.14 = 0x00. Reg.15 = 0x10. {DAC_D9 : DAC_D0} = b'00000000 10' = 2							
Mux_Current is set to 29µA ±3µA (±10.2%)		Reg.14 = 0x00. Reg.15 = 0x11. {DAC_D9 : DAC_D0} = b'00000000 11' = 3							
Mux_Current is set to 38.7µA ±3.3µA (±8.5%)		Reg.14 = 0x01. Reg.15 = 0x00. {DAC_D9 : DAC_D0} = b'00000001 00' = 4							
Mux_Current is set to 48.4µA ±3.6µA (±7.5%)		Reg.14 = 0x01. Reg.15 = 0x01. {DAC_D9 : DAC_D0} = b'00000001 01' = 5							
Mux_Current is set to 58.1µA ±3.9µA (±6.8%)		Reg.14 = 0x01. Reg.15 = 0x10. {DAC_D9 : DAC_D0} = b'00000001 10' = 6							
Mux_Current is set to 67.7µA ±4.3µA (±6.3%)		Reg.14 = 0x01. Reg.15 = 0x11. {DAC_D9 : DAC_D0} = b'00000001 11' = 7							
Mux_Current is set to 77.4µA ±4.6µA (±5.9%)		Reg.14 = 0x02. Reg.15 = 0x00. {DAC_D9 : DAC_D0} = b'00000010 00' = 8							
Mux_Current is set to 87.1µA ±4.9µA (±5.6%)		Reg.14 = 0x02. Reg.15 = 0x01. {DAC_D9 : DAC_D0} = b'00000010 01' = 9							
Mux_Current is set to 96.8µA ±5.2µA (±5.4%)		Reg.14 = 0x02. Reg.15 = 0x10. {DAC_D9 : DAC_D0} = b'00000010 10' = 10							
Mux_Current is set to 106.5µA ±5.5µA (±5.2%)		Reg.14 = 0x02. Reg.15 = 0x11. {DAC_D9 : DAC_D0} = b'00000010 11' = 11							
Mux_Current is set to 116.1µA ±5.9µA (±5.1%)		Reg.14 = 0x03. Reg.15 = 0x00. {DAC_D9 : DAC_D0} = b'00000011 00' = 12							
Mux_Current is set to 125.8µA ±6.2µA (±4.9%)		Reg.14 = 0x03. Reg.15 = 0x01. {DAC_D9 : DAC_D0} = b'00000011 01' = 13							
Mux_Current is set to 135.5µA ±6.5µA (±4.8%)		Reg.14 = 0x03. Reg.15 = 0x10. {DAC_D9 : DAC_D0} = b'00000011 10' = 14							
Mux_Current is set to 145.2µA ±6.8µA (±4.7%)		Reg.14 = 0x03. Reg.15 = 0x11. {DAC_D9 : DAC_D0} = b'00000011 11' = 15							
Mux_Current is set to 154.8µA ±7.2µA (±4.6%)		Reg.14 = 0x04. Reg.15 = 0x00. {DAC_D9 : DAC_D0} = b'00000100 00' = 16							
Mux_Current is set to 164.5µA ±7.5µA (±4.5%)		Reg.14 = 0x04. Reg.15 = 0x01. {DAC_D9 : DAC_D0} = b'00000100 01' = 17							
Mux_Current is set to 174.2µA ±7.8µA (±4.5%)		Reg.14 = 0x04. Reg.15 = 0x10. {DAC_D9 : DAC_D0} = b'00000100 10' = 18							
Mux_Current is set to 183.9µA ±8.1µA (±4.4%)		Reg.14 = 0x04. Reg.15 = 0x11. {DAC_D9 : DAC_D0} = b'00000100 11' = 19							
Mux_Current is set to 193.5µA ±8.5µA (±4.4%)		Reg.14 = 0x05. Reg.15 = 0x00. {DAC_D9 : DAC_D0} = b'00000101 00' = 20							
Mux_Current is set to 203.2µA ±8.8µA (±4.3%)		Reg.14 = 0x05. Reg.15 = 0x01. {DAC_D9 : DAC_D0} = b'00000101 01' = 21							
Mux_Current is set to 212.9µA ±9.1µA (±4.3%)		Reg.14 = 0x05. Reg.15 = 0x10. {DAC_D9 : DAC_D0} = b'00000101 10' = 22							
Mux_Current is set to 222.6µA ±9.4µA (±4.2%)		Reg.14 = 0x05. Reg.15 = 0x11. {DAC_D9 : DAC_D0} = b'00000101 11' = 23							
Mux_Current is set to 232.3µA ±9.7µA (±4.2%)		Reg.14 = 0x06. Reg.15 = 0x00. {DAC_D9 : DAC_D0} = b'00000110 00' = 24							
Mux_Current is set to 241.9µA ±10.1µA (±4.2%)		Reg.14 = 0x06. Reg.15 = 0x01. {DAC_D9 : DAC_D0} = b'00000110 01' = 25							
Mux_Current is set to 251.6µA ±10.4µA (±4.1%)		Reg.14 = 0x06. Reg.15 = 0x10. {DAC_D9 : DAC_D0} = b'00000110 10' = 26							
Mux_Current is set to 261.3µA ±10.7µA (±4.1%)		Reg.14 = 0x06. Reg.15 = 0x11. {DAC_D9 : DAC_D0} = b'00000110 11' = 27							
Mux_Current is set to 271µA ±11µA (±4.1%)		Reg.14 = 0x07. Reg.15 = 0x00. {DAC_D9 : DAC_D0} = b'00000111 00' = 28							
Mux_Current is set to 280.6µA ±11.4µA (±4%)		Reg.14 = 0x07. Reg.15 = 0x01. {DAC_D9 : DAC_D0} = b'00000111 01' = 29							
Mux_Current is set to 290.3µA ±11.7µA (±4%)		Reg.14 = 0x07. Reg.15 = 0x10. {DAC_D9 : DAC_D0} = b'00000111 10' = 30							
Mux_Current is set to 300µA ±10µA (±3.3%)		Reg.14 = 0x07. Reg.15 = 0x11. {DAC_D9 : DAC_D0} = b'00000111 11' = 31							

19.15 Register address 16: Calibration

The Calibration register 16 is used at the factory for calibration of the amplifier offset and testing of the multiplexer and programmable current sources. It contains 4 functions, only one of which may be active at a time (Table 32 on page 48 and Table 33 on page 48).

These functions affect the inputs to the instrumentation amplifier, the multiplexer current source, and over-ride the settings of the Non-Inverting Mux Channel Select register 3 (Table 19 on page 36) and/or the Inverting Mux Channel Select register 4 (Table 20 on page 37).

The I GND function causes the inverting input of the instrumentation amplifier to be connected to AGND. This provides a convenient ground connection for local single ended inputs without using the SE_RTN pin. The other 3 functions are available for periodic circuit testing by the system controller if required.

The setting in the Calibration register 16 is ignored (over-ridden) if one of more of the 4-bits [D6:D3] in the Power Status register 2 is set. These settings monitor the VREF, +5V, VEE, and VCC rails. See Table 18 on page 35.

Table 32. Calibration Register Function Details

Function Selected	Instrumentation Amplifier Modification	Function Behavior	Register Over-Ridden
I GND	Non-inverting input connected to multiplexer as normal Inverting input tied to AGND instead of multiplexer	This option connects the instrumentation amplifier's inverting input to GND internally. This allows the acquisition of a single-ended signal using only one CH input. The inverting input can alternatively be connected to an external GND via the SE_RTN pin using the Inverting Mux Channel Select register (Table 20 on page 37). See Figure 10 on page 26 for a connection example	Inverting Mux Channel Select register 4 (Table 20 on page 37)
NP Cont Check	Non-inverting input tied to VREF/2 instead of multiplexer Inverting input connected to the multiplexer current source (set as normal) as well as the multiplexer **See Figure 20 on page 49**	Use this setting to perform a continuity check of the instrumentation amplifier's inverting input multiplexer. An open multiplexer path (including input source) is detected by the current source pulling up the inverting input higher than VREF/2 causing the amplifier output to go low. If an external sensor is properly attached, the voltage read by the ADC is the difference of VREF/2 and the product of the current source and the impedance of the sensor plus the impedance of the two multiplexer switches encountered in the current path.	Non-Inverting Mux Channel Select register 3 (Table 19 on page 36) Current Mux Channel Select register 6 (Table 22 on page 39)
Cont Check	Non-inverting input connected to the multiplexer current source (set as normal) as well as the multiplexer Inverting input is connected to the multiplexer as normal **See Figure 21 on page 49**	Use this setting to perform a continuity check of the instrumentation amplifier's non-inverting input multiplexer. An open multiplexer path (including input source) is detected by the current source pulling up the non-inverting input causing the amplifier output to go high. A working multiplexer path allows the total resistance of the two multiplexers in series with the input source to be measured as a voltage drop due to the current source. If the inverting input is selected as the same channel input as the non-inverting input, then the resistance of the non-inverting input multiplexer can be measured	Current Mux Channel Select register 6 (Table 22 on page 39)
IA Short	Non-inverting input connected to multiplexer as normal Inverting input is tied to the non-inverting input	This option allows the instrumentation amplifier's offset and common mode errors to be measured	Inverting Mux Channel Select register 4 (Table 20 on page 37)

Table 33: Register 16: Calibration

Register Description		Register Address	Register Data							
			D7	D6	D5	D4	D3	D2	D1	D0
Power Status register		**16 0x10**	**IA Short**	**-**	**-**	**Cont Check**	**NP Cont Check**	**-**	**I GND**	**ISET**
Default register setting on POR or $\overline{\text{RESET}}$			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Factory test setting. Always write this register with ISET = 0		16 0x10	x	x	x	x	x	x	x	0
Unused register bits. Values written are stored and read back			x	0/1	0/1	x	x	0/1	x	0
Instrumentation amplifier's non-inverting input voltage is modified as follows:	**Instrumentation amplifier's inverting input voltage is modified as follows:**									
-	-		0	x	x	0	0	x	0	0
-	Tied to non-inverting input		1	x	x	x	x	x	x	0
-	Tied to AGND		0	x	x	x	x	x	1	0
Tied to VREF	Current source applied		0	x	x	x	1	x	0	0
Current source applied	-		0	x	x	1	0	x	0	0

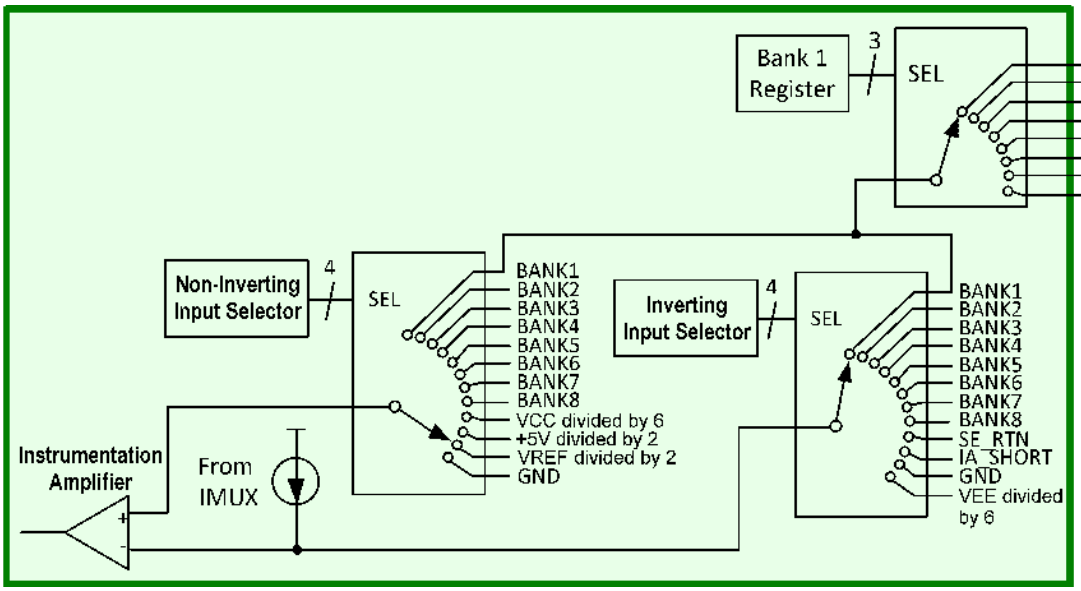


Figure 20. Inverting Multiplexer Terminal Continuity Check Connections (Calibration register 16 = 0x08)

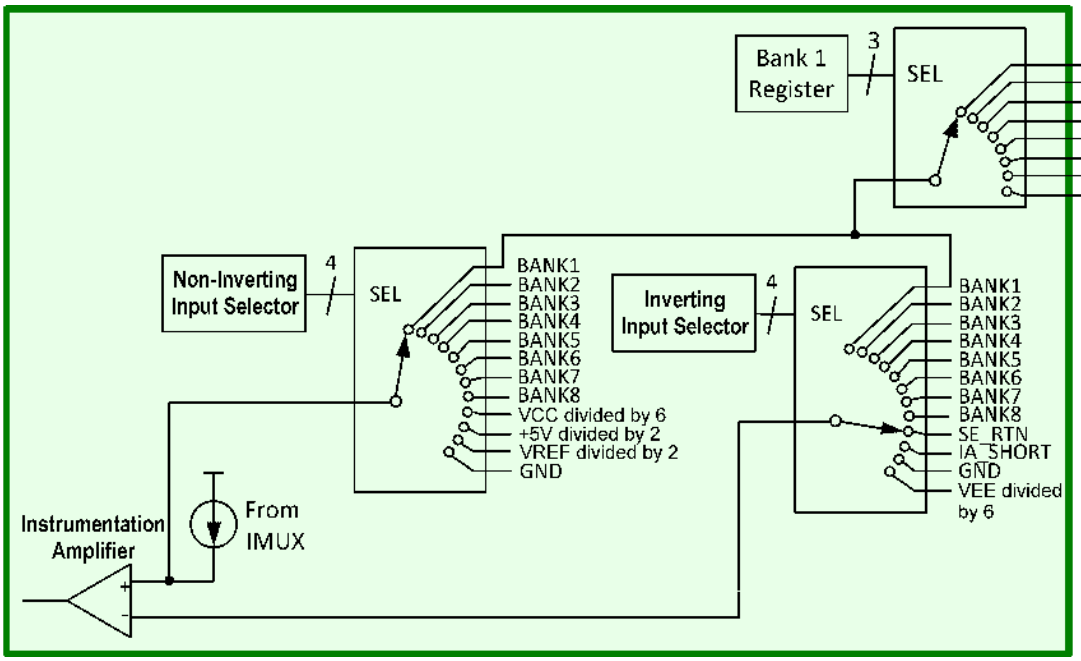


Figure 21. Continuity Check Connections (Calibration register 16 = 0x10)

19.16 Register address 17: OTP

The OTP register enables the user to temporarily over-ride the factory programmed OTP trim settings, and adjust the values as desired. The default values can be restored back from OTP via the same register. The default values are also restored from OTP when a reset is performed by either toggling the $\overline{\text{RESET}}$ pin or via the Master Reset register 0 (Table 16 on page 33).

To adjust any trim values, write 0x01 to register 17 (Table 34) to preload registers 18 to 22 with the factory programmed OTP settings. Then write 0x00 to register 17 to allow registers 18 to 22 to be written, but not enable those registers contents to be used by the LX7730 yet. Now make any changes to the Trim registers 18 to 23 (Table 35) in any order. Finally, active the use of the registers 18 to 22 as the trim settings by writing 0x02 to register 17.

The Trim registers 18 to 23 can be modified on the fly while activated (when register 17 = 0x02). Note however that the bits for ADCvtoi[4:0] and vtoi[4:0] are spread over two registers.

The offs[4:0] bits D3 to D0 in register 19 allow the total analog front end offset (instrumentation amplifier plus filters to the ADC input at ADC_IN to be adjusted. Adjustment are easily monitored using the ADC.

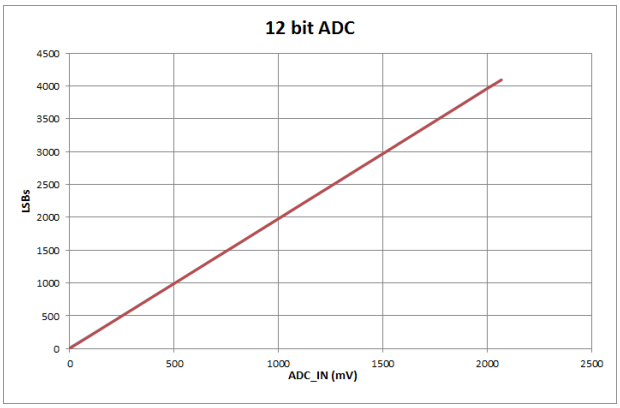
Table 34: Register 17: OTP

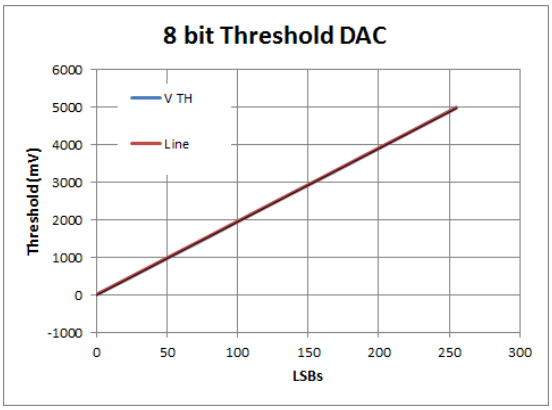
Register Description	Register Address	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
OTP register	**17 0x11**	-	-	-	-	-	-	**OTP out select**	**OTP in select**
Default register setting on POR or $\overline{\text{RESET}}$		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
No action	17 0x11	x	x	x	x	x	x	x	0
Registers 18 to 22 are loaded with the POR or $\overline{\text{RESET}}$ default settings		x	x	x	x	x	x	x	1
Trim values are set according to factory OTP values		x	x	x	x	x	x	0	x
Trim values are set according to the data in registers 18 to 22		x	x	x	x	x	x	1	x
Unused register bits. Values written are stored and read back		0/1	0/1	0/1	0/1	0/1	0/1	x	x

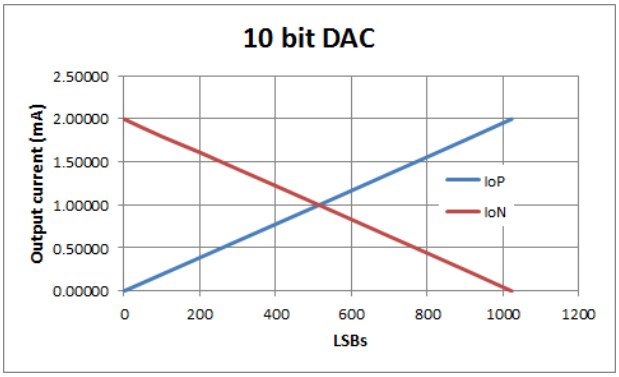
Table 35: Registers 18 to 22: Trim

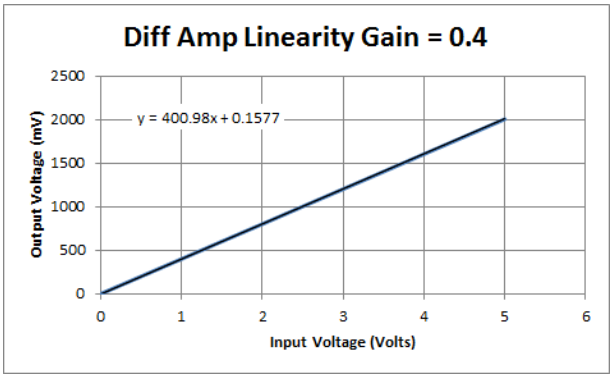
Register Description	Register Address	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Trim register 18	**18 0x12**	**cmux2**	**cmux1**	**cmux0**	**vref4**	**vref3**	**vref2**	**vref1**	**vref0**
VREF adjust		x	x	x	**vref[4:0]**				
10-bit IDAC reference adjust		**cmux[2:0]**			x	x	x	x	x
Trim register 19	**19 0x13**	**vbgtc3**	**vbgtc2**	**vbgtc1**	**vbgtc0**	**offs3**	**offs2**	**offs1**	**offs0**
Instrumentation amplifier offset adjust		x	x	x	x	**offs[3:0]**			
Bandgap temperature coefficient adjust		**vbgtc[3:0]**				x	x	x	x
Trim register 20	**20 0x14**	**vbg4**	**vbg3**	**vbg2**	**vbg1**	**vbg0**	**vtoi4**	**vtoi3**	**vtoi2**
Global current source adjust, trimmed first. Note: vtoi[4:0] is spread over registers 20 & 21		x	x	x	x	x	**vtoi[4:2]**		
Bandgap value adjust		**vbg[4:0]**					x	x	x
Trim register 21	**21 0x15**	**vtoi1**	**vtoi0**	**osc3**	**osc2**	**osc1**	**osc0**	**ADC vtoi4**	**ADC vtoi3**
ADC current reference adjust. Note: ADCvtoi[4:0] is spread over registers 20 & 22		x	x	x	x	x	x	**ADCvtoi[4:3]**	
Charge pump clock adjust		x	x	**osc[3:0]**				x	x
Global current source adjust, trimmed first. Note: vtoi[4:0] is spread over registers 20 & 21		**vtoi[1:0]**		x	x	x	x	x	x
Trim register 22	**22 0x16**	**ADC vtoi2**	**ADC vtoi1**	**ADC vtoi0**	-	-	-	-	-
Unused register bits. Values written are stored and read back		x	x	x	0/1	0/1	0/1	0/1	0/1
ADC current reference adjust. Note: ADCvtoi[4:0] is spread over registers 20 & 22		**ADCvtoi[2:0]**			x	x	x	x	x
Trim register 23	**23 0x17**	**lo_dis**	-	-	-	-	-	-	-
Unused register bits. Values written are stored and read back		x	0/1	0/1	0/1	0/1	0/1	0/1	0/1
No action		0	x	x	x	x	x	x	x
Take all I/O pins Hi-Z for input threshold testing		1	x	x	x	x	x	x	x

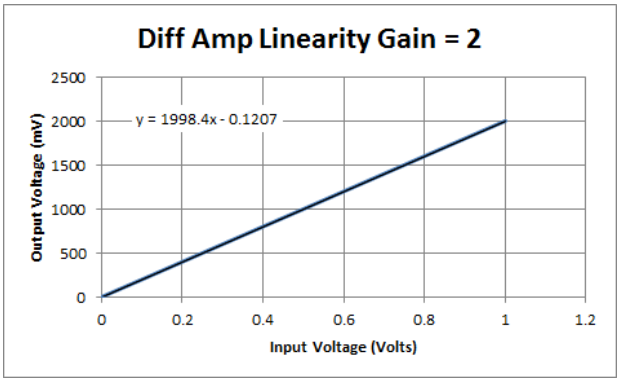
20 Characteristic Curves

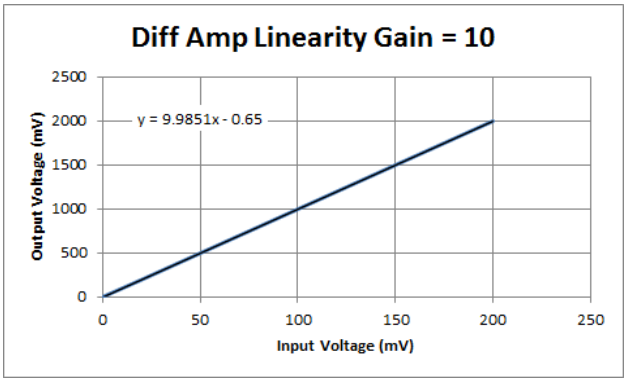


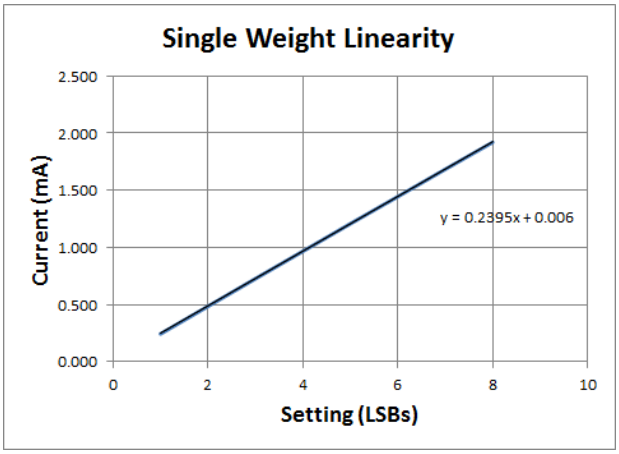


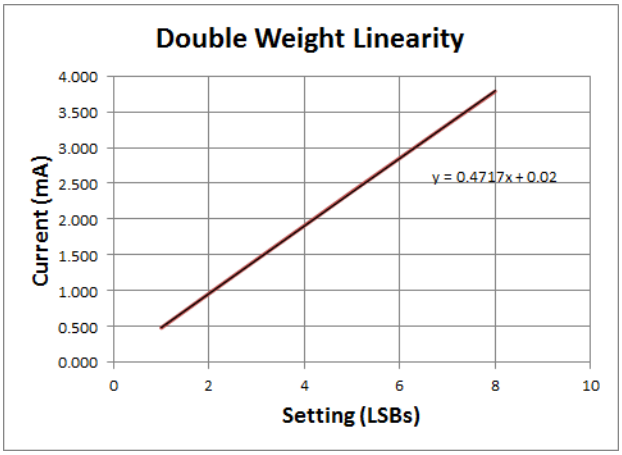


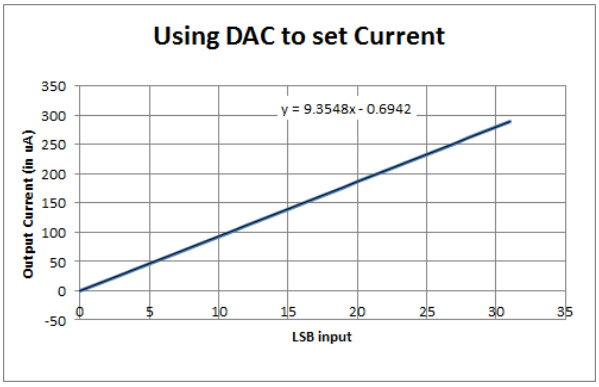


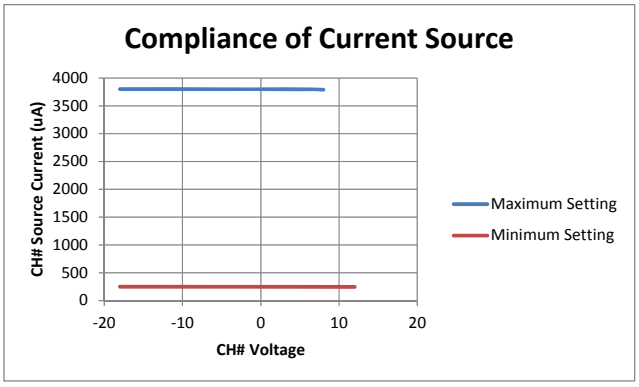




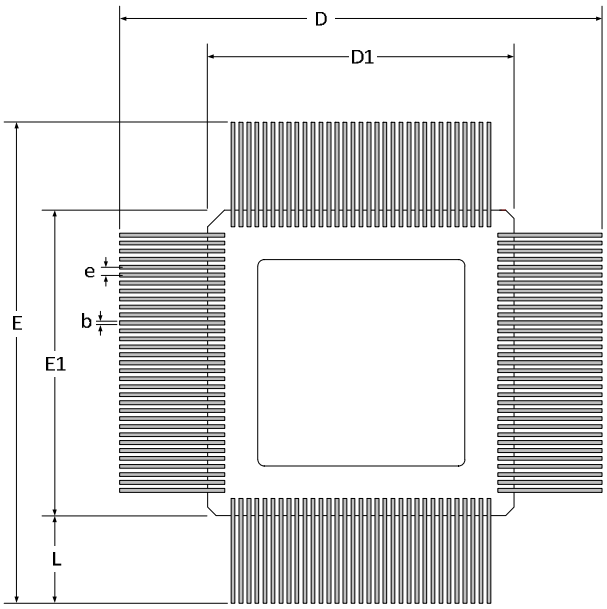


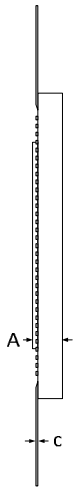






21 CQFP-132 (Ceramic Quad Flat Pack) Dimensions





Dim	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	1.93	2.39	0.076	0.094
b	0.23	0.33	0.009	0.013
c	0.125	0.20	0.0049	0.0079
D	39.37 typ		1.55 typ	
D1	24.00	24.26	0.945	0.955
e	0.635 BSC		0.025 BSC	
E	39.37 typ		1.55 typ	
E1	24.00	24.25	0.945	0.955
L	7.62 typ		0.30 typ	

Figure 22. CQFP-132 Package Dimensions

Note:
1. Package includes non-conductive ceramic tie-bars mechanically connected to all pins
2. Parts are shipped with untrimmed and unformed leads
3. Package mass is 4.6g typ with 14mm leads (trimmed flush with non-conductive ceramic tie-bars, tie bars discarded)
4. The metal package top is electrically isolated from the body of the package
5. The lid and lead material is Kovar with NiAu plating

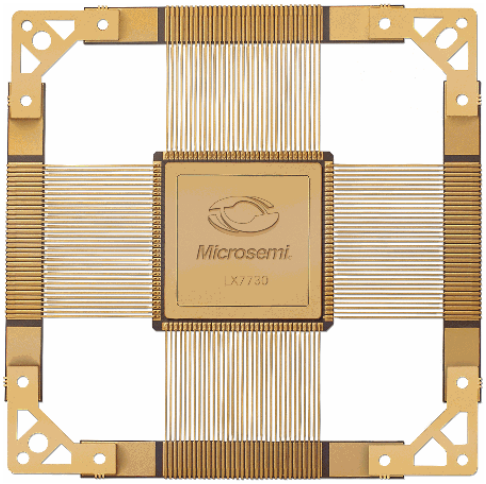
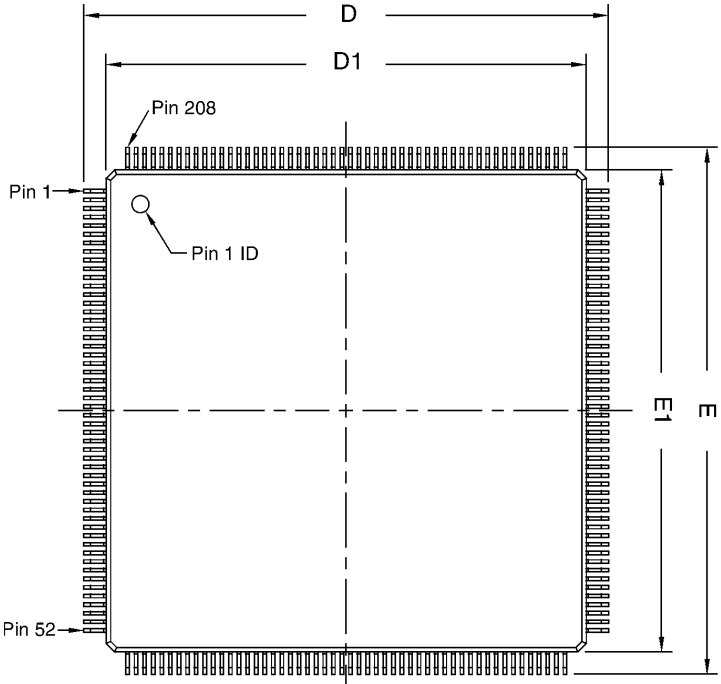
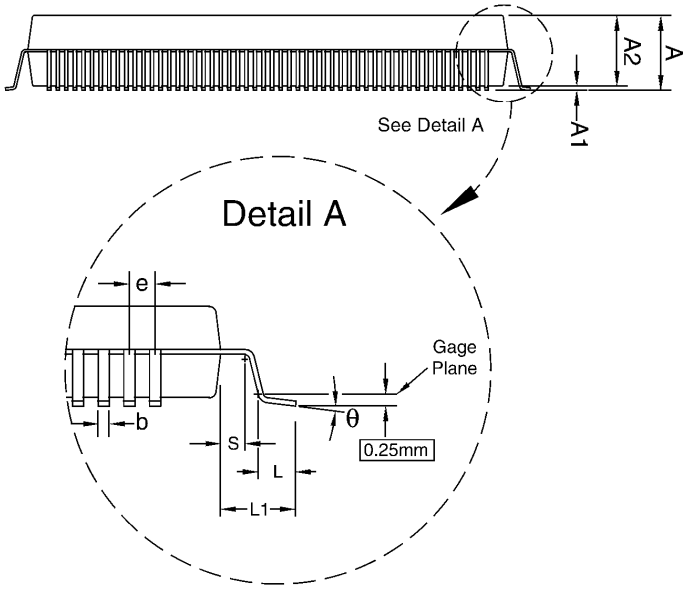


Figure 23. Package as shipped with non-conductive ceramic tie-bars, untrimmed and unformed leads

22 QFP-208 (Metric Quad Flat Pack) Dimensions





Dim	Millimeters			Inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	3.70	4.07	-	0.146	0.160
A1	0.25	0.33	-	0.010	0.013	-
A2	3.20	2.37	3.60	0.126	0.093	0.142
b	0.17	0.22	0.27	0.007	0.009	0.011
D	30.60 BSC			1.20 BSC		
D1	28.00 BSC			1.10 BSC		
e	0.50 BSC			0.01969		
E	30.60 BSC			1.20 BSC		
E1	28.00 BSC			1.10 BSC		
L	0.50	0.60	0.75	0.020	0.024	0.030
L1	1.30 REF			0.051 REF		
S	0.40	-	-	0.016	-	-
Θ	0°	-	7°	0°	-	7°

Notes

1. Copper lead material with Pb-free matte Sn lead finish
2. JEDEC outline reference: MS-029 variation FA-1
3. Mold compound is G700M
4. Package mass is 6.5g typ

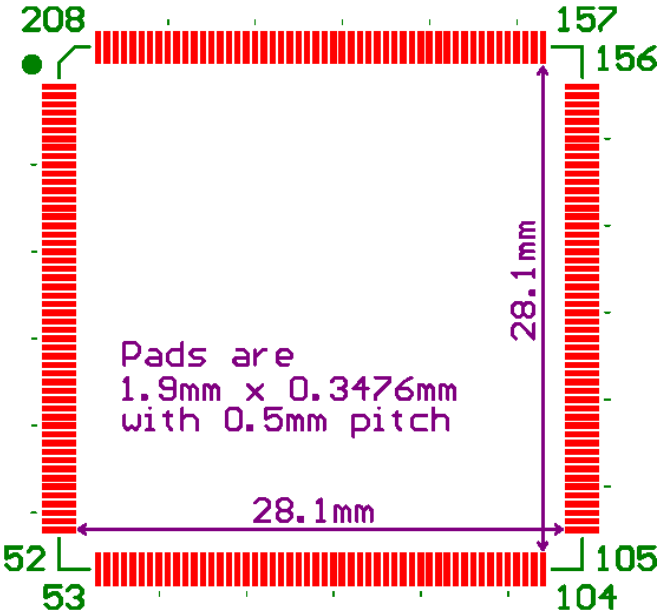


Figure 24. QFP-132 Typical PCB Foil Pattern (0.006" gap between pads)

23 Change Log

Date	Issue	Changes
2018-05-10	1.4	Release before change log started
2019-07-12	2.0	Electrical characteristic table changes: ESD susceptibility in Absolute Maximum Ratings split into two lines for clarity. Data sheet body revised significantly for clarity
2019-09-09	2.1	Typos fixed in text, Tables 4 & 5. Added maximum limit for operating current with external VEE to EC table. Added package mass
2019-10-31	2.2	Low power version added (VCC operating current I_{VCC} reduced from 85mA maximum to 78mA, VCC standby current I_{VCC} reduced from 7mA maximum to 6.75mA). CLK pin clarified as 125kHz to 500kHz clock. Parallel interface figures merged into one for clarity. Details and guidelines added for register 8 operations
2020-01-24	2.3	QFP-208 plastic package added
2020-06-10	2.4	Section 14 expanded to clarify operation with negative-going single-ended inputs. Noted that CQFP-132 ES part is not hermetic, lid and lead material is Kovar, and lid is isolated. Typo in section 1 title. Typo in Table 1 used $\overline{\text{RESET}}$ instead of $\overline{\text{EXT\_REF}}$. Typos in EC Table used LX7300 instead of LX7730. Corrected flows for LMMF-V and LMMF-Q in ordering table. Clarified krad to krad(Si) and added SAM3X8ERT to first page. Swapped QFP-208 and CQFP-132 pin configuration drawings to match pin description order. Clarified that SPI transactions must be 15 bits long. Split Table 13 into two tables. Added heatsinking section. Noted in section 15.1.1 and Figure 9 that SE_RTN is available as a differential inverting input.

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