

2.7-V TO 5.5-V LOW-POWER DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTER WITH INTERNAL REFERENCE AND POWER DOWN

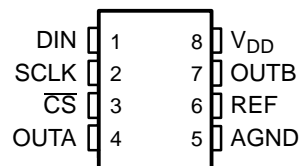
FEATURES

- Dual 12-Bit Voltage Output DAC
- Programmable Internal Reference
- Programmable Settling Time:
 - 1 μ s in Fast Mode,
 - 3.5 μ s in Slow Mode
- Compatible With TMS320 and SPI™ Serial Ports
- Differential Nonlinearity <0.5 LSB Typ
- Monotonic Over Temperature

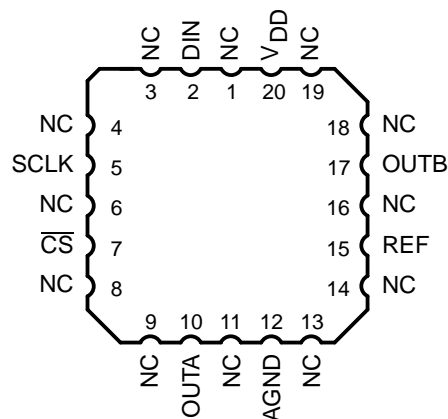
APPLICATIONS

- Digital Servo Control Loops
- Digital Offset and Gain Adjustment
- Industrial Process Control
- Machine and Motion Control Devices
- Mass Storage Devices

D, JG PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



DESCRIPTION

The TLV5638 is a dual 12-bit voltage output DAC with a flexible 3-wire serial interface. The serial interface allows glueless interface to TMS320, SPI™, QSPI™, and Microwire™ serial ports. It is programmed with a 16-bit serial string containing 4 control and 12 data bits.

The resistor string output voltage is buffered by a x2 gain rail-to-rail output buffer. The buffer features a Class AB output stage to improve stability and reduce settling time. The programmable settling time of the DAC allows the designer to optimize speed vs power dissipation. With its on-chip programmable precision voltage reference, the TLV5638 simplifies overall system design.

Because of its ability to source up to 1 mA, the reference can also be used as a system reference. Implemented with a CMOS process, the device is designed for single supply operation from 2.7 V to 5.5 V. It is available in an 8-pin SOIC package to reduce board space in standard commercial, industrial, and automotive temperature ranges. It is also available in JG and FK packages in the military temperature range.



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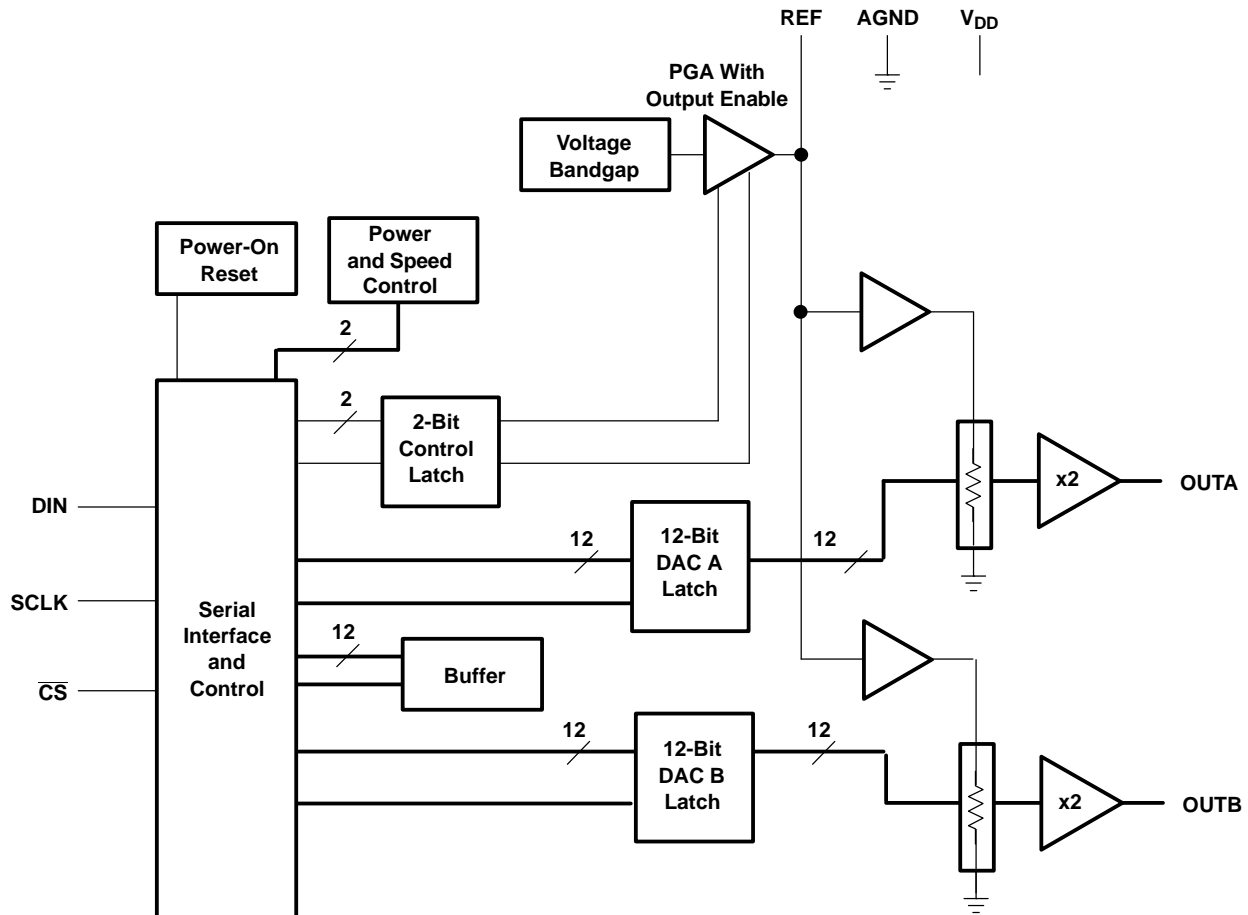
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS

| T _A | PACKAGE | | |
|----------------|-------------------------|------------------|------------------|
| | SOIC (D) | CERAMIC DIP (JG) | 20 PAD LCCC (FK) |
| 0°C to 70°C | TLV5638CD | — | — |
| 40°C to 85°C | TLV5638ID | — | — |
| 40°C to 125°C | TLV5638QD TLV5638QDR | — | — |
| 55°C to 125°C | — | TLV5638MJG | TLV5638MFK |

FUNCTIONAL BLOCK DIAGRAM



Terminal Functions

| TERMINAL NAME | NO. | I/O/P | DESCRIPTION |
|------------------|-----|-------|--|
| AGND | 5 | P | Ground |
| \overline{CS} | 3 | I | Chip select. Digital input active low, used to enable/disable inputs |
| DIN | 1 | I | Digital serial data input |
| OUT A | 4 | O | DAC A analog voltage output |
| OUT B | 7 | O | DAC B analog voltage output |
| REF | 6 | I/O | Analog reference voltage input/output |
| SCLK | 2 | I | Digital serial clock input |
| V _{DD} | 8 | P | Positive power supply |

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | UNIT | |
|--|-----------------------------------|----------------|
| Supply voltage (V _{DD} to AGND) | 7 V | |
| Reference input voltage range | -0.3 V to V _{DD} + 0.3 V | |
| Digital input voltage range | -0.3 V to V _{DD} + 0.3 V | |
| Operating free-air temperature range, T _A | TLV5638C | 0°C to 70°C |
| | TLV5638I | -40°C to 85°C |
| | TLV5638Q | -40°C to 125°C |
| | TLV5638M | -55°C to 125°C |
| Storage temperature range, T _{stg} | -65°C to 150°C | |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C | |

(1) Stresses beyond those listed under „ absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under „ recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE T _A = 25°C ⁽¹⁾ | T _A = 70°C POWER RATING | T _A = 85°C POWER RATING | T _A = 125°C POWER RATING |
|---------|---------------------------------------|---|---------------------------------------|---------------------------------------|--|
| D | 635 mW | 5.08 mW/°C | 407 mW | 330 mW | 127 mW |
| FK | 1375 mW | 11.00 mW/°C | 880 mW | 715 mW | 275 mW |
| JG | 1050 mW | 8.40 mW/°C | 672 mW | 546 mW | 210 mW |

(1) This is the inverse of the traditional Junction-to-Ambient thermal Resistance (R_{θJA}). Thermal Resistances are not production tested and are for informational purposes only.

RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|--------------------------------------|-----------------------|-------|----------------------|------|
| Supply voltage, V _{DD} | V _{DD} = 5 V | 4.5 | 5 | 5.5 | V |
| | V _{DD} = 3 V | 2.7 | 3 | 3.3 | V |
| Power on reset, POR | | 0.55 ⁽¹⁾ | | 2 ⁽¹⁾ | V |
| High-level digital input voltage, V _{IH} | V _{DD} = 2.7 V | 2 | | | V |
| | V _{DD} = 5.5 V | 2.4 | | | |
| Low-level digital input voltage, V _{IL} | V _{DD} = 2.7 V | | | 0.6 | V |
| | V _{DD} = 5.5 V | TLV5638C and TLV5638I | | 1 | V |
| | | TLV5638Q and TLV5638M | | 0.8 | |
| Reference voltage, V _{ref} to REF terminal | V _{DD} = 5 V ⁽²⁾ | AGND | 2.048 | V _{DD} -1.5 | V |
| Reference voltage, V _{ref} to REF terminal | V _{DD} = 3 V ⁽²⁾ | AGND | 1.024 | V _{DD} -1.5 | V |
| Load resistance, R _L | | 2 | | | kΩ |
| Load capacitance, C _L | | | | 100 | pF |
| Clock frequency, f _{CLK} | | | | 20 | MHz |
| Operating free-air temperature, T _A | TLV5638C | 0 | | 70 | °C |
| | TLV5638I | 40 | | 85 | |
| | TLV5638Q | 40 | | 125 | |
| | TLV5638M | 55 | | 125 | |

- (1) This parameter is not tested for Q and M suffix devices.
- (2) Due to the x2 output buffer, a reference input voltage ≥ (V_{DD}-0.4 V)/2 causes clipping of the transfer function. The output buffer of the internal reference must be disabled, if an external reference is used.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions, V_{ref} = 2.048 V, V_{ref} = 1.024 V (unless otherwise noted)

| POWER SUPPLY | | | | | | |
|--------------------------------------|---|-------------------------------------|-------------------------|-----|-----|------|
| PARAMETER | TEST CONDITIONS | | TLV5638C, I TLV5638M | | | UNIT |
| | | | MIN | TYP | MAX | |
| I _{DD} Power supply current | No load, All inputs = AGND or V _{DD} , DAC latch = 0x800 | V _{DD} = 5 V, Int. ref. | Fast | 4.3 | 7 | mA |
| | | | Slow | 2.2 | 3.6 | |
| | | V _{DD} = 3 V, Int. ref. | Fast | 3.8 | 6.3 | mA |
| | | | Slow | 1.8 | 3.0 | |
| | | V _{DD} = 5 V, Ext. ref. | Fast | 3.9 | 6.3 | mA |
| | | | Slow | 1.8 | 3.0 | |
| | | V _{DD} = 3 V, Ext. ref. | Fast | 3.5 | 5.7 | mA |
| | | | Slow | 1.5 | 2.6 | |
| Power-down supply current | | | 0.01 | 10 | μA | |
| PSRR Power supply rejection ratio | Zero scale, ⁽¹⁾ | | | 65 | dB | |
| | Full scale, ⁽²⁾ | | | 65 | | |

- (1) Power supply rejection ratio at zero scale is measured by varying V_{DD} and is given by: PSRR = 20 log [(E_{ZS}(V_{DD}max) - E_{ZS}(V_{DD}min))/V_{DD}max]
- (2) Power supply rejection ratio at full scale is measured by varying V_{DD} and is given by: PSRR = 20 log [(E_G(V_{DD}max) - E_G(V_{DD}min))/V_{DD}max]

ELECTRICAL CHARACTERISTICS (Continued)

 over recommended operating conditions, $V_{ref} = 2.048\text{ V}$, $V_{ref} = 1.024\text{ V}$ (unless otherwise noted)

| STATIC DAC SPECIFICATIONS | | | | | | | |
|--|---|--|------------------|-------|-------|--------------|----------------|
| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
| Resolution | | | | 12 | | | bits |
| INL | Integral nonlinearity, end point adjusted | See (1) | C and I suffixes | | ±1.7 | ±4 | LSB |
| | | | Q and M suffixes | | ±1.7 | ±6 | LSB |
| DNL | Differential nonlinearity | See (2) | | | ±0.4 | ±1 | LSB |
| E_{ZS} | Zero-scale error (offset error at zero scale) | See (3) | | | | ±24 | mV |
| $E_{ZS}TC$ | Zero-scale-error temperature coefficient | See (4) | | | 10 | | ppm/°C |
| E_G | Gain error | See (5) | | | | ±0.6 | % full scale V |
| E_GTC | Gain error temperature coefficient | See (6) | | | 10 | | ppm/°C |
| OUTPUT SPECIFICATIONS | | | | | | | |
| V_O | Output voltage | $R_L = 10\text{ k}\Omega$ | | 0 | | $V_{DD}-0.4$ | V |
| | Output load regulation accuracy | $V_O = 4.096\text{ V}, 2.048\text{ V}, R_L = 2\text{ k}\Omega$ | | | | ±0.25 | % full scale V |
| REFERENCE PIN CONFIGURED AS OUTPUT (REF) | | | | | | | |
| $V_{ref}(OUTL)$ | Low reference voltage | | | 1.003 | 1.024 | 1.045 | V |
| $V_{ref}(OUTH)$ | High reference voltage | $V_{DD} > 4.75\text{ V}$ | | 2.027 | 2.048 | 2.069 | V |
| $I_{ref}(\text{source})$ | Output source current | | | | | 1 | mA |
| $I_{ref}(\text{sink})$ | Output sink current | | | -1 | | | mA |
| | Load capacitance | | | | | 100 | pF |
| PSRR | Power supply rejection ratio | | | | -65 | | dB |
| REFERENCE PIN CONFIGURED AS INPUT (REF) | | | | | | | |
| V_I | Input voltage | | | 0 | | $V_{DD}-1.5$ | V |
| R_I | Input resistance | | | | 10 | | M Ω |
| C_I | Input capacitance | | | | 5 | | pF |
| | Reference input bandwidth | REF = $0.2 V_{pp} + 1.024\text{ V dc}$ | Fast | | 1.3 | | MHz |
| | | | Slow | | 525 | | kHz |
| | Reference feedthrough | REF = $1 V_{pp}$ at 1.024 V dc (7) | | | -80 | | dB |
| DIGITAL INPUTS | | | | | | | |
| I_{IH} | High-level digital input current | $V_I = V_{DD}$ | | | | 1 | μA |
| I_{IL} | Low-level digital input current | $V_I = 0\text{ V}$ | | -1 | | | μA |
| C_i | Input capacitance | | | | 8 | | pF |

- (1) The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors. Tested from code 32 to 4095.
- (2) The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
- (3) Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
- (4) Zero-scale-error temperature coefficient is given by: $E_{ZS} TC = [E_{ZS}(T_{max}) - E_{ZS}(T_{min})]/V_{ref} \times 10^6 / (T_{max} - T_{min})$.
- (5) Gain error is the deviation from the ideal output ($2V_{ref} - 1\text{ LSB}$) with an output load of $10\text{ k}\Omega$ excluding the effects of the zero-error.
- (6) Gain temperature coefficient is given by: $E_G TC = [E_G(T_{max}) - E_G(T_{min})]/V_{ref} \times 10^6 / (T_{max} - T_{min})$.
- (7) Reference feedthrough is measured at the DAC output with an input code = $0x000$.

ELECTRICAL CHARACTERISTICS (Continued)

over recommended operating conditions, $V_{ref} = 2.048\text{ V}$, $V_{ref} = 1.024\text{ V}$ (unless otherwise noted)

| ANALOG OUTPUT DYNAMIC PERFORMANCE | | | | | | |
|-----------------------------------|------------------------------------|--|------|-----|--------------------------|------------------------|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| $t_{s(FS)}$ | Output settling time, full scale | $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, See ⁽¹⁾ | Fast | 1 | 3 | μs |
| | | | Slow | 3.5 | 7 | |
| $t_{s(CC)}$ | Output settling time, code to code | $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, See ⁽²⁾ | Fast | 0.5 | 1.5 | μs |
| | | | Slow | 1 | 2 | |
| SR | Slew rate | $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, See ⁽³⁾ | Fast | 12 | | $\text{V}/\mu\text{s}$ |
| | | | Slow | 1.8 | | |
| Glitch energy | | $\text{DIN} = 0\text{ to }1$, $\text{FCLK} = 100\text{ kHz}$, $\overline{\text{CS}} = V_{DD}$ | 5 | | $\text{nV}\cdot\text{s}$ | |
| SNR | Signal-to-noise ratio | $f_s = 480\text{ kSPS}$, $f_{out} = 1\text{ kHz}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$ | 69 | 74 | dB | |
| S/(N+D) | Signal-to-noise + distortion | | 58 | 67 | | |
| THD | Total harmonic distortion | | 69 | 57 | | |
| Spurious free dynamic range | | | 57 | 72 | | |

- (1) Settling time is the time for the output signal to remain within $\pm 0.5\text{ LSB}$ of the final measured value for a digital input code change of $0x020$ to $0xFDF$ and $0xFDF$ to $0x020$ respectively. Not tested, assured by design.
- (2) Settling time is the time for the output signal to remain within $\pm 0.5\text{ LSB}$ of the final measured value for a digital input code change of one count. Not tested, assured by design.
- (3) Slew rate determines the time it takes for a change of the DAC output from 10% to 90% full-scale voltage.

DIGITAL INPUT TIMING REQUIREMENTS

| | MIN | NOM | MAX | UNIT |
|---|-----|-----|-----|------|
| $t_{su(CS-CK)}$ Setup time, $\overline{\text{CS}}$ low before first negative SCLK edge | 10 | | | ns |
| $t_{su(C16-CS)}$ Setup time, 16 th negative SCLK edge (when D0 is sampled) before $\overline{\text{CS}}$ rising edge | 10 | | | ns |
| t_{wH} SCLK pulse width high | 25 | | | ns |
| t_{wL} SCLK pulse width low | 25 | | | ns |
| $t_{su(D)}$ Setup time, data ready before SCLK falling edge | 10 | | | ns |
| $t_{h(D)}$ Hold time, data held valid after SCLK falling edge | 5 | | | ns |

PARAMETER MEASUREMENT INFORMATION

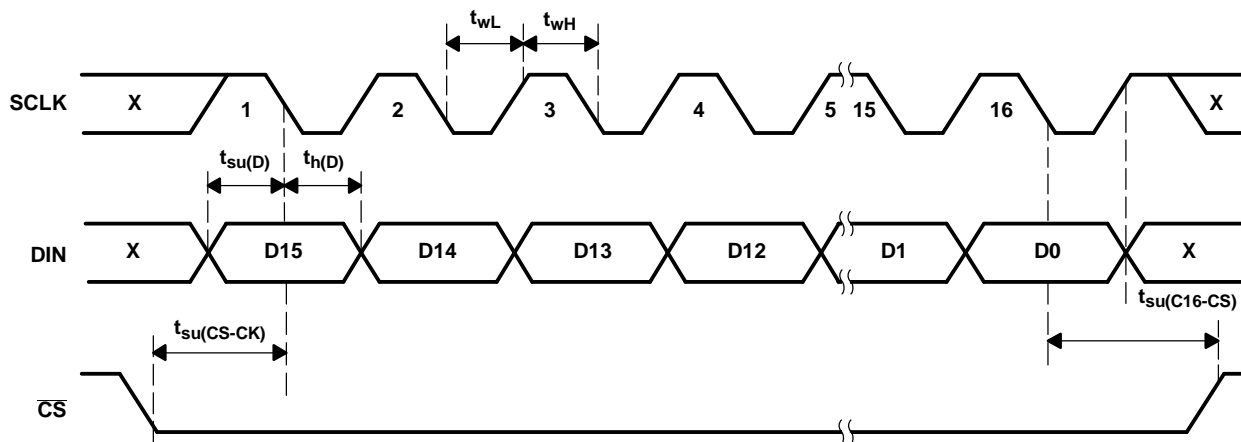


Figure 1. Timing Diagram

TYPICAL CHARACTERISTICS

**POWER DOWN SUPPLY CURRENT
VS
TIME**

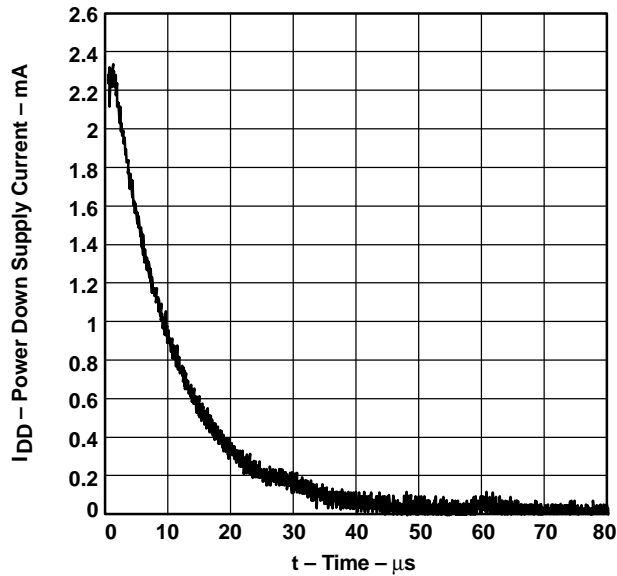


Figure 2.

**SUPPLY CURRENT
VS
FREE-AIR TEMPERATURE**

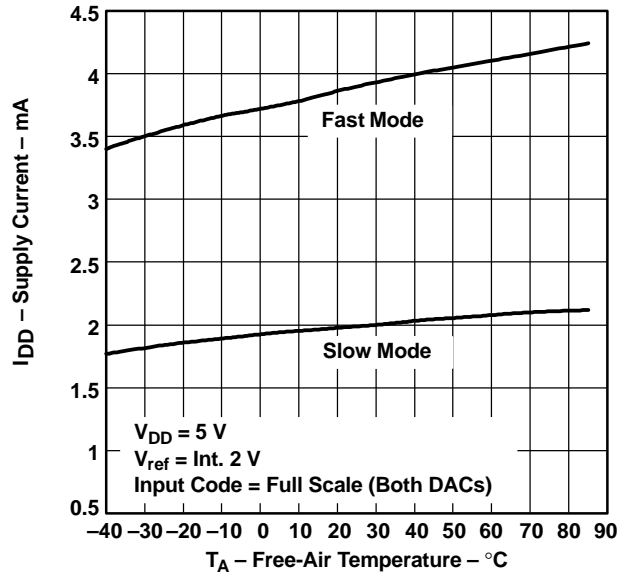


Figure 3.

**SUPPLY CURRENT
VS
FREE-AIR TEMPERATURE**

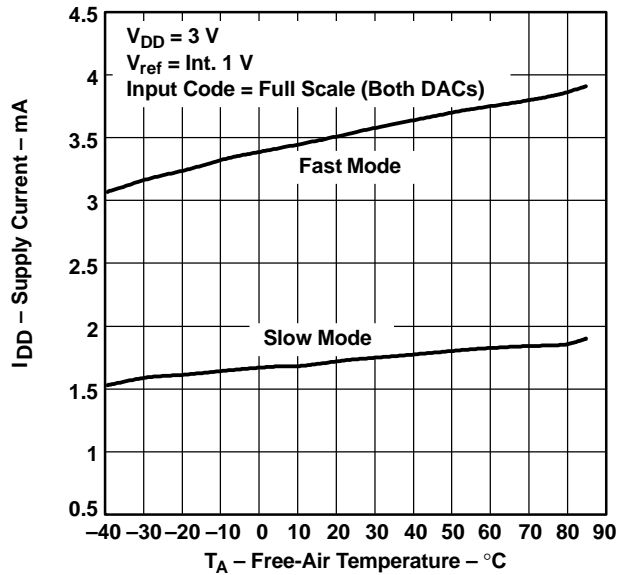


Figure 4.

**OUTPUT VOLTAGE
VS
LOAD CURRENT**

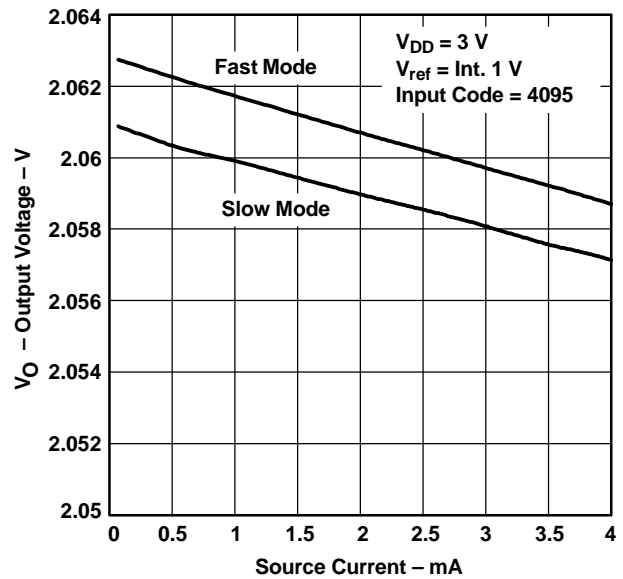


Figure 5.

TYPICAL CHARACTERISTICS (continued)

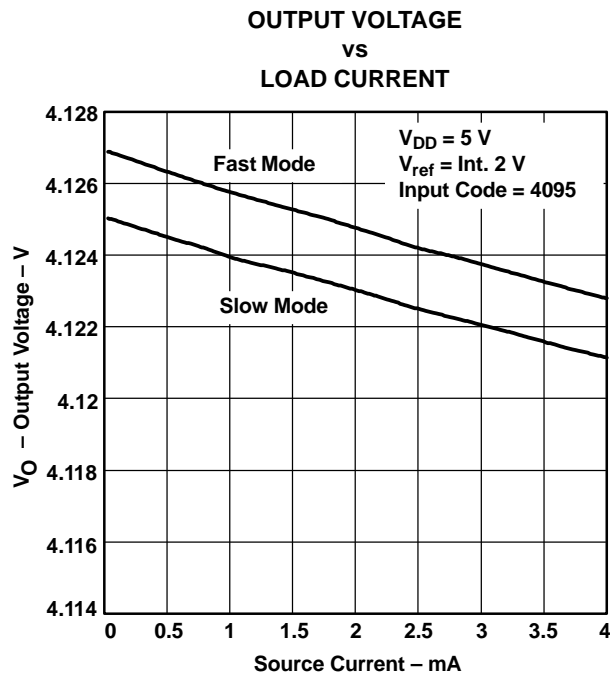


Figure 6.

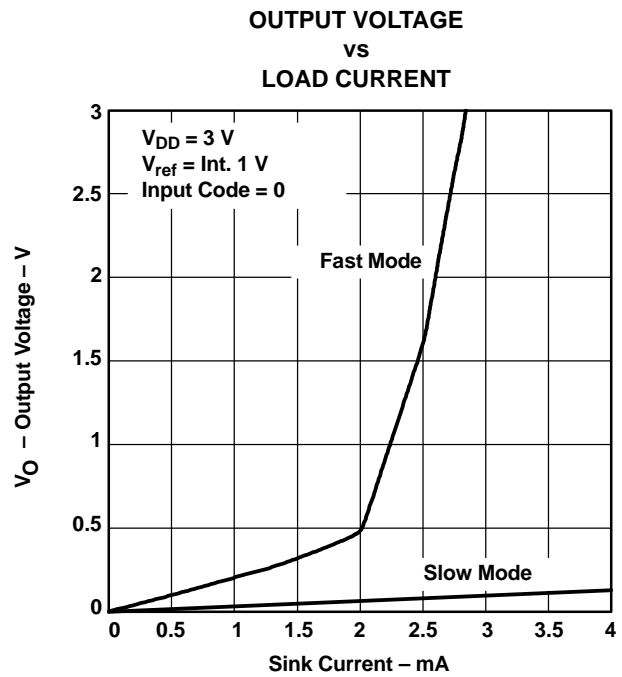


Figure 7.

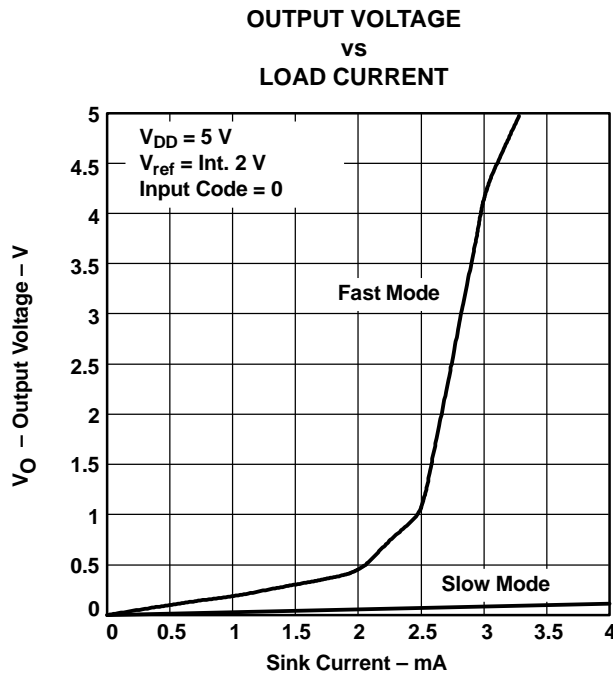


Figure 8.

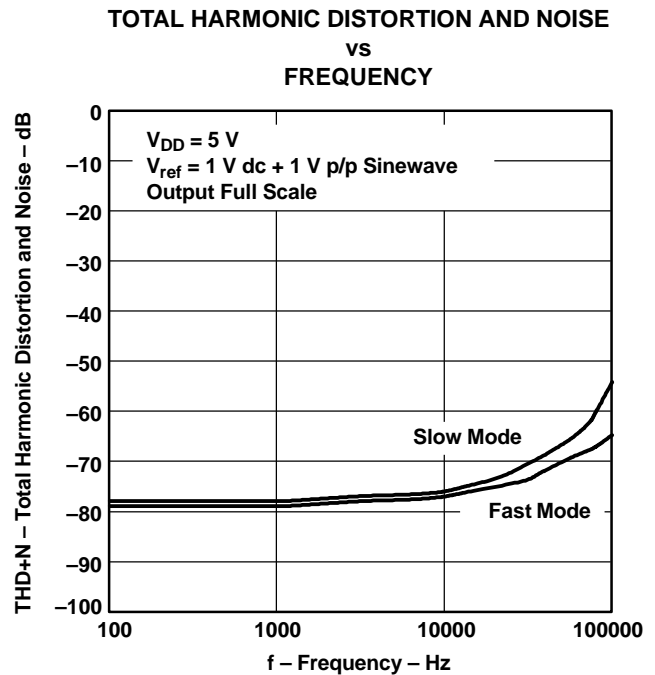


Figure 9.

TYPICAL CHARACTERISTICS (continued)

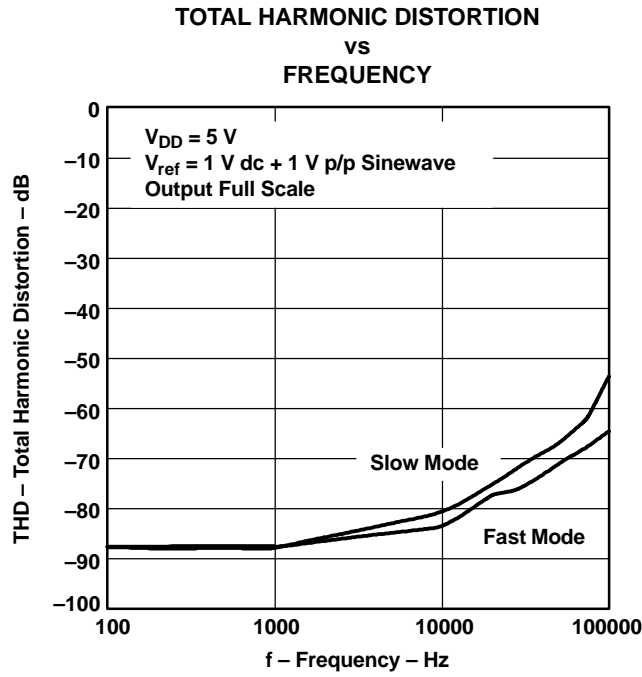
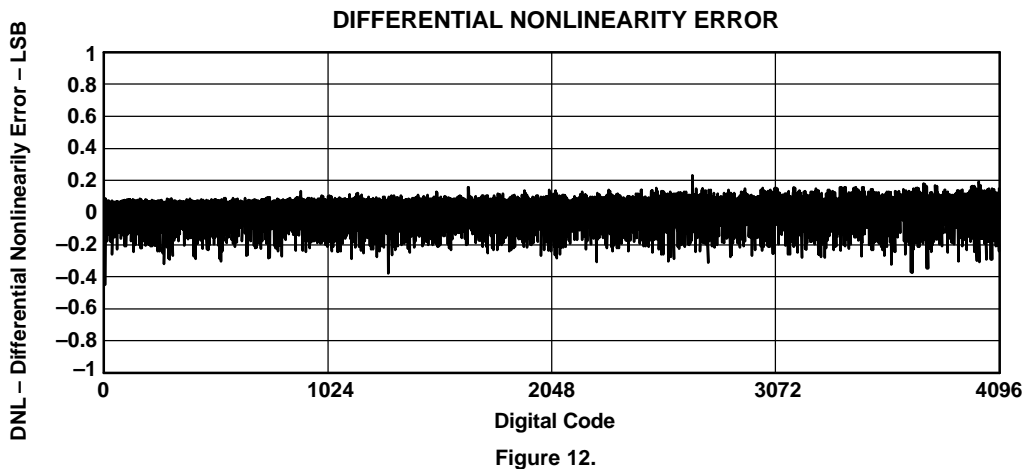
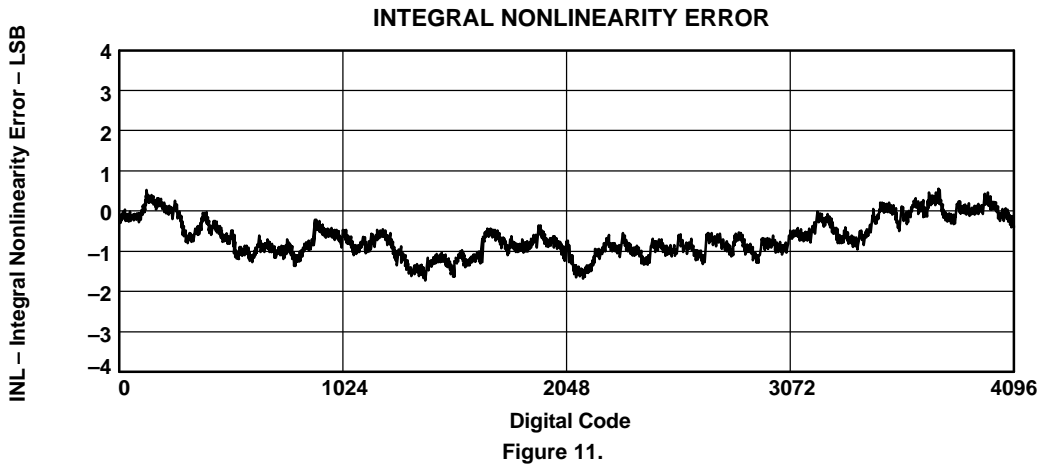


Figure 10.



APPLICATION INFORMATION

GENERAL FUNCTION

The TLV5638 is a dual 12-bit, single supply DAC, based on a resistor string architecture. It consists of a serial interface, a speed and power-down control logic, a programmable internal reference, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by reference) is given by:

$$2 \text{ REF } \frac{\text{CODE}}{0x1000} \text{ [V]}$$

Where REF is the reference voltage and CODE is the digital input value in the range 0x000 to 0xFFFF. A power on reset initially puts the internal latches to a defined state (all bits zero).

SERIAL INTERFACE

A falling edge of $\overline{\text{CS}}$ starts shifting the data bit-per-bit (starting with the MSB) to the internal register on the falling edges of SCLK. After 16 bits have been transferred or $\overline{\text{CS}}$ rises, the content of the shift register is moved to the target latches (DAC A, DAC B, BUFFER, CONTROL), depending on the control bits within the data word.

Figure 13 shows examples of how to connect the TLV5638 to TMS320, SPI™, and Microwire™.

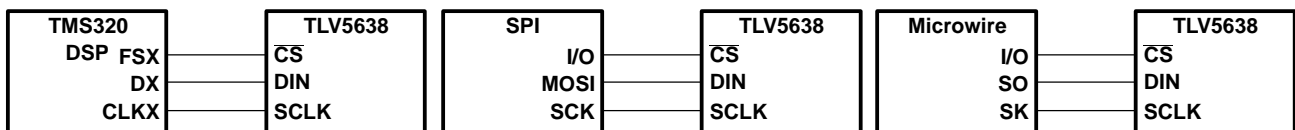


Figure 13. Three-Wire Interface

Notes on SPI™ and Microwire™: Before the controller starts the data transfer, the software has to generate a falling edge on the pin connected to $\overline{\text{CS}}$. If the word width is 8 bits (SPI™ and Microwire™), two write operations must be performed to program the TLV5638. After the write operation(s), the holding registers or the control register are updated automatically on the 16th positive clock edge.

SERIAL CLOCK FREQUENCY AND UPDATE RATE

The maximum serial clock frequency is given by:

$$f_{\text{sclkmax}} = \frac{1}{t_{\text{whmin}} + t_{\text{wlmin}}} = 20 \text{ MHz}$$

The maximum update rate is:

$$f_{\text{updatemax}} = \frac{1}{16 (t_{\text{whmin}} + t_{\text{wlmin}})} = 1.25 \text{ MHz}$$

Note, that the maximum update rate is just a theoretical value for the serial interface, as the settling time of the TLV5638 has to be considered, too.

EXAMPLES OF OPERATION:

1. Set DAC A output, select fast mode, select internal reference at 2.048 V:

a. Set reference voltage to 2.048 V (CONTROL register)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

b. Write new DAC A value and update DAC A output:

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|------------------------|-----|----|----|----|----|----|----|----|----|----|----|
| 1 | 1 | 0 | 0 | New DAC A output value | | | | | | | | | | | |

The DAC A output is updated on the rising clock edge after D0 is sampled.

To output data consecutively using the same DAC configuration, it is not necessary to program the CONTROL register again.

2. Set DAC B output, select fast mode, select external reference:

a. Select external reference (CONTROL register):

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

b. Write new DAC B value to BUFFER and update DAC B output:

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|---|-----|----|----|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 0 | New BUFFER content and DAC B output value | | | | | | | | | | | |

The DAC A output is updated on the rising clock edge after D0 is sampled.

To output data consecutively using the same DAC configuration, it is not necessary to program the CONTROL register again.

3. Set DAC A value, set DAC B value, update both simultaneously, select slow mode, select internal reference at 1.024 V:

a. Set reference voltage to 1.024 V (CONTROL register)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

b. Write data for DAC B to BUFFER:

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-----------------|-----|----|----|----|----|----|----|----|----|----|----|
| 0 | 0 | 0 | 1 | New DAC B value | | | | | | | | | | | |

c. Write new DAC A value and update DAC A and B simultaneously:

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-----------------|-----|----|----|----|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 0 | New DAC A value | | | | | | | | | | | |

Both outputs are updated on the rising clock edge after D0 from the DAC A data word is sampled.

To output data consecutively using the same DAC configuration, it is not necessary to program the CONTROL register again.

1. Set power-down mode:

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| X | X | 1 | X | X | X | X | X | X | X | X | X | X | X | X | X |

X = Don't care

LINEARITY, OFFSET, AND GAIN ERROR USING SINGLE ENDED SUPPLIES

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset, the output voltage may not change with the first code, depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in [Figure 14](#).

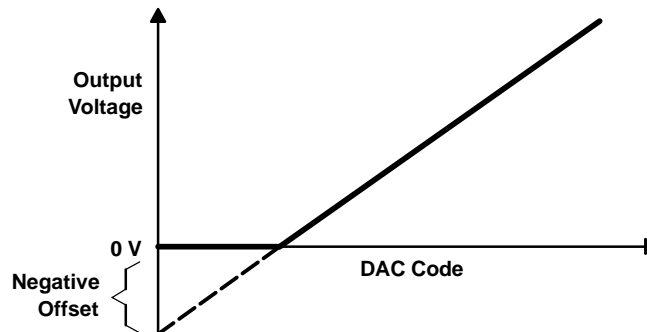


Figure 14. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage.

DEFINITIONS OF SPECIFICATIONS AND TERMINOLOGY

Integral Nonlinearity (INL)

The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

Differential Nonlinearity (DNL)

The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

Zero-Scale Error (E_{ZS})

Zero-scale error is defined as the deviation of the output from 0 V at a digital input value of 0.

Gain Error (E_G)

Gain error is the error in slope of the DAC transfer function.

Total Harmonic Distortion (THD)

THD is the ratio of the rms value of the first six harmonic components to the value of the fundamental signal. The value for THD is expressed in decibels.

Signal-to-Noise Ratio + Distortion (S/N+D)

S/N+D is the ratio of the rms value of the output signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

Spurious Free Dynamic Range (SFDR)

Spurious free dynamic range is the difference between the rms value of the output signal and the rms value of the largest spurious signal within a specified bandwidth. The value for SFDR is expressed in decibels.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|------------------------------------|-------------------------|
| 5962-9957601Q2A | ACTIVE | LCCC | FK | 20 | 1 | RoHS-Exempt & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9957601Q2A TLV5638 MFKB | Samples |
| 5962-9957601QPA | ACTIVE | CDIP | JG | 8 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 9957601QPA TLV5638M | Samples |
| TLV5638CD | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 5638C | Samples |
| TLV5638CDG4 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 5638C | Samples |
| TLV5638CDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 5638C | Samples |
| TLV5638CDRG4 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 5638C | Samples |
| TLV5638ID | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 5638I | Samples |
| TLV5638IDG4 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 5638I | Samples |
| TLV5638IDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 5638I | Samples |
| TLV5638MFKB | ACTIVE | LCCC | FK | 20 | 1 | RoHS-Exempt & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9957601Q2A TLV5638 MFKB | Samples |
| TLV5638MJGB | ACTIVE | CDIP | JG | 8 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 9957601QPA TLV5638M | Samples |
| TLV5638QD | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | V5638 | Samples |
| TLV5638QDG4 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | V5638 | Samples |
| TLV5638QDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | V5638 | Samples |
| TLV5638QDRG4 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | V5638 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLV5638, TLV5638M :

- Catalog : [TLV5638](#)
- Enhanced Product : [TLV5638-EP](#), [TLV5638-EP](#)
- Military : [TLV5638M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV5638CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV5638IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV5638QDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV5638CDR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TLV5638IDR | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| TLV5638QDR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9957601Q2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| TLV5638CD | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TLV5638CDG4 | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TLV5638ID | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| TLV5638IDG4 | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| TLV5638MFKB | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| TLV5638QD | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TLV5638QDG4 | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

D0008A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

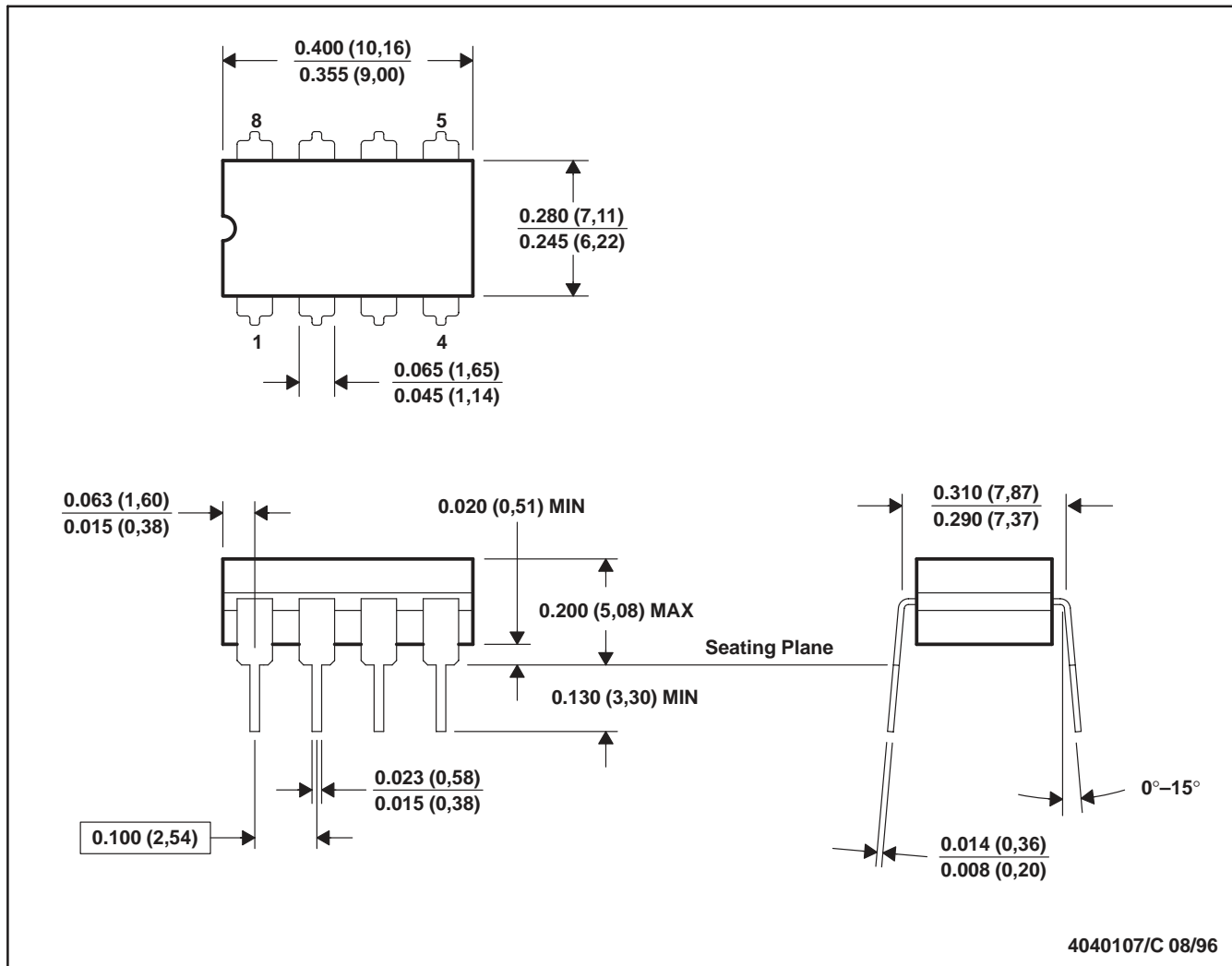
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

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