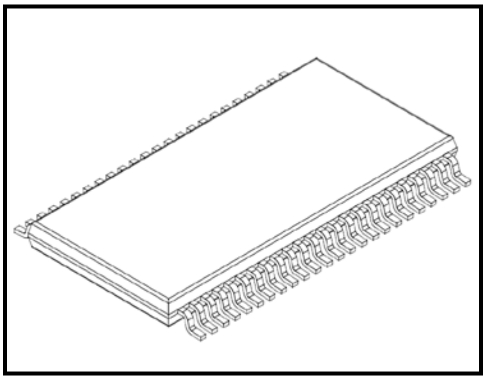
TOSHIBA BiCMOS Integrated Circuit Bi-CMOS Silicon Monolithic

TB9045FNG-120

DCDC Convertor & Multi Output Regulator



HTSSOP48-P-300-0.50
Weight: 204.6mg (typ.)

TB9045FNG is a multi output power supply IC for automotive system power supply incorporating 2 DCDC convertors, a series power supply and 3 tracking regulators. Both high efficiency and low noise output are concurrently achieved by a DCDC power supply and a series power supply, respectively.

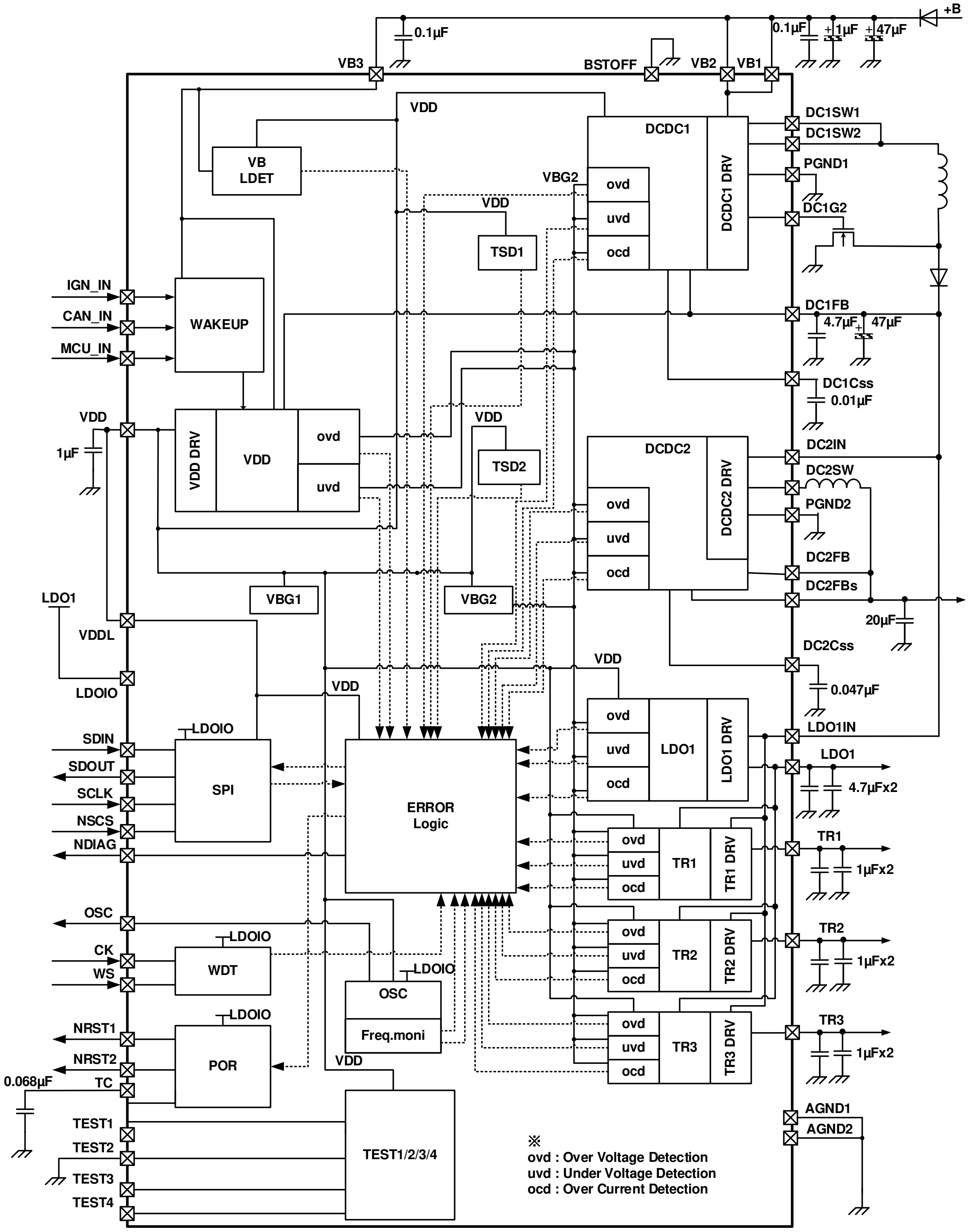
It incorporates various monitoring functions for abnormalities in power supply and MCU, and enables transmitting monitoring statuses to an external system via SPI communication.

1. Features

- 2 DCDC convertor circuits
    - DCDC1: Synchronous rectifying buck-boost convertor with built-in 6V output
    - DCDC2: Synchronous rectifying buck convertor with built-in 1V system output
- 4 built-in output series power supply circuits
    - LDO1: Output voltage 5.0V
    - TR1 to 3 output voltage LDO1 and tuning voltage (3 ch)
- Output voltage monitoring & reset output
    - High voltage & low voltage & overcurrent monitoring
    - Power-on reset (2-channel output pins)
    - Watchdog timer
- Built-in SPI communication
    - To output notification signals for various abnormalities in a power supply function
- 2-channel built-in reference voltage circuits (Main function and monitoring function)
- Built-in oscillator circuit
- Built-in frequency monitoring function for oscillator circuit
- Built-in Analog BIST
- Built-in Logic BIST
- Operating temperature range: -40 to 125 °C
- Package: HTSSOP48-P-300-0.50
- AEC-Q100 Qualified 1.1
- TM-SIL^{TM}
    - Developed according to ISO 26262 ASIL-D
    - Safety Manual and Safety Analysis Report
    - Functional redundancy and built-in ABIST and LBIST
    - SPI interface with CRC check

The product(s) is/are compatible with RoHS regulations (EU directive 2011 / 65 / EU) as indicated, if any, on the packaging label ("[[G]]/RoHS COMPATIBLE", "[[G]]/RoHS [[Chemical symbol(s) of controlled substance(s)]]", "RoHS COMPATIBLE" or "RoHS COMPATIBLE, [[Chemical symbol(s) of controlled substance(s)]]>MCV").

2. Block diagram



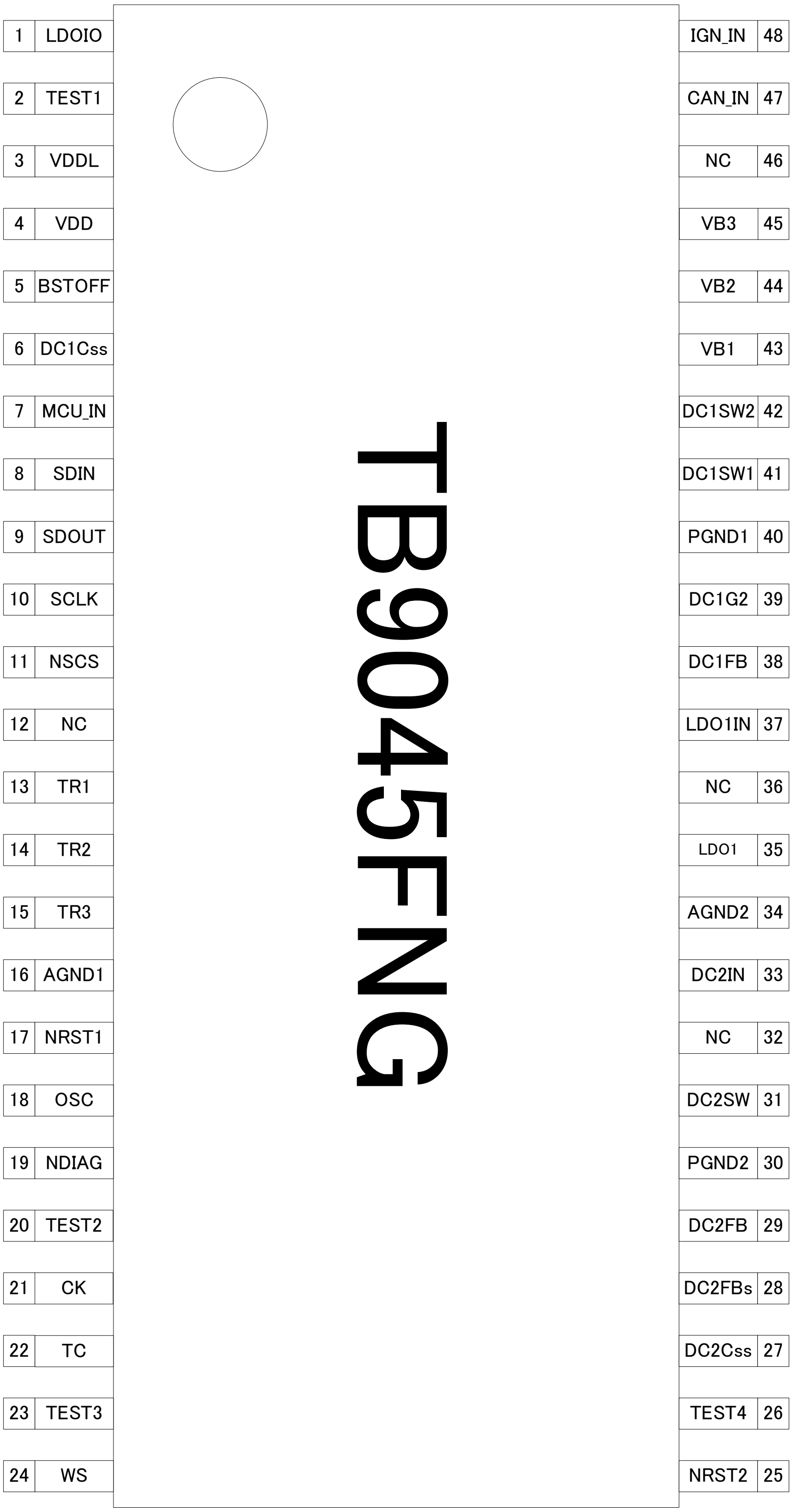
Note: The block diagram may show some of the functional blocks, circuits, or constants in abbreviated or simplified format for clarity in describing the relevant features.

3. Pin description

No.	Pin name	I/O	Function	Configuration	Pull-up/down		Remarks
1	LDOIO	I	Pull-up power supply of MCU I/F pin and IO buffer connection pin	—	—	—	Connect it to LDO1.
2	TEST1	I	Test pin	BIP	—	—	Leave this pin open.
3	VDDL	I	Logic power input pin	—	—	—	Connect it to VDD.
4	VDD	O	VDD power output pin for internal circuit	DMOS	—	—	—
5	BSTOFF	I	Switching pin between buck-boost mode/buck mode	CMOS	PD	50kΩ	Connection to AGND in buck-boost mode, connection to VDD in buck mode.
6	DC1Css	I/O	DCDC1 soft start time setting pin	CMOS	—	—	—
7	MCU_IN	I	Wake-up signal input pin from microcomputer	CMOS	PD	100kΩ	—
8	SDIN	I	SPI serial data input pin	CMOS	PD	50kΩ	—
9	SDOUT	O	SPI serial data output pin	CMOS	—	—	—
10	SCLK	I	SPI clock input pin	CMOS	PD	50kΩ	—
11	NSCS	I	SPI chip select pin	CMOS	PU	50kΩ	It is pulled up to LDOIO inside IC.
12	NC	—	Non connection pin	—	—	—	Leave this pin open.
13	TR1	O	Tracker output 1	DMOS	—	—	—
14	TR2	O	Tracker output 2	DMOS	—	—	—
15	TR3	O	Tracker output 3	DMOS	—	—	—
16	AGND1	-	GND	—	—	—	—
17	NRST1	O	Reset signal output pin 1 (for MCU)	O.D.	PU	4.7kΩ	It is pulled up to LDOIO inside IC.
18	OSC	O	Clock output	CMOS	—	—	—
19	NDIAG	O	Output pin for flag signal notifying error information	O.D.	PU	4.7kΩ	It is pulled up to LDOIO inside IC.
20	TEST2	I	Test pin	CMOS	PD	50kΩ	Connect it to GND.
21	CK	I	Watchdog clock input pin	CMOS	PD	50kΩ	—
22	TC	I/O	Time setting capacitor pin for reset timer	CMOS	—	—	—
23	TEST3	O	Test pin	CMOS	—	—	Leave this pin open.
24	WS	I	Switching pin between ON/OFF of watchdog function	CMOS	PD	50kΩ	Function turned on at L input and function turned off at H input
25	NRST2	O	Reset signal output pin 2 (for driver)	O.D.	PU	4.7kΩ	It is pulled up to LDOIO inside IC.
26	TEST4	O	Test pin	CMOS	—	—	Leave this pin open.
27	DC2Css	I/O	DCDC2 soft start time setting pin	CMOS	—	—	—
28	DC2FBs	I	DCDC2 output voltage feed-back detection SENSE pin	CMOS	—	—	—
29	DC2FB	I	DCDC2 output voltage feed-back detection pin	CMOS	—	—	—
30	PGND2	-	DCDC2 GND pin	—	—	—	Connect it to GND.
31	DC2SW	O	DCDC2 switching output pin	DMOS	—	—	—
32	NC	—	Non connection pin	—	—	—	Leave this pin open.

No.	Pin name	I/O	Function	Configuration	Pull-up/down		Remarks
33	DC2IN	I	DCDC2 input pin	—	—	—	—
34	AGND2	—	GND	—	—	—	—
35	LDO1	O	Series power supply LDO1 output pin	CMOS	—	—	—
36	NC	—	Non connection pin	—	—	—	Leave this pin open.
37	LDO1IN	I	Series power supply LDO1 input pin	—	—	—	—
38	DC1FB	I	DCDC1 output voltage feed-back detection pin	DMOS	—	—	—
39	DC1G2	O	DCDC1 GATE driver pin	DMOS	—	—	Leave this pin open if boost mode is not in use.
40	PGND1	-	DCDC1 GND pin	—	—	—	Connect it to GND.
41	DC1SW1	O	DCDC1 switching output pin 1	DMOS	—	—	This pin is to be short-circuited with DC1SW2.
42	DC1SW2	O	DCDC1 switching output pin 2	DMOS	—	—	This pin is to be short-circuited with DC1SW1.
43	VB1	I	Power supply voltage input pin 1	—	—	—	—
44	VB2	I	Power supply voltage input pin 2	—	—	—	—
45	VB3	I	Power supply voltage input pin 3	—	—	—	—
46	NC	-	Non connection pin	—	—	—	Leave this pin open.
47	CAN_IN	I	Wake-up signal from CAN	DMOS	PD	250kΩ	—
48	IGN_IN	I	Input pin for wake-up signal from IGN	DMOS	PD	250kΩ	—

4. Pin layout


1 LDOIO
2 TEST1
3 VDDL
4 VDD
5 BSTOFF
6 DC1Css
7 MCU_IN
8 SDIN
9 SDOUT
10 SCLK
11 NSCS
12 NC
13 TR1
14 TR2
15 TR3
16 AGND1
17 NRST1
18 OSC
19 NDIAG
20 TEST2
21 CK
22 TC
23 TEST3
24 WS
25 NRST2
26 TEST4
27 DC2Css
28 DC2FBs
29 DC2FB
30 PGND2
31 DC2SW
32 NC
33 DC2IN
34 AGND2
35 LDO1
36 NC
37 LDO1IN
38 DC1FB
39 DC1G2
40 PGND1
41 DC1SW1
42 DC1SW2
43 VB1
44 VB2
45 VB3
46 NC
47 CAN_IN
48 IGN_IN
TB9045FNG

5. Functional description

Some of the functional blocks of the block diagram of this chapter, the circuit or constant labels, might have been omitted or simplified for clarity.

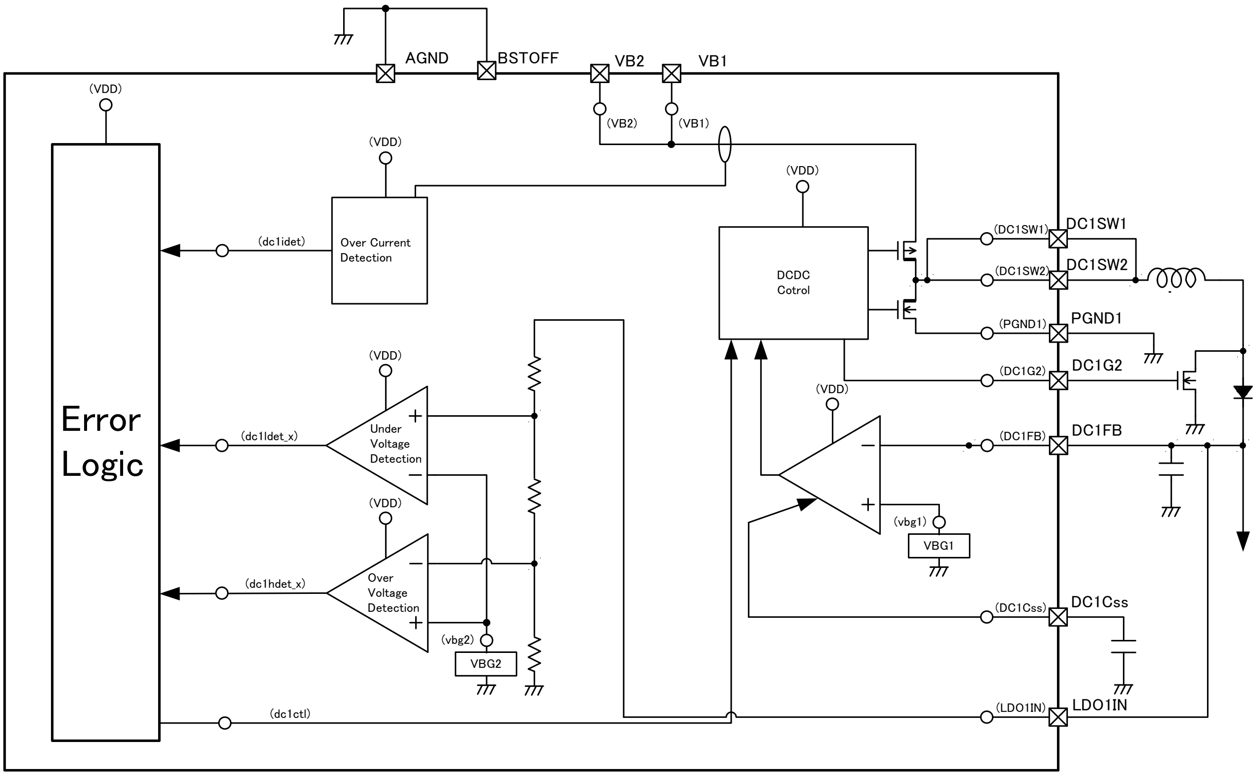
5.1. DCDC Convertor

DCDC1

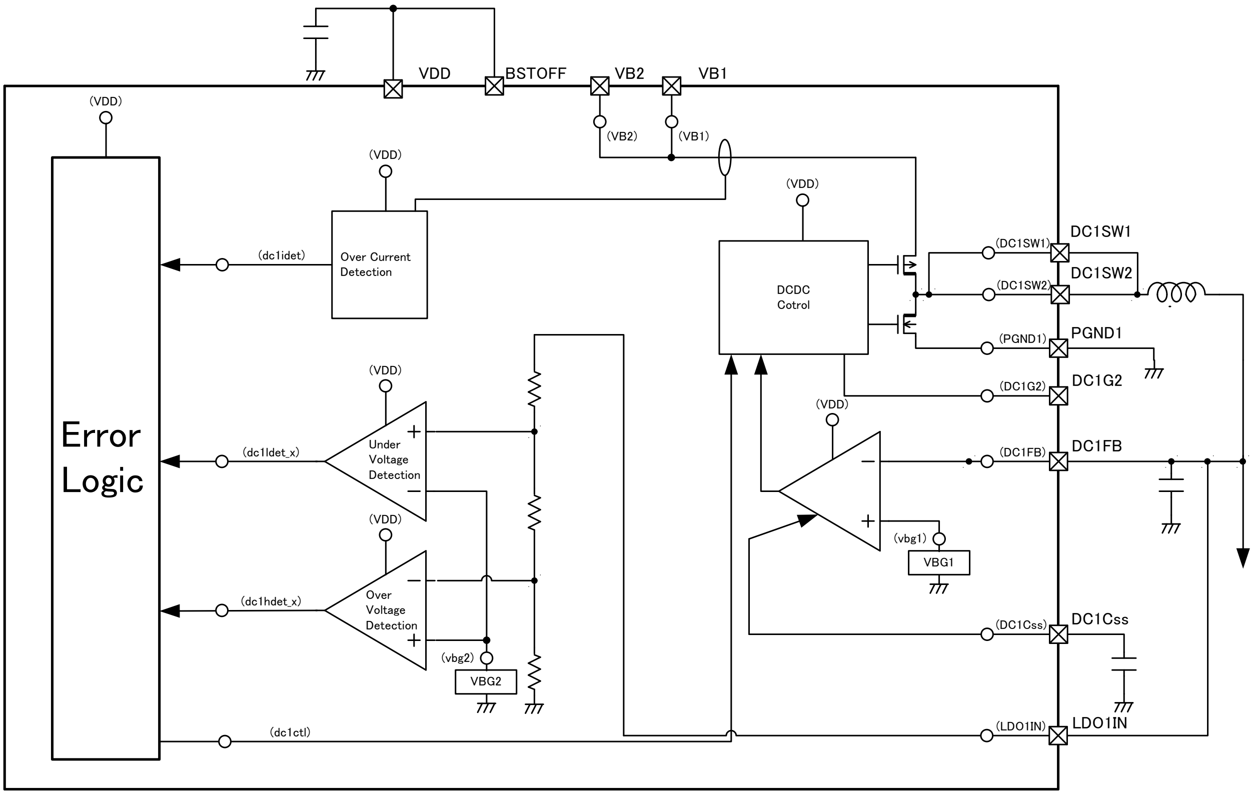
It is buck-boost DCDC convertor with input voltage VB1/2 and 6V output voltage. For buck mode, it is a synchronous rectifying type incorporating output driver MOS and rectification MOS. For boost mode, it is a diode rectifying type having external driver MOS and rectifier diode.

- Switching frequency is 400 kHz.
- It incorporates functions of overcurrent detection and high/low voltage detection (not used in low voltage detection).
- It incorporates phase compensating capacitor.
- The capacitor connected to DC1Css pin can control voltage rising time.
- Buck mode enables use of DCDC convertor for buck mode (with BSTOFF = VDD set). Switching between buck-boost mode and buck mode during IC operation must not be performed.

At the time of using DCDC convertor for buck-boost mode



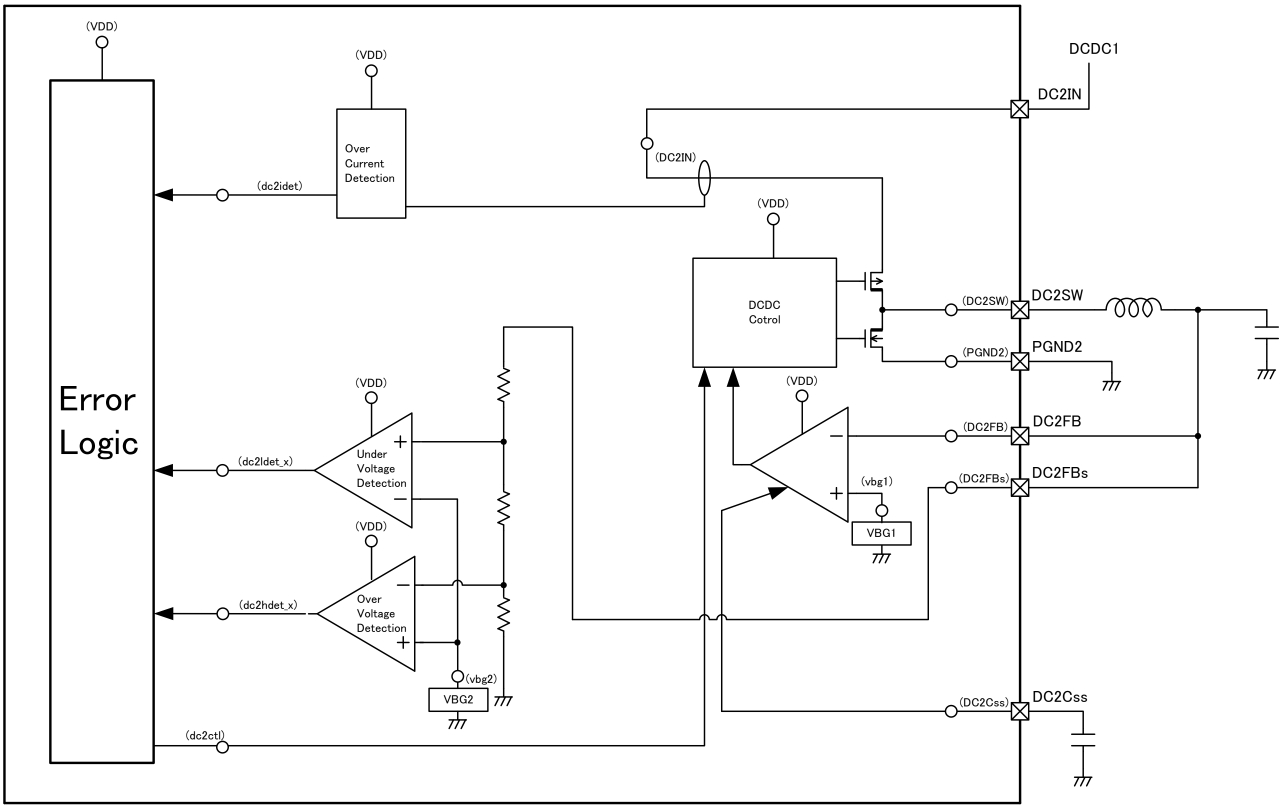
At the time of using DCDC convertor for buck mode



DCDC2

It is buck DCDC convertor with 6V input voltage (DCDC1). It is a synchronous rectifying type incorporating output driver MOS and rectification MOS. 6V output from DCDC1 convertor must be used as input voltage.

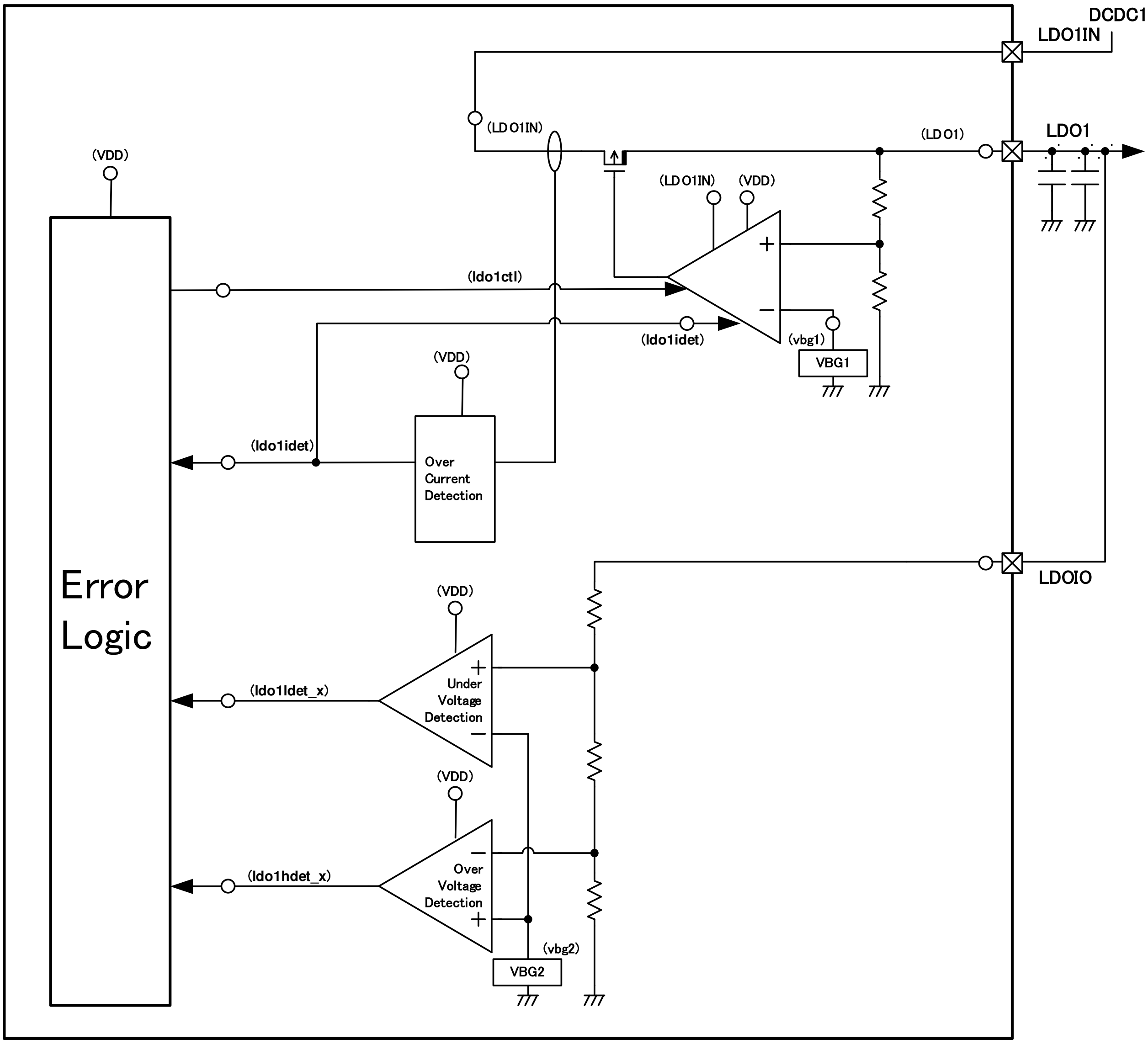
- Maximum output current is 800mA. (Set current consumption considering allowable dissipation and heat generation.)
- Switching frequency is 2 MHz.
- It incorporates functions of overcurrent detection and high/low voltage detection.
- It incorporates phase compensating capacitor.
- The capacitor connected to DC2Css pin can control voltage rising time.



5.2. Series Power Supply

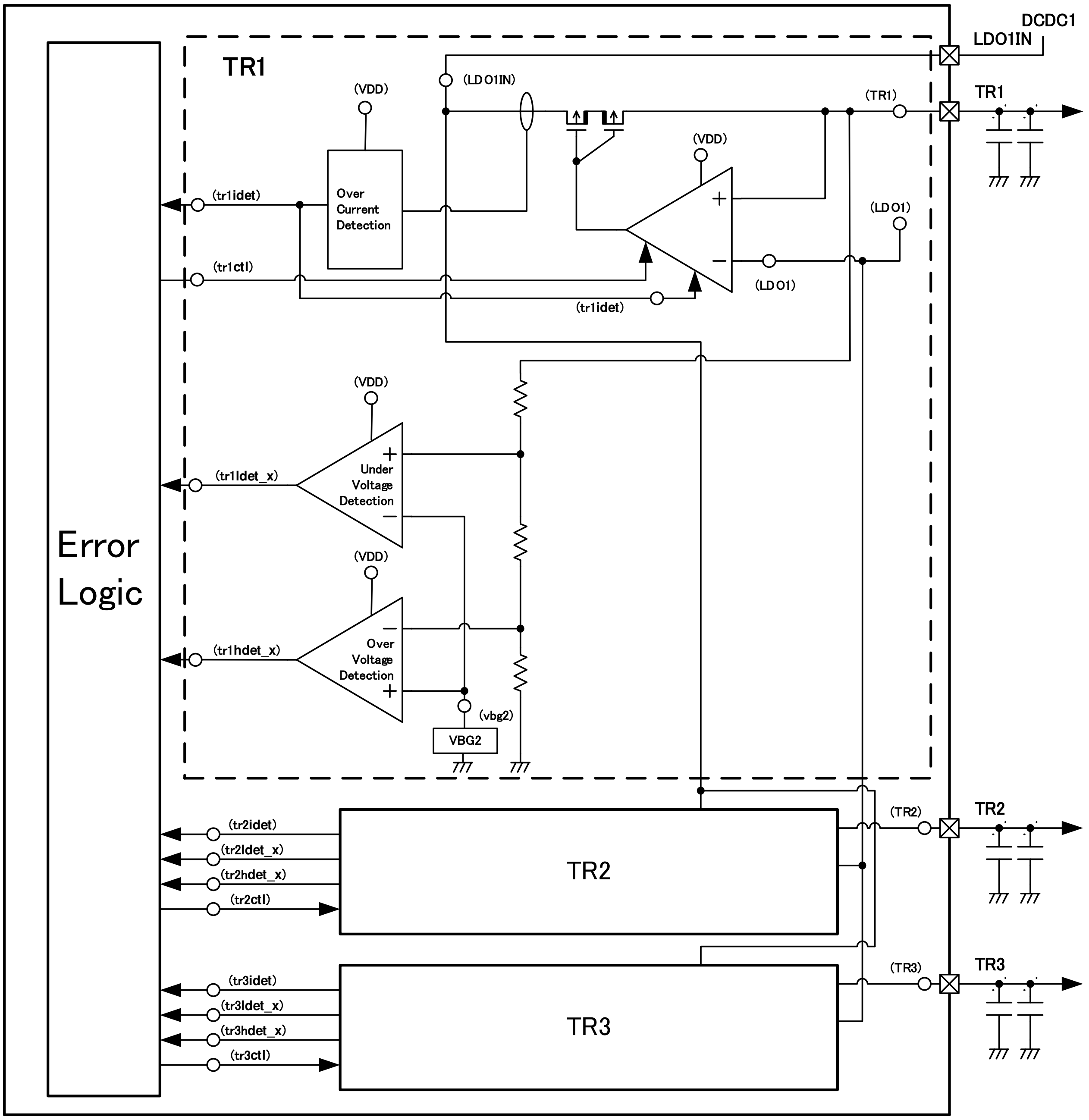
LDO1

- It is a series power supply incorporating output driver MOS.
- 6V output from DCDC1 convertor must be used as input voltage.
- Output voltage is 5V±0.1V, and output current maximum 400mA.
- It incorporates functions of overcurrent detection and high/low voltage detection. (Set current consumption considering allowable dissipation and heat generation.)
- It incorporates phase compensating capacitor.



TR1, TR2, TR3

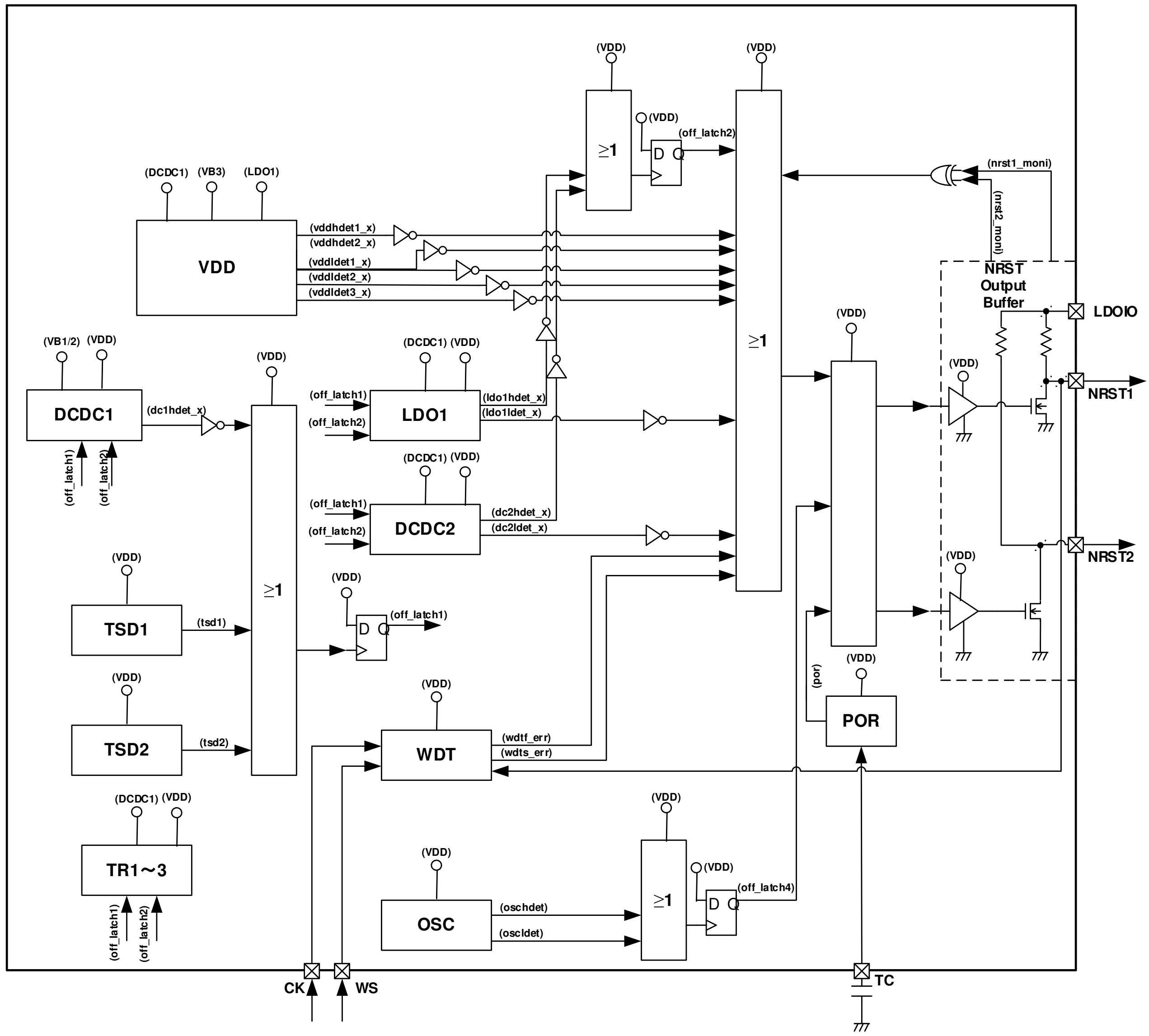
- It is a tracker power supply incorporating output driver MOS.
- Output voltage is linked with LDO1.
- Output current of TR1, TR2 or TR3 is maximum 100mA.
- It incorporates functions of overcurrent detection (minimum 100mA for TR1, TR2 and TR3 respectively) and high/low voltage detection (TR1, TR2, and TR3). (Set current consumption considering allowable dissipation and heat generation.)
- It enables turning off TR1, TR2 and TR3 independently via SPI communication.



5.3. Abnormality Detection Function

It incorporates abnormality detection function as follows.

Reset output system diagram at the time of abnormality detection



Power supply operational matrix (Initial value as register setting)

* Relaunch of power supply input VB1,VB2 and VB3 or relaunch by IGN_IN/CAN_IN/MCU_IN control is required to release off-latch (mode).

* "During start-up" is defined as the period until low voltage detection of each power supply is released, and "after start-up (in operation)" as the subsequent period.

* During off-latch (mode) or turning off, output voltage is proactively discharged with a discharge resistor and turned off.

* If restart is requested during discharging, start-up operation is executed even with discharging.

■ During operation (Initial value as register setting)

Abnormality detection	Power supply	VDD	DCDC1	LDO1	DCDC2	TR1 to 3	NRST1/2	NDIAG
Overcurrent detection	**DCDC1**	Operation continued	**Overcurrent detection off-latch**	Operation continued* **1**	Operation continued* **1**	Operation continued* **1**	L * 4	L Latch
	LDO1	Operation continued	Operation continued	**Overcurrent limitation** Operation continued **(voltage drop)**	Operation continued **(turned off at LDO1 drop detection) * 5**	Operation continued * **2**	L* 4	L Latch
	DCDC2	Operation continued	Operation continued	Operation continued	**Overcurrent detection off-latch**	Operation continued	L* 5	L Latch
	TR1 to 3	Operation continued	Operation continued	Operation continued	Operation continued	**Overcurrent limitation** Operation continued* **3**	—	L Latch
High voltage detection	**VDD**	**High voltage OFF**	**OFF**	**OFF**	**OFF**	**OFF**	L	L *6
	DCDC1	Operation continued	**High voltage off-latch**	**Off-latch**	**Off-latch**	**Off-latch**	L * 4	L Latch
	LDO1	Operation continued	**Off-latch**	**High voltage off-latch**	**Off-latch**	**Off-latch**	L	L Latch
	DCDC2	Operation continued	**Off-latch**	**Off-latch**	**High voltage off-latch**	**Off-latch**	L	L Latch
	TR1 to 3	Operation continued	Operation continued	Operation continued	Operation continued	**High voltage** Operation continued	—	L Latch
Low voltage detection	**VB3**	Operation continued	**OFF**	**OFF**	**OFF**	**OFF**	L * 4	L Latch
	VDD	**Low voltage**	**OFF**	**OFF**	**OFF**	**OFF**	L	L
	DCDC1	Operation continued	**Low voltage**	Operation continued	Operation continued	Operation continued	—	—
	LDO1	Operation continued	Operation continued	**Low voltage**	**OFF**	Operation continued* 2	L	L Latch
	DCDC2	Operation continued	Operation continued	Operation continued	**Low voltage**	Operation continued	L	L Latch
	TR1 to 3	Operation continued	Operation continued	Operation continued	Operation continued	**Low voltage**	—	L Latch
Overheat detection	—	Operation continued	**Off-latch**	**Off-latch**	**Off-latch**	**Off-latch**	L * 4	L Latch
Abnormal frequency	—	Operation continued	**Off-latch**	**Off-latch**	**Off-latch**	**Off-latch**	L	L Latch

*** 1: The operation continues, but the output is suspended because of DCDC1 off-latch (mode).**

*** 2: The operation continues, but voltage drops following LDO1 behavior.**

*** 3: The operation continues, but output voltage drops in conjunction with current value.**

*** 4: It becomes L if DCDC2 or LDO1 detects low voltage.**

*** 5: It becomes L if DCDC2 detects low voltage.**

*** 6: During operation VDD If high voltage is detected, low voltage detection is also accompanied by OFF operation, so it may look like a L latch.**

■ **During start-up (Initial value as register setting)**

Abnormality detection	Power supply	VDD	DCDC1	LDO1	DCDC2	TR1 to 3	NRST1/2	NDIAG
Overcurrent detection	**DCDC1**	Normal start-up	**overcurrent detection off-latch**	**Start-up failure**	**Start-up failure**	**Start-up failure**	L* 1	L Latch
	LDO1	Normal start-up	Normal start-up	**Overcurrent limitation** Normal start-up	Normal start-up	Normal start-up	—	L Latch
		Normal start-up	Normal start-up	**Overcurrent limitation** Start-up failure	Start-up failure	Start-up failure	L * 2	L Latch
	DCDC2	Normal start-up	Normal start-up	Normal start-up	**Overcurrent detection off-latch**	Normal start-up	L * 3	L Latch
	TR1 to 3	Normal start-up	Normal start-up	Normal start-up	Normal start-up	**Overcurrent limitation** Normal start-up	—	L Latch
		Normal start-up	Normal start-up	Normal start-up	Normal start-up	**Overcurrent limitation** Start-up failure	—	L Latch
High voltage detection	**VDD**	**High voltage off**	**Start-up failure**	**Start-up failure**	**Start-up failure**	**Start-up failure**	L	L
	DCDC1	Normal start-up	**High voltage off-latch**	**Start-up failure**	**Start-up failure**	**Start-up failure**	L* 1	L Latch
	LDO1	Normal start-up	**Off-latch**	**High voltage off-latch**	**Start-up failure**	**Off-latch**	L	L Latch
	DCDC2	Normal start-up	**Off-latch**	**Off-latch**	**High voltage off-latch**	**Off-latch**	L	L Latch
	TR1 to 3	Normal start-up	Normal start-up	Normal start-up	Normal start-up	**High voltage** Normal start-up	—	L Latch
Low voltage detection	**VB3**	Normal start-up	**Start-up failure**	**Start-up failure**	**Start-up failure**	**Start-up failure**	L* 1	L Latch
	VDD	**Low voltage**	**Start-up failure**	**Start-up failure**	**Start-up failure**	**Start-up failure**	L	L
	DCDC1	Normal start-up	**Low voltage**	**Start-up failure**	**Start-up failure**	**Start-up failure**	—	—
	LDO1	Normal start-up	Normal start-up	**Low voltage**	**Start-up failure**	**Low voltage**	L	L Latch
	DCDC2	Normal start-up	Normal start-up	Normal start-up	**Low voltage**	Normal start-up	L	L Latch
	TR1 to 3	Normal start-up	Normal start-up	Normal start-up	Normal start-up	**Low voltage**	—	L Latch
Overheat detection	**—**	Normal start-up	**Start-up failure**	**Start-up failure**	**Start-up failure**	**Start-up failure**	L * 1	L Latch
Abnormal frequency	**—**	Normal start-up	**Start-up failure**	**Start-up failure**	**Start-up failure**	**Start-up failure**	L	L Latch

*** 1: It becomes L if DCDC2 or LDO1 detects low voltage.**

*** 2: It becomes L when DCDC2 or LDO1 detects low voltage.**

*** 3: It becomes L if DCDC2 detects low voltage.**

The timing when the abnormal detection becomes effective at the time of start

Abnormality detection	Power supply	Protection start	Diag start
Overcurrent detection	DCDC1	DCDC1 start	ABIST end
	LDO1	LDO1 start	LDO1 Low voltage detection •release
	DCDC2	DCDC2 start	ABIST end
	TR1 to 3	TR1 to 3 start	NRST1 release
High voltage detection	VDD	ABIST end	ABIST end
	DCDC1	DCDC1 start	ABIST end
	LDO1	LDO1 start	ABIST end
	DCDC2	DCDC2 start	ABIST end
	TR1 to 3	TR1 to 3 start	ABIST end
Low voltage detection	VB3	ABIST end	ABIST end
	VDD	Always	Always
	DCDC1	—	—
	LDO1	LDO1 Low voltage detection •release	LDO1 Low voltage detection •release
	DCDC2	DCDC2 Low voltage detection •release	DCDC2 Low voltage detection •release
	TR1 to 3	NRST1 release	NRST1 release
Overheat detection	—	ABIST end	ABIST end
Abnormal frequency	—	ABIST end	ABIST end
NRST1/2 monitoring	—	ABIST end	ABIST end
NDIAG monitoring	—	ABIST end	ABIST end

Overcurrent abnormality detection operation

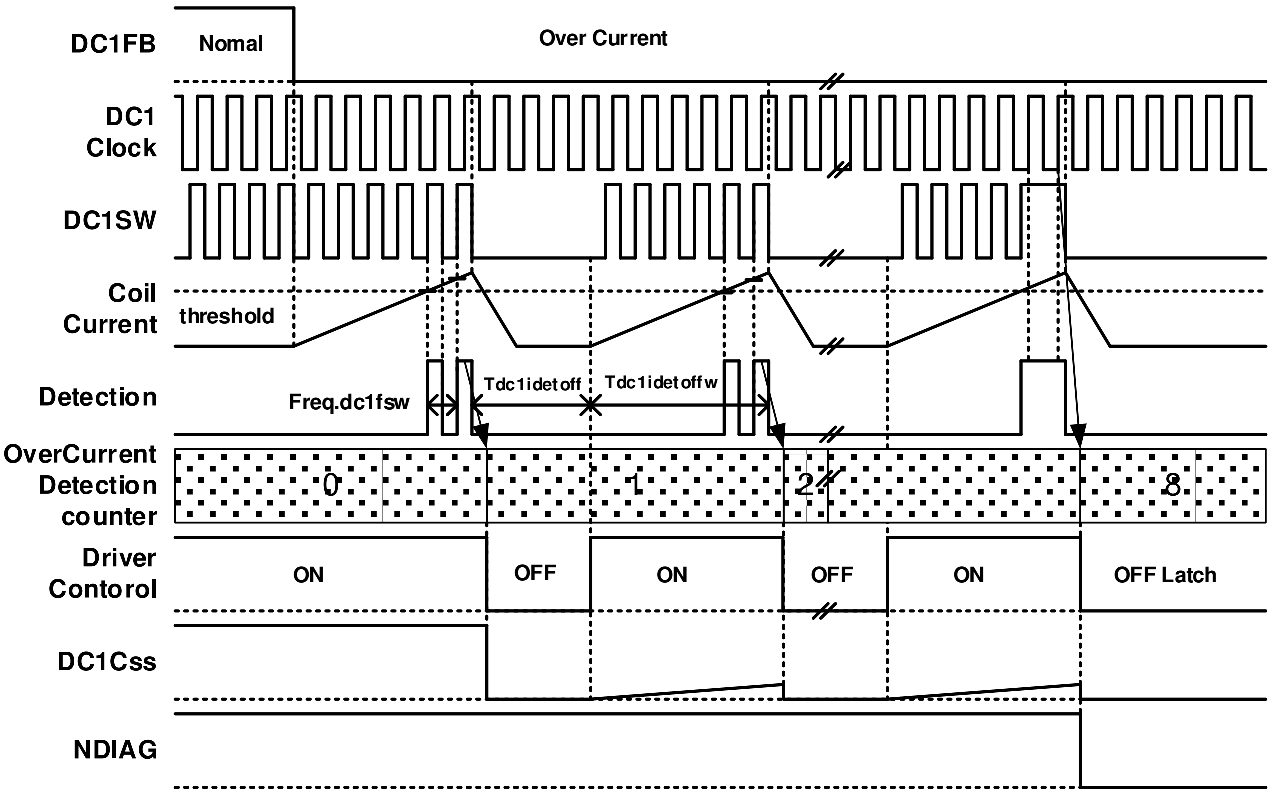
Overcurrent detection function is incorporated for the output of DCDC1, DCDC2, LDO1, TR1, TR2 and TR3. Each detection result is input to error logic, which outputs NDIAG if any overcurrent is detected. NDIAG becomes “H” in normal status, and NDIAG becomes “L” at overcurrent detection.

DCDC1 overcurrent operation

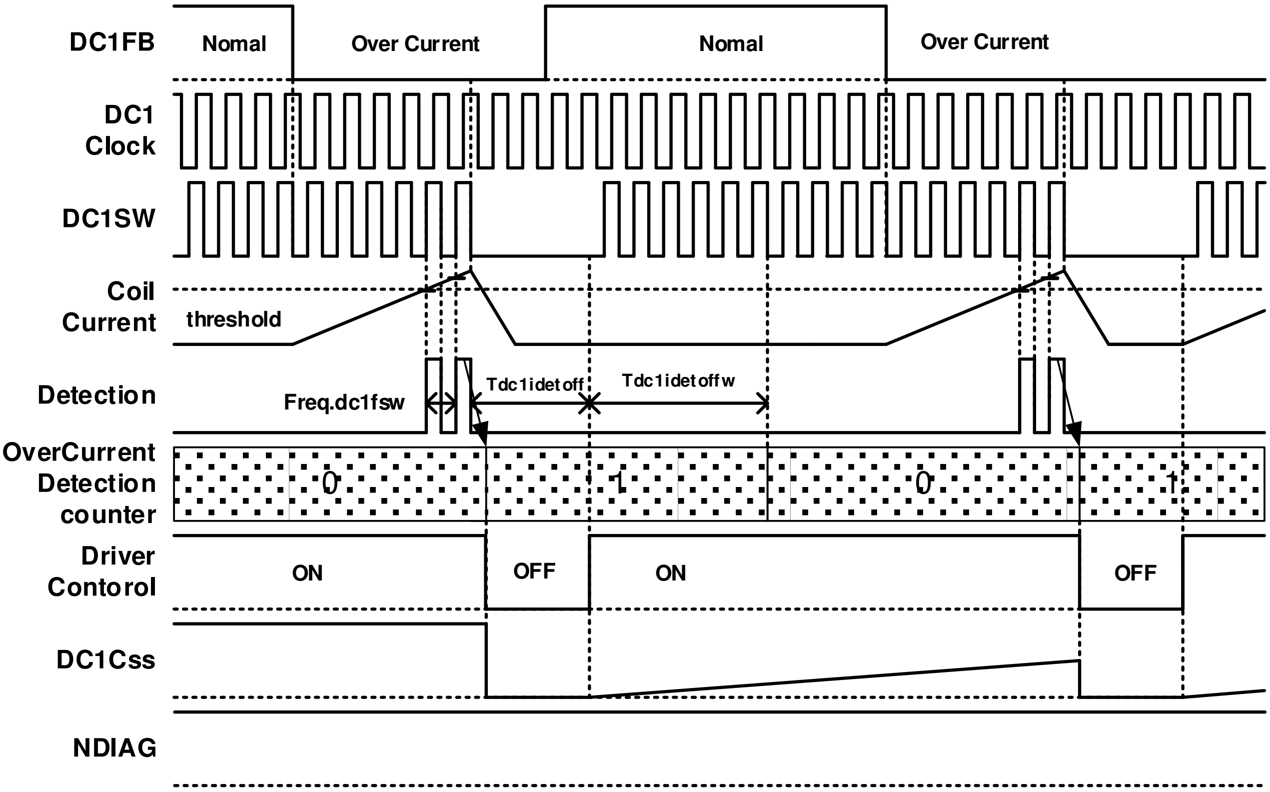
DCDC1 detection & control method

It turns off built-in output driver MOS at overcurrent detection. It turns it on after a certain period of time (with frequency of 400 kHz), and is in a switching mode to turn it off for 2 ms at re-detection of overcurrent. It is to latch off and suspend DCDC1 power supply function, if overcurrent status continues even after repeating the switching mode 8 times. At overcurrent detection, it is to output information on abnormality detected to error logic and set NDIAG to L.
After the Tdc1idetoff(typ.2ms) turn-off mode, overcurrent detection counter is reset if overcurrent is not detected in Tdc1idetoffw(maximum 2ms).
For details, refer to the following table and timing chart.

ON/OFF switching operation at DCDC1 overcurrent detection (off-latch)



ON/OFF switching operation at DCDC1 overcurrent detection (with detection reset)



DCDC2 overcurrent operation

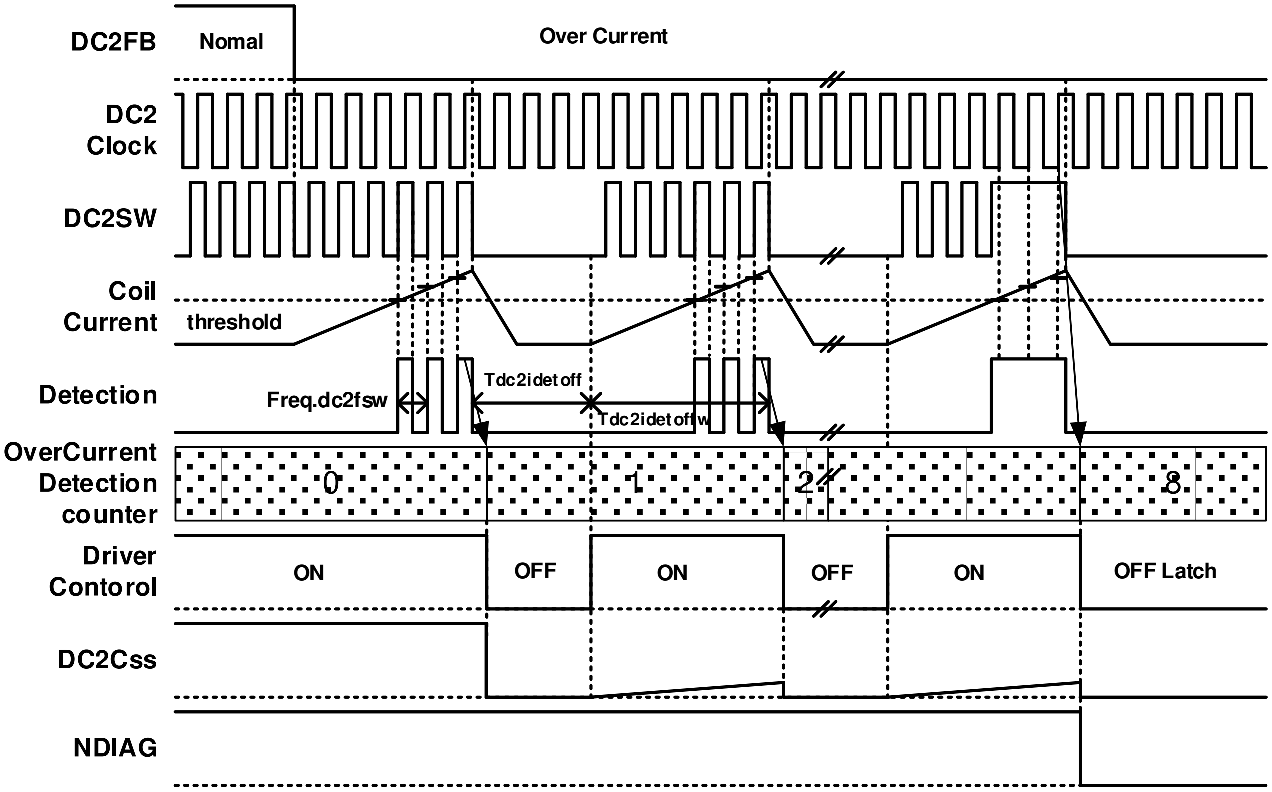
DCDC2 detection & control method

It turns off built-in output driver MOS at overcurrent detection. It turns it on after a certain period of time (with frequency of 2 MHz), and is in a switching mode to turn it off for 2 ms at re-detection of overcurrent. It is to latch off and suspend DCDC1 power supply function, if overcurrent status continues even after repeating the switching mode 8 times. At overcurrent detection, it is to output information on abnormality detected to error logic and set NDIAG to L.

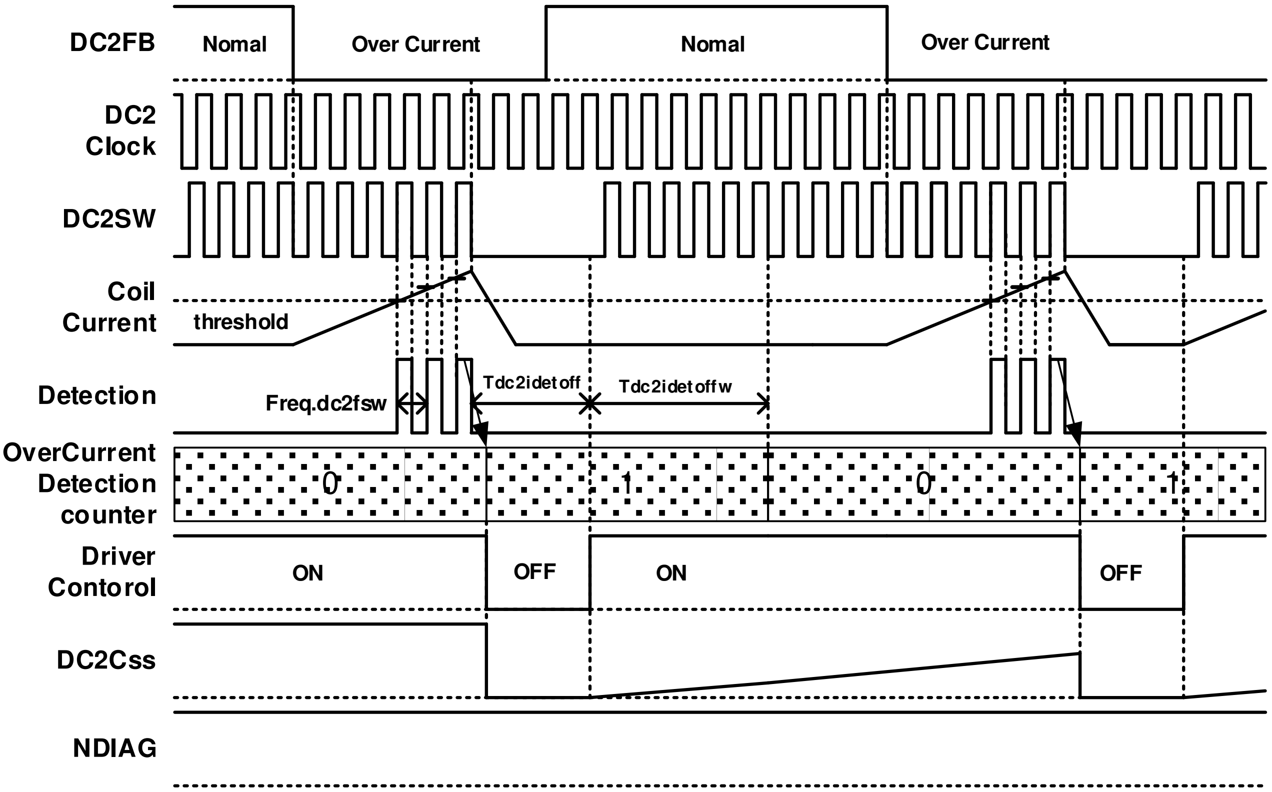
After the Tdc1idetoff(typ.2ms) turn-off mode, overcurrent detection counter is reset if overcurrent is not detected in Tdc1idetoffw(maximum 2ms).

For details, refer to the following table and timing chart.

ON/OFF switching operation at DCDC2 overcurrent detection (off-latch)

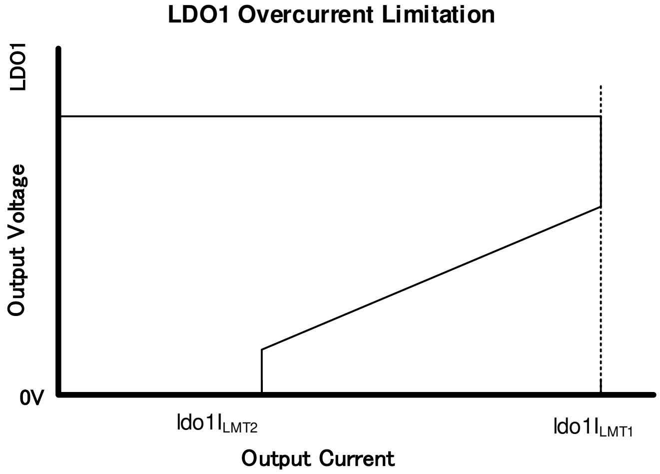


ON/OFF switching operation at DCDC2 overcurrent detection (with detection reset)



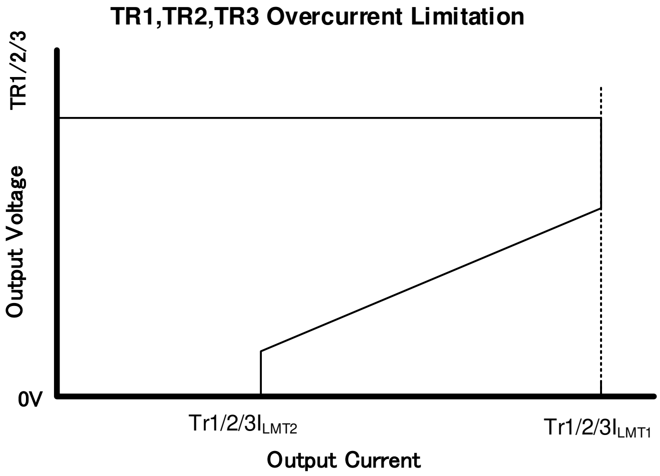
LDO1 overcurrent operation

LDO1 incorporates a current limiter. The current limiter starts operating at overcurrent detection, and outputs a signal of limiter operation, information on abnormality detected, to error logic and set NDIAG to L. For details, refer to the table below.



TR1, TR2, TR3 overcurrent operation

TR1, TR2, TR3 incorporate a current limiter. The current limiter starts operating at overcurrent detection, and outputs a signal of limiter operation, information on abnormality detected, to error logic and set NDIAG to L. For details, refer to the table below.



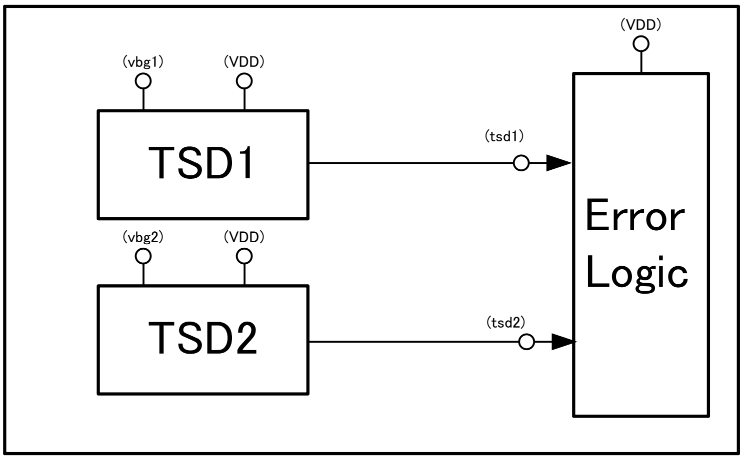
List of operation of overcurrent detection values

Monitoring function	SPI setting	Setting bit	Operation	Initial value	ABIST	Writing to register	NDIAG
DCDC1 overcurrent	Applicable	0	DCDC1 operation continued	-	○	○	L Latch
		1	DCDC1 off-latch (8 times)	○	○	○	L Latch
DCDC2 overcurrent	Applicable	0	DCDC2 operation continued	-	○	○	L Latch
		1	DCDC2 off-latch (8 times)	○	○	○	L Latch
LDO1 overcurrent	Not applicable	—	LDO1 current limiter	-	○	○	L Latch
TR1 overcurrent	Not applicable	—	TR1 current limiter	-	○	○	L Latch
TR2 overcurrent	Not applicable	—	TR2 current limiter	-	○	○	L Latch
TR3 overcurrent	Not applicable	—	TR3 current limiter	-	○	○	L Latch

* Only at the time of starting until NRST1 is released, TR1/2/3 overcurrent detection function does not start operation to write in register and NDIAG does not become L.

Overheat detection

This product incorporates an overheat detection function. It stops after latching off power supply circuits of DCDC1, DCDC2, LDO1 and TR1 to 3, if junction temperature Tj exceeds overheat detection temperature TSD1 or TSD2 = 170 °C (typ.) (Only at the time of overheat detection, processing to turn off DCDC1, DCDC2, LDO1 and TR1 to 3 is selectable by SPI setting.)

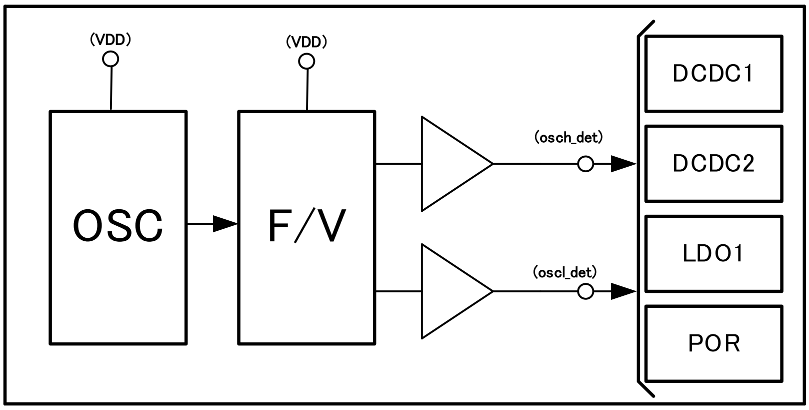


List of operation of overheat detection values

Monitoring function	SPI setting	Setting bit	Operation	Initial value	ABIST	Writing to register	NDIAG
Overheat detection	Applicable	0	DCDC1, DCDC2, LDO1 and TR1 to 3 turned off	—	○	○	L Latch
		1	DCDC1, DCDC2, LDO1 and TR1 to 3 off-latch	○	○	○	L Latch

Oscillation frequency monitoring

- ➢ F/V convertor and voltage comparator are to detect abnormality in high frequency and low frequency.
- ➢ If abnormal frequency is detected, it latches off DCDC1, DCDC2, LDO1 and TR1 to 3 simultaneously with NRST1/2 = L and NDIAG = L.



5.4. Watchdog Timer

Watchdog timer

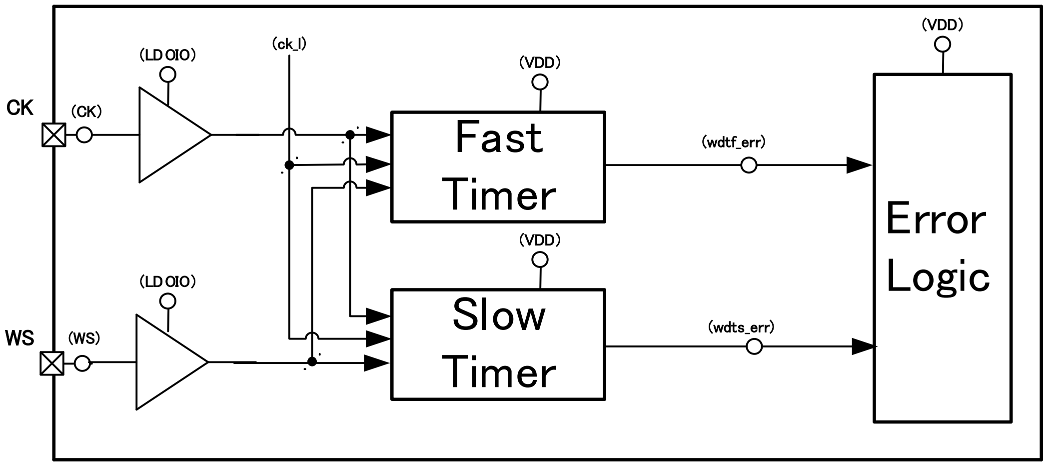
- It is a window type to detect both low speed and high speed abnormalities of watchdog clear pulse (CK input). If either of them is detected (*1), reset signals of NRST1 and NRST2 = L, and NDIAG = L are output.
- Validity/invalidity of high speed abnormality detection is selectable via SPI communication.
- Validity/invalidity of watchdog timer is selectable by WS pin setting. (In the case of invalidity selected, NRST2 becomes L.)
- Whether or not to latch NRST1 and NRST2 = L at watchdog error detection is selectable by register setting.
- It counts the number of times that NRST1 and NRST2 become L output due to watchdog timer, and when this count reaches 5 times, NRST1 and NRST2 become L latch. However, if a clear pulse is input during counting, the count is cleared at that point.

*1 High speed abnormality detection is to be counted on a high speed detection counter. If the detection is counted 10 consecutive times with no normal input of clear pulse, reset signals of NRST1 and NRST2 = L, and NDIAG = L are output.

	Condition for counting	**Condition for WDT reset output**	**Condition for initializing counter value**	**Remarks**
Watchdog timer Counter	At valid WDT function	Low speed abnormality detection	Normal input of clear pulse or reset output or watchdog timer low speed abnormality detection or watchdog timer high speed abnormality detection or WS pin = H or at invalid WDT function	―
Watchdog timer high speed detection counter	At valid WDT function & WDT high speed abnormality detection	WDT high speed abnormality detection 10 consecutive times of detection	Reset output or normal input of clear pulse or WS pin =H or at invalid WDT function	―
Watchdog timer reset counter	Watchdog reset detection attributable to watchdog timer	Reset output is latched with reset counter value = 5. (Reset output latch is not released with WS = H.)	Normal input of clear pulse or WS pin = H or at invalid WDT function	Stopping counting at watchdog timer reset counter = 5
CK counter	At valid WDT function (only the first time after the validation)	typ. 256 ms count	Normal input of clear pulse or WS pin = H	―

* Valid WDT monitoring function: when clear pulse is input within start-up waiting time
Invalid WDT monitoring function: after Power-on reset (including recovery from low voltage)
In the case of WS pin = H

Watchdog timer function block



Watchdog timer start-up waiting time

In this IC, with the WS pin set to L, if a clear pulse is input from the MCU within the watchdog timer activation wait time (typ. 256 ms) after the power on reset is released, WDT monitoring is performed. However, if reset is generated 5 consecutive times without clear pulse input from the MCU, it will be off-latched.

If watchdog timer function is set invalid by WS pin setting, the start-up waiting time also becomes invalid.

- In the case of no clear pulse detected because of broken MCU during the start-up ⇒ reset
- In the case of too fast clear pulse because of broken MCU during the start-up ⇒ high speed detection after WDT monitoring has become valid ⇒ reset

Condition for NRST2 release

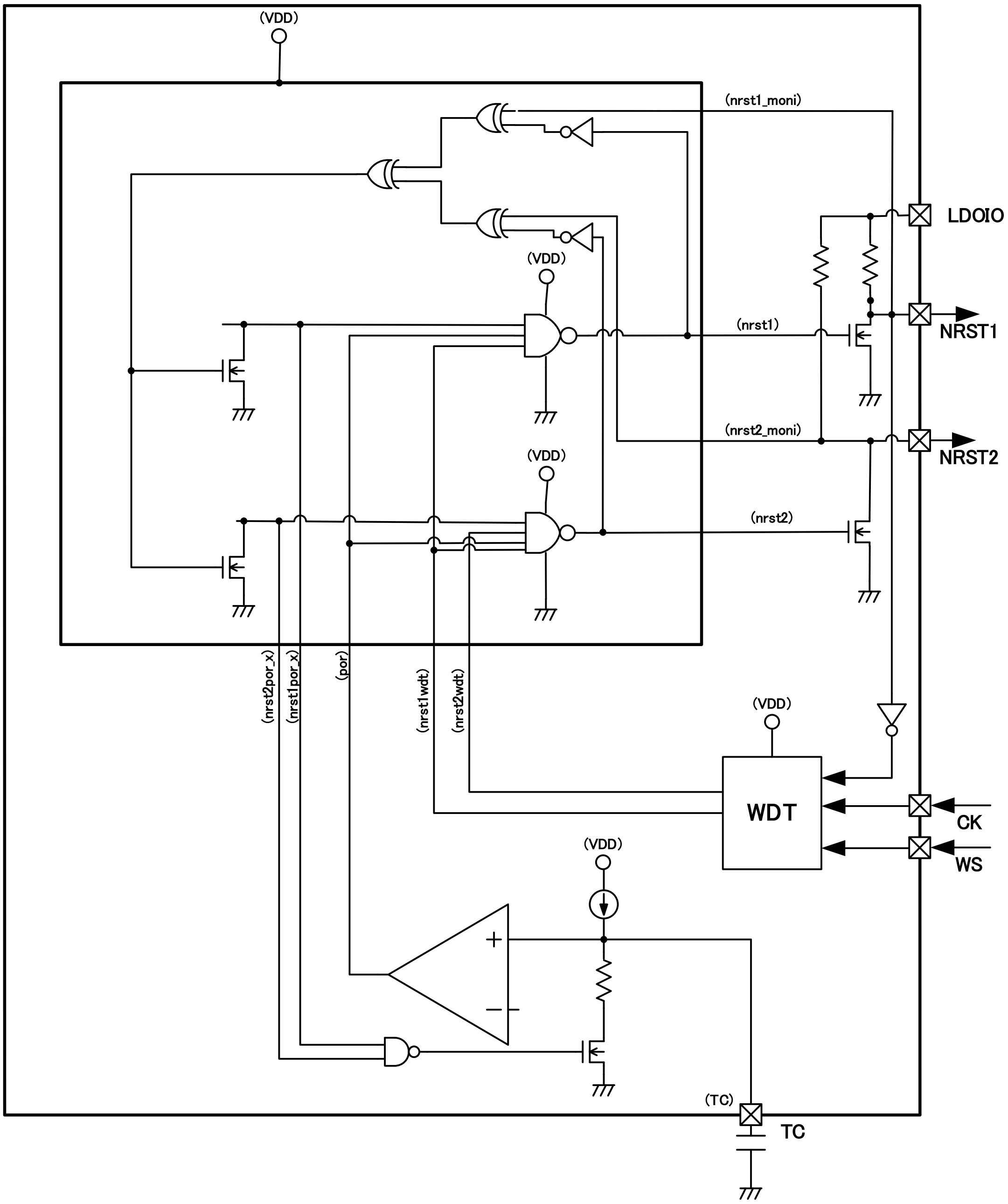
A microcomputer judges the operation normal and releases NRST2 if WDT clear signal is input within normal time (to be set in register) after WDT monitoring starts at clear pulse input within the start-up waiting time.

If watchdog timer function is set invalid by WS pin setting, NRST2 becomes L.

5.5. Power-on Reset Function

Power-on reset

- Once DCDC2 and LDO1 output voltage shows normal values (with low voltage detection released), Power-on reset timer function starts operating. After Power-on reset time, NRST1 becomes H and the reset is released.
- Power-on reset time is changeable with external capacity (TC).



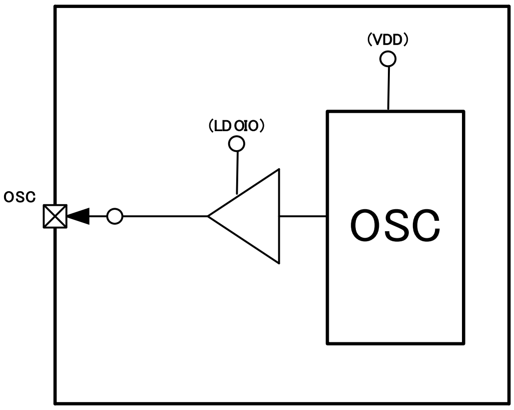
Reset output monitoring function

- Reset output is constantly monitored. The output of NRST1 and NRST2 error logic is to be compared to the pin logic. If the latter differs from the former, reset output monitoring abnormality is detected with NRST1= NRST2 = off,NDIAG=L latch.

5.6. Clock Generation Function

Oscillator circuit

- It is a C/R oscillator with built-in capacitor and resistor. Oscillation frequency is 8 MHz (typ.)
- It is used for DCDC convertor switching, and logic circuit clock.
- The setting by SPI communication allows outputting divided clock from OSC pin.
- It incorporates a detection circuit to output DIAG signal at the event of abnormal oscillation frequency.
- It incorporates a spread spectrum function. Whether to validate the function is selectable via SPI communication.



5.7. SPI Communication

SPI communication circuit consists of SPI core circuit and register read circuit block.

NSCS becomes “L” only during communication, otherwise it is always “H”.

SCLK is used to synchronize communication between IC and microcomputer. The microcomputer writes data in SDIN at rising edge of clock, and IC reads it at the next falling edge. IC writes data in SDOUT at rising edge of clock, and the microcomputer reads it at the next falling edge.

SDIN receives the data bit from the microcomputer in the order of MSB to LSB.

SDOUT sends the data bit to the microcomputer in the order of MSB to LSB. The output is in push-pull configuration, and will be high-impedance at the time of NSCS = “H”.

The IC has NSCS pin with built-in pull-up resistor, and SCLK and SDIN pins with built-in pull-down resistors.

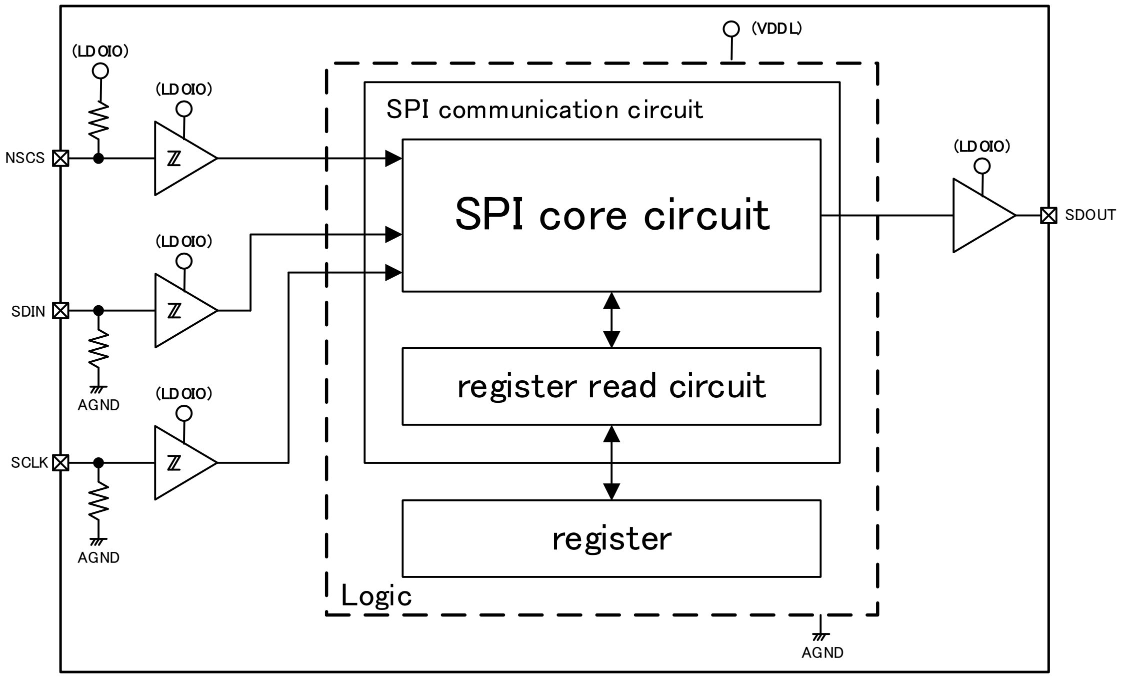
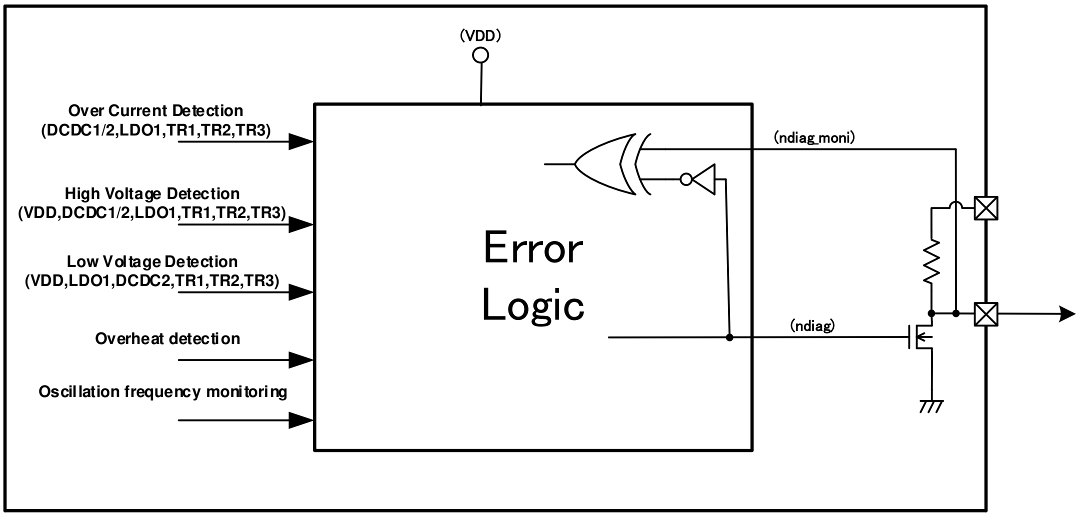


Fig. 5.7.a Block diagram for SPI communication circuit

5.8. Error Logic

Error logic function

- If power IC monitoring results are not acceptable, NDIAG = L is output. The abnormality data is written simultaneously in the register incorporated in SPI.
- The output of NDAIG error logic is to be compared to the pin logic constantly. If the latter differs from the former, NDAIG output monitoring abnormality is detected with NDAIG=L-latch.
- If all the detected abnormalities become normal and abnormality data written in the register is cleared, the status returns to NDIAG = H.

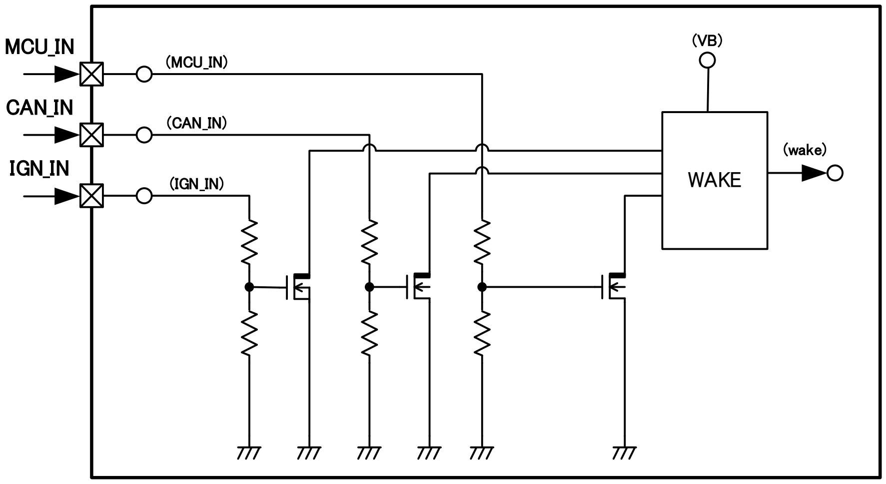


Error logic circuit block diagram

5.9. Wake-up Function

Wake-up circuit

➢ This IC starts by receiving one of the 3 inputs (IGN_IN, CAN_IN, MCU_IN).The following shows the configuration.



Operation truth table

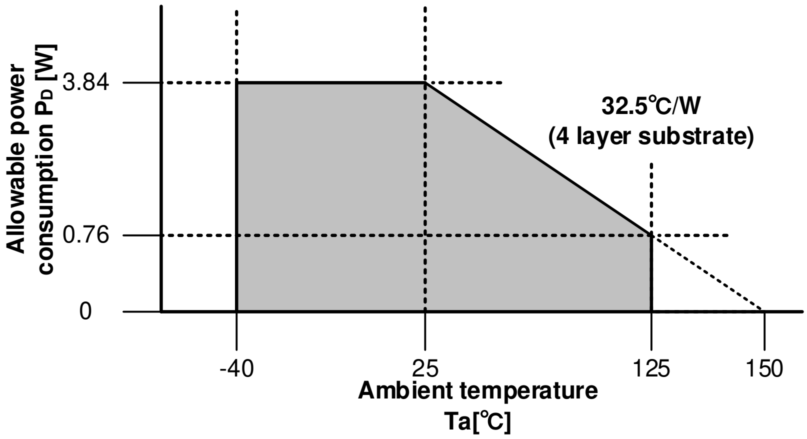
Input			Output
CAN_IN	IGN_IN	MCU_IN	wake
“L”	“L”	“L”	“L”
“H”	“＊”	“＊”	“H”
“＊”	“H”	“＊”	“H”
“＊”	“*”	“H”	“H”

※ “＊”: No Care

6. Absolute maximum ratings (Ta = 25 °C)

Item	Signal	Pin	Rating	Unit	Condition
Power voltage	V_B	VB1,VB2,VB3	-0.3 to 18	V	—
			18 to 28(≤1h)		—
			28 to 40(≤1s)		—
	V_{LDO1}	LDO1	-0.3 to 6	V	—
	V_{DD}	VDD	-0.3 to 6	V	—
Input voltage	V_{IN1}	IGN_IN,CAN_IN,	-0.3 to 18	V	—
			18 to 28(≤1h)		—
			28 to 40(≤1s)		—
	V_{IN2}	MCU_IN	-0.3 to 6	V	—
	V_{IN3}	DC1FB,DC2IN, LDO1IN	-0.3 to V_B+0.3	V	$V_{IN2} \leq 18$ $V_{IN2} \leq 28$(≤1h)
	V_{IN4}	LDOIO	-0.3 to V_{LDO1IN}+0.3	V	$V_{IN4} \leq 6V$
	V_{IN5}	TC,WS SDIN,SCLK,NSCS,CK	-0.3 to V_{LDOIO}+0.3	V	$V_{IN5} \leqq 6V$
	V_{IN6}	BSTOFF,DC1Css, DC2Css,TEST1,TEST2,TEST3,TEST4,VDDL, DC2FB,DC2FBs	-0.3 to V_{DD}+0.3	V	$V_{IN6} \leqq 6V$
Output voltage	V_{OUT1}	DC1SW1, DC1SW2	-0.3 to V_B+0.3	V	$V_{out2} \leq 18$ $V_{out2} \leq 28$(≤1h) $V_{out2} \leq 28$ to 40(1s)
	V_{OUT2}	DC1G2, DC2SW	-0.3 to V_B+0.3	V	$V_{out2} \leq 18$ $V_{out2} \leq 28$(≤1h)
	V_{OUT3}	NRST1,NRST2, NDIAG, SDOUT, OSC	-0.3 to V_{LDO1}+0.3	V	$V_{OUT3} \leq 6V$
	V_{OUT4}	TR1, TR2, TR3	-2 to V_B+0.3	V	$V_{out4} \leq 18$ $V_{out4} \leq 28$(≤1h)
Output current	I_{OUT1}	DC1SW1, DC1SW2	dc1I_{DET}	A	—
	I_{OUT2}	DC2SW	—		—
	I_{OUT3}	LDO1	ldo1I_{LMT1}		—
	I_{OUT4}	TR1,TR2,TR3,	tr1I_{LMT1}/ tr2I_{LMT1}/ tr3I_{LMT1}		—
Allowable dissipation	P_D	—	Refer to Fig.6.1.	W	—
Operating temperature	Topr	—	-40 to 125	°C	—
Storage temperature	Tstg	—	-55 to 150	°C	—

Note: Absolute maximum ratings are a set of ratings that must not be exceeded, for even a moment. Exceeding the absolute maximum ratings may cause IC breakdown, deterioration and/or damage, and consequently may damage other equipment than IC. Please keep the specified absolute maximum ratings unfailingly in any operating conditions for designing, and use the product within the specified operating ranges.



Substrate size 76.2×114.3×1.6 mm Soldering on substrate board: applicable

Fig.6.1 Allowable dissipation

7. Electrical characteristics

(Unless otherwise specified, VB1/VB2/VB3 = 2.7 to 28V in buck-boost mode/6V to 28V in buck mode (over 5.6V in buck-boost mode/over 6V in buck mode during start-up), Ta = -40 to 125 °C)

Item	Signal	Pin	Measurement condition	Minimum	Standard	Maximum	Unit
Overall characteristics							
Stand-by current	I_{CC-STB}	VB1,VB2,VB3	$I_{VB1}+I_{VB2}+I_{VB3}$ IGN_IN=CAN_IN=MCU_IN= 0V,VB1/2/3=12V,Ta=25°C	—	—	5	μA
Current consumption 1	Icc1	VB1,VB2,VB3	VB1/2/3=12V, I_{LDO1}=300mA, I_{TR1}=100mA,I_{TR2}=I_{TR3}=40mA, I_{DCDC2}=0mA	—	—	350	mA
Current consumption 2	Icc2	VB1,VB2,VB3	VB1/2/3=18V, I_{LDO1}=300mA, I_{TR1}=100mA,I_{TR2}=I_{TR3}=40mA, I_{DCDC2}=0mA	—	—	240	mA
Current consumption 3	Icc3	VB1,VB2,VB3	(VB1/2/3=18V I_{LDO1}=50mA I_{TR1}=I_{TR2}=I_{TR3}=20mA, I_{DCDC2}=400mA)	—	—	200	mA
Current consumption 4	Icc4	VB1,VB2,VB3	I_{LDO1}=0mA I_{TR1}=I_{TR2}=I_{TR3}=0mA, I_{DCDC2}=0mA	—	—	26	mA

(Unless otherwise specified, VB1/VB2/VB3 = 2.7 to 28V in buck-boost mode/6V to 28V in buck mode
(over 5.6V in buck-boost mode/over 6V in buck mode during start-up), Ta = -40 to 125 °C)

Item	Signal	Pin	Measurement condition	Minimum	Standard	Maximum	Unit
DCDC1 power supply							
Output voltage	V_{DC1}	DC1FB	VB pin voltage 7.0V to:10 to 800mA	5.7	6.0	6.3	V
			VB pin voltage 6.2 to 7.0V: 10 to 500mA	5.7	—	7.0	
			VB pin voltage 4.0V to 6.2V: 10 to 500mA 2.7V to 4.0V: 10 to 400mA	5.7	6.0	6.3	
			VB pin Voltage(Back mode) 7.0V to:10 to 800mA	5.7	6.0	6.3	
			VB pin Voltage(Back mode) 6.8V to 7V:10 to 800mA 6.0 to 6.8V:10 to 500mA	5.7	—	7.0	
Output current	Idc1		VB3 pin voltage 7.0V and over	800	—	—	mA
			VB3 pin voltage 4.0V to 7.0V	500	—	—	
			VB3 pin voltage 2.7V to 4.0V	400	—	—	
			VB3 pin Voltage (Back mode) 6.8V to	800	—	—	
			VB3 pin Voltage (Back mode) 6.0V to 6.8V	500	—	—	
Switching frequency	$dc1f_{SW}$	—	—	340	400	460	kHz
Soft start time	$dc1t_{SS}$	—	Refer to Fig.7.1. Time from 0 → 5.5 V DC1Css=0.01μF *	0.8	1.6	2.4	ms
Overcurrent detection current	$dc1I_{DET}$	—	—	1.5	2.15	2.8	A
Overcurrent detection off time	$Tdc1_{idetoff}$	—	—	—	2	—	ms
Overcurrent detection off waiting time	$Tdc1_{idetoffw}$	—	—	—	2	—	ms
Number of times of overcurrent detected	$Ndc1_{idetoff}$	—	—	—	8	—	times
H output voltage of gate driver for boost mode	$dc1V_{GH}$	DC1G2	Iout=-20mA	V_{DC1} -0.5	—	V_{DC1}	V
			Iout=-20mA (DCDC1 start & V_{DC1}<5.3V)	3.1	—	V_{DC1}	
L output voltage of gate driver for boost mode	$dc1V_{GL}$		Iout=20mA	—	—	0.5	V
DCDC2 power supply							
Output voltage	V_{DC2}	DC2FB /DC2FBs	Iload= 10mA to 800mA	1.17	1.20	1.23	V
Output current	Idc2		—	800	—	—	mA
Switching frequency	$dc2f_{SW}$	—	—	1.7	2	2.3	MHz
Soft start time	$dc2t_{SS}$	—	Refer to Fig.7.2. Time from 0→0.95*V_{DC2}[V] DC2Css=0.047μF *	0.8	1.6	2.4	ms
Overcurrent detection current	$dc2I_{DET}$	—	—	0.8	1.6	3.0	A
Overcurrent detection off time	$Tdc2_{idetoff}$	—	—	—	2	—	ms
Overcurrent detection off waiting time	$Tdc2_{idetoffw}$	—	—	—	2	—	ms
Number of times of overcurrent detected	$Ndc2_{idetoff}$	—	—	—	8	—	times
Output discharge resistance	R_{dc2dis}	DC2FB	—	40	90	180	Ω
LDO1 power supply							
Output voltage	V_{LDO1}	LDO1	Iload=1 to 400mA	4.9	5.0	5.1	V
Load stability	V_{LOAD}	LDO1	VLDO1IN=6V I_{LOAD1}=1 to 400mA	-1	0.2	1	%

Item	Signal	Pin	Measurement condition	Minimum	Standard	Maximum	Unit
Current limiter 1	$Ido1I_{LMT1}$	LDO1	—	400	—	800	mA
Current limiter 2	$Ido1I_{LMT2}$	LDO1	LDO1=0V	—	—	100	mA
Output discharge resistance	$R_{ldo1dis}$	LDO1	—	60	130	220	Ω

* The standard value for soft start time is specified for ICs. Please note that fluctuations of external capacity in DC1Css and DC2Css pins are not considered.

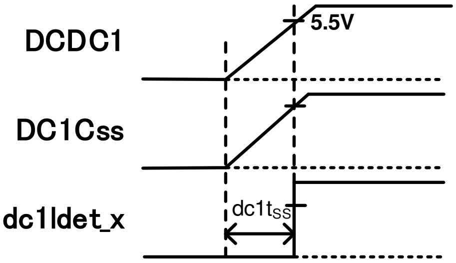


Fig.7.1 Soft start time for DCDC1

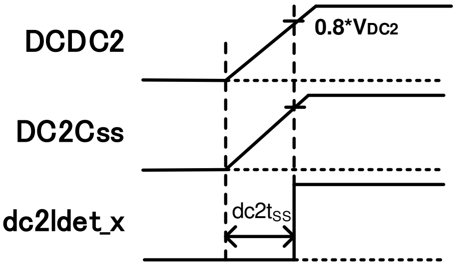


Fig.7.2 Soft start time for DCDC2

(Unless otherwise specified, VB1/VB2/VB3 = 2.7 to 28V in buck-boost mode/6V to 28V in buck mode (over 5.6V in buck-boost mode/over 6V in buck mode during start-up), Ta = -40 to 125 °C)

Item	Signal	Pin	Measurement condition	Minimum	Standard	Maximum	Unit
TR1 power supply							
Voltage difference	$V_{TR1\text{-}LDO1}$	TR1 LDO1	$I_{LDO1LOAD}$=1 to 400mA $I_{TR1LOAD}$ =1 to 100mA	-20	0	20	mV
Current limiter 1	$tr1I_{LMT1}$	TR1	—	100	—	300	mA
Current limiter 2	$tr1I_{LMT2}$	TR1	TR1=0V	—	—	26	mA
Output pull-down resistor	$tr1_{RPD}$	TR1	—	5	10	20	kΩ
TR2 power supply							
Voltage difference	$V_{TR2\text{-}LDO1}$	TR2 LDO1	$I_{LDO1LOAD}$=1 to 400mA $I_{TR2LOAD}$ =1 to 100mA	-20	0	20	mV
Current limiter 1	$tr2I_{LMT1}$	TR2	—	100	—	300	mA
Current limiter 2	$tr2I_{LMT2}$	TR2	TR2=0V	—	—	26	mA
Output pull-down resistor	$tr2_{RPD}$	TR2	—	5	10	20	kΩ
TR3 power supply							
Voltage difference	$V_{TR3\text{-}LDO1}$	TR3 LDO1	$I_{LDO1LOAD}$=1 to 400mA $I_{TR3LOAD}$ =1 to 100mA	-20	0	20	mV
Current limiter 1	$tr3I_{LMT1}$	TR3	—	100	—	300	mA
Current limiter 2	$tr3I_{LMT2}$	TR3	TR3=0V	—	—	26	mA
Output pull-down resistor	$tr3_{RPD}$	TR3	—	5	10	20	kΩ
VDD power supply							
Output voltage	V_{VDD}	VDD	—	4.5	5.0	5.5	V
Start-up VB3 voltage	Vstvb3	VDD/VB3	—	—	—	5.3	V
LDOIO							
LDOIO current	I_{LDOIO}	LDOIO	LDOIO connects LDO1	—	—	7.2	mA

(Unless otherwise specified, VB1/VB2/VB3 = 2.7 to 28V in buck-boost mode/6V to 28V in buck mode (over 5.6V in buck-boost mode/over 6V in buck mode during start-up), Ta = -40 to 125 °C)

Item	**Signal**	**Pin**	**Measurement condition**	**Minimum**	**Standard**	**Maximum**	**Unit**
Power-on reset							
Output voltage	V_{OL}	NRST1/2	I_{OL}=2mA	—	—	0.3	V
Output leak current	I_{LEAK}		V_{OUT}=LDOIO	—	—	5	μA
Pull-up resistor	R_{RST}		—	3.3	4.7	6.1	kΩ
Power-on reset	t_{POR}	NRST1	Refer to Fig.7.3.	320×C_T	400×C_T	480×C_T	ms
L retaining voltage	V_{RL}	NRST1/2	Refer to Fig.7.4	—	—	1.2	V
NRST 1/2 terminal abnormality detection filter time	tfVTHNR 1/2		Time until NRST 1/2 detects logic abnormality after H / L output	4	8	16	μs
NRST 1/2 terminal abnormality detection threshold High side	VhTHNR 1/2		Detection threshold after tfVTHNR 1/2 at H output	—	2.3	2.5	V
NRST 1/2 terminal abnormality detection threshold Low side	VTHNR1/2		Detection threshold after tfVTHNR 1/2 at Low output	1.5	1.8	—	V
Input current	I_{IN}	TC	—	-13	-10	-7	μA
Discharge resistance	R_{DIS}		—	0.5	1	2	kΩ
Threshold voltage	V_{IH}		—	3.75	4	4.25	V
Watchdog timer							
Watchdog - S	t_{WD-S}	CK	(Watchdog timer time on low speed side) Register is set to initial value.	5.0	6.0	7.5	ms
Watchdog - S max	$t_{WD-Smax}$		(Maximum pre-configurable time for watchdog timer on low speed side)	40.0	48.0	60.0	ms
Watchdog - S min	$t_{WD-Smin}$		(Minimum pre-configurable time for watchdog timer on low speed side)	5.0	6.0	7.5	ms
Watchdog - F	t_{WD-F}		(Watchdog timer time on high speed side). Register is set to initial value.	0.41	0.50	0.63	ms
Watchdog - F max	$t_{WD-Fmax}$		(Maximum pre-configurable time for watchdog timer on high speed side)	3.3	4.0	5.0	ms
Watchdog - F min	$t_{WD-Fmin}$		(Minimum pre-configurable time for watchdog timer on high speed side)	0.41	0.50	0.63	ms
Watchdog reset pulse width	t_{wdr}		—	111	160	226	μs
Watchdog clock pulse High width	t_{Wh}		Input detectable H width	1	—	—	μs
Watchdog clock pulse Low width	t_{Wl}		Input detectable L width	1	—	—	μs
Watchdog timer waiting time for initial start-up			Length of time between Power-on reset and initial watchdog clear pulse input	213	256	320	ms

Item	Signal	Pin	Measurement condition	Minimum	Standard	Maximum	Unit
Input current	I_{IH}	CK, WS	$V_{IN}=V_{LDO1}$	50	100	200	μA
	I_{IL}		V_{IN}=0V	-5	—	5	
Input voltage	V_{IH}		—	$0.75\times V_{LDO1}$	—	—	V
	V_{IL}		—	—	—	$0.25\times V_{LDO1}$	

* The standard value for Power-on reset is specified for ICs. Please note that fluctuations of C_T [μF] are not considered. Minimum time at an instantaneous power failure is 264 x C_T [ms].

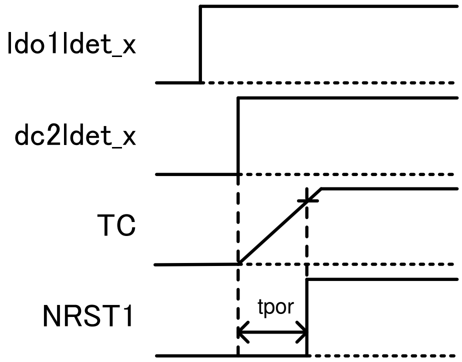


Fig.7.3 Power-on reset

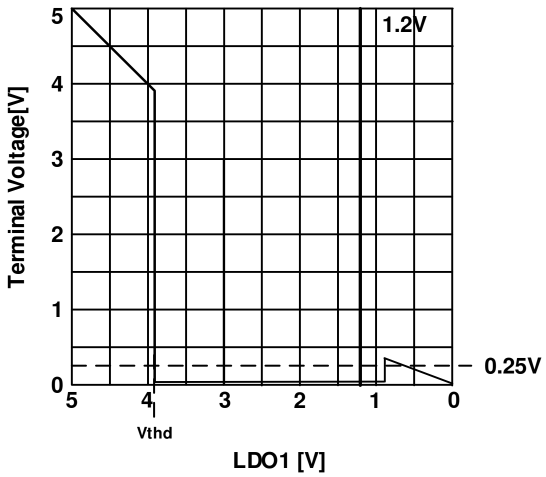


Fig.7.4 L retaining voltage

(Unless otherwise specified, VB1/VB2/VB3 = 2.7 to 28V in buck-boost mode/6V to 28V in buck mode (over 5.6V in buck-boost mode/over 6V in buck mode during start-up), Ta = -40 to 125 °C)

Item	Signal	Pin	Measurement condition	Minimum	Standard	Maximum	Unit
Power supply voltage monitoring							
DCDC1 high voltage detection	VhTH6	DC1FB	Detected	8.7	9.0	9.3	V
DCDC1 high voltage detection released	VhTH6(-)		Released	8.6	8.9	9.2	
DCDC1 high voltage detection difference voltage	dVhTH6		VhTH6-VDC1	2.7	3.0	3.3	
DCDC1 high voltage detection filtering time	tfVhTH		—	0.5	1.0	2.0	ms
DCDC2 high voltage detection	VhTH1.2	DC2FB	Detected	1.248	1.274	1.299	V
DCDC2 high voltage detection difference voltage	dVhTH1.2		VhTH1.2-VDC2(-)	0.018	0.074	0.129	
DCDC2 high voltage detection filtering time	tfVhTH		—	5	15	30	μs
LDO1 high voltage detection	VhTH5	LDO1	Detected	5.2	5.3	5.4	V
LDO1 high voltage detection released	VhTH5(-)		Released	5.1	5.2	5.3	
LDO1 high voltage detection difference voltage	dVhTH5		VhTH5-VLDO1	0.2	0.3	0.4	
LDO1 high voltage detection filtering time	tfVhTH		—	5	15	30	μs
DCDC2 low voltage detection	VTH1.2	DC2FB	Detected	1.101	1.123	1.146	V
DCDC2 low voltage detection difference voltage	dVTH1.2		VDC2 (-)-VTH1.2	0.024	0.077	0.129	
DCDC2 low voltage detection filtering time	tfVTH		—	5	15	30	μs
LDO1 low voltage detection released	VTH5(+)	LDO1	Released	4.7	4.8	4.9	V
LDO1 low voltage detection	VTH5		Detected	4.6	4.7	4.8	
LDO1 low voltage detection difference voltage	dVTH5		VLDO1-VTH5	0.15	0.30	0.45	
LDO1 low voltage detection filtering time	tfVTH		—	5	15	30	μs
VDD low voltage detection	V_{THD}	VDD	—	3.6	3.7	3.8	V
VDD high voltage detection	V_{THhD}		—	5.55	5.75	5.95	V

(Unless otherwise specified, VB1/VB2/VB3 = 2.7 to 28V in buck-boost mode/6V to 28V in buck mode
(over 5.6V in buck-boost mode/over 6V in buck mode during start-up), Ta = -40 to 125 °C)

Item	Signal	Pin	Measurement condition	Minimum	Standard	Maximum	Unit
Power supply voltage monitoring							
TR1 high voltage detection	VhTHtr1	TR1	Detected	5.2	5.4	5.6	V
TR1 high voltage detection released	VhTHtr(-)1		Released	5.1	5.3	5. 5	
TR1 high voltage detection difference voltage	dVhTHtr1		VhTHtr1-Vtr1	0.2	0.4	0.6	
TR1 high voltage detection filtering time	tfVhTH		—	5	15	30	μs
TR1 low voltage detection released	VTHtr(+)1		Released	4.5	4.7	4.9	V
TR1 low voltage detection	VTHtr1		Detected	4.4	4.6	4.8	
TR1 low voltage detection difference voltage	dVTHtr1		Vtr1-VTHtr1	0.2	0.4	0.6	
TR1 low voltage detection filtering time	tfVTH		—	5	15	30	μs
TR2 high voltage detection	VhTHtr2	TR2	Detected	5.2	5.4	5.6	V
TR2 high voltage detection released	VhTHtr(-)2		Released	5.1	5.3	5.5	
TR2 high voltage detection difference voltage	dVhTHtr2		VhTHtr2-Vtr2	0.2	0.4	0.6	
TR2 high voltage detection filtering time	tfVhTH		—	5	15	30	μs
TR2 low voltage detection released	VTHtr(+)2		Released	4.5	4.7	4.9	V
TR2 low voltage detection	VTHtr2		Detected	4.4	4.6	4.8	
TR2 low voltage detection difference voltage	dVTHtr2		Vtr2-VTHtr2	0.2	0.4	0.6	
TR2 low voltage detection filtering time	tfVTH		—	5	15	30	μs
TR3 high voltage detection	VhTHtr3	TR3	Detected	5.2	5.4	5.6	V
TR3 high voltage detection released	VhTHtr(-)3		Released	5.1	5.3	5.5	
TR3 high voltage detection difference voltage	dVhTHtr3		VhTHtr3-Vtr3	0.2	0.4	0.6	
TR3 high voltage detection filtering time	tfVhTH		—	5	15	30	μs
TR3 low voltage detection released	VTHtr(+)3		Released	4.5	4.7	4.9	V
TR3 low voltage detection	VTHtr3		Detected	4.4	4.6	4.8	
TR3 low voltage detection difference voltage	dVTHtr3		Vtr3-VTHtr3	0.2	0.4	0.6	
TR3 low voltage detection filtering time	tfVTH		—	5	15	30	μs

(Unless otherwise specified, VB1/VB2/VB3 = 2.7 to 28V in buck-boost mode/6V to 28V in buck mode (over 5.6V in buck-boost mode/over 6V in buck mode during start-up), Ta = -40 to 125 °C)

Item	Signal	Pin	Measurement condition	Minimum	Standard	Maximum	Unit
Power supply voltage monitoring							
VB low voltage detection	VTHvb(-)	VB3	At buck-boost mode detected	2.3	2.5	2.7	V
			At buck mode detected	5.4	5.6	5.8	
VB low voltage detection released	VTHvb(+)	VB3	At buck-boost mode released	4.4	5.3	5.6	V
			At buck mode released	5.6	5.8	6.0	
VB low voltage detection filtering time	tfVTH	VB3	—	5	15	30	μs

(Unless otherwise specified, VB1/VB2/VB3 = 2.7 to 28V in buck-boost mode/6V to 28V in buck mode (over 5.6V in buck-boost mode/over 6V in buck mode during start-up), Ta = -40 to 125 °C)

Item	Signal	Pin	Measurement condition	Minimum	Standard	Maximum	Unit
Input and output characteristics							
Input current	I_{IH}	IGN_IN	Vin=12V	25	50	100	μA
	I_{IL}		Vin=0V	-5	—	5	
Input voltage	V_{IH}		—	3	—	—	V
	V_{IL}		—	—	—	0.9	
Filtering time	tfVTHh		IGN_IN=0⇒under VB (rising) Time before rising to VDD=1.5V	3	—	50	μs
	tfVTHl		IGN_IN= under VB⇒0 (falling) Time before falling to VDD=4.5V	8	—	300	
Input current	I_{IH}	CAN_IN	Vin=12V	25	50	100	μA
	I_{IL}		Vin=0V	-5	—	5	
Input voltage	V_{IH}		—	3	—	—	V
	V_{IL}		—	—	—	0.9	
Filtering time	tfVTHh		CAN_IN=0⇒under VB (rising) Time before rising to VDD=1.5V	3	—	50	μs
	tfVTHl		CAN_IN= under VB⇒0 (falling) Time before falling to VDD=4.5V	8	—	300	
Input current	I_{IH}	MCU_IN	Vin=5V	25	50	100	μA
	I_{IL}		Vin=0V	-5	—	5	
Input voltage	V_{IH}		—	3	—	—	V
	V_{IL}		—	—	—	0.9	
Filtering time	tfVTHh		MCU_IN=0⇒under LDO1 (rising) Time before rising to VDD=1.5V	3	—	50	μs
	tfVTHl		MCU_IN= under LDO1⇒0 (falling) Time before falling to VDD=4.5V	8	—	300	
Input current	I_{IH}	BSTOFF	V_{IN}=5V	50	100	200	μA
	I_{IL}		V_{IN}=0V	—	—	10	
Input voltage	V_{IH}		—	0.75×V_{LDO1}	—	—	V
	V_{IL}		—	—	—	0.25×V_{LDO1}	
Output voltage	V_{OL}	NDIAG	I_{OL}=2mA	—	—	0.3	V
Output leak current	I_{LEAK}		Vin=V_{LDO1}	—	—	5	μA
Pull-up resistor	R_{diag}		—	3.3	4.7	6.1	kΩ
NRST 1/2 terminal abnormality detection filter time	tfVTHND		Time until NDIAG detects logic abnormality after H / L output	4	8	16	μs
NDIAG terminal abnormality detection threshold High side	VhTHND		Detection threshold after tfVTHND at H output	—	2.3	2.5	V
NDIAG terminal abnormality detection threshold Low side	VTHND		Detection threshold after tfVTHND at Low output	1.5	1.8	—	V
NDAIG L retaining voltage	VRL		Refer to Fig.7.4	—	—	1.2	V
OSC							

Item	Signal	Pin	Measurement condition	Minimum	Standard	Maximum	Unit
Oscillation frequency	fosc	—	—	6.8	8	9.2	MHz
Oscillation frequency monitoring	fosc_h	—	—	9.7	—	17.8	MHz
	fosc_l	—	—	3.0	—	6.3	MHz
Output Voltage	V_{OH}	OSC	I_{OH}=-2mA	0.9×V_{LDO1}	—	—	V
	V_{OL}		I_{OL}=2mA	—	—	0.1×V_{LDO1}	
TSD							
Overheat detection	TSD1, TSD2	—	—	155	170	190	°C
Overheat detection filtering time	tfTSD1, tfTSD2	—	—	5	15	30	μs

(Unless otherwise specified, VB1/VB2/VB3 = 2.7 to 28V in buck-boost mode/6V to 28V in buck mode
(over 5.6V in buck-boost mode/over 6V in buck mode during start-up), Ta = -40 to 125 °C)

Item	Signal	Pin	Measurement condition	Minimum	Standard	Maximum	Unit
ABIST/LBIST							
Waiting time for evaluation	TGDs1	—	—	—	—	30	μs
Waiting time for start-up	TGDs2	—	—	—	—	50	μs
ABIST evaluation time	TGDsa	—	—	—	—	1.2	ms
LBIST evaluation time	TGDsb	—	—	—	—	3	ms
SPI DC characteristics							
Input current	I_{IH}	SDIN, SCLK	$V_{IN}=V_{LDO1}$	50	100	200	μA
	I_{IL}		$V_{IN}=0V$	-5	—	5	
	I_{IH}	NSCS	$V_{IN}=V_{LDO1}$	-5	—	-5	
	I_{IL}		$V_{IN}=0V$	-200	-100	-50	
Input voltage	V_{IH}	SDIN, SCLK, NSCS	—	$0.75 \times V_{LDO1}$	—	—	V
	V_{IL}		—	—	—	$0.25 \times V_{LDO1}$	
Output voltage	V_{OH}	SDOUT	$I_{OH}=-2mA$	$0.9 \times V_{LDO1}$	—	—	V
	V_{OL}		$I_{OL}=2mA$	—	—	$0.1 \times V_{LDO1}$	
Output leak current	I_{LEAK}		—	-1	—	1	μA
SPI AC characteristics							
Valid waiting time	Tcsclk	NSCS SCLK	fop = 2MHz (Time from NSCS falling edge to SCLK rising edge)	250	—	—	ns
Invalid waiting time	Tckcs	SCLK NSCS	(Time from the latest SCLK falling edge to NSCS rising edge)	250	—	—	ns
NSCS falling - SDOUT delay time	Tcsdo	NSCS SDOUT	Cload=100pF (Time from NSCS falling edge to SDOUT non-3-state condition)	—	—	340	ns
SDOUT - NSCS rising delay time	Tdocs	NSCS SDOUT	Cload=100pF (Time from NSCS rising edge to SDOUT 3-state condition)	—	—	100	ns
SDIN setting time	Tdick	SDIN SCLK	(Time when SDIN is valid before SCLK falling edge)	120	—	—	ns
SDIN holding time	Tckdi	SCLK SDIN	(Time when SDIN is valid after SCLK falling edge)	120	—	—	ns
SDOUT valid time	Tckdo	SCLK SDOUT	Cload=100pF (Time from SCLK rising edge to valid output data)	—	—	100	ns
NSCS invalid time	Tcsh	NSCS	(Invalid time between consecutive NSCSs)	5	—	—	μs
Operation frequency	fop	SCLK	-	—	—	2	MHz

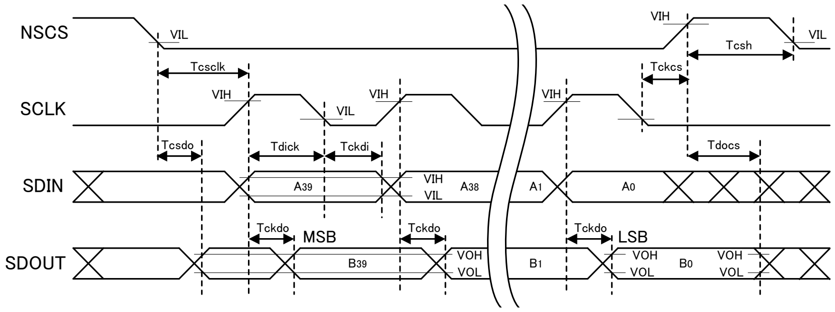
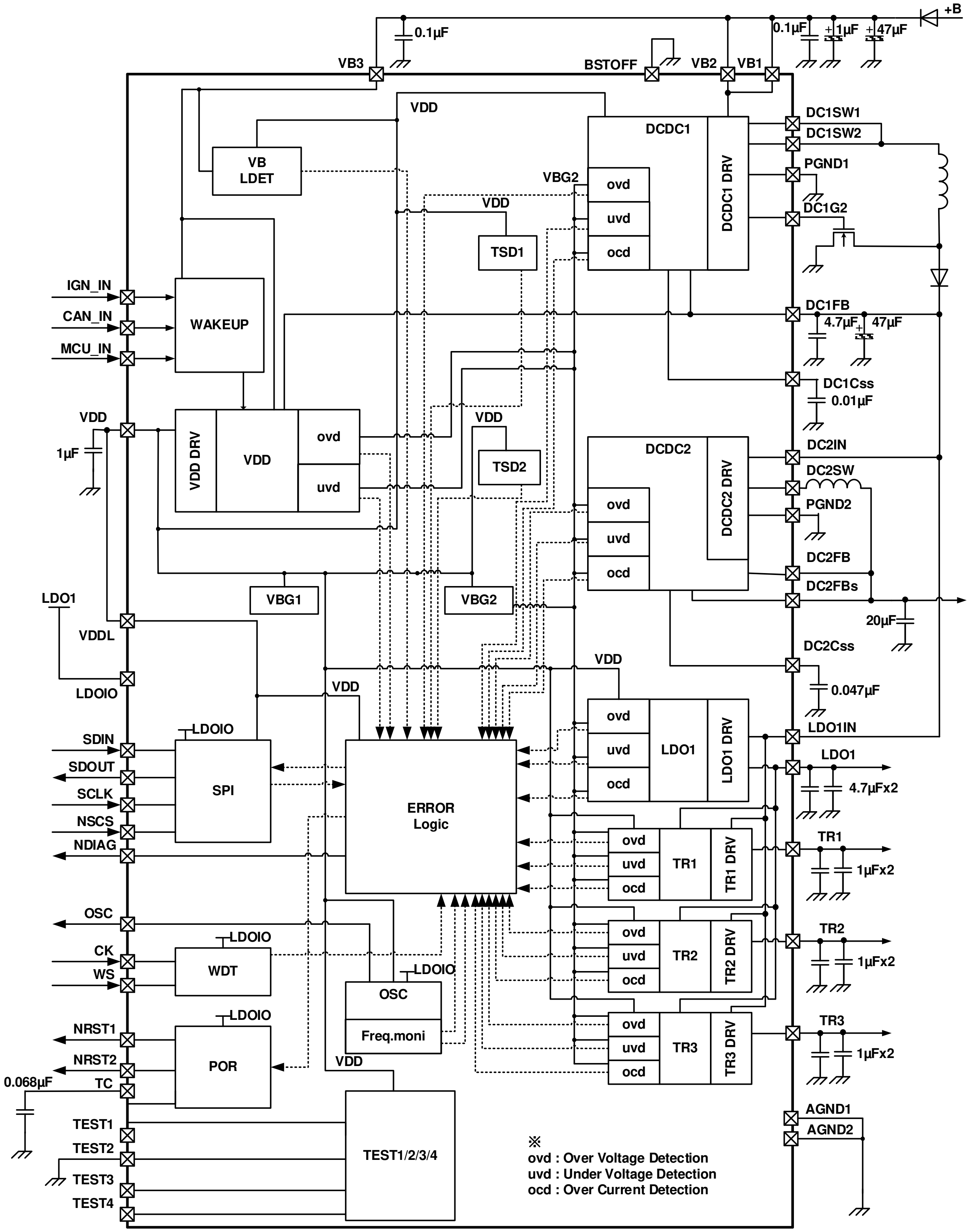


Fig.7.5 SPI Communication electrical characteristic

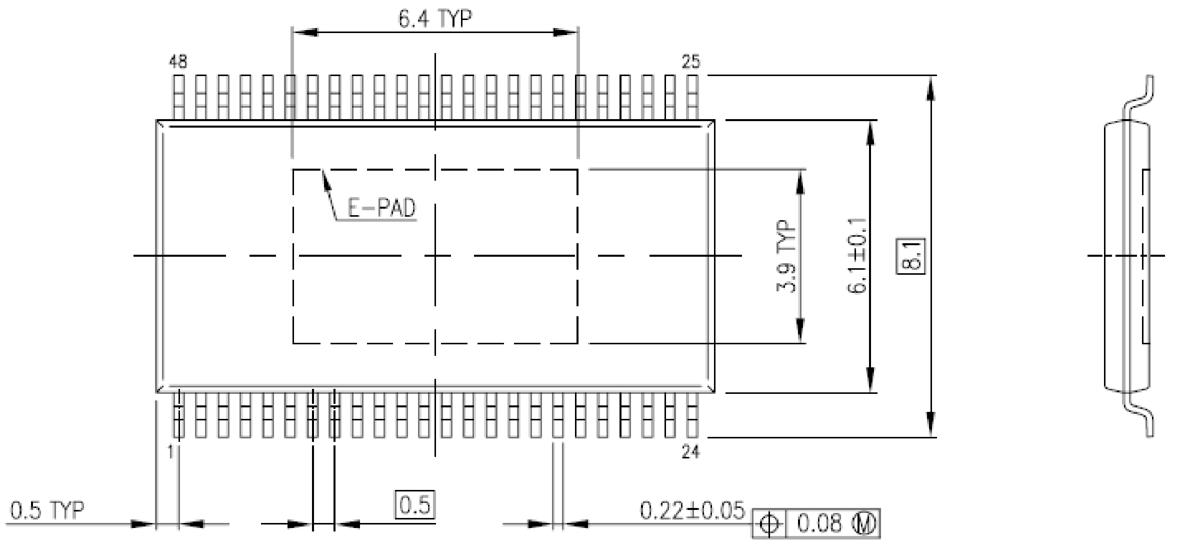
8. Examples of application circuit

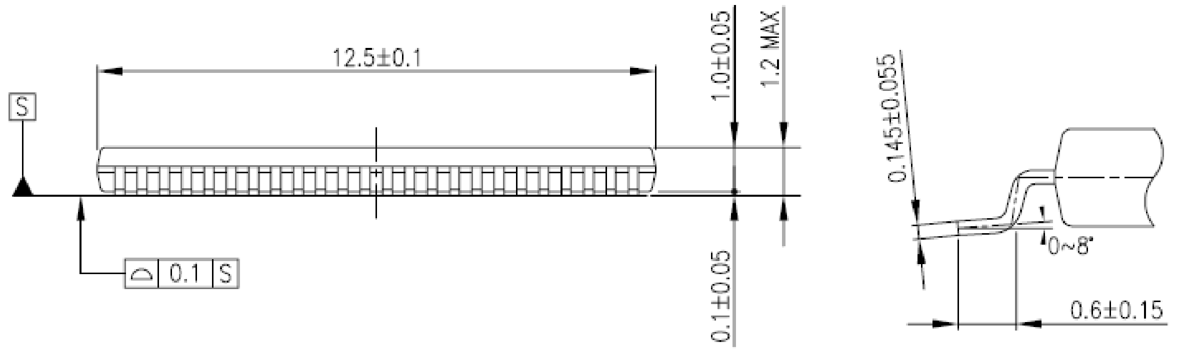


9. Package dimensions

HTSSOP48-P-300-0.50

“Unit : mm”





10. Revision history

Ver	Signal	Large category	Small category	Specification change	Date of revision
1.0	-	-	-	new	2019-06-04
1.1	1.1	Features	-	Added description of AEC-Q100 and functional safety	2019-12-10

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, and lifesaving and / or life supporting medical equipment. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

https://toshiba.semicon-storage.com/