User's Guide
SLVU436–January 2011

TPS40170EVM-578 Evaluation Module

The TPS40170EVM-578 evaluation module (EVM) is a synchronous buck converter providing a fixed 5-V output at up to 6 A from a 10-V to 60-V input bus. The EVM is designed to start up from a single supply; no additional bias voltage is required for start-up. The module uses the TPS40170 high-performance, wide-input voltage, synchronous buck controller.

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1 Introduction

1.1 Description

TPS40170EVM-578 is designed to use an unregulated bus voltage between 10 V and 60 V to provide a regulated 5-V output at up to 6 A of load current. TPS40170EVM-578 is designed to demonstrate the TPS40170 controller in a typical wide-input bus converter application while providing a number of non-invasive test points to evaluate the performance and capabilities of the TPS40170 in a typical application.

1.2 Applications

- Wide-input, unregulated bus applications
- Non-isolated telecom/datacom converters
- Automotive electronics

1.3 Features

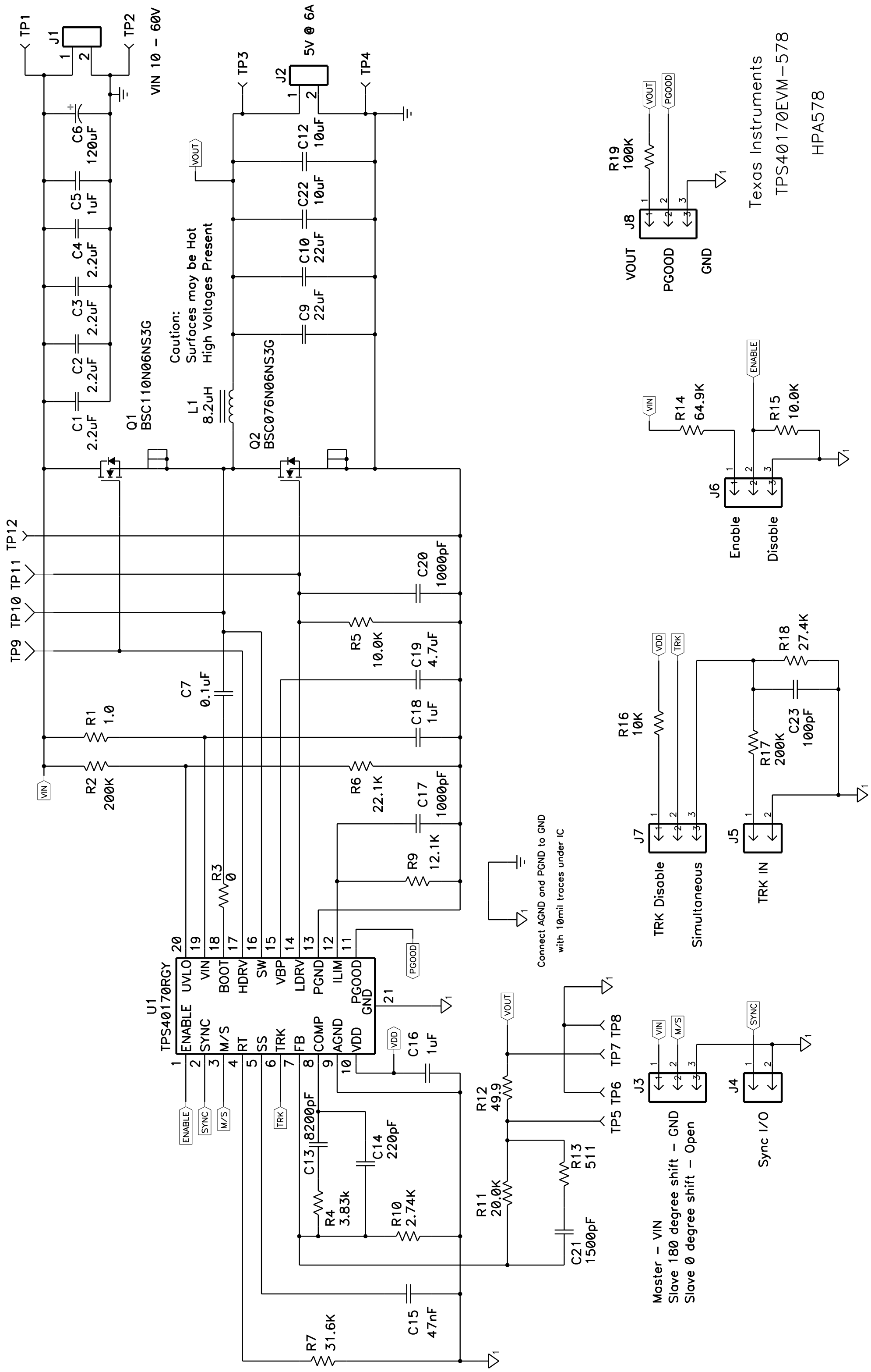
- 10-V to 60-V input voltage rating (down to 6 V with UVLO resistor change)
- 5-V ±2% output voltage rating
- 6-A, steady-state load current
- 94% efficiency 24 V to 5 V at 6 A
- 300-kHz switching frequency
- Simple access to IC features including synchronization, tracking, power good, and enable
- Convenient test points for simple, non-invasive measurements of converter performance and features.

2 TPS40170EVM-578 Electrical Performance Specifications

Table 1. TPS40170EVM-578 Electrical and Performance Specifications

Parameter		Notes and Conditions	Min	Typ	Max	Unit
Input Characteristics						
V_{IN}	Input Voltage		10	24	60	V
I_{IN}	Input Current	V_{IN} = 24 V, I_{OUT} = 6 A	–	1.3	1.5	A
	No-Load Input Current	V_{IN} = 24 V, I_{OUT} = 0 A	–	35	40	mA
V_{IN_UVLO}	Input UVLO	I_{OUT} = 10 A		9		V
Output Characteristics						
V_{OUT1}	Output Voltage 1	V_{IN} = 24 V, I_{OUT} = 3 A	4.85	5	5.15	V
	Line Regulation	V_{IN} = 10 V to 60 V	–	–	0.5%	
	Load Regulation	I_{OUT} = 0 A to 6 A	–	–	0.5%	
V_{OUT_ripple}	Output Voltage Ripple	V_{IN} = 24 V, I_{OUT} = 6 A	–	–	80	mVpp
I_{OUT1}	Output Current 1	V_{IN} = 10 V to 60 V	0		6	A
Systems Characteristics						
F_{SW}	Switching Frequency		270	300	330	kHz
ηpk	Peak Efficiency	V_{IN} = 24 V	–	94%	–	
η	Full-Load Efficiency	V_{IN} = 24 V, I_{OUT} = 6 A	–	94%	–	

3 TPS40170EVM-578 Schematic



NOTE: For Reference Only, See Table 3 for Specific Values

Figure 1. TPS40170EVM-578 Schematic

4 Connector and Test Point Descriptions

4.1 Enable Jumper - J6

TPS40170EVM-578 is designed with an Enable jumper (J6) using a 3-pin, 0.1-inch spacing header and shunt. Installing a shunt in the J6 Enable position connects the Enable pin to VIN and enables the TPS40170 controller. When the shunt is removed or installed in the Disable position, the ENABLE pin is pulled to ground. This forces the output into a high-impedance state (approximately 22 kΩ to GND).

4.2 Tracking Jumper – J7, J5

TPS40170EVM-578 is designed with a tracking enable/disable jumper (J7) using a 3-pin, 0.1-inch spacing header and shunt. Installing a shunt in J7 in the Simultaneous position connects the TRK pin to TRK IN (J5) through a matched divider. This forces VOUT to track the lower of TRK IN or the programmed output voltage (5 V).

Installing a shunt in J7 in the TRK Disable position connects TRK to VDD and disables the tracking feature. J7 must be set in this position if no input is present on the TRK IN input.

4.3 Synchronization Jumper – J3, J4

TPS40170EVM-578 is designed with a Synchronization mode jumper (J3) using a 3-pin, 0.1-inch spacing header and shunt. Installing a shunt in J3 in the Master position connects the M/S (master/slave) pin to VIN and programs the Master synchronization mode. The TPS40170 controller outputs a 50% duty cycle 3.3V SYNC signal to the SYNC I/O connector (J4). The rising edge of the SYNC signal is synchronized to the rising edge of the high-side FET (Q1).

Installing a shunt in J3 in the Slave 180 Position connects the M/S pin to GND and programs Slave 180 synchronization mode. In this mode, the SYNC I/O connector is used as an input, and the TPS40170 controller synchronizes the rising edge of the high-side FET (Q1) to the falling edge of the SYNC I/O input.

Removing the shunt from J3 leaves the M/S pin floating and programs Slave 0 synchronization mode. In this mode, the SYNC I/O connector is used as an input and the TPS40170 controller synchronizes the turnon of the high-side FET (Q1) to the rising edge of the SYNC I/O input.

In SLAVE mode, SYNC frequency must be between 270 kHz and 330 kHz. If no signal is provided at the SYNC I/O connector, switching is reduced to 240 kHz.

4.4 Power Good Jumper – J8

TPS40170EVM-578 is designed with a Power Good mode jumper (J8) using a 3-pin, 0.1-inch spacing header and shunt. Placing a shunt in J8 in the VOUT position connects Power Good to VOUT via a 100-kΩ resistor.

Removing the shunt from the J8 position leaves the PGOOD and GND pins available to connect PGOOD to the enable input of another EVM board with no active pullup.

4.5 Test Point Descriptions

Table 2. Test Point Description

Test Point	Label	Use	Section
TP1	VIN	Measurement Test Point for Input Voltage	4.5.1
TP2	GND	Ground Test Point for Input Voltage	4.5.1
TP3	VOUT	Measurement Test Point for Output Voltage	4.5.2
TP4	GND	Ground Test Point for Output Voltage	4.5.2
TP5	CHB	Measurement Test Point for Channel B of Loop Response	4.5.3
TP6	SGND	Ground Test Point for Channel B of Loop Response	4.5.3
TP7	CHA	Measurement Test Point for Channel A of Loop Response	4.5.3
TP8	SGND	Ground Test Point for Channel A of Loop Response	4.5.3

Table 2. Test Point Description (continued)

Test Point	Label	Use	Section
TP9	HDRV	Measurement Test Point for High-Side Gate Driver Voltage	4.5.4
TP10	SW	Measurement Test Point for Switching Node Voltage	4.5.4
TP11	LDRV	Measurement Test Point for Low-Side Gate Driver Voltage	4.5.4
TP12	PGND	Ground Test Point for Switch Node and Gate Drive Voltages	4.5.4

4.5.1 Input Voltage Monitoring – TP1 and TP2

TPS40170EVM-578 provides two test points for measuring the input voltage applied to the module. This allows the user to measure the actual input module voltage without losses from input cables and connectors. All input voltage measurements must be made between TP1 and TP2. To use TP1 and TP2, connect a voltmeter positive input to TP1 and input terminal to TP2.

4.5.2 Output Voltage Monitoring – TP3 and TP4

TPS40170EVM-578 provides two test points for measuring the output voltage generated by the module. This allows the user to measure the actual module output voltage without losses from output cables and connectors. All input voltage measurements must be made between TP3 and TP4. To use TP3 and TP4, connect a voltmeter positive input to TP3 and negative input to TP4.

4.5.3 Loop Response Testing – TP5, TP6, TP7, TP8, and R12

TPS40170EVM-578 provides four test points (two Signal and two Ground) for measuring the control-loop frequency response. This allows the user to measure the actual module loop response without modifying the evaluation board. A transformer isolated signal up to 30 mV can be injected between TP5 and TP7. The injected signal amplitude can be measured by the ac-coupled amplitude at CHA (TP7) and the resulting output voltage deviation can be measured at CHB (TP5). See Figure 4 for additional detail.

4.5.4 Switching Waveform Monitoring – TP9, TP10, TP11, and TP12

TPS40170EVM-578 provides three surface test points and a local power ground for measuring the switching waveforms of the module’s power stage. This allows the user to monitor actual switching waveforms during operation. Pads of exposed PCB copper are used rather than test point loops to minimize EMI radiation from the high transient voltages on the switch node. Switching waveform measurements must be made using Power Ground (TP12) as the ground reference for more accurate measurements.

5 Test Setup

5.1 Equipment

5.1.1 Voltage Source

V_{IN}

The input voltage source (VIN) needs to be a 0-V to 60-V variable dc source capable of supplying 3.5 Adc.

5.1.2 Meters

A1: Input Current Meter. 0-Adc to 3.5-Adc ammeter

V1: Input Voltage Meter. 0-V to 60-V voltmeter

V2: Output Voltage Meter. 0-V to 6-V voltmeter

5.1.3 Loads

LOAD1:

Output Load. Electronic Load set for Constant Current or Constant Resistance capable of 0 Adc to 6 Adc at 5 Vdc

5.1.4 Oscilloscope

For Output Voltage Ripple: Oscilloscope needs to be an analog or digital oscilloscope set for ac-coupled measurement with 20-MHz bandwidth limiting. Use 20-mV/division vertical resolution, 1-µs/division horizontal resolution.

For Switching Waveforms: Oscilloscope needs to be an analog or digital oscilloscope set for dc-coupled measurement with 20-MHz bandwidth limiting. Use 5-V/division or 10-V/division vertical resolution and 1-µs/division horizontal resolution.

5.1.5 Recommended Wire Gauge

VIN to J1
The connection between the source voltage (VIN) and J1 of TPS40170EVM-578 can carry as much as 3.5 Adc of current. The minimum recommended wire size is AWG 16 with the total length of wire less than 2 feet (1-foot input, 1-foot return).

J2 to LOAD1
The connection between the source voltage (VIN) and J1 of TPS40170EVM-578 can carry as much as 6 Adc of current. The minimum recommended wire size is AWG 14 with the total length of wire less than 2 feet (1-foot input, 1-foot return)

5.1.6 Other

Fan
The TPS40170EVM-578 evaluation module includes components that can get hot to the touch when operating. Because this evaluation module is not enclosed to allow probing of circuit nodes, a small fan capable of 200-400 LFM is recommended to reduce component temperatures when operating.

5.2 Equipment Setup

Shown in Figure 2 is the basic test setup recommended to evaluate the TPS40170EVM-578. Note that although the return for J1 and JP2 are the same system ground, the connections must remain separate as shown in Figure 2.

5.2.1 Procedure

1. Working at an ESD workstation, ensure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses must also be worn.
2. Prior to connecting the dc input source, V_{IN}, it is advisable to limit the source current from V_{IN} to 3.5 A maximum. Ensure that VIN is initially set to 0 V and connected as shown in Figure 2.
3. Connect VIN to J1 as shown in Figure 2.
4. Connect the ammeter A1 between VIN and J1 as shown in Figure 2.
5. Connect the voltmeter V1 to TP1 and TP2 as shown in Figure 2.
6. Connect the voltmeter V2 to TP3 and TP4 as shown in Figure 2.
7. Connect the oscilloscope Probes to desired test points per Table 2.
8. Place the fan as shown in Figure 2 and turn on, ensuring that air blows directly across the evaluation module.

5.2.2 Diagram

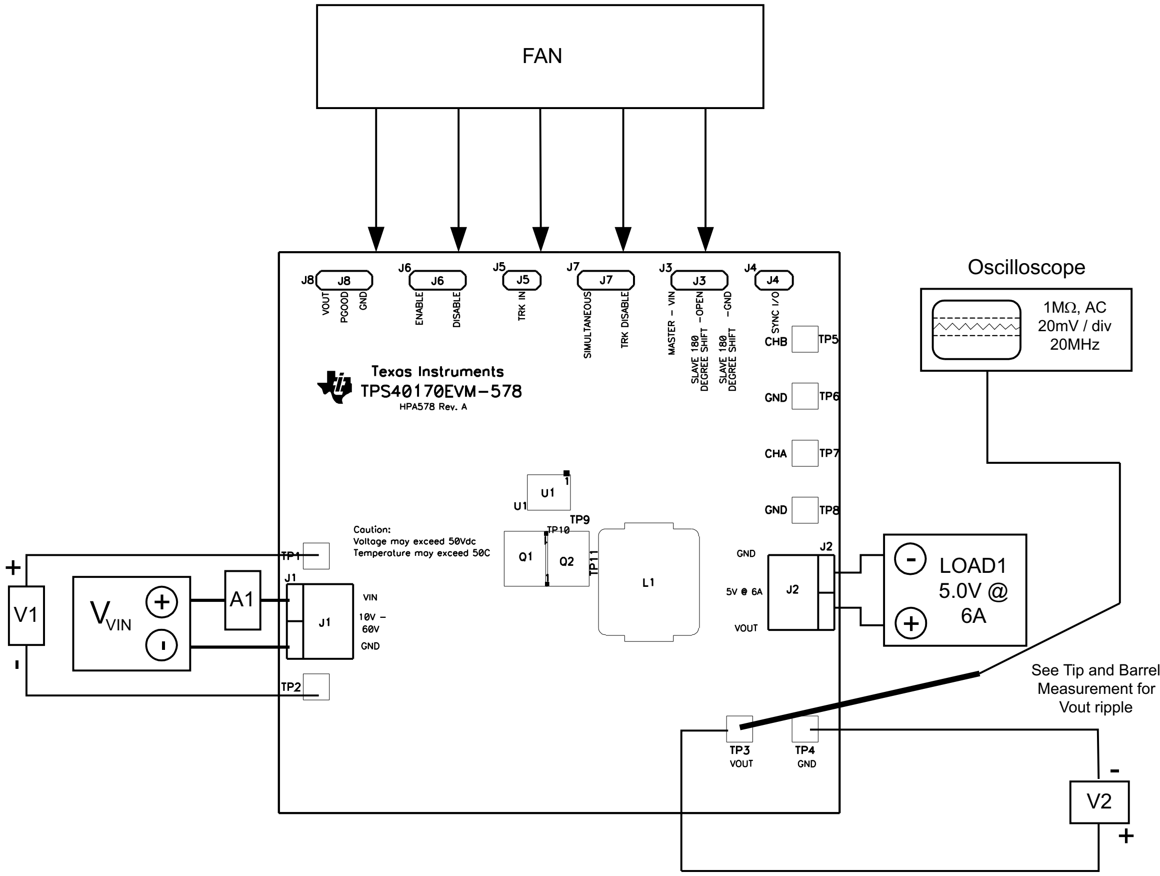


Figure 2. TPS40170EVM-578 Recommended Test Setup

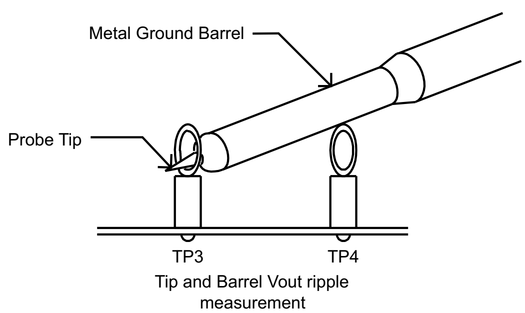


Figure 3. Output Ripple Measurement – Tip and Barrel Using TP3 and TP4

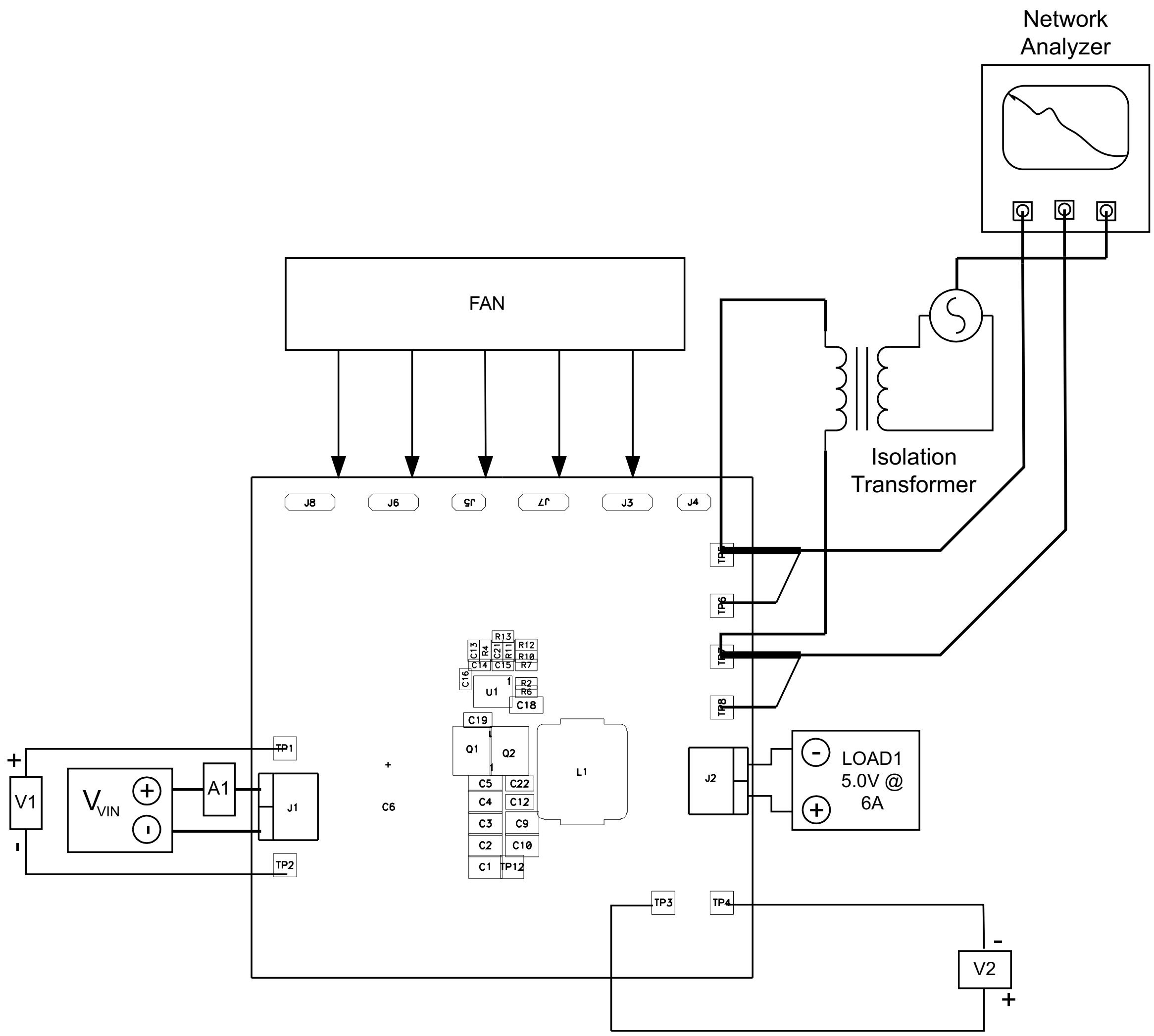


Figure 4. Control Loop Measurement Setup

5.3 Start-Up/Shut-Down Procedure

1. Verify Shunt Positions for desired operating configuration per Section 4.
2. Increase VIN from 0 Vdc to 12 Vdc.
3. Vary LOAD1 from 0 Adc to 6 Adc.
4. Vary VIN from 10 V to 60 V.
5. Decrease VIN to 0 V.
6. Decrease LOAD1 to 0 A.

5.4 Output Ripple Voltage Measurement Procedure

1. Follow Section 5.3 steps 1–5 to set VIN and LOAD1 to desired operating condition.
2. Connect oscilloscope probe with exposed metal barrel to TP3 and TP4 per Figure 3.
3. Set oscilloscope per Section 5.1.4.
4. Follow Section 5.3, steps 6 and 7 to power down.

5.5 Control Loop Gain and Phase Measurement Procedure

1. Follow Section 5.3 steps 1–5 to set Vin and LOAD1 to desired operating condition.

2. Connect 1-kHz to 1-MHz isolation transformer to TP5 and TP7 as shown in Figure 4.
3. Connect input signal amplitude measurement probe (channel A) to TP7 as shown in Figure 4.
4. Connect output signal amplitude measurement probe (channel B) to TP5 as shown in Figure 4.
5. Connect ground lead of channel A and channel B to TP6 and TP8 as shown in Figure 4.
6. Inject 30-mV or less signal across R3 through isolation transformer.
7. Sweep frequency from 1 kHz to 1 MHz with 10-Hz or lower post filter.
8. Control loop gain can be measured by $20 \times \text{LOG}\left(\frac{\text{Channel B}}{\text{Channel A}}\right)$
9. Control loop phase can be measured by the phase difference between channel A and channel B
10. Follow Section 5.3 Steps 6 and 7 to power down.

5.6 Equipment Shutdown

1. Shut down oscilloscope.
2. Shut down LOAD1.
3. Shut down VIN.
4. Shut down fan.

6 TPS40170EVM-578 Test Data

Figure 5 through Figure 11 present typical performance curves for the TPS40170EVM-578. Because actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

6.1 Efficiency

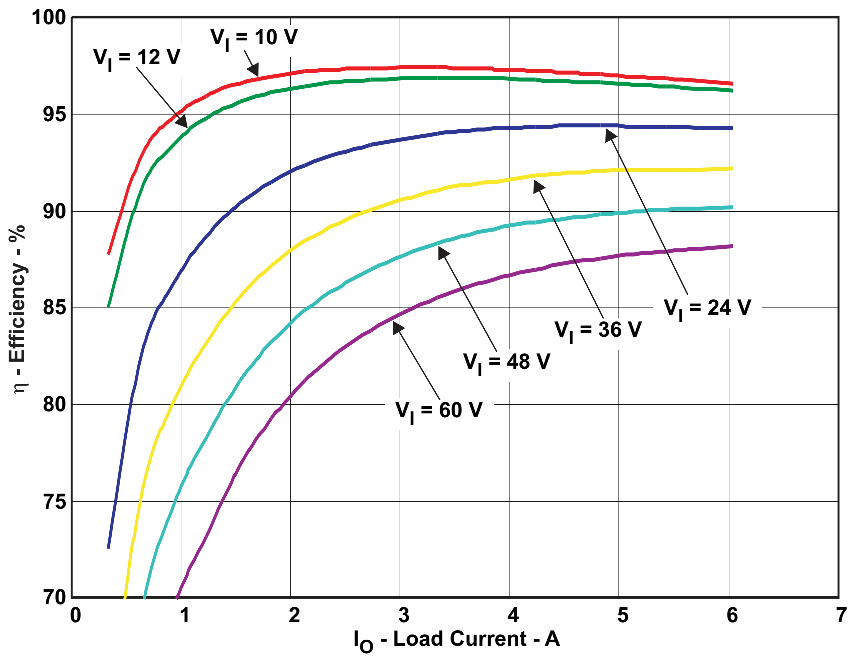


Figure 5. TPS40170EVM-578 Efficiency vs Load Current

6.2 Line and Load Regulation

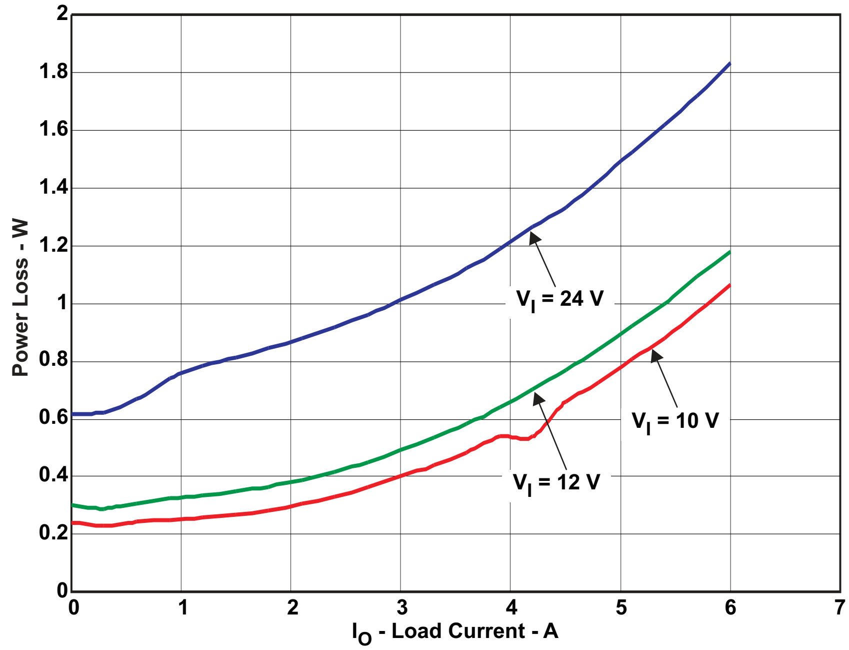


Figure 6. TPS40170EVM-578 Power Loss vs Load Current

6.3 Output Voltage Ripple

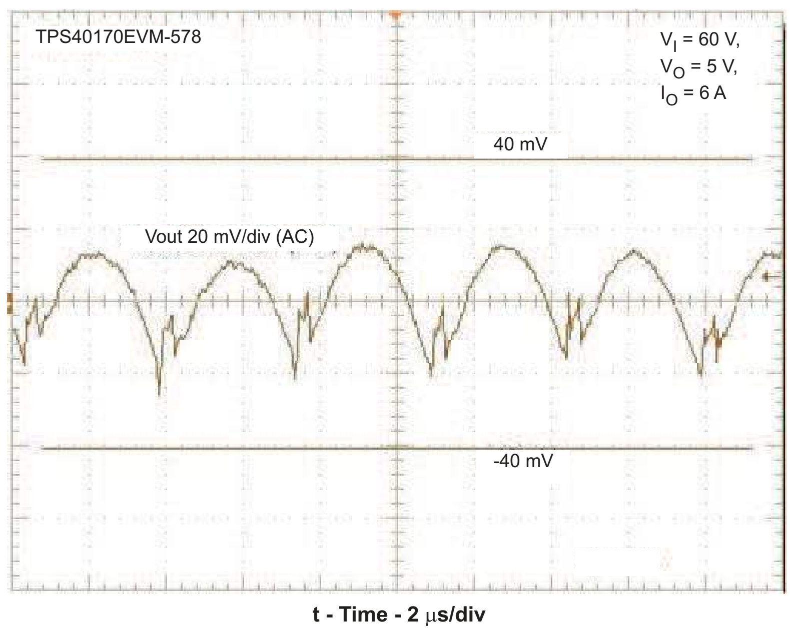


Figure 7. TPS40170EVM-578 Output Voltage Ripple

6.4 Switch Node

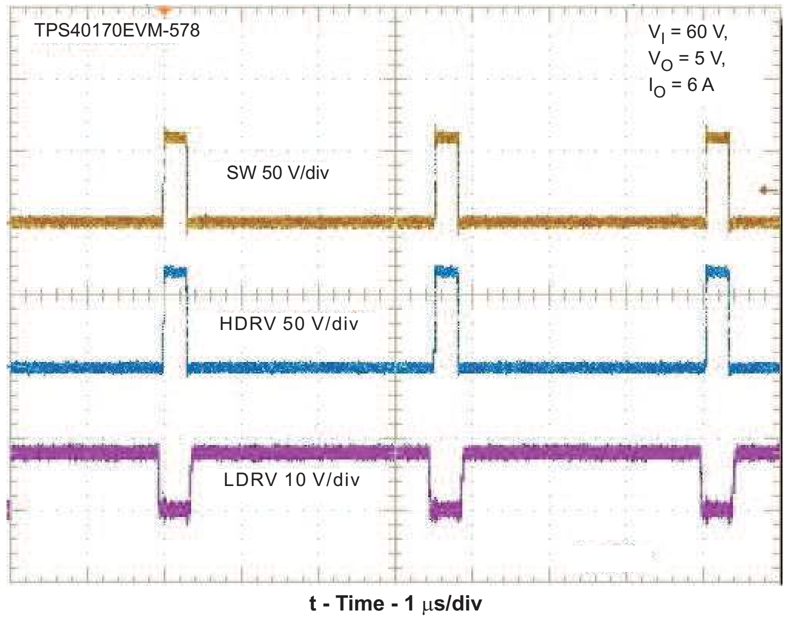


Figure 8. TPS40170EVM-578 Switching Waveforms

6.5 Control Loop Bode Diagram

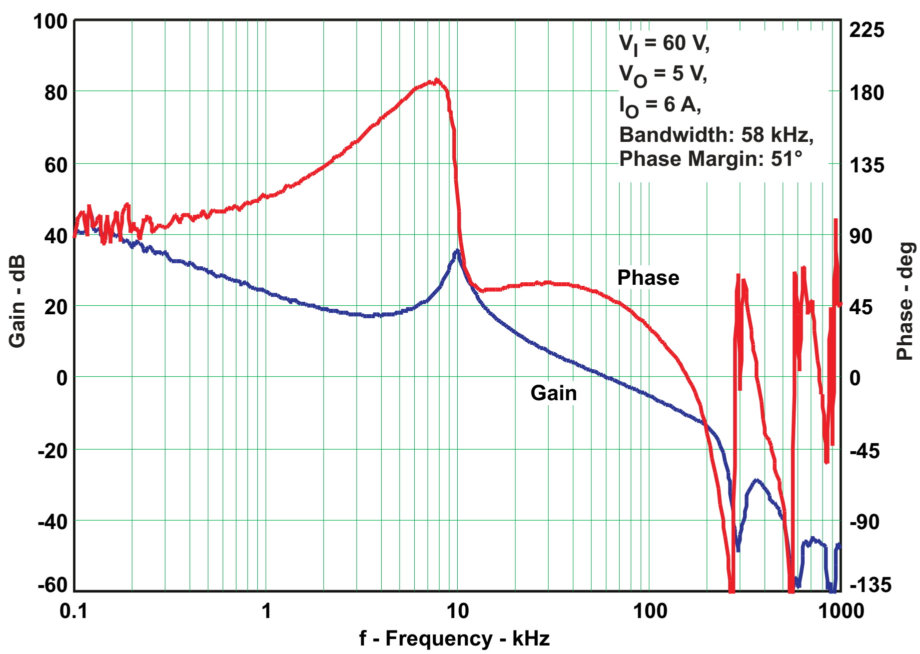


Figure 9. TPS40170EVM-578 Gain and Phase vs Frequency

6.6 Input Transient Response

The TPS40170 controller incorporates high-bandwidth voltage feedforward PWM control. This significantly improves the input transient response of the controller, allowing it to maintain regulation through large input transients.

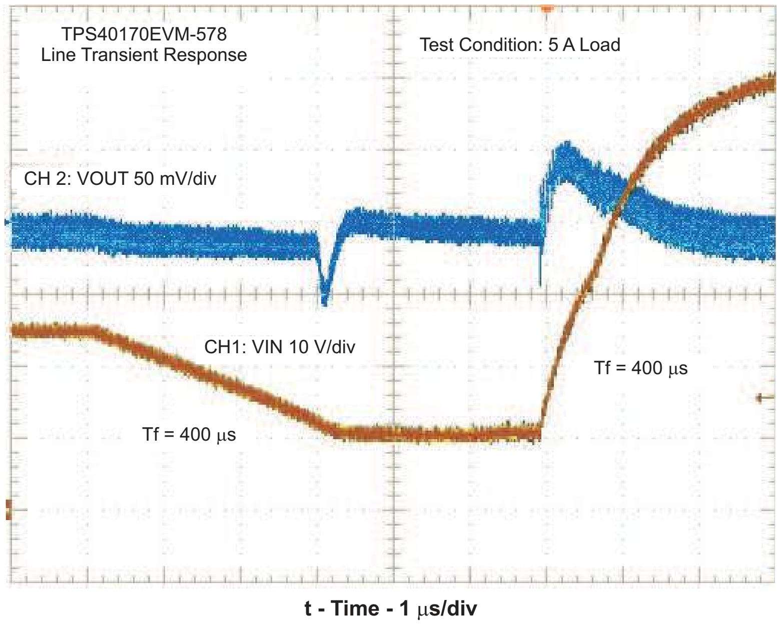


Figure 10. TPS40170EVM-578 Output Voltage During Input Transients

7 TPS40170EVM-578 Assembly Drawings and Layout

Figure 11 through Figure 17 show the design of the TPS40170EVM-578 printed-circuit board (PCB). The EVM has been designed using a 4-layer, 2-oz copper-clad circuit board 3 inch x 3 inch with all power components on the top to allow the user to easily view, probe, and evaluate the TPS40170 control IC in a practical application. Moving power components to both sides of the PCB or using additional internal layers can offer additional size reduction for space-constrained systems.

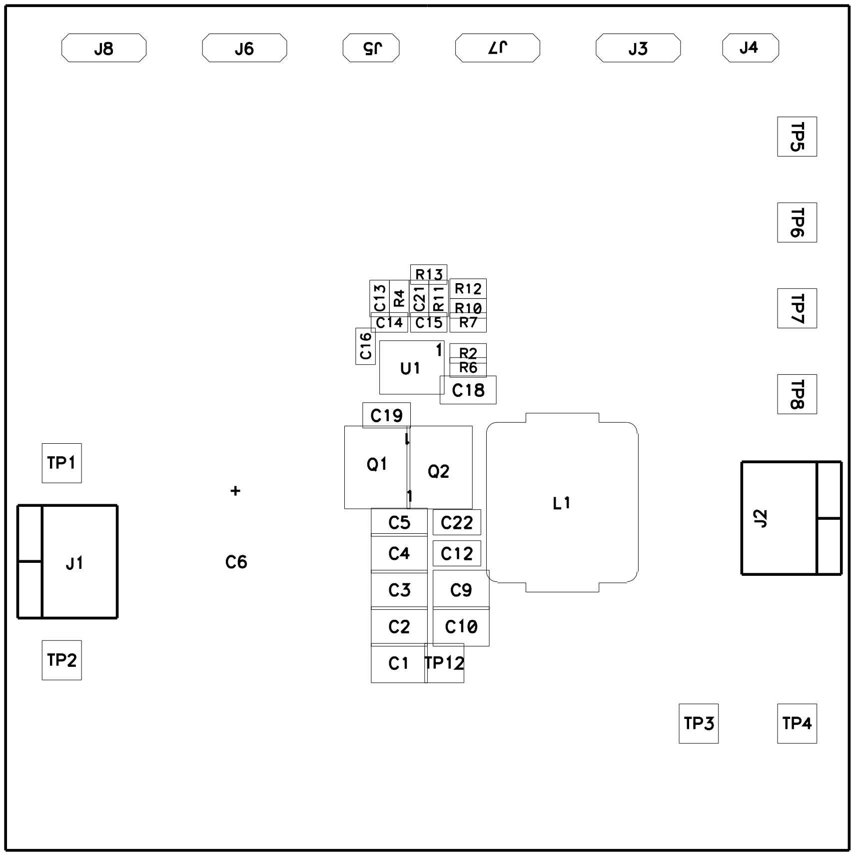


Figure 11. TPS40170EVM-578 Component Placement, Viewed From Top

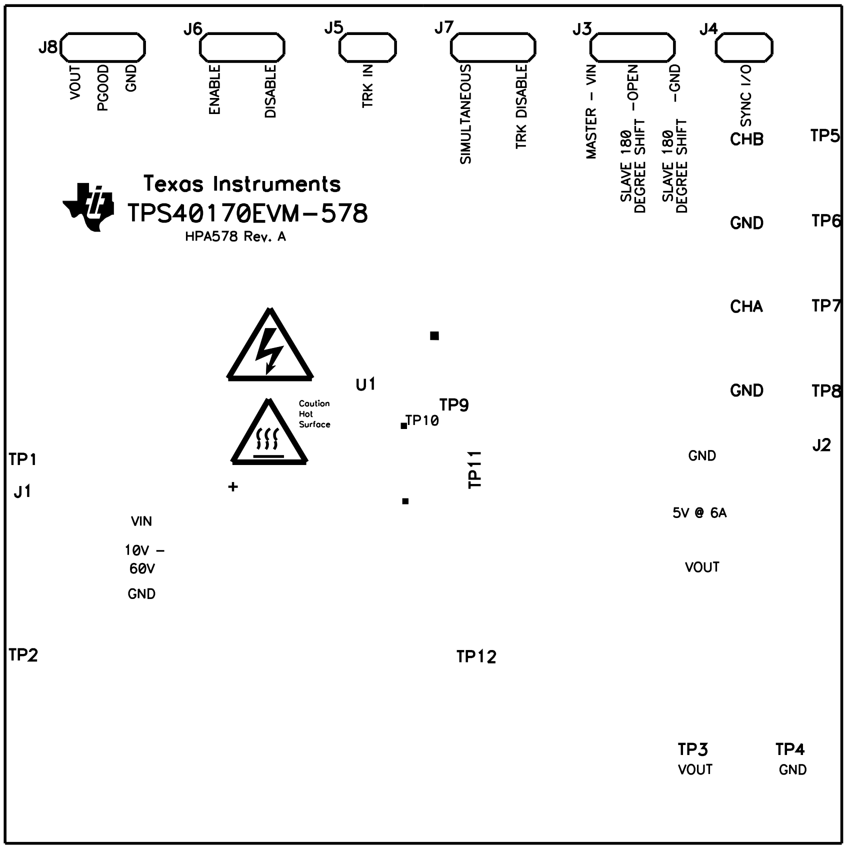


Figure 12. TPS40170EVM-578 Silk Screen, Viewed From Top

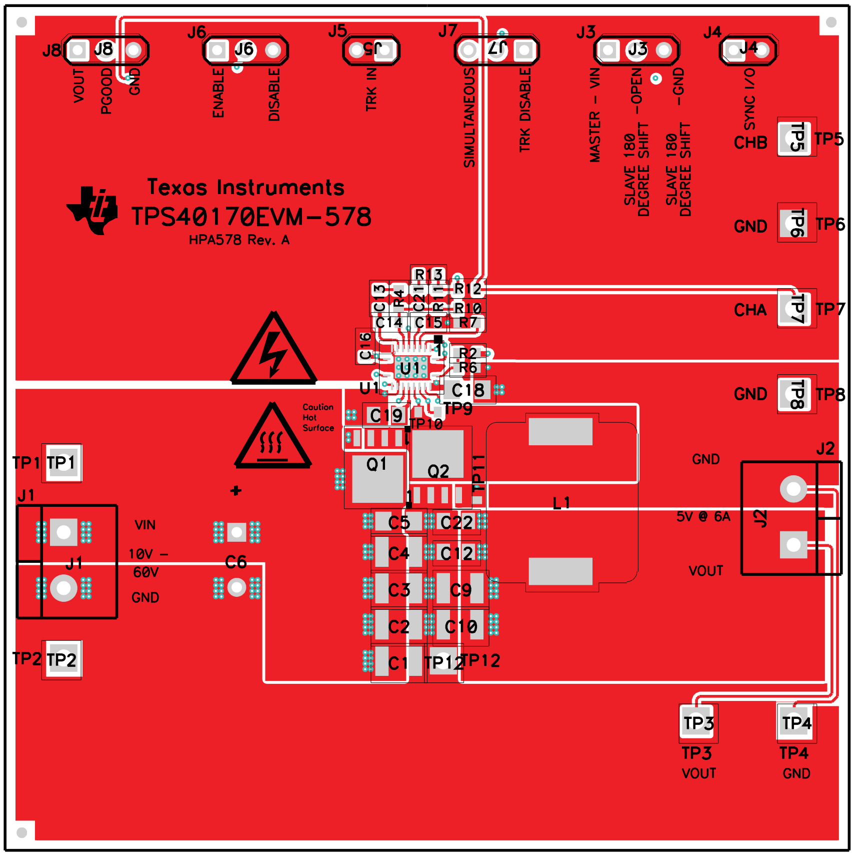


Figure 13. TPS40170EVM-578 Top Copper, Viewed From Top

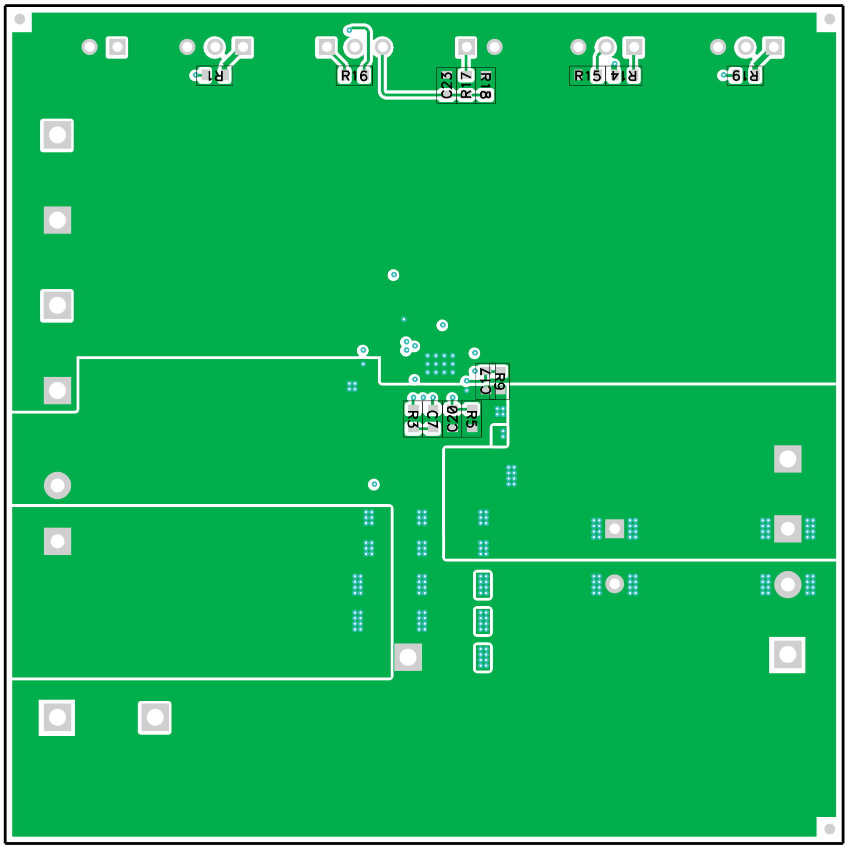


Figure 14. TPS40170EVM-578 Bottom Copper, Viewed From Bottom

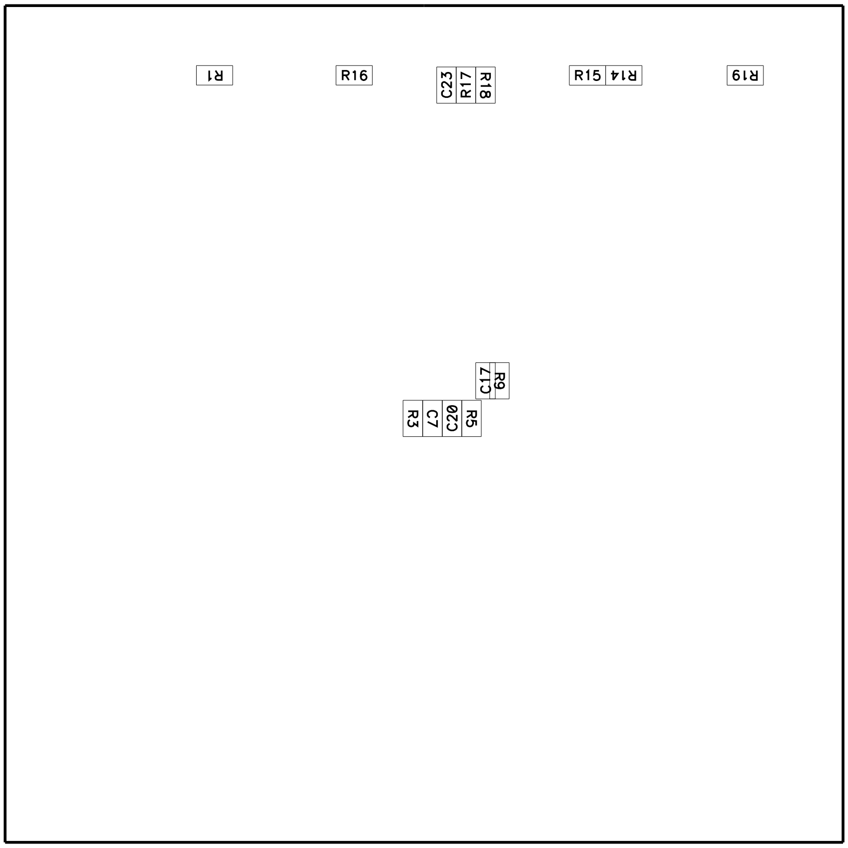


Figure 15. TPS40170EVM-578 Component Placement, Viewed From Bottom

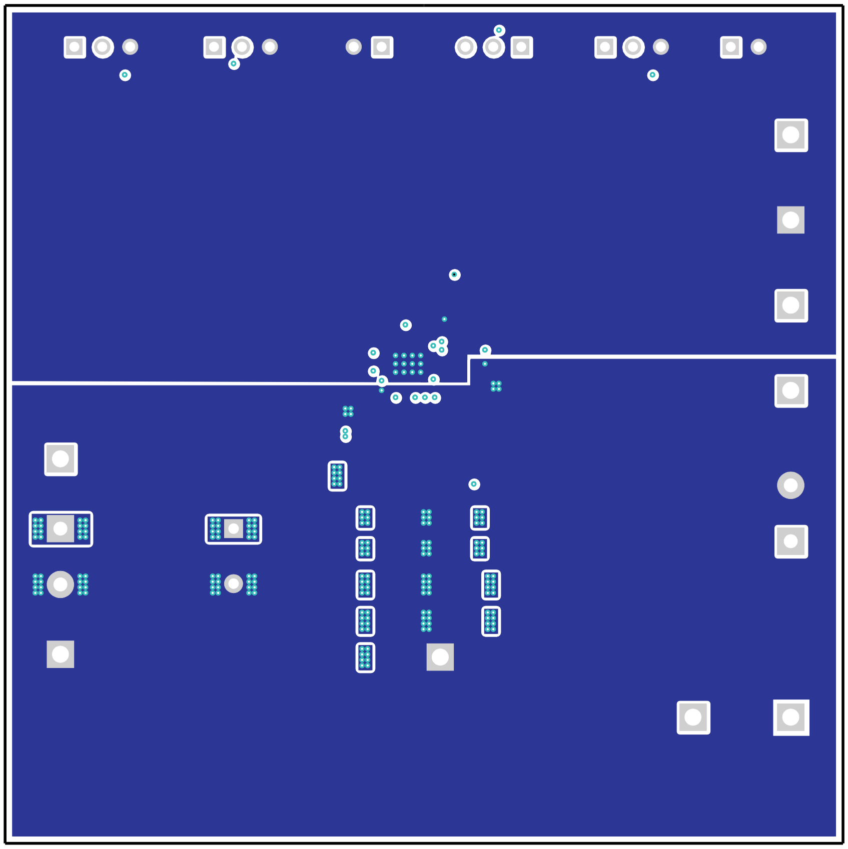


Figure 16. TPS40170EVM-578 Internal 1, X-Ray View From Top

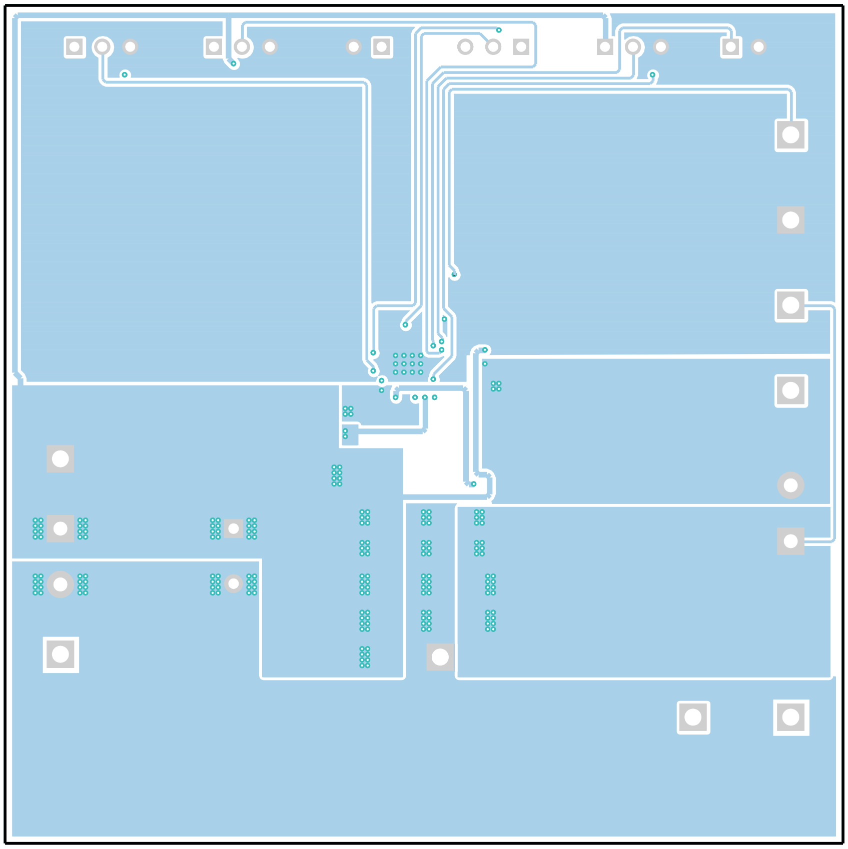


Figure 17. TPS40170EVM-578 Internal 2, X-Ray View from Top

8 Bill of Materials

Table 3. TPS40170EVM-578 Bill of Materials

Qty	RefDes	Value	Description	Size	Part Number	MFR
4	C1–C4	2.2 µF	Capacitor, Ceramic, 100V, X7R, 15%	1210	Std	Std
2	C12, C22	10 µF	Capacitor, Ceramic, 16V, X5R, 15%	0805	Std	Std
1	C13	8200 pF	Capacitor, Ceramic, 50V, X7R, 15%	0603	Std	Std
1	C14	220 pF	Capacitor, Ceramic, 50V, X7R, 15%	0603	Std	Std
1	C15	47 nF	Capacitor, Ceramic, 50V, X7R, 15%	0603	Std	Std
1	C16	1 µF	Capacitor, Ceramic, 16V, X7R, 15%	0603	Std	Std
2	C17, C20	1000 pF	Capacitor, Ceramic, 50V, X7R, 15%	0603	Std	Std
1	C19	4.7 µF	Capacitor, Ceramic, 16V, X5R, 15%	0805	Std	Std
1	C21	1500 pF	Capacitor, Ceramic, 50V, X7R, 15%	0603	Std	Std
1	C23	100 pF	Capacitor, Ceramic, 50V, X7R, 15%	0603	Std	Std
2	C5, C18	1 µF	Capacitor, Ceramic, 100V, X7R, 15%	1206	Std	Std
1	C6	120 µF	Capacitor, Aluminum, 63V, 20%, KZE Series	0.315 inch	KZE63VB121M10X16LL	Chemi-Con
1	C7	0.1 µF	Capacitor, Ceramic, 50V, X7R, 15%	0603	Std	Std
2	C9, C10	22 µF	Capacitor, Ceramic, 16V, X7R, 15%	1210	Std	Std
2	J1, J2	D120/2DS	Terminal Block, 2-pin, 15-A, 5.1mm	0.40 x 0.35 inch	D120/2DS	OST
4	J3, J6–J8	PTC03SAAN	Header, Male 3-pin, 100mil spacing	0.100 inch x 3	PTC03SAAN	Sullins
2	J4, J5	PTC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PTC02SAAN	Sullins
1	L1	8.2 µH	Inductor, SMT, 10A, 16 mΩ	0.51 x 0.51 inch	IHLP5050FDER8R2M01	Vishay
1	Q1	BSC110N06NS3G	MOSFET, Nch, 60V, 50A, 11 mΩ	TDSON-8	BSC110N06NS3G	Infineon

Table 3. TPS40170EVM-578 Bill of Materials (continued)

Qty	RefDes	Value	Description	Size	Part Number	MFR
1	Q2	BSC076N06NS3G	MOSFET, Nch, 60V, 50A, 7.6 mΩ	TDSON-8	BSC076N06NS3G	Infineon
1	R1	1	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R10	2.74K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R11	20.0K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R12	49.9	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R13	511	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R14	64.9K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R18	27.4K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R19	100K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R2, R17	200K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	3.83k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
3	R5, R15, R16	10.0K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	22.1K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	31.6K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R9	12.1K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	TP1, TP3	5010	Test Point, Red, Thru Hole	0.125 x 0.125 inch	5010	Keystone
5	TP2, TP4, TP6, TP8, TP12	5011	Test Point, Black, Thru Hole	0.125 x 0.125 inch	5011	Keystone
2	TP5, TP7	5012	Test Point, White, Thru Hole	0.125 x 0.125 inch	5012	Keystone
3	TP9–TP11		Test Point, SM, 2x3mm	0.118 x 0.079 inch		
1	U1	TPS40170RGY	IC, 4.5V–60V Wide Input Sync. PWM Buck Controller	QFN-20	TPS40170RGY	TI
4	–		Shunt, 100-mil, Black	0.100	929950-00	3M

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Please read the User’s Guide and, specifically, the Warnings and Restrictions notice in the User’s Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI’s environmental and/or safety programs, please contact the TI application engineer or visit www.ti.com/esh.

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FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 8 V to 60 V and the output voltage range of 2.5 V to 6 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.