LED Drivers for LCD Backlights

2ch Boost up type White LED Driver for large LCD

BD9416FS

1.1 General Description

BD9416FS is a high efficiency driver for white LEDs and is designed for large LCDs. BD9416FS has a boost DCDC converter that employs an array of LEDs as the light source.
BD9416FS has some protection functions against fault conditions, such as over-voltage protection (OVP), over current limit protection of DCDC (OCP), LED OCP protection, and Over boost protection (FBMAX). Therefore it is available for the fail-safe design over a wide range output voltage.

Features

- DCDC Converter with Current Mode
- LED Protection Circuit (Over Boost Protection, LED OCP Protection)
- Over Voltage Protection (OVP) for the Output Voltage VOUT
- Adjustable Soft Start
- Adjustable Oscillation Frequency of DCDC
- Analog Dimming from 0.2V to 3.0V
- LED Dimming PWM Over Duty Protection(ODP)

Applications

- TV, Computer Display, LCD Backlighting

Key Specifications

- Operating Power Supply Voltage Range: 9.0V to 35.0V
- Oscillator Frequency of DCDC: 150kHz (R_{RT}=100kΩ)
- Operating Current: 5.1mA(Typ)
- Operating Temperature Range: -40°C to +105°C

1.2 Packages

	W(Typ) x D(Typ) x H(Max)
SSOP-A24 (BD9416FS)	10.00mm x 7.80mm x 2.10mm
	Pin pitch 0.8mm

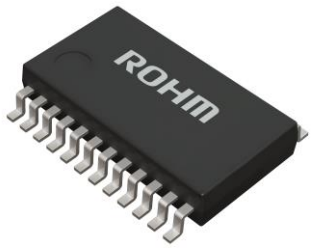


Figure 1. SSOP-A24

1.3 Typical Application Circuit

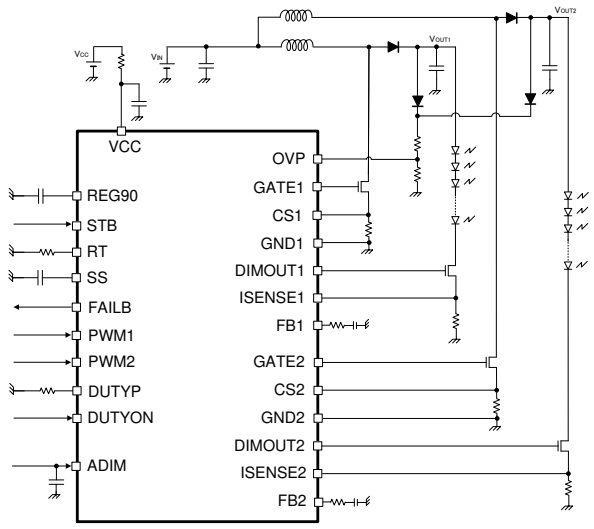


Figure 2. Typical Application Circuit

Contents

1.4 Pin Configuration

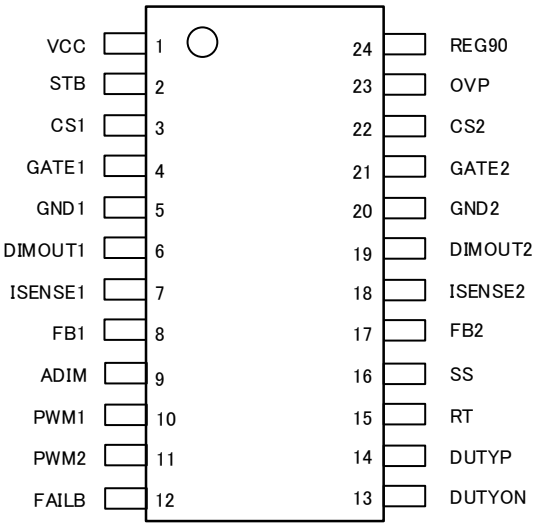


Figure 3. Pin Configuration

1.5 Pin Descriptions

No.	Pin Name	IN/OUT	Function
1	VCC	IN	Power supply pin
2	STB	IN	IC ON/OFF pin
3	CS1	IN	DC/DC output current detect pin, OCP input pin ch1
4	GATE1	OUT	DC/DC switching output pin ch1
5	GND1	-	GND ch1
6	DIMOUT1	OUT	Dimming signal output for NMOS ch1
7	ISENSE1	IN	LED current detection input pin ch1
8	FB1	OUT	Error amplifier output pin ch1
9	ADIM	IN	ADIM signal input pin
10	PWM1	IN	External PWM dimming signal input pin ch1
11	PWM2	IN	External PWM dimming signal input pin ch2
12	FAILB	OUT	Error detection output pin
13	DUTYON	IN	Over Duty Protection ON/OFF pin
14	DUTYP	OUT	Over Duty Protection reference frequency setting pin
15	RT	OUT	DC/DC switching frequency setting pin
16	SS	OUT	Soft start setting pin
17	FB2	OUT	Error amplifier output pin ch2
18	ISENSE2	IN	LED current detection input pin ch2
19	DIMOUT2	OUT	Dimming signal output for NMOS ch2
20	GND2	-	GND ch2
21	GATE2	OUT	DC/DC switching output pin ch2
22	CS2	IN	DC/DC output current detect pin, OCP input pin ch2
23	OVP	IN	Over voltage protection detection pin
24	REG90	OUT	9.0V output voltage pin

1.6 Block Diagram

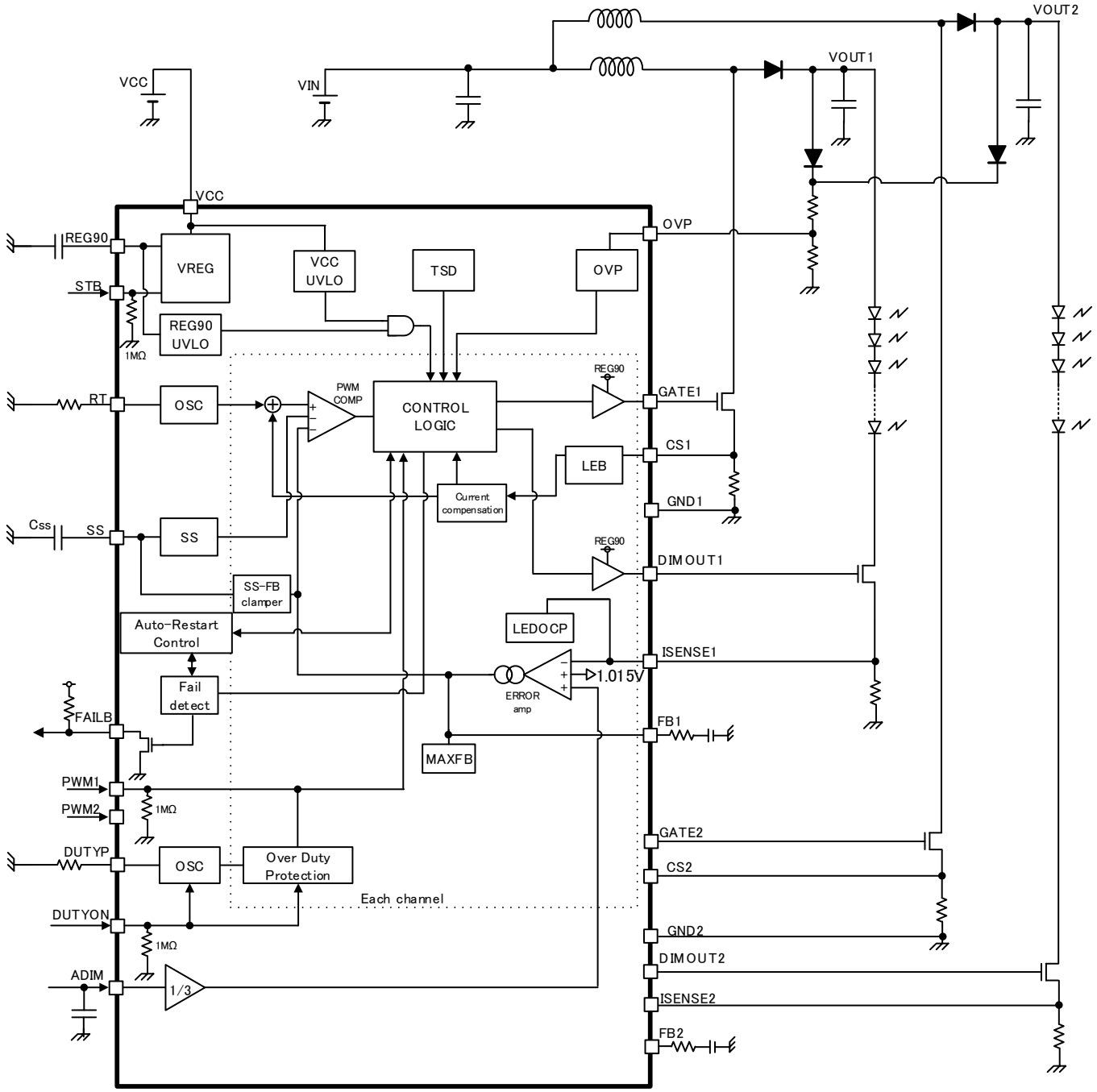


Figure 4. Block Diagram

1.7 Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	-0.3 to +36	V
SS, RT, ISENSE1, ISENSE2, FB1, FB2, CS1, CS2, DUTYP Pin Voltage	V_{SS},V_{RT},$V_{ISENSE1}$, $V_{ISENSE2}$, V_{FB1},V_{FB2}, V_{CS1},V_{CS2},V_{DUTYP}	-0.3 to +7	V
REG90, DIMOUT1, DIMOUT2, GATE1, GATE2 Pin Voltage	V_{REG90},$V_{DIMOUT1}$, $V_{DIMOUT2}$,V_{GATE1}, V_{GATE2}	-0.3 to +13	V
OVP, PWM1, PWM2, ADIM, STB, FAILB, DUTYON Pin Voltage	V_{OVP},V_{PWM1},V_{PWM2}, V_{ADIM},V_{STB},V_{FAILB}, V_{DUTYON}	-0.3 to +20	V
Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.*

1.8 Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
SSOP-A24				
Junction to Ambient	θ_{JA}	104.4	54.1	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	7	6	°C/W

(Note 1) Based on JESD51-2A(Still-Air).

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

1.9 Recommended Operating Ranges

Parameter	Symbol	Range	Unit
Operating Temperature Range	Topr	-40 to +105	°C
Power Supply Voltage	V_{CC}	9.0 to 35.0	V
DC/DC Oscillation Frequency	f_{SW}	50 to 1000	kHz
Effective Range of ADIM Signal	V_{ADIM}	0.2 to 3.0	V
PWM Input Frequency	f_{PWM}	90 to 2000	Hz

2.0 Electrical Characteristics (Unless otherwise specified VCC=24V Ta=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
【Total Current Consumption】						
Circuit Current	I_{CC}	—	5.1	10.2	mA	V_{STB}=3.0V, V_{PWM}=3.0V
Circuit Current (standby)	I_{ST}	—	55	110	μA	V_{STB}=0V
【UVLO Block】						
Operation Voltage（VCC）	V_{UVLO_VCC}	6.5	7.5	8.5	V	V_{CC}=SWEEP UP
Hysteresis Voltage（VCC）	V_{UHYS_VCC}	—	300	600	mV	V_{CC}=SWEEP DOWN
【DC/DC Block】						
ISENSE Threshold Voltage 1	V_{LED1}	0.225	0.233	0.242	V	V_{ADIM}=0.7V
ISENSE Threshold Voltage 2	V_{LED2}	0.656	0.667	0.677	V	V_{ADIM} =2.0V
ISENSE Threshold Voltage 3	V_{LED3}	0.988	1.000	1.012	V	V_{ADIM} =3.0V
ISENSE Clamp Voltage	V_{LED4}	0.989	1.015	1.040	V	V_{ADIM} =3.3V (as masking analog dimming)
Oscillation Frequency	f_{CT}	142.5	150.0	157.5	KHz	R_{RT}=100kΩ
RT Short Protection Range	V_{RT_DET}	-0.3	-	$+V_{RTN}$ ×90% *(Note 5)*	V	V_{RT}=SWEEP DOWN
RT Terminal Voltage	V_{RT}	1.6	2.0	2.4	V	R_{RT} =100kΩ
GATE Pin MAX DUTY Output	MAX_DUTY	90	95	99	%	R_{RT} =100kΩ
GATE Pin ON Resistance (as source)	R_{ONSOG}	2.5	5.0	10.0	Ω	
GATE Pin ON Resistance (as sink)	R_{ONSIG}	2.0	4.0	8.0	Ω	
SS Pin Source Current	I_{SSSO}	-3.75	-3.00	-2.25	μA	V_{SS}=2.0V
SS Pin ON Resistance at OFF	R_{SS_L}	-	3.0	5.0	kΩ	
【DC/DC Block】						
Soft Start Ended Voltage	V_{SS_END}	3.52	3.70	3.88	V	V_{SS} =SWEEP UP
FB Source Current	I_{FBSO}	-115	-100	-85	μA	V_{ISENSE}=0.2V, V_{ADIM}=3.0V, V_{FB}=1.0V
FB Sink Current	I_{FBSI}	85	100	115	μA	V_{ISENSE}=2.0V, V_{ADIM}=3.0V, V_{FB}=1.0V
【DC/DC Protection Block】						
OCP Detect Voltage	V_{OCP}	360	400	440	mV	V_{CS}=SWEEP UP
OCP Latch Off Detect Voltage	V_{OCPLT}	0.85	1.00	1.15	V	V_{CS} =SWEEP UP
OVP Detect Voltage	V_{OVP}	2.88	3.00	3.12	V	V_{OVP}=SWEEP UP
OVP Detect Hysteresis	V_{OVP_HYS}	150	200	250	mV	V_{OVP}=SWEEP DOWN
OVP Pin Leak Current	I_{OVP_LK}	-2	0	+2	μA	V_{OVP}=4.0V, V_{STB}=3.0V
【LED Protection Block】						
LED OCP Detect Voltage	V_{LEDOCP}	2.88	3.00	3.12	V	V_{ISENSE}=SWEEP UP
Over Boost Detection Voltage	V_{FBH}	3.84	4.00	4.16	V	V_{FB}=SWEEP UP
【Dimming Block】						
ADIM Pin Leak Current	I_{LADIM}	-2	0	+2	μA	V_{ADIM}=2.0V
ISENSE Pin Leak Current	I_{L_ISENSE}	-2	0	+2	μA	V_{ISENSE}=4.0V
DIMOUT Source ON Resistance	R_{ONSOD}	4.0	8.0	16.0	Ω	
DIMOUT Sink ON Resistance	R_{ONSID}	3.0	6.5	13.0	Ω	
【REG90 Block】						
REG90 Output Voltage 1	V_{REG90_1}	8.910	9.000	9.090	V	I_O=0mA
REG90 Output Voltage 2	V_{REG90_2}	8.865	9.000	9.135	V	I_O=-15mA
REG90 Available Current	$\lvert I_{REG90} \rvert$	15	-	-	mA	
REG90_UVLO Detect Voltage	V_{REG90_TH}	5.22	6.00	6.78	V	V_{REG90}=SWEEP DOWN, V_{STB}=0V

(Note 5) V_{RTN} is the RT terminal voltage at normal operation.

2.0 Electrical Characteristics (Unless otherwise specified VCC=24V Ta=25°C) - continued

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
【STB Block】						
STB Pin HIGH Voltage	V_{STB_H}	2.0	-	18	V	
STB Pin LOW Voltage	V_{STB_L}	-0.3	-	+0.8	V	
STB Pull Down Resistance	R_{STB}	600	1000	1400	kΩ	V_{STB}=3.0V
【PWM Block】						
PWM Pin HIGH Voltage	V_{PWM_H}	1.5	-	18	V	
PWM Pin LOW Voltage	V_{PWM_L}	-0.3	-	+0.8	V	
PWM Pin Pull Down Resistance	R_{PWM}	600	1000	1400	kΩ	V_{PWM}=3.0V
【DUTYON Block】						
DUTYON Pin HIGH Voltage	V_{DTYON_H}	1.5	-	18	V	
DUTYON Pin LOW Voltage	V_{DTYON_L}	-0.3	-	+0.8	V	
DUTYON Pin Pull Down Resistance	R_{DTYON}	600	1000	1400	kΩ	V_{DUTYON}=3.0V
【Over Duty Protection Block】						
PWM ODP Protection Detect Duty	D_{ODP}	-	35	-	%	f_{PWM}=120Hz, R_{DUTYP}=341kΩ
DUTYP Short Protection Range	V_{DTYP_DET}	-0.3	-	$+V_{DUTYPN}$ ×90% *(Note 6)*	V	V_{DUTYP}=SWEEP DOWN
DUTYP Terminal Voltage	V_{DTYP}	1.6	2.0	2.4	V	R_{DUTYP}=100kΩ
【Filter Block】						
Abnormal Detection Timer	t_{CP}	-	20	-	ms	f_{CT}=800kHz
AUTO Timer	t_{AUTO}	-	163	-	ms	f_{CT}=800kHz
【FAILB Block 】						
FAILB Pin LOW Voltage	V_{FAILBL}	0.25	0.5	1.0	V	I_{FAILB}=1mA

(Note 6) V_{DUTUPN} is the DUTYP terminal voltage at normal operation.

2.1 Typical Performance Curves (Reference data)

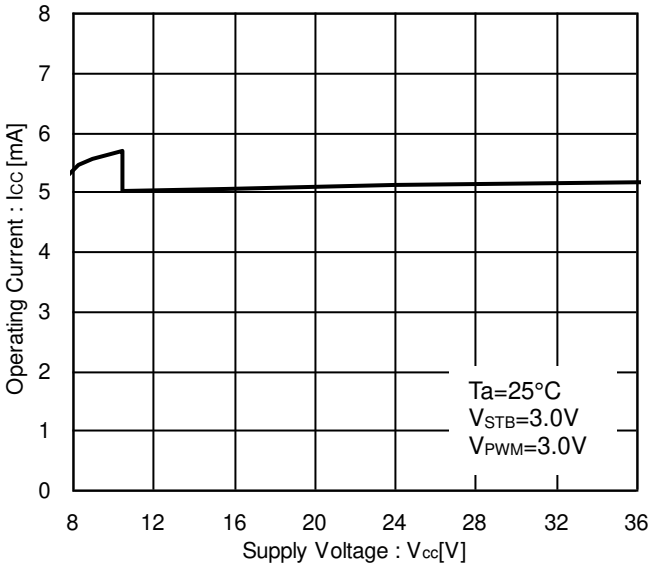


Figure 5. Operating Circuit Current vs Input Voltage

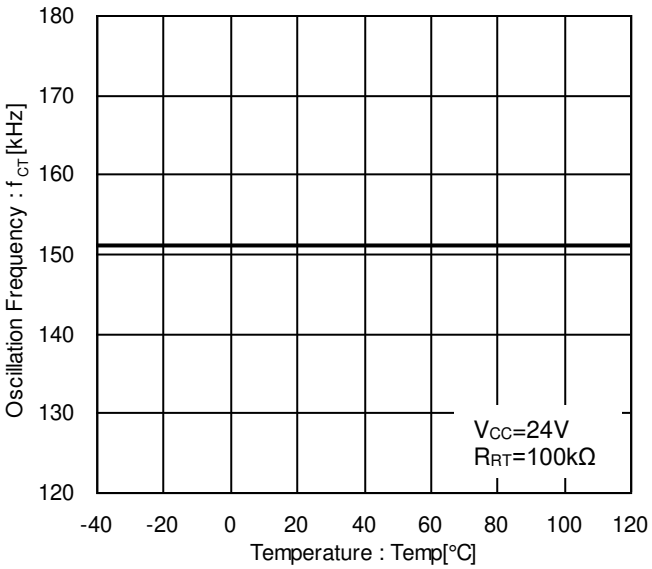


Figure 6. Oscillation Frequency vs Temperature

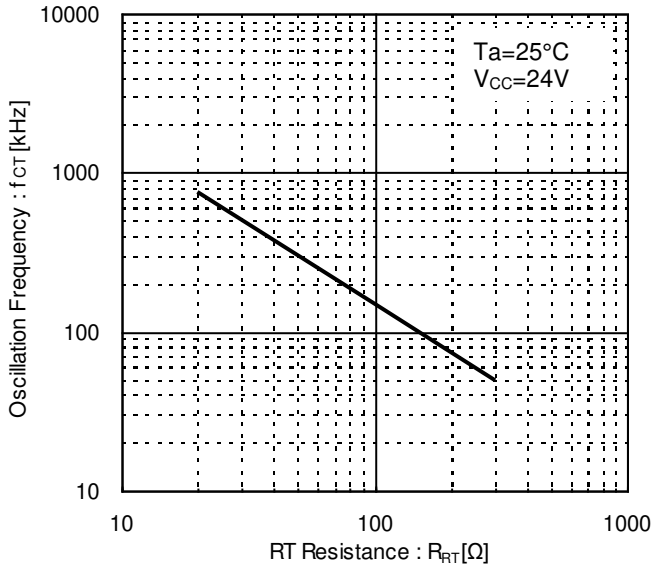


Figure 7. Oscillation Frequency vs RT Resistance

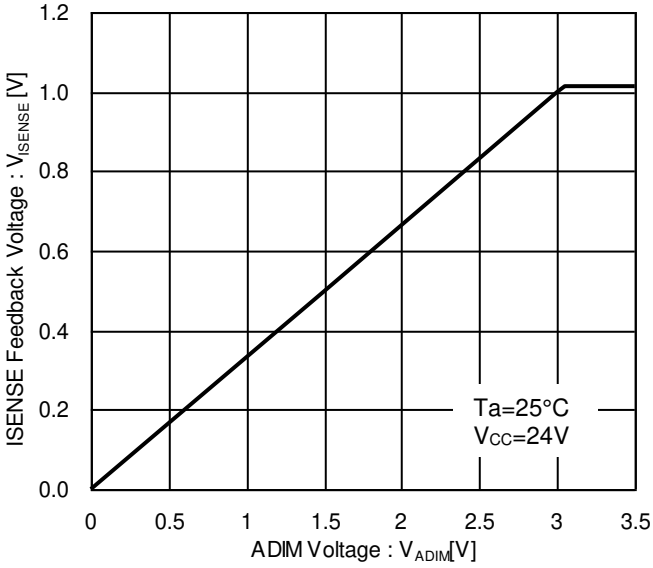


Figure 8. ISENSE Feedback Voltage vs ADIM Voltage

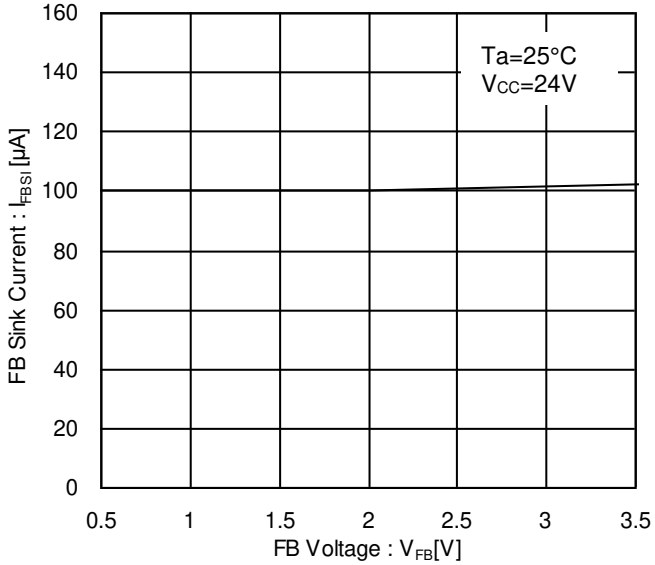


Figure 9. FB Sink Current vs FB Voltage

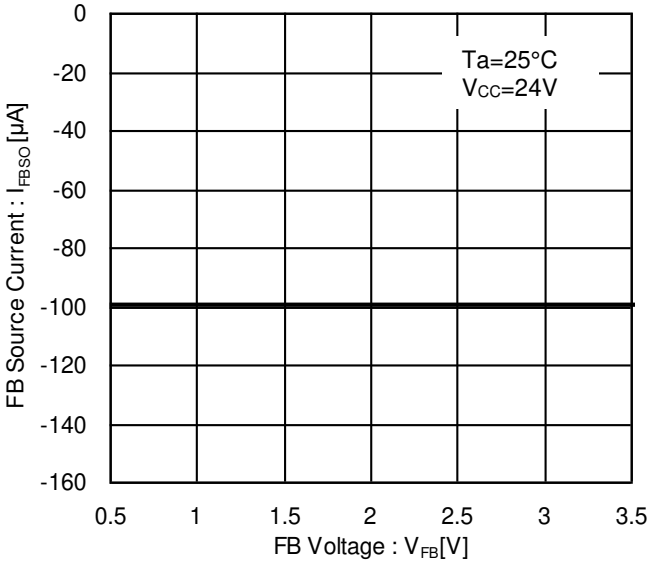


Figure 10. FB Source Current vs FB Voltage

2.2 Pin Descriptions

Pin 1: VCC

This is the power supply pin of the IC. Input range is from 9.0V to 35.0V.
The operation starts when the supply is greater than 7.5V(Typ) and shuts down when the supply is less than 7.2V(Typ).

Pin 2: STB

This is the ON/OFF setting terminal of the IC. This pin is available for reset at shut down. Input reset-signal to this terminal to reset IC from latch-off. At startup, internal bias starts at high level, and then DCDC boost starts after PWM rising edge is detected.
Note: IC status (IC ON/OFF) changes depending on the voltage applied to STB terminal. Avoid the use of intermediate level (from 0.8V to 2.0V).

Pin 3: CS1 , Pin 22: CS2

The CS pins have two functions.

1. DC / DC current mode Feedback terminal

The inductor current is converted to the CS pin voltage by the sense resistor R_{CS}. This voltage compared to the voltage set by error amplifier controls the output pulse.

2. Inductor current limit (OCP) terminal

The CS terminal also has an over current protection (OCP). If the voltage is more than 0.4V(Typ), the switching operation will be immediately stopped. And the next boost pulse will be restarted to normal frequency.
In addition, when the CS voltage is more than 1.0V(Typ) during four GATE clocks, IC will be latched off. Above OCP operation, if the current continues to flow even when GATE=L because of the destruction of the boost MOS, IC will stop operation completely.

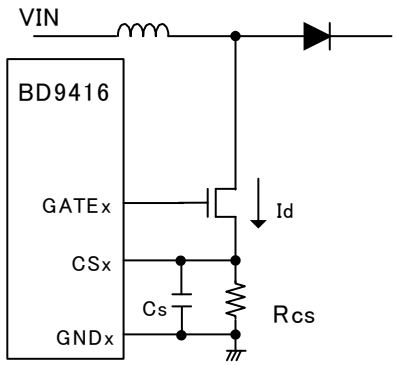


Figure 11. CS terminal circuit example

Both of the above functions are enabled after 300ns(Typ) when GATE pin asserts high, because the Leading Edge Blanking function (LEB) is included into this IC to prevent the effect of noise.
Please refer to section “3.3.1 Calculation Method for the Current Rating of DCDC Parts”, for detailed explanation.
If the capacitance Cs on the figure to the right is increased to a value in the micro order, please be careful that the limited value of NMOS drain current Id is more than the simple calculation. Because the current Id flows not only through Rcs but also through Cs, the CS pin voltage moves according to Id.

Pin 4: GATE1 , Pin 21: GATE2

These are the output terminals for driving the gate of the boost MOSFET. The high level is REG90. Frequency can be set by the resistor connected to RT. Refer to <RT> pin description for the frequency setting.
The phase lag of GATE1 and GATE2 is shown in Figure below. This Figure illustrates the waveform as both GATE pin output the maximum duty. The inrush current of the VIN terminal can be suppressed because each channel turns on alternately.

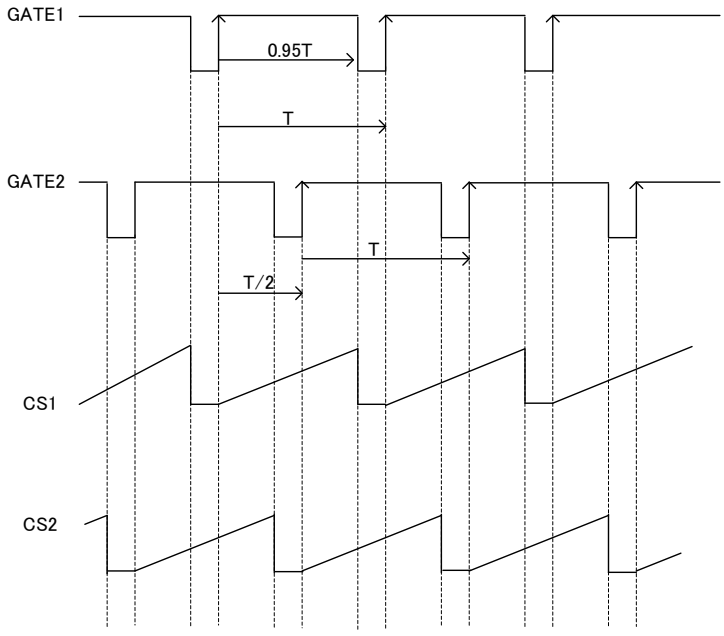


Figure 12. GATE timing chart

Pin 5: GND1 , Pin 20: GND2

These are the GND pins of the IC.

Pin 6: DIMOUT1 , Pin 19: DIMOUT2

These are the output pins for external dimming NMOS. The table below shows the rough output logic of each operation state, and the output H level is REG90. Please refer to “3.5 Timing Chart” for detailed explanations, because DIMOUT logic has an exceptional behavior. Please insert the resistor R_{DIM} between the dimming MOS gate to improve the over shoot of LED current, as PWM turns from low to high.

Status	DIMOUT output
Normal	Same logic to PWM
Abnormal	GND Level

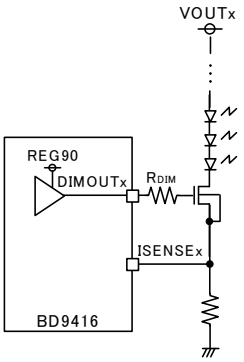


Figure 13. DIMOUT terminal circuit example

Pin 7: ISENSE1 , Pin 18: ISENSE2

These are the input pins for the current detection. The error amplifier compares with the lower voltage between 1/3 of the analog modulated light pin ADIM and 1.015V(Typ). It also detects abnormal LED over current ISENSE=3.0V(Typ). If GATE pin continues during four CLKs (equivalent to 40µs at fosc = 100kHz), the latch turns off. (Please refer to section “3.5.7 Timing Chart”.)

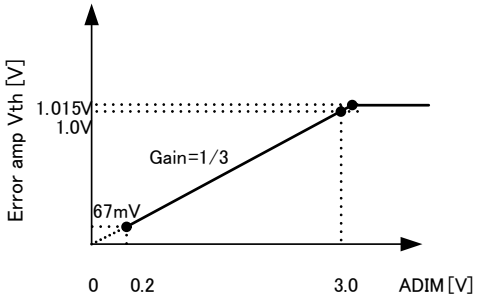


Figure 14. Relationship of the feedback voltage and ADIM

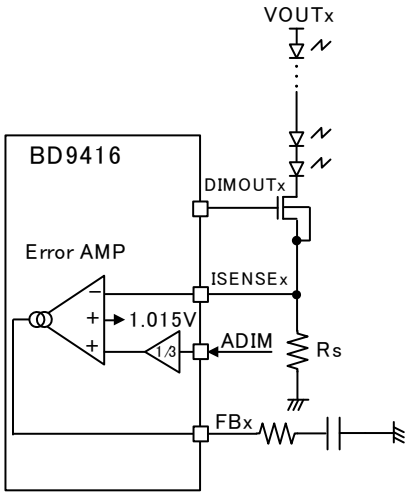


Figure 15. ISENSE terminal circuit example

Pin 8: FB1 , Pin 17: FB2

These are the output pins of error amplifier.
FB pin rises with the same slope as the SS pin during the soft-start period.
After soft -start completion (V_{SS}>3.7V(Typ)), it operates as follows.

When PWM=H, it detects ISENSE terminal voltage and outputs error signal compared to analog dimming signal (ADIM).
When PWM=L, IC holds the voltage at the edge of PWM=H to L, and operates to hold the adjacent voltage.
It detects over boost (FBMAX) over V_{FB}=4.0V(Typ). After the SS completion, if V_{FB}>4.0V and PWM=H continues after 4clk GATE, the CP counter starts. After that, only the V_{FB}>4.0V is monitored. When CP counter reaches 16384clk (2^{14}clk), IC will be latched off. (Please refer to section “3.5.6 Timing Chart”.)

The loop compensation setting is described in section "3.4 Loop Compensation".

Pin 9: ADIM

This is the input pin for analog dimming signal. The ISENSE feedback point is set as 1/3 of this pin bias. If V_{ADIM} is supplied more than 3.0V(Typ), ISENSE feedback voltage is clamped to limit the flow of LED large current. In this condition, the input current is generated. Please refer to <ISENSE> terminal explanation.

Pin 10: PWM1 , Pin 11: PWM2

These are the PWM dimming signal input pins. The high / low level of PWM pins are the following.

State	PWM input voltage
PWM=H	V_{PWM}=1.5V to 18.0V
PWM=L	V_{PWM}=−0.3V to +0.8V

Pin 12: FAILB

This is fail signal output (OPEN DRAIN) pin. At normal operation, NMOS will be in the OPEN state, during abnormality detection NMOS will be in the ON (500Ω(Typ)) state.

Pin 13: DUTYON

This is the ON/OFF setting terminal of the LED PWM Over Duty Protection (ODP). By adjusting DUTYON input voltage, the ON/OFF state of the ODP is changed.

State	DUTYON input voltage
ODP=ON	V_{DUTYON}=-0.3V to +0.8V
ODP=OFF	V_{DUTYON}=1.5V to 18.0V

Pin 14: DUTYP

This is the pin that sets the ODP. The ODP (Over Duty Protection) is the function to limit DUTY of LED PWM frequency f_{PWM} by ODP detection Duty (ODP_{duty}) set by resistance (R_{DUTY}) connected to DUTYP pin.

○Relationship between LED PWM frequency f_{PWM}, ODP Detection Duty ODP_{duty} and DUTYP resistance (ideal)

$$R_{DUTYP}=\frac{1172\times ODP_{duty}[\%]}{f_{PWM}[Hz]} \quad [k\Omega]$$

The R_{DUTYP} setting ranges from 15kΩ to 500kΩ.
The setting example is separately described in the section "3.2.5 ODP Setting".

Pin 15: RT

This is the pin that sets the DC/DC switching frequency. DCDC frequency is decided by connected RT resistor.

○The relationship between the frequency and RT resistance value **(ideal)**

$$R_{RT}=\frac{15000}{f_{SW}[kHz]} \quad [k\Omega]$$

The oscillation setting ranges from 50kHz to 1000kHz.
The setting example is separately described in the section "3.2.4 DCDC Oscillation Frequency Setting".

Pin 16: SS

This is the pin which sets the soft start interval of DC/DC converter. It performs the constant current charge of 3.0μA(Typ) to external capacitance Css. The switching duty of GATE output will be limited during 0V to 3.7V(Typ) of the SS voltage. So the soft start interval Tss can be expressed as follows

$$T_{SS}=1.23\times 10^{6}\times C_{SS} \quad [s]$$ Css: the external capacitance of the SS pin.

SS pin becomes L because it never became PWM=H after the latch turns OFF or reset is canceled. When SS capacitance is under 1nF, please note if the in-rush current during startup is too large, or if over boost detection (FBMAX) mask timing is too short.
Please refer to soft start behavior in the section "3.5.4 Timing Chart ".

Pin 23: OVP

The OVP terminal is the input for over-voltage protection. If OVP is more than 3.0V(Typ), the over-voltage protection (OVP) will work. At the moment of these detections, it sets GATE=L, DIMOUT=L and starts to count up the abnormal interval. If OVP detection continued to count four GATE clocks, IC reaches latch off. (Please refer to "3.5.5 Timing Chart")
The OVP pin is high impedance, because the internal resistance is not connected to a certain bias.
Even if OVP function is not used, pin bias is still required because the open connection of this pin is not a fixed potential.
The setting example is separately described in the section "3.2.6 OVP Setting".

Pin 24: REG90

This is the 9.0V(Typ) output pin. Available current is 15mA (Min).
Please place the ceramic capacitor connected to REG90 pin (1.0μF to 10μF) closest to REG90-GND pin.

2.3 List of The Protection Function Detection Condition (Typ Condition)

Protect function	Detection pin	Detect condition			Release condition	Timer operation	Protection type
		Detection condition	PWM	SS			
FBMAX	FB	V_{FB}>4.0V	H(4clk)	V_{SS}>3.7V	V_{FB}<4.0V	2^{14}clk	Immediately auto-restart after detection (Judge periodically whether normal or not)
LED OCP	ISENSE	V_{ISENSE}>3.0V	-	-	V_{ISENSE}<3.0V	4clk	Immediately auto-restart after detection (Judge periodically whether normal or not)
RT GND SHORT	RT	V_{RT}<V_{RTN}×90% *(Note 6)*	-	-	V_{RT}>V_{RTN}×90% *(Note 6)*	No	Restart by release
RT HIGH SHORT	RT	V_{RT}>5V	-	-	V_{RT}<5V	No	Restart by release
REG90UVO	REG90	V_{REG90}<6.0V	-	-	V_{REG90}>6.5V	No	Restart by release
VCC UVLO	VCC	V_{CC}<7.2V	-	-	V_{CC}>7.5V	No	Restart by release
OVP	OVP	V_{OVP}>3.0V	-	-	V_{OVP}<2.8V	4clk	Immediately auto-restart after detection (Judge periodically whether normal or not)
OCP	CS	V_{CS}>0.4V	-	-	-	No	Pulse by Pulse
OCP LATCH	CS	V_{CS}>1.0V	-	-	V_{CS}<1.0V	4clk	Immediately auto-restart after detection (Judge periodically whether normal or not)
DUTYP GND SHORT	DUTYP	V_{DUTYP} <V_{DUTYPN}×90% *(Note 7)*	-	-	V_{DUTYP} >V_{DUTYPN}×90% *(Note 7)*	No	Restart by release
DUTYP HIGH SHORT	DUTYP	V_{DUTYP}>5V	-	-	V_{DUTYP}<5V	No	Restart by release
ODP *(Note 8)*	PWM	DUTYON=H and PWM_{duty}>ODP_{duty} *(Note 9)*	H	-	-	No	Cycle by Cycle

The clock number of timer operation corresponds to the boost pulse clock.
(Note 6) V_{RTN} is the RT voltage at normal operation.
(Note 7) V_{DUTYPN} is the DUTYP voltage at normal operation.
(Note 8) About ODP, when PWM is inputted from low to high, PWM Duty count start and when PWM is inputted from high to low, the counter is reset. When PWM duty is set to 100%,after ODP works once, the GATE and DIMOUT outputs maintain low till PWM is inputted from high to low.
(Note 9) PWM_{duty} is the Duty of PWM signal into PWM terminal and ODP_{duty} is the Duty decided by the resister connecting to DUTY terminal.

2.4 List of The Protection Function Operation

Protect function	Operation of the protect function			
	DC/DC gate output	Dimming transistor (DIMOUT) logic	SS pin	FAILB pin
FBMAX	Stop after timer latch	Low after timer latch	Discharge after timer latch	Low after timer latch
LED OCP	Stop immediately	Immediately high, Low after timer latch	Discharge after timer latch	Low after timer latch
RT GND SHORT	Stop immediately	Immediately low	Not discharge	-
RT HIGH SHORT	Stop immediately	Immediately low	Not discharge	-
STB	Stop immediately	Low after REG90UVLO detects	Discharge immediately	High
REG90UVLO	Stop immediately	Immediately low	Discharge immediately	High
VCC UVLO	Stop immediately	Immediately low	Discharge immediately	High
OVP	Stop immediately	Immediately low	Discharge after timer latch	Low after timer latch
OCP	Stop immediately	Normal operation	Not discharge	-
OCP LATCH	Stop immediately *(Note10)*	Low after timer latch	Discharge after timer latch	Low after timer latch
DUTYP GND SHORT	Stop immediately	Immediately low	Not discharge	-
DUTYP HIGH SHORT	Stop immediately	Immediately low	Not discharge	-
ODP	Stop immediately	Immediately low	Not discharge	-

Please refer to section “3.5 Timing Chart” for details.
(Note 10) Stop immediately due to detecting OCP before OCP_LATCH

3.1 Application Circuit Example

Introduce an example application using the BD9416FS.

3.1.1 Basic Application Example

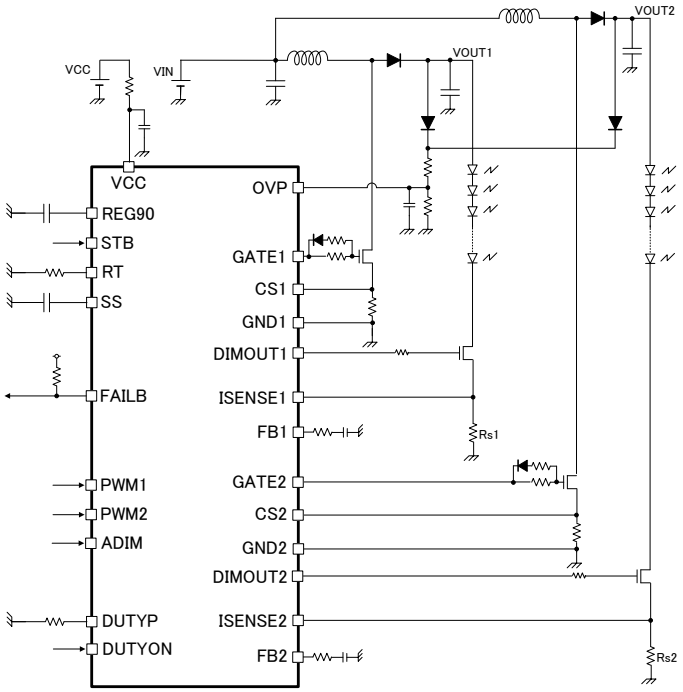


Figure 16. Basic application example

3.1.2 Only Used 1ch Example

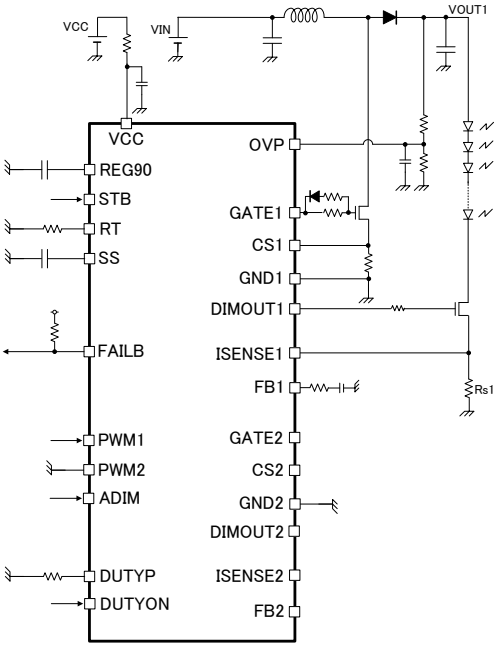


Figure 17. Example circuit for only used 1ch

3.1.3 Analog Dimming or PWM Dimming Examples

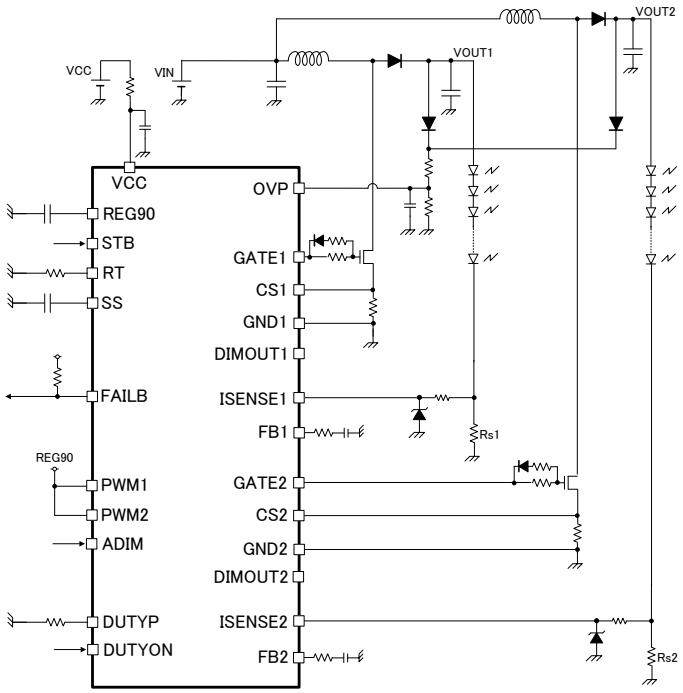


Figure 18. Example circuit for analog dimming

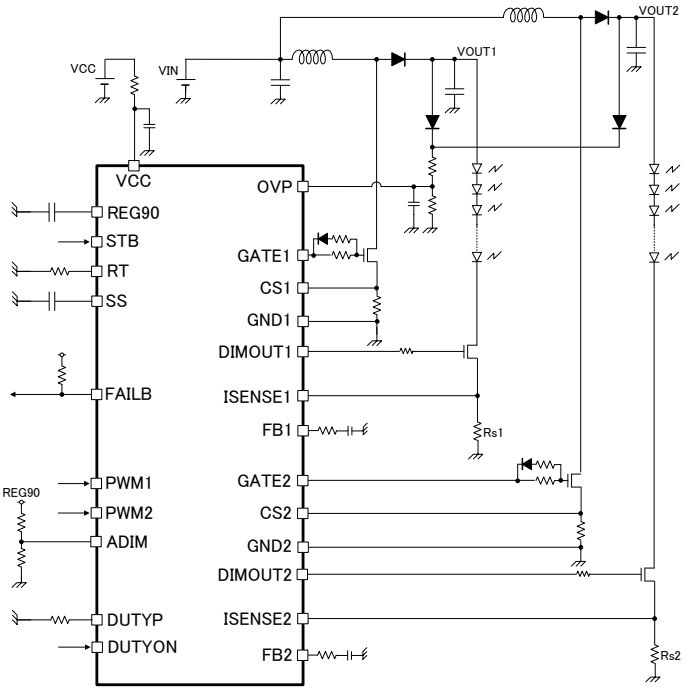


Figure 19. Example circuit for PWM dimming

3.2 External Components Selection

3.2.1 Start Up Operation and Soft Start External Capacitance Setting

The below explanation is the start up sequence of this IC

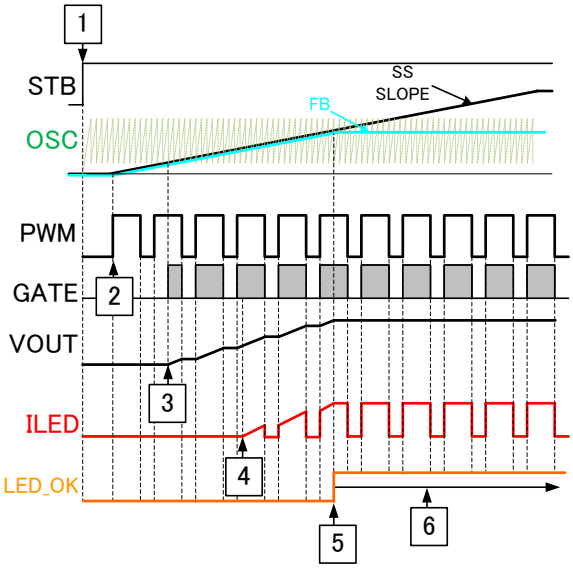


Figure 20. Startup waveform

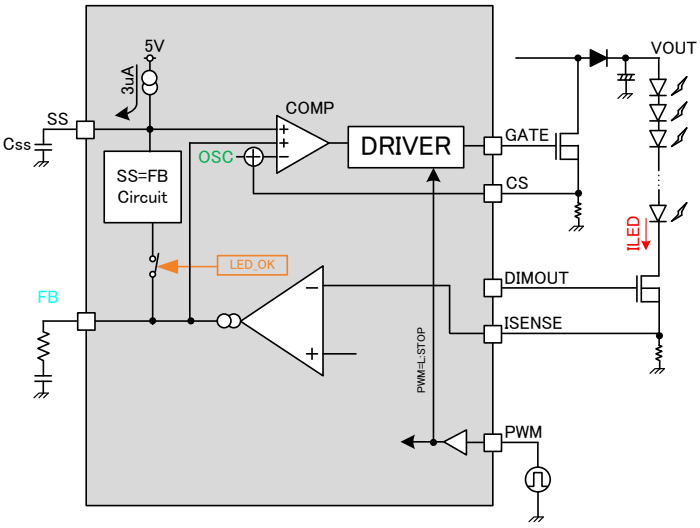


Figure 21. Circuit behavior at startup

○Explanation of start up sequence

1. Reference voltage REG90 starts by STB=H.
2. SS starts to charge at the time of first PWM=H. At this moment, the SS voltage of slow-start starts to equal FB voltage,and the circuit becomes V_{FB}=V_{SS} regardless of PWM logic.
3. When V_{FB}=V_{SS} reaches the lower point of internal sawtooth waveform, GATE terminal outputs pulse and starts to boost VOUT.
4. VOUT is increased and VOUT reaches the voltage to be able to flow LED current.
5. If LED current flows over the set level, FB=SS circuit disconnects and startup behavior completes.
6. Then it continues normal operation by feedback of ISENSE terminal. If LED current doesn't flow when V_{SS} becomes over 3.7V(Typ), SS=FB circuit completes immediately and FBMAX protection starts.

○Method of setting SS external capacitance

According to the sequence described above, start time when completed at V_{FB}=V_{SS} can be thought of as the time until FB voltage reaches the feedback point from STB=ON.
The capacitance of SS terminal is defined as Css and the feedback voltage of FB terminal is defined as V_{FB}. The equation relating Css and V_{FB} to T_{SS} is as follows.

$$T_{SS} = \frac{C_{SS}[\mu F] \times V_{FB}[V]}{3[\mu A]} \quad [s]$$

If Css is set to a very small value, rush current flows into the inductor at startup.
On the contrary, if Css is increased too much, LED will light up gradually.
The constant to set varies depending on characteristics required by Css and also differs by factors, such as voltage rise ratio, output capacitance, DCDC frequency, and LED current. Please confirm with the system.

【Setting example】

When Css=0.1μF, Iss=3μA, and startup completes at V_{FB} =3.7V, SS setting time is as follows.

$$T_{SS} = \frac{0.1 \times 10^{-6}[F] \times 3.7[V]}{3 \times 10^{-6}[A]} = 0.123[s]$$

3.2.2 VCC Series Resistance Setting

Here are the following effects of inserting series resistor Rvcc into VCC line.
(i) It is possible to suppress the heat generation of the IC, when the voltage VCC is reduced.
(ii) It can limit the inflow current to VCC line.
However, if resistance Rvcc is set to a large value, VCC voltage is reduced below minimum operation voltage (V_{CC}<9V). Rvcc must be set to an appropriate series resistance.

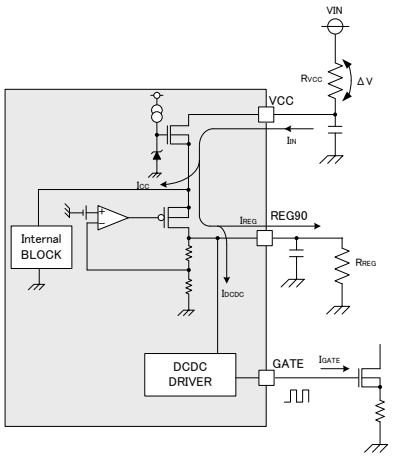


Figure 22. VCC series resistance circuit example

IC's inflow current line I_{IN} has the following inflow lines.
・IC's circuit current⋯I_{CC}
・Current of R_{REG} connected to REG90⋯I_{REG}
・Current to drive FET's Gate⋯I_{GATE}
These decide the voltage ΔV at R_{VCC}.
VCC terminal voltage at that time can be expressed as follows.

$$V_{CC}[V] = V_{IN}[V] - (I_{CC}[A] + I_{DCDC}[A] + I_{REG}[A]) \times R_{VCC}[\Omega] > 9[V]$$

Here, judgement is the 9V minimum operation voltage.
Please consider a sufficient margin when setting the series resistor of VCC.

【setting example】
Above equation is translated as follows.

$$R_{VCC}[\Omega] < \frac{V_{IN}[V] - 9[V]}{I_{CC}[A] + I_{DCDC}[A] + I_{REG}[A]}$$

When V_{IN}=24V, I_{CC}=2.0mA, R_{REG}=10kΩ and I_{DCDC}=2mA, R_{VCC}'s value is calculated as follows.

$$R_{VCC}[\Omega] < \frac{24[V] - 9[V]}{0.0051[A] + 0.002[A] + 9.0[V]/10000[\Omega]} = 1.88[k\Omega]$$

(I_{CC} is 5.1mA(Typ)) . Please set each values with tolerance and margin.

3.2.3 LED current setting

LED current can be adjusted by setting the resistance R_S [Ω] which connects to ISENSE pin and V_{ADIM} [V].

Relationship between R_S and I_{LED} current

With DC dimming (V_{ADIM}<3.0V)

$$R_S[\Omega] = \frac{1}{3}\frac{V_{ADIM}[V]}{I_{LED}[A]}[\Omega]$$

Without DC dimming (V_{ADIM}>3.0V)

$$R_S[\Omega] = \frac{1.015[V]}{I_{LED}[A]}[\Omega]$$

【setting example】
If I_{LED} current is 200mA and V_{ADIM} is 2.0V, we can calculate R_S as below.

$$R_S[\Omega] = \frac{1}{3}\frac{V_{ADIM}[V]}{I_{LED}[A]} = \frac{1}{3}\frac{2.0[V]}{0.2[A]} = 3.33[\Omega]$$

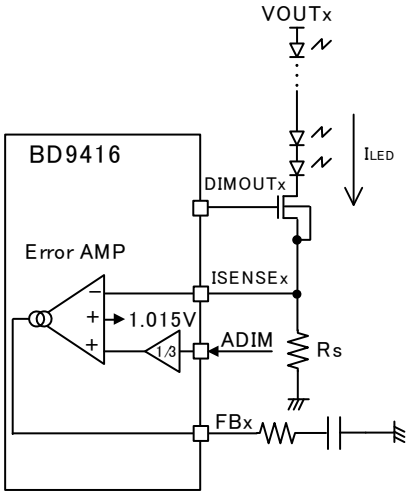


Figure 23. LED current setting example

3.2.4 DCDC Oscillation Frequency Setting

R_{RT} which connects to RT pin sets the oscillation frequency f_{SW} of DCDC.

○Relationship between frequency f_{SW} and RT resistance (ideal)

$$R_{RT} = \frac{15000}{f_{SW}[kHz]} \quad [k\Omega]$$

【setting example】

When DCDC frequency fsw is set to 200kHz, R_{RT} is as follows.

$$R_{RT} = \frac{15000}{f_{SW}[kHz]} = \frac{15000}{200[kHz]} = 75[k\Omega]$$

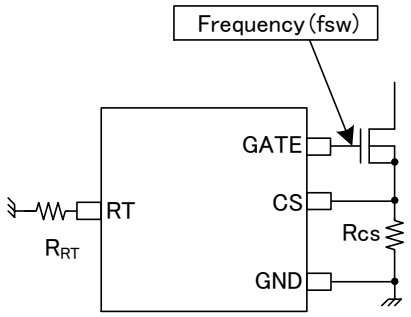


Figure 24. RT terminal setting example

3.2.5 ODP Setting

R_{DUTYP} which connects to ODP pin sets the ODP detection duty.

○Relationship between LED PWM frequency f_{PWM}, ODP Detection Duty and DUTYP resistance (ideal)

$$R_{DUTYP} = \frac{1172 \times ODP_{duty}[\%]}{f_{PWM}[Hz]} \quad [k\Omega]$$

【setting example】

When LED PWM frequency f_{PWM} is set to 120Hz and ODP Detection Duty (ODP_{duty}) is set to 35%, R_{DUTYP} is as follows.

$$R_{DUTYP} = \frac{1172 \times 35[\%]}{120[Hz]} = 341.8[k\Omega]$$

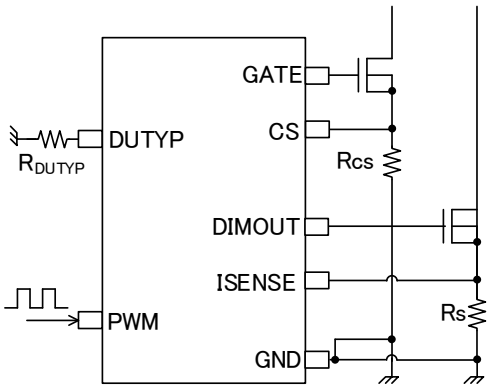


Figure 25. ODP setting example

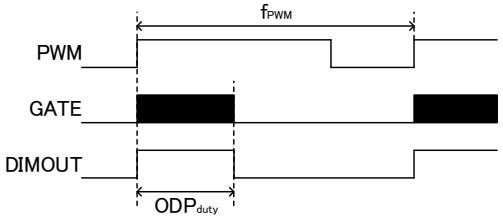


Figure 26. The GATE and the DIMOUT waveform as PWM dimming (ODP)

3.2.6 OVP Setting

The OVP terminal is the input for over-voltage protection of the output voltage.

The OVP pin is in high impedance state, because the internal resistance is not connected to a certain bias.

Detection voltage of VOUT is set by dividing resistors R1 and R2. The resistor values can be calculated by the formula below.

○OVP detection equation

If VOUT is boosted abnormally, V_{OVPDET} is the detect voltage of OVP, R1, R2 can be expressed by the following formula.

$$R1 = R2[k\Omega] \times \frac{V_{OVPDET}[V] - 3.0[V]}{3.0[V]} [k\Omega]$$

○OVP release equation

By using R1 and R2 in the above equation, the release voltage of OVP, V_{OVPCAN} can be expressed as follows.

$$V_{OVPCAN} = 2.8[V] \times \frac{R1[k\Omega] + R2[k\Omega]}{R2[k\Omega]} [V]$$

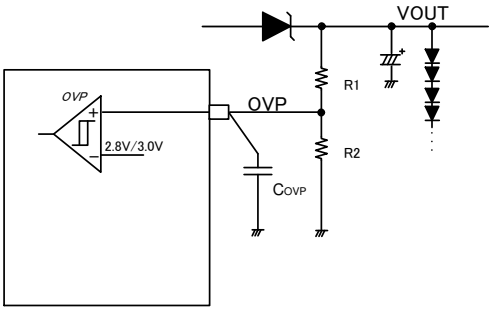


Figure 27. OVP setting example

【setting example】
If the normal output voltage, VOUT is 40V, the detect voltage of OVP is 48V, R2 is 10kΩ, R1 is calculated as follows.

$$R1 = R2[k\Omega] \times \frac{V_{OVPDET}[V] - 3.0[V]}{3.0[V]} = 10[k\Omega] \times \frac{48[V] - 3[V]}{3[V]} = 150[k\Omega]$$

By using these R1 and R2, the release voltage of OVP, V_{OVPCAN} can be calculated as follows.

$$V_{OVPCAN} = 2.8[V] \times \frac{R1[k\Omega] + R2[k\Omega]}{R2[k\Omega]} = 2.8[V] \times \frac{10[k\Omega] + 150[k\Omega]}{10[k\Omega]} = 44.8[V]$$

3.2.7 Timer Latch Time Setting, Auto-Restart Timer Setting

About over boost protection (FBMAX), timer latch time is set by counting the clock frequency which is set at the RT pin. About the behavior from abnormal detection to latch-off, please refer to the section “3.5.6 Timing Chart”.

If the condition V_{FB} >4.0V(Typ) and PWM=H continues for more than four GATE clocks, it is counted as unusual. After that, only the FB voltage is monitored and latch occurs after the time below has passed.

$$LATCH_{TIME} = 2^{14} \times \frac{R_{RT}}{1.5 \times 10^{10}} = 16384 \times \frac{R_{RT}[k\Omega]}{1.5 \times 10^{7}}[s]$$

And Auto-Restart Time after latch off can be expressed by the following formula.

$$AUTO_{TIME} = 2^{17} \times \frac{R_{RT}}{1.5 \times 10^{10}} = 131072 \times \frac{R_{RT}[k\Omega]}{1.5 \times 10^{7}}[s]$$

Here, $LATCH_{TIME}$ = time until latch condition occurs, $AUTO_{TIME}$ = auto restart timer’s time
R_{RT} = Resistor value connected to RT pin

【setting example】
Timer latch time when RT=100kΩ

$$LATCH_{TIME} = 16384 \times \frac{R_{RT}[k\Omega]}{1.5 \times 10^{7}} = 16384 \times \frac{100[k\Omega]}{1.5 \times 10^{7}} = 109.2[ms]$$

$$AUTO_{TIME} = 131072 \times \frac{R_{RT}[k\Omega]}{1.5 \times 10^{7}} = 131072 \times \frac{100[k\Omega]}{1.5 \times 10^{7}} = 873.8[ms]$$

3.3 DCDC Parts Selection

3.3.1. OCP Setting / Calculation Method for the Current Rating of DCDC Parts

OCP detection stops the switching when the CS pin voltage is more than 0.4V(Typ). The resistor value of CS pin, R_{CS} needs to be considered after calculating the peak current in coil L. In addition, the current rating of DCDC external parts should be greater than the peak current of the coil.
Shown below are the calculation method of the coil peak current, the selection method of Rcs (the resistor value of CS pin) and the current rating of the external DCDC parts at Continuous Current Mode.

(the calculation method of the coil peak current, Ipeak at Continuous Current Mode)

At first, since the ripple voltage at CS pin depends on the application condition of DCDC, the following variables are used.
Vout voltage= V_{OUT} [V]
LED total current= I_{OUT} [A]
DCDC input voltage of the power stage = V_{IN} [V]
Efficiency of DCDC =η[%]
And then, the average input current I_{IN} is calculated by the following equation.

$$I_{IN} = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]}[A]$$

And the ripple current of the inductor L (ΔIL[A]) can be calculated by using DCDC the switching frequency, fsw, as follows.

$$\Delta IL = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]}[A]$$

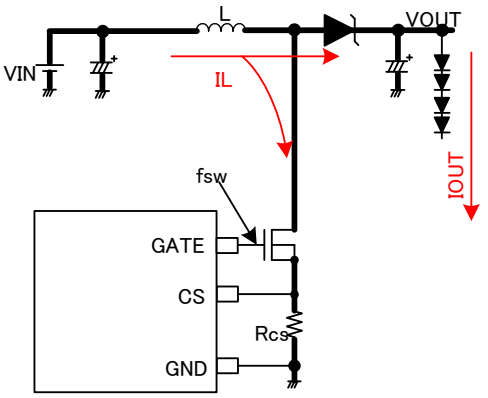


Figure 28. Circuit Structure of DCDC parts

On the other hand, the peak current of the inductor Ipeak can be expressed as follows.

$$Ipeak = I_{IN}[A] + \frac{\Delta IL[A]}{2}[A] \quad \cdots (1)$$

Therefore, the bottom of the ripple current I_{Min} is

$$I_{Min} = I_{IN}[A] - \frac{\Delta IL[A]}{2} \quad or \quad 0$$

If I_{Min} >0, the operation mode is CCM (Continuous Current Mode), otherwise the mode is DCM (Discontinuous Current Mode).

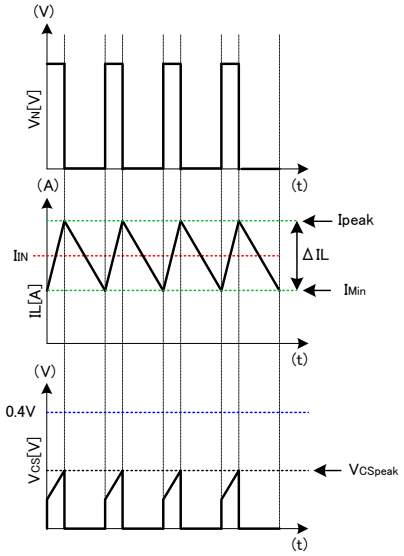


Figure 29. Coil current waveform

(the selection method of Rcs at Continuous Current Mode)

Ipeak flows into Rcs and that causes the voltage signal to CS pin. (Please refer to the timing chart at the right)
Peak voltage $V_{CSpeak}$is as follows.

$$V_{CSpeak} = R_{CS} \times I_{peak}[V]$$

As this V_{CSpeak} reaches 0.4V(Typ), the DCDC output stops switching.
Therefore, Rcs value is necessary to meet the condition below.

$$R_{CS} \times I_{peak}[V] << 0.4[V]$$

(the current rating of the external DCDC parts)

The peak current as the CS voltage reaches OCP level (0.4V (Typ)) is defined as I_{peak_det}

$$I_{peak\_det} = \frac{0.4[V]}{R_{CS}[\Omega]}[A] \quad \cdots (2)$$

The relationship among I_{peak} (equation (1)), I_{peak_det} (equation (2)) and the current rating of parts is required to meet the following

I_{peak} << I_{peak_det} << The current rating of parts

Please make the selection of the external parts such as FET, Inductor, diode meet the above condition.

[setting example]
Output voltage = V_{OUT} [V] = 40V
LED total current = I_{OUT} [A] = 0.48A
DCDC input voltage of the power stage = V_{IN} [V] = 24V
Efficiency of DCDC =η[%] = 90%
Averaged input current I_{IN} is calculated as follows.

$$I_{IN}[A] = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]} = \frac{40[V] \times 0.48[A]}{24[V] \times 90[\%]} = 0.89[A]$$

If the switching frequency, f_{SW} = 200kHz, and the inductor, L=100μH, the ripple current of the inductor L (ΔIL[A]) can be calculated as follows.

$$\Delta IL = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]} = \frac{(40[V] - 24[V]) \times 24[V]}{100 \times 10^{-6}[H] \times 40[V] \times 200 \times 10^{3}[Hz]} = 0.48[A]$$

Therefore the inductor peak current, Ipeak is

$$\boxed{I_{peak} = I_{IN}[A] + \frac{\Delta IL[A]}{2}[A] = 0.89[A] + \frac{0.48[A]}{2} = 1.13[A]}$$ …calculation result of the peak current

If Rcs is assumed to be 0.3Ω

$$\boxed{V_{CSpeak} = R_{CS} \times I_{peak} = 0.3[\Omega] \times 1.13[A] = 0.339[V] << 0.4V}$$ …Rcs value confirmation

The above condition is met.
And I_{peak_det}, the current OCP works, is

$$I_{peak\_det} = \frac{0.4[V]}{0.3[\Omega]} = 1.33[A]$$

If the current rating of the used parts is below 2A,

$I_{peak} << I_{peak\_det} <<$ The current rating $\boxed{= 1.13[A] << 1.33[A] << 2.0[A]}$ …current rating confirmation of DCDC parts

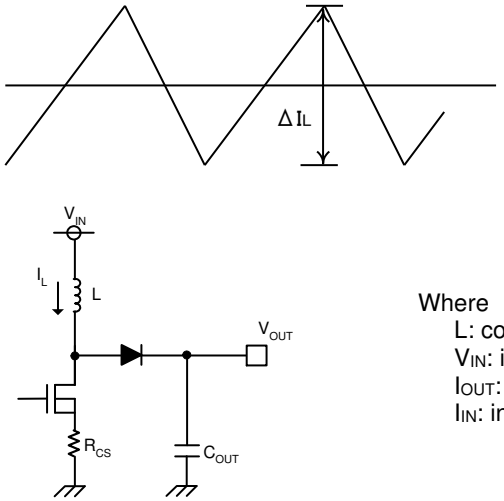
This inequality meets the above relationship. The parts selection is proper.
And I_{MIN}, the bottom of the IL ripple current, can be calculated as follows.

$$I_{Min} = I_{IN}[A] - \frac{\Delta IL[A]}{2}[A] = 1.13[A] - 0.48[A] = 0.65[A] >> 0$$

This inequality implies that the operation is continuous current mode.

3.3.2. Inductor Selection

The inductor value affects the input ripple current, as shown the previous section 3.3.1.



$$\Delta IL = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]}[A]$$

$$I_{IN}[A] = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]}[A]$$

$$I_{peak} = I_{IN}[A] + \frac{\Delta IL[A]}{2}[A]$$

Where

L: coil inductance [H] V_{OUT}: DCDC output voltage [V]
V_{IN}: input voltage [V]
I_{OUT}: output load current (the summation of LED current) [A]
I_{IN}: input current [A] f_{SW}: oscillation frequency [Hz]

Figure 30. Inductor current waveform and diagram

In continuous current mode, ⊿IL is set to 30% to 50% of the output load current in many cases.
In using smaller inductor, the boost is operated in discontinuous current mode in which the coil current returns to zero at every period.

*The current exceeding the rated current value of inductor passing through the coil causes magnetic saturation, and this results in to a decrease in efficiency. Inductor needs to be selected to have adequate margin such that the peak current does not exceed the rated current value of the inductor.
*To reduce inductor loss and improve efficiency, inductor with low resistance components (DCR, ACR) needs to be selected

3.3.3. Output Capacitance Cout Selection

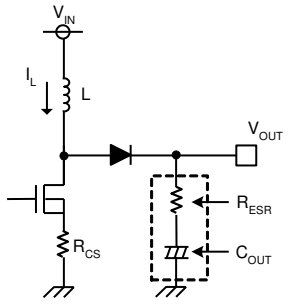


Figure 31. Output capacitor diagram

Output capacitor C_{OUT} needs to be selected in consideration of equivalent series resistance R_{ESR} required to smooth out the ripple voltage. Be aware that the required LED current may not be observed due to decrease in LED terminal voltage if the output ripple component is high.
Output ripple voltage ⊿V_{OUT} is determined by Equation (4):

$$\Delta V_{OUT} = \Delta IL \times R_{ESR}[V] \quad (3)$$

When the coil current is charged to the output capacitor as MOS turns off, a large output ripple is caused. Large ripple voltage of the output capacitor may cause the LED current ripple.

* Rating of capacitor needs to be selected to have adequate margin against output voltage.
*To use an electrolytic capacitor, adequate margin against allowable current is also necessary. Be aware that the LED current is larger than the set value momentarily especially in the case that LED is provided with PWM dimming.

3.3.4. Switching MOSFET Selection

There is no problem if the absolute maximum rating is larger than the rated current of the inductor L, or is larger than the sum of the tolerance voltage of C_{OUT} and the rectifying diode V_F. The product with small gate capacitance (injected charge) needs to be selected to achieve high-speed switching.

* One with over current protection setting or higher is recommended.
* The selection of one with small on resistance results in high efficiency.

3.3.5. Rectifying Diode Selection

A schottky barrier diode which has current ability higher than the rated current of L, reverse voltage larger than the tolerance voltage of C_{OUT}, and most importantly, low forward voltage V_F needs to be selected.

3.4 Loop Compensation

A current mode DCDC converter has one pole (phase lag) f_p due to CR filter composed of the output capacitor and the output resistance (= LED current) and one zero (phase lead) f_Z by the output capacitor and the ESR of the capacitor. Moreover, a step-up DCDC converter has RHP zero (right-half plane zero point) f_{ZRHP} which is unique with the boost converter. This zero may cause the unstable feedback. To avoid this by RHP zero, the loop compensation that the cross-over frequency f_c, set as follows, is suggested.

fc = f_{ZRHP} /5 (f_{ZRHP}: RHP zero frequency)

Considering the response speed, the calculated constant below is not always completely optimized. It needs to be adequately verified with an actual device.

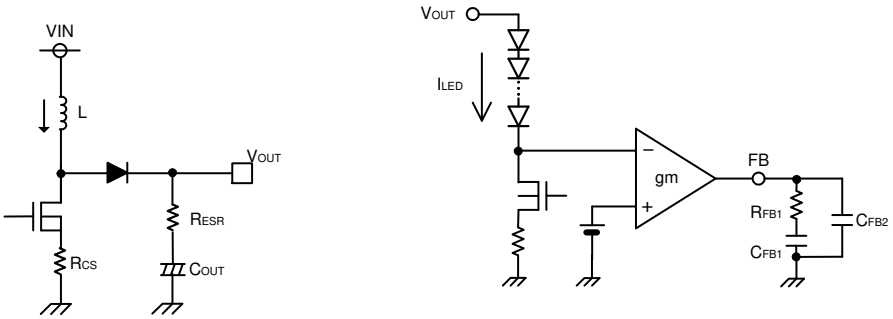


Figure 32. Output stage and error amplifier diagram

i. Calculate the pole frequency fp and the RHP zero frequency f_{ZRHP} of DC/DC converter

$$f_p = \frac{I_{LED}}{2\pi \times V_{OUT} \times C_{OUT}} [Hz] \qquad f_{ZRHP} = \frac{V_{OUT} \times (1-D)^2}{2\pi \times L \times I_{LED}} [Hz]$$

Where I_{LED} = the summation of LED current, $D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$ (Continuous Current Mode)

ii. Calculate the phase compensation of the error amp output (f_c = f_{ZRHP}/5)

$$R_{FB1} = \frac{f_{RHZP} \times R_{CS} \times I_{LED}}{5 \times f_p \times gm \times V_{OUT} \times (1-D)} [\Omega]$$

$$C_{FB1} = \frac{1}{2\pi \times R_{FB1} \times f_C} = \frac{5}{2\pi \times R_{FB1} \times f_{ZRHP}} [F]$$

$$gm = 4.0 \times 10^{-4} [S]$$

The above equation is described for lighting LED without the oscillation. The value may cause a large error if the quick response for the abrupt change of dimming signal is required.

To improve the transient response, R_{FB1} needs to be increased, and C_{FB1} needs to be decreased. It needs to be adequately verified with an actual device to consider part to part variation since phase margin could be decreased.

3.5 Timing Chart

3.5.1 PWM Start up 1 (Input PWM Signal After Input STB Signal)

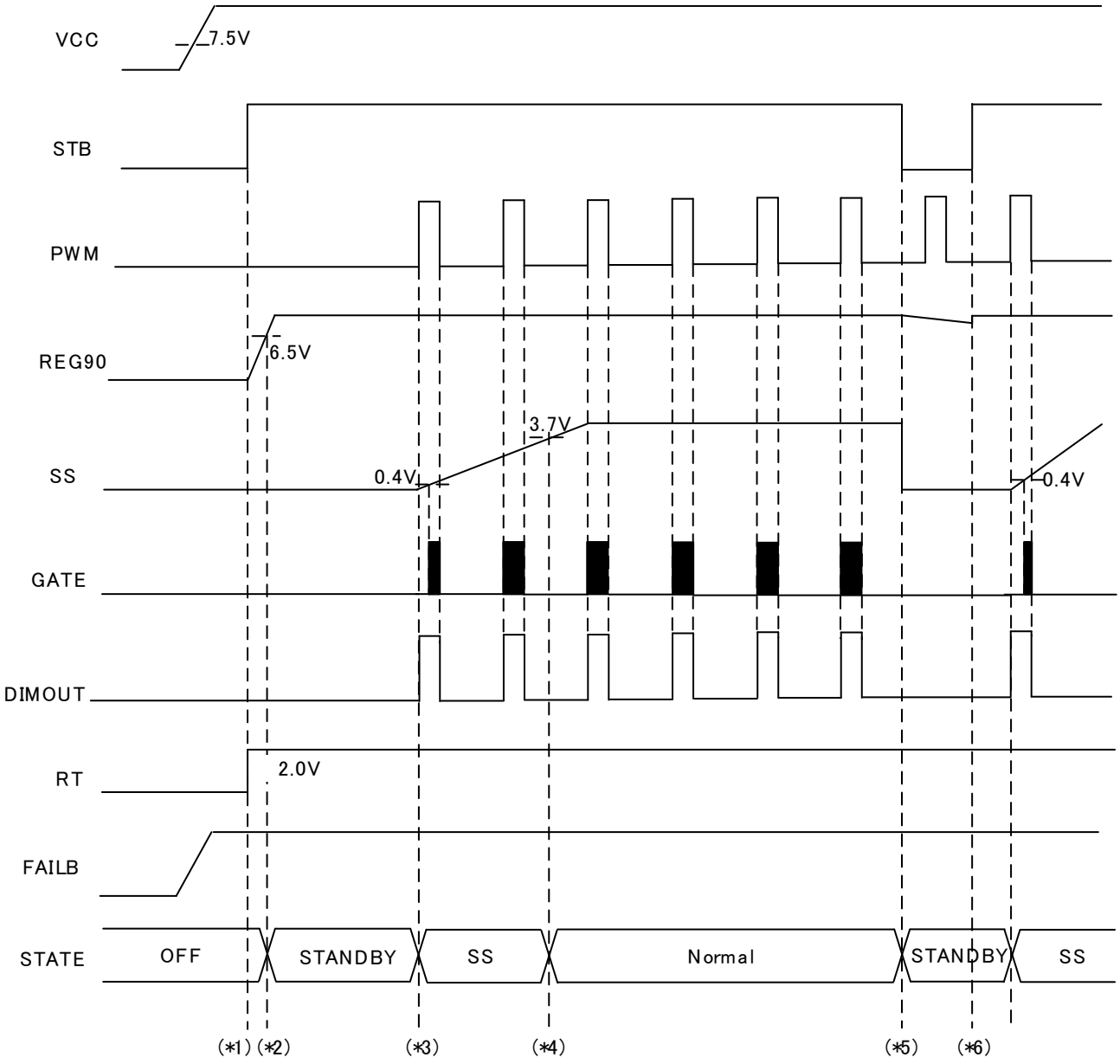


Figure 33. PWM Start Up 1 (Input PWM Signal After Input STB Signal)

(*1)…REG90 starts up when STB is changed from Low to High. In the state where the PWM signal is not supplied, SS terminal is not charged and DCDC does not start to operate, either.
(*2)…When REG90 is more than 6.5V(Typ), the reset signal is released.
(*3)…The charge of the pin SS starts at the positive edge of PWM=L to H, and the soft start starts. And while the SS is less than 0.4V, the pulse does not output. The pin SS continues charging in spite of the assertion of PWM or OVP level.
(*4)…The soft start interval will end once the voltage of the pin SS, Vss reaches 3.7V(Typ). By this time, it boosts V_{OUT} to the voltage where the set LED current flows. The abnormal detection of FBMAX starts to be monitored.
(*5)…As STB=L, the boost operation is stopped immediately.
(*6)…In this diagram, before the charge period is completed, STB is changed to High again. As STB=H again, the boost operation restarts the next PWM=H. It is the same operation as the timing of (*2). (For capacitance setting of SS terminal, please refer to the section 3.2.1.

3.5.2 PWM Start Up 2 (Input STB Signal after Inputted PWM Signal)

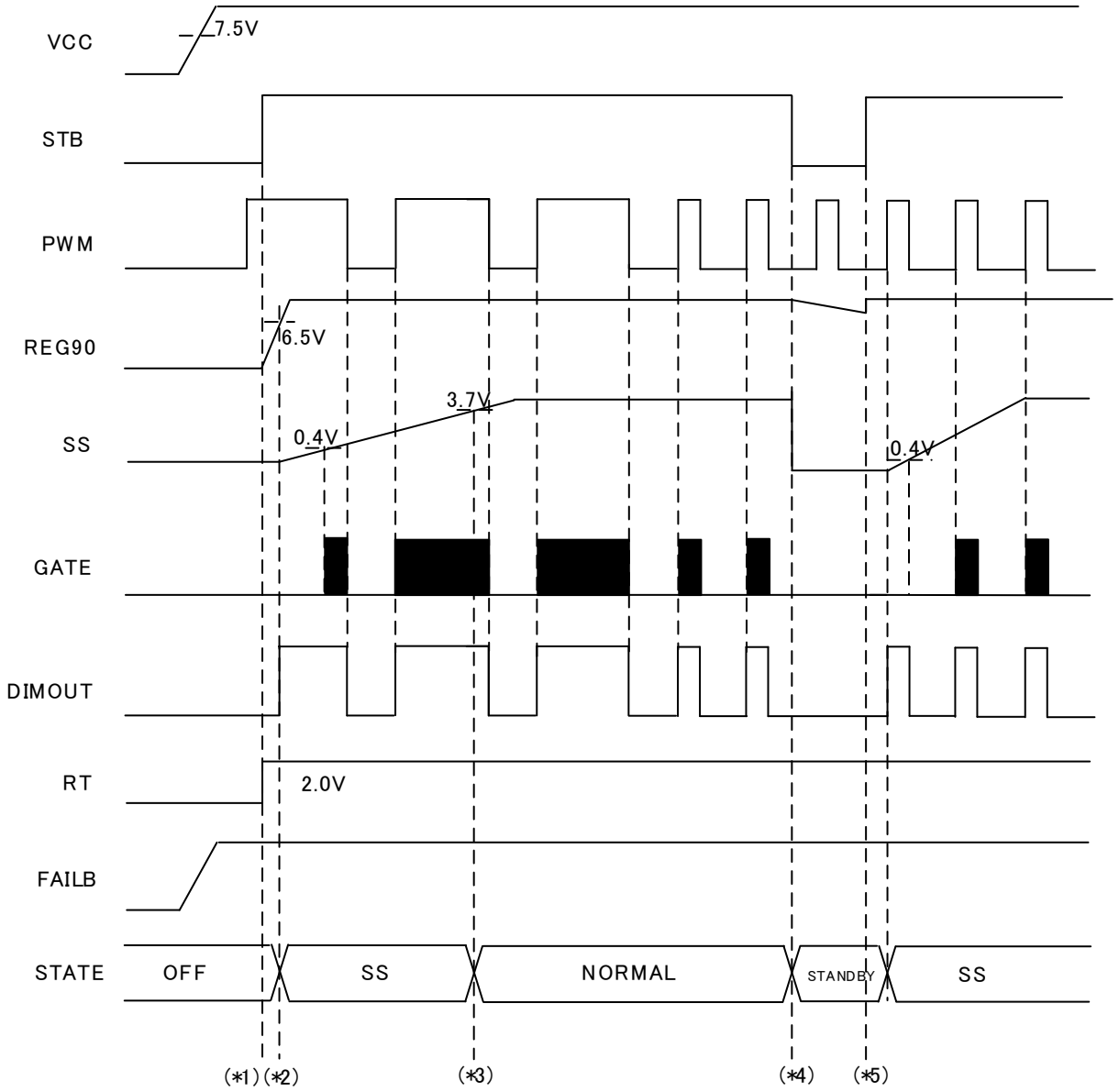


Figure 34. PWM Start Up 2 (Input STB Signal After Inputted PWM Signal)

(*1)…REG90 starts up when STB=H.
(*2)…When REG90UVLO releases or PWM is supplied to the edge of PWM=L→H, SS charge starts and soft start period is started. And while the SS is less than 0.4V, the pulse does not output. The pin SS continues charging in spite of the assertion of PWM or OVP level.
(*3)…The soft start interval will end once the voltage of the pin SS, Vss reaches 3.7V(typ.). By this time, it boosts V_{OUT} to the point where the set LED current flows. The abnormal detection of FBMAX starts to be monitored.
(*4)…As STB=L, the boost operation is stopped immediately.
(*5)…In this diagram, before the discharge period is completed, STB is changed to High again. As STB=H again, operation will be the same as the timing of (*1).

3.5.3 Turn Off

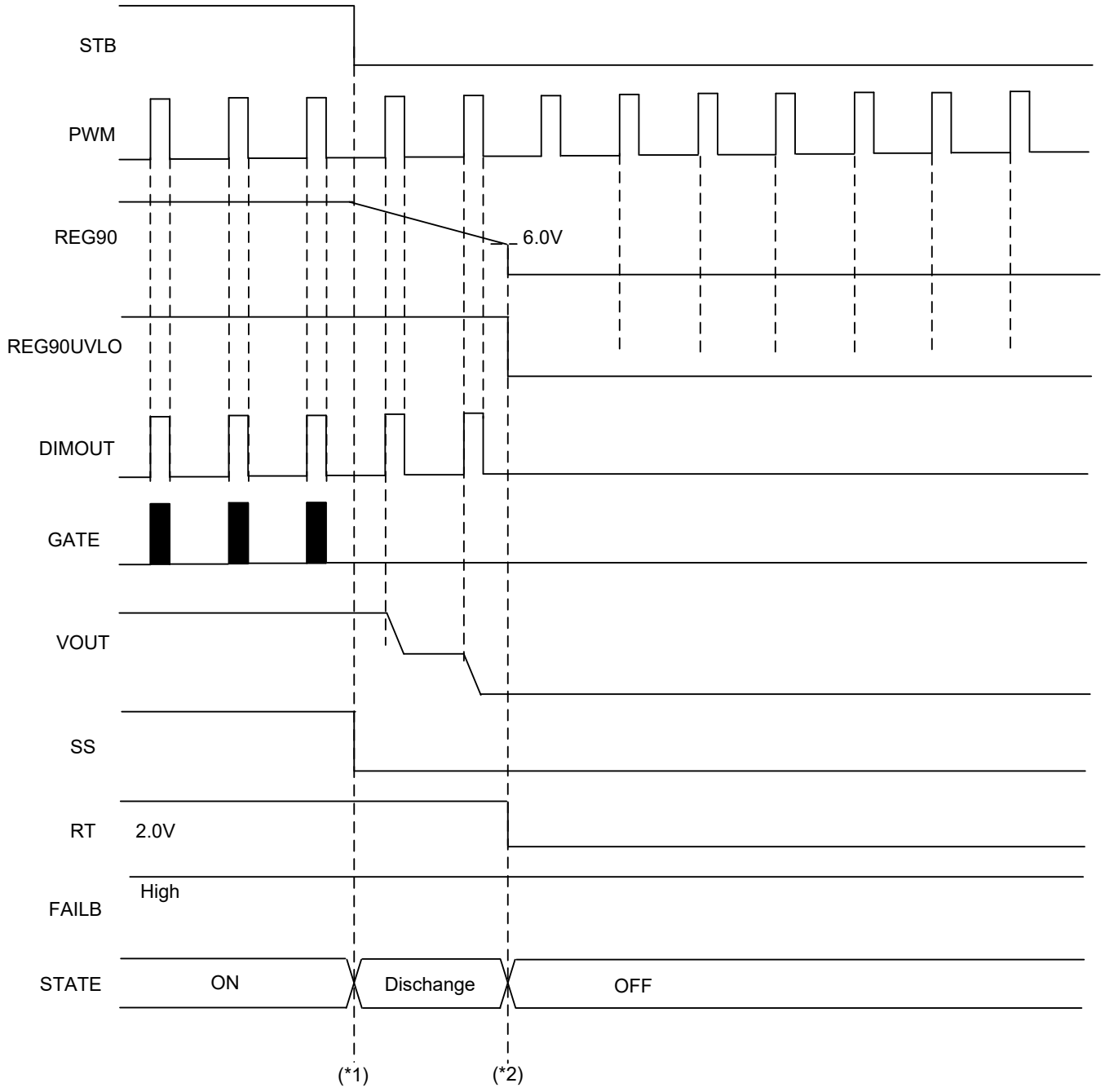


Figure 35. Turn Off

(*1)…As STB=H→L, boost operation stops and REG90 starts to discharge.
(*2)…While STB=L, REG90UVLO=H, DIMOUT becomes same as PWM. When V_{REG90}=9.0V is less than 6.0V(Typ), IC changes to OFF state. REG90 capacitor is discharged quickly and V_{RT} becomes 0V at the same time. VOUT is discharged completely until this time. It should be set to avoid sudden brightness.

3.5.4 Soft Start Function

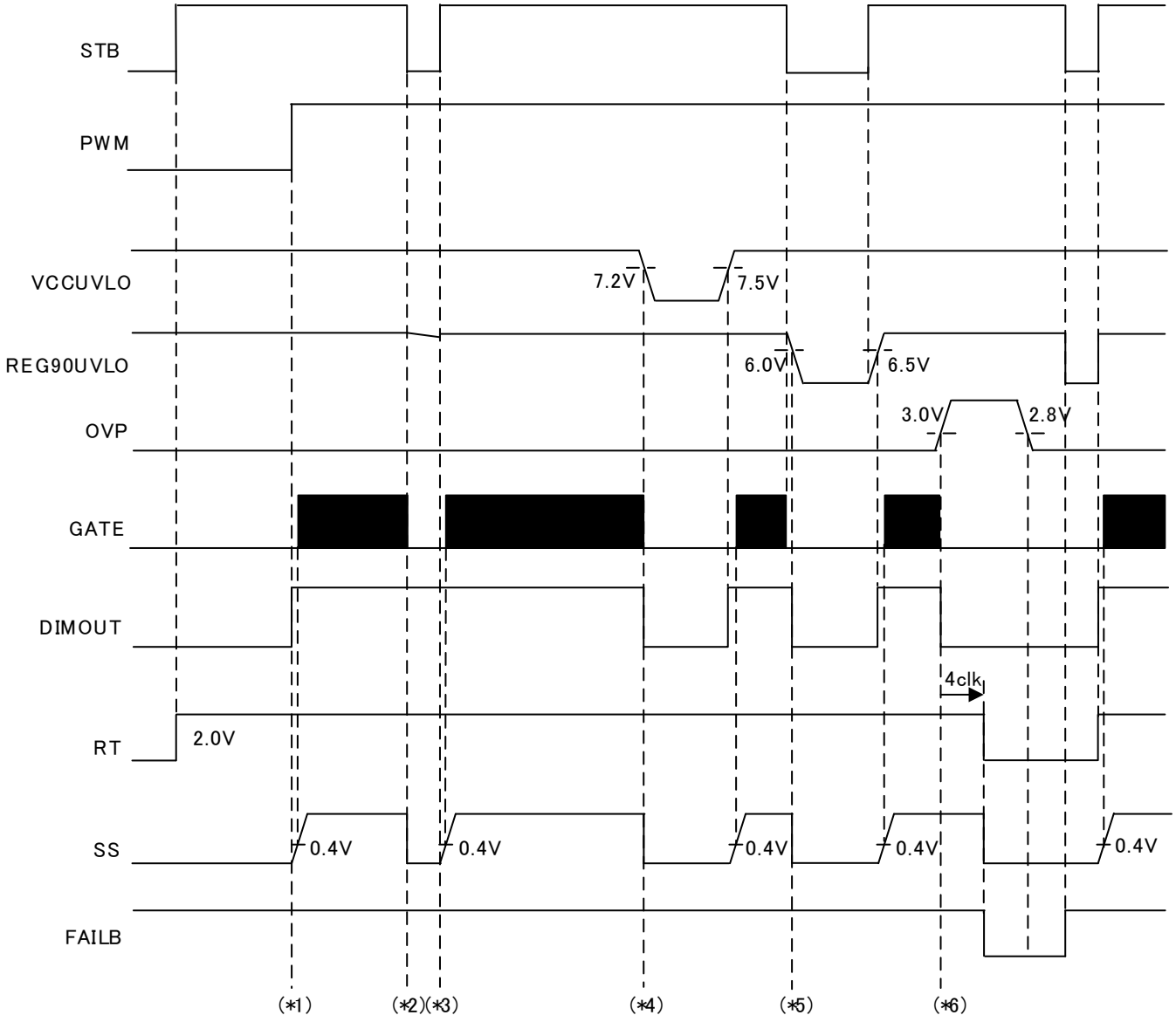


Figure 36. Soft Start Function

(*1)…The SS pin charge does not start by just STB=H. PWM=H is required to start the soft start. In the low SS voltage, the GATE pin duty depends on the SS voltage. And while the SS is less than 0.4V, the pulse does not output.
(*2)…By the time STB=L, the SS pin is discharged immediately. Because of REG90UVLO=H, RT is still High.
(*3)…As the STB recovered to STB=H, The SS charge starts immediately by the logic PWM=H in this chart.
(*4)…The SS pin is discharged immediately by the VCCUVLO=L.
(*5)…The SS pin is discharged immediately by the REG90UVLO=L.
(*6)…Unusual detection to latch OFF including OVP detection turns OFF latch, only after SS pin is discharged.

3.5.5 OVP Detection

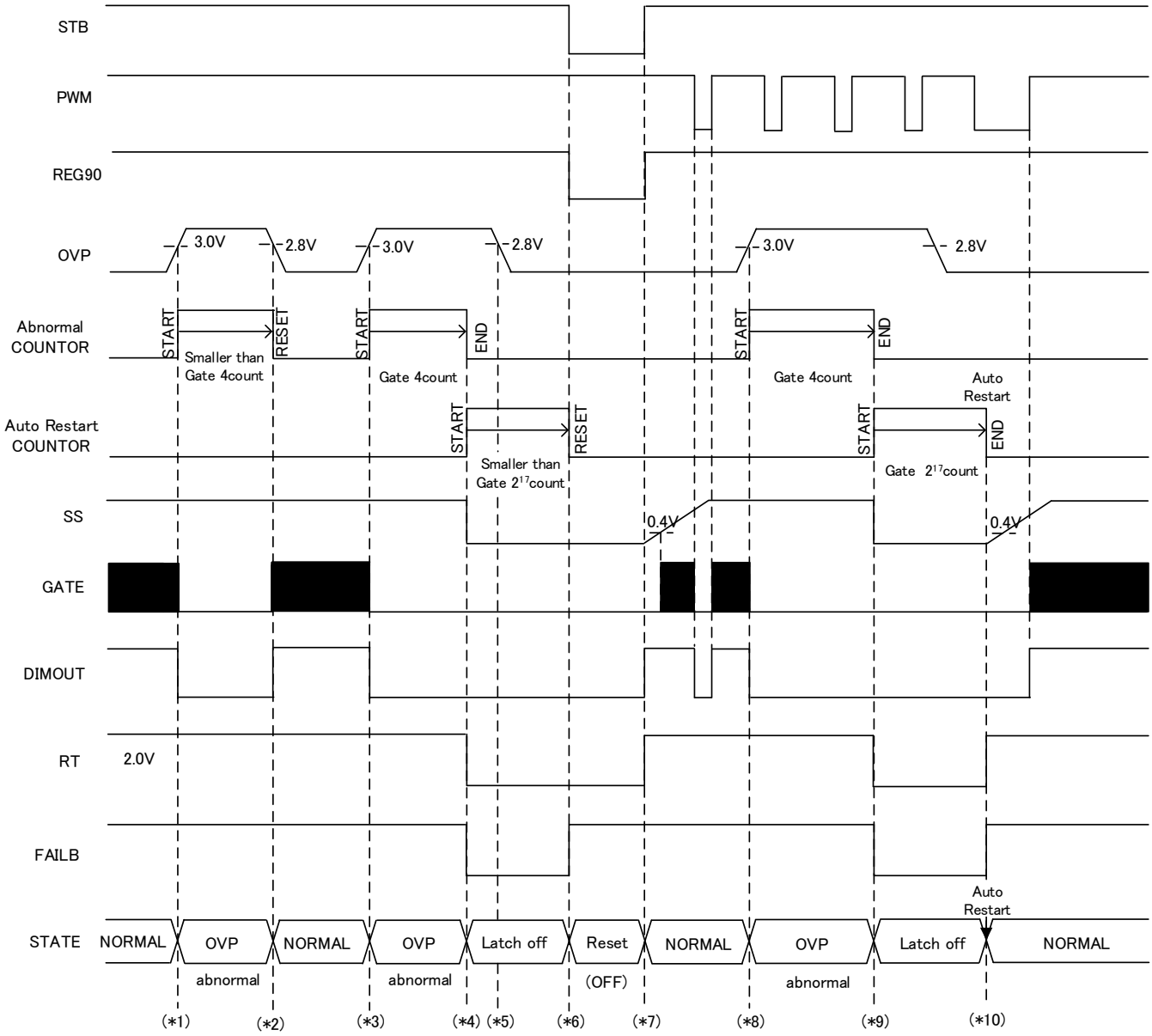


Figure 37. OVP Detection

(*1)…As OVP is detected, the output GATE=L, DIMOUT=L, and the abnormal counter starts.
(*2)…If OVP is released within 4 clocks of abnormal counter of the GATE pin frequency, the boost operation restarts.
(*3)…As the OVP is detected again, the boost operation is stopped.
(*4)…As the OVP detection continues up to 4 count by the abnormal counter, IC will be latched off. After latch off, auto counter starts counting.
(*5)… Once IC is latched off, the boost operation doesn't restart even if OVP is released.
(*6)… STB=L can release latch off. At the same time, Auto Restart counter is reset.
(*7)…Normal operation starts when STB is changed from Low to High.
(*8)…The operation of the OVP detection is not related to the logic of PWM. OVP detects and abnormal counter starts.
(*9)…same as (*4)
(*10)…When auto counter reaches 131072clk (2^{17}clk), IC will be auto-restarted. At this time, if V_{OVP} is normal level, IC state shifts to normal.

3.5.6 FBMAX Detection

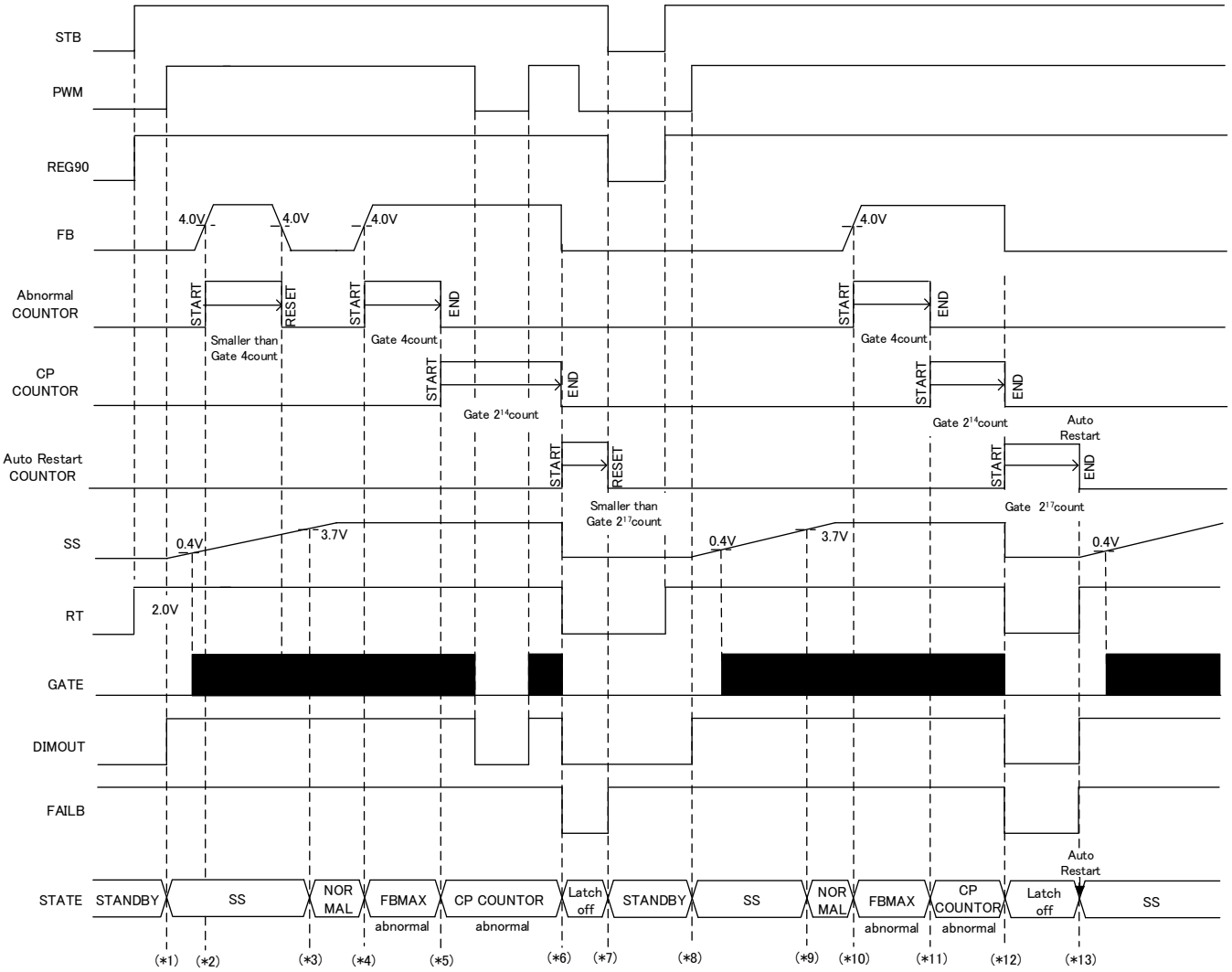


Figure 38. FBMAX Detection

(*1) …When PWM is changed to high, soft-start starts.
(*2) …During the soft start, it is not judged as an abnormal state even if the FB=H(V_{FB} >4.0V(Typ)).
(*3) …When V_{SS} reaches to 3.7V, soft-start finishes.
(*4) …When the PWM=H and FB=H, the abnormal counter start immediately.
(*5)…The CP counter will start if the PWM=H and the FB=H detection continues up to 4 clocks of the GATE frequency. Once the count starts, only FB level is monitored.
(*6)…When the FBMAX detection continues till the CP counter reaches 16384clk (2^{14}clk), IC will be latched off. The latch off interval ($LATCH_{TIME}$) can be calculated by the external resistor of RT pin. (Please refer to the section 3.2.7.)
(*7)…STB=L can release latch off.
(*8)…When PWM is set from low to high, IC starts normal start-up..
(*9)…same as (*3)
(*10)…same as (*4)
(*11)…same as (*5)
(*12)…same as (*6)
(*13)…When auto counter reaches 131072clk (2^{17}clk), IC will be auto-restarted. At this time, if V_{FB} is normal level, IC state shifts to normal.

3.5.7 LED OCP Detection

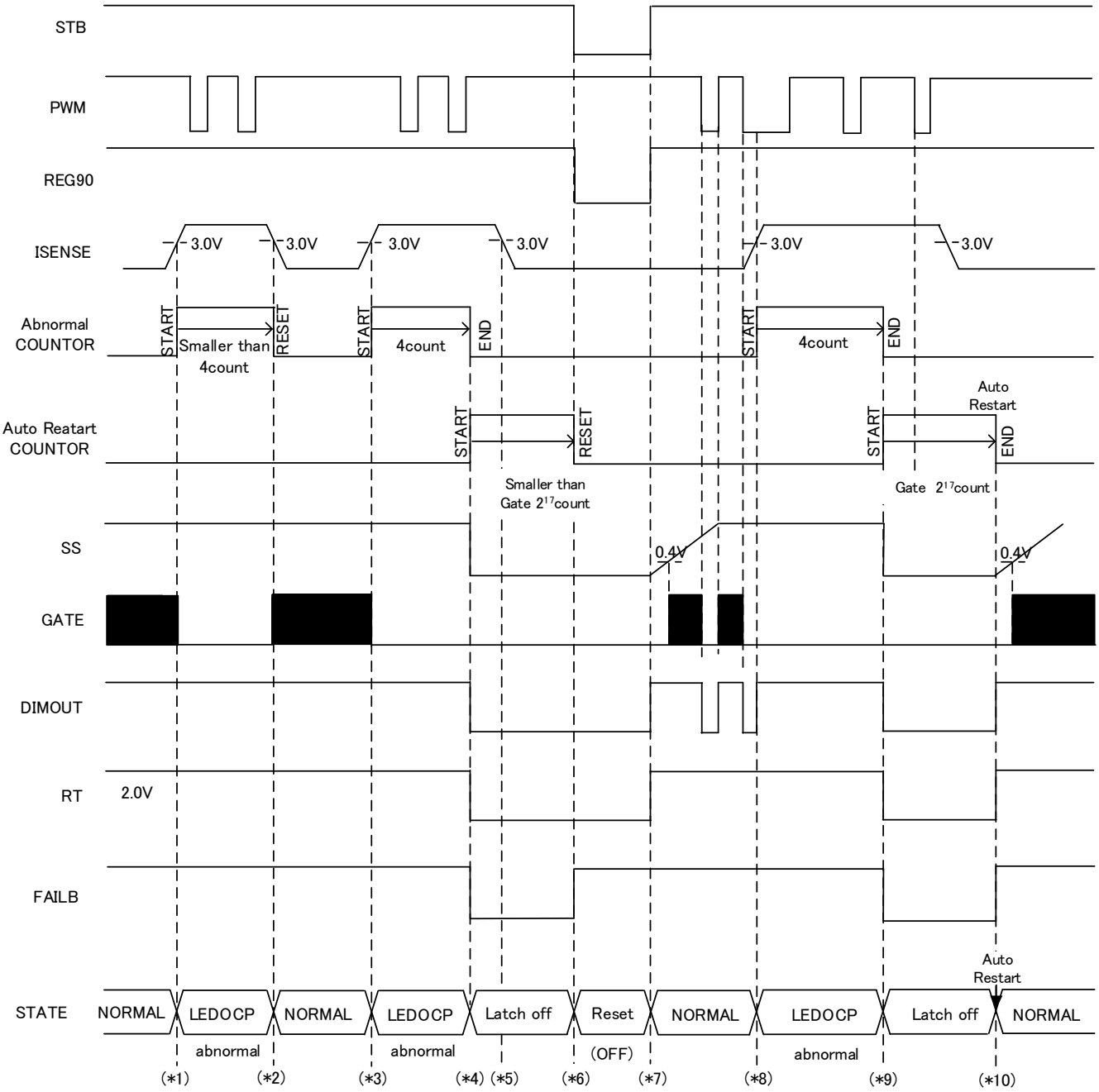


Figure 39. LED OCP Detection

(*1)…If V_{ISENSE}>3.0V(Typ), LEDOCP is detected, and GATE becomes L. To detect LEDOCP continuously, The DIMOUT is forced high, regardless of the PWM dimming signal.
(*2)…When the LEDOCP releases within 4 counts of the GATE frequency, the boost operation restarts.
(*3) …As the LEDOCP is detected again, the boost operation is stopped.
(*4)…If the LEDOCP detection continues up to 4 counts of GATE frequency. IC will be latch off. After latched off, auto counter starts counting.
(*5)…Once IC is latched off, the boost operation doesn't restart even if the LEDOCP releases.
(*6)…STB=L can release latch off.
(*7)…When STB is set from low to high, IC starts normal start-up.
(*8)…The operation of the LEDOCP detection is not related to the logic of the PWM.
(*9)…same as (*4)
(*10)…When auto counter reaches 131072clk (2^{17}clk), IC will be auto-restarted. At this time, if V_{ISENSE} is normal level, IC state shifts to normal.

3.5.8 ODP Operation

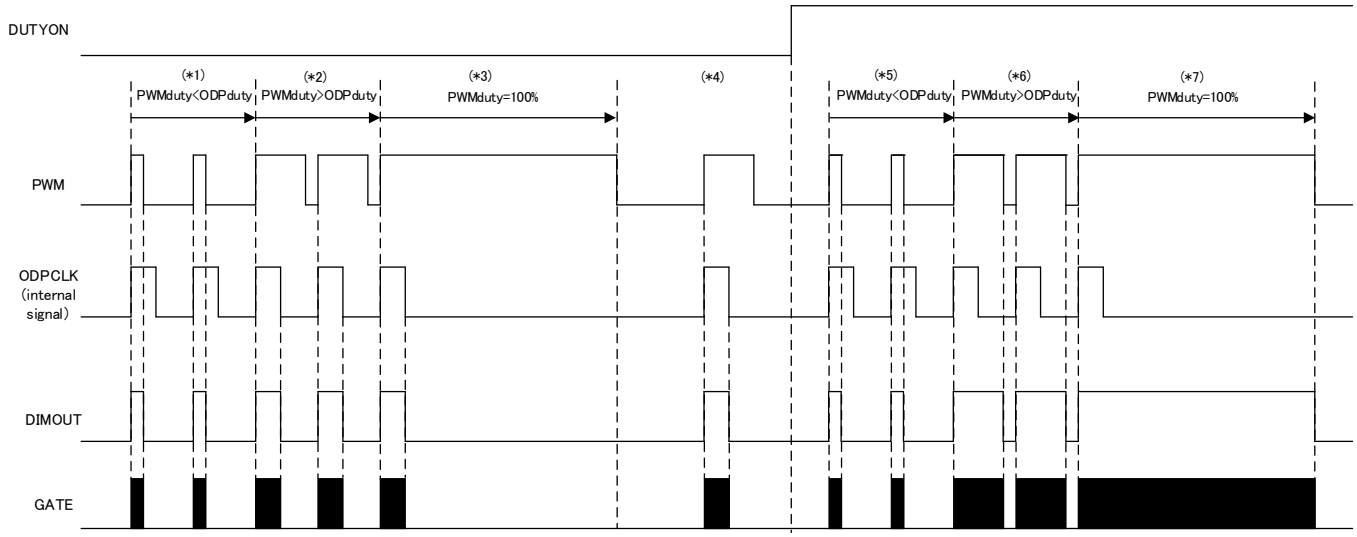


Figure 40. ODP Operation

(*1)…When DUTYON=L and PWM pin's duty (PWM_{duty}) is smaller than internal ODPCLK's duty (ODP_{duty}), PWM_{duty} is reflected to DIMOUT and GATE.
(*2)…When DUTYON=L and PWM pin's duty (PWM_{duty}) is larger than internal ODPCLK's duty (ODP_{duty}), ODP_{duty} is reflected to DIMOUT and GATE.
(*3)…When DUTYON=L and PWM pin's duty (PWM_{duty}) is equal to internal ODPCLK's duty (ODP_{duty}), ODP_{duty} is reflected to DIMOUT and GATE only once, and then until PWM is changed from low to high, DIMOUT and GATE output is low.
(*4) … When PWM is changed from low to high, ODP_{duty} is reflected to DIMOUT and GATE again.
(*5)(*6)(*7)…When DUTYON=L, PWM_{duty} is reflected to DIMOUT and GATE.

Please refer to the section "3.2.5 ODP Setting " for ODP_{duty} setting.

3.6 I/O Equivalent Circuits

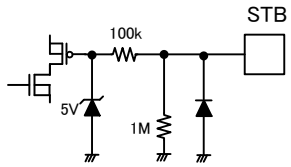
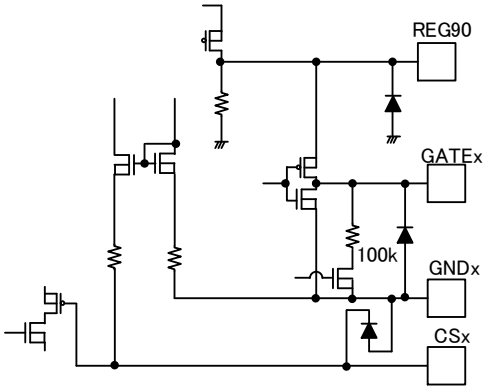
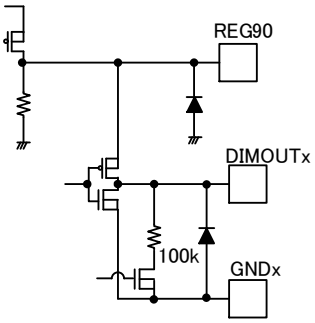
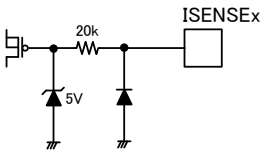
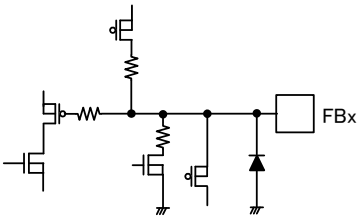
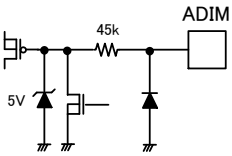
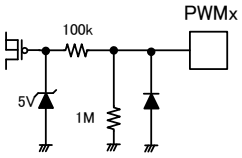
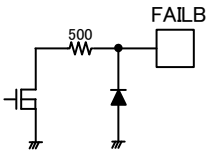
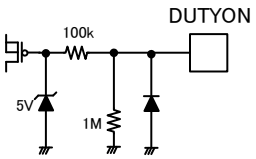
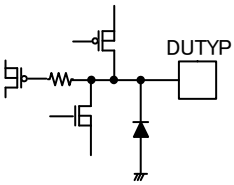
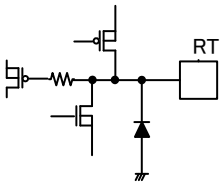
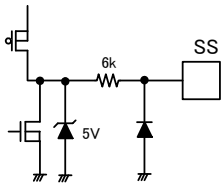
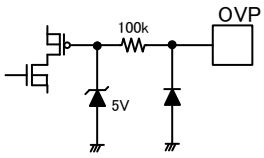
STB	GATE1 / GATE2 / REG90 / CS1 / CS2	DIMOUT1 / DIMOUT2 / GND1 / GND2
		
ISENSE1 / ISENSE2	**FB1 / FB2**	**ADIM**
		
PWM1 / PWM2	**FAILB**	**DUTYON**
		
DUTYP	**RT**	**SS**
		
OVP		
		

Figure 41. Equivalent Circuits

Operational Notes

1.Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2.Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3.Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4.Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5.Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6.Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7.Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8.Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9.Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10.Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

11.Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

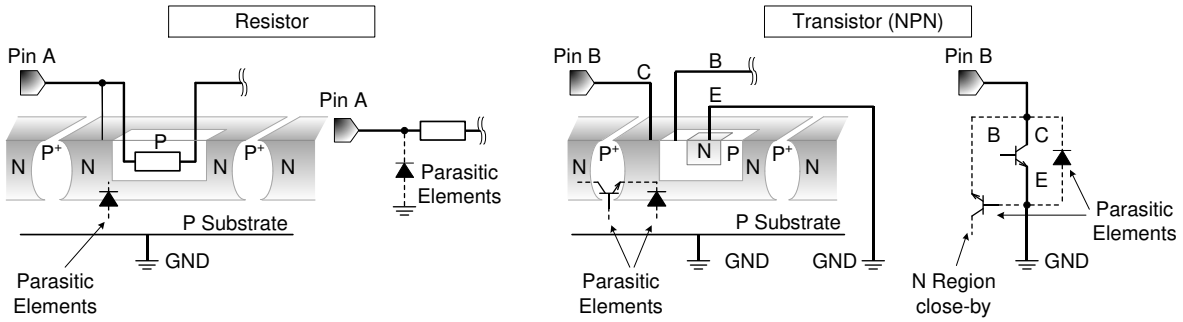


Figure 42. Example of monolithic IC structure

12.Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13.Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

14.Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

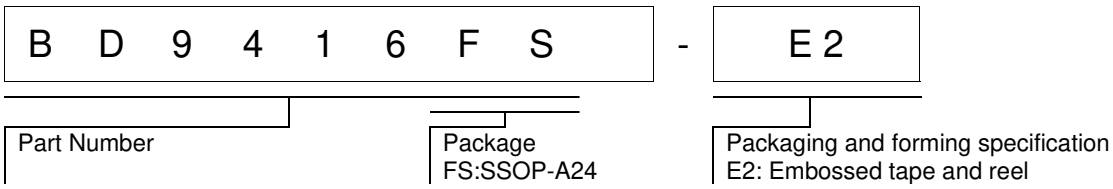
15.Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

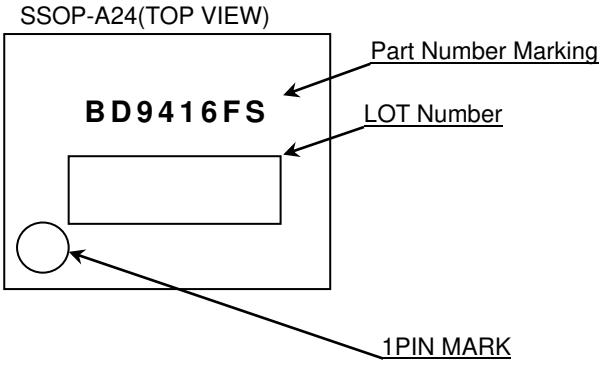
16.Disturbance Light

In a device where a portion of silicon is exposed to light such as in a WL-CSP and chip products, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

Ordering Information



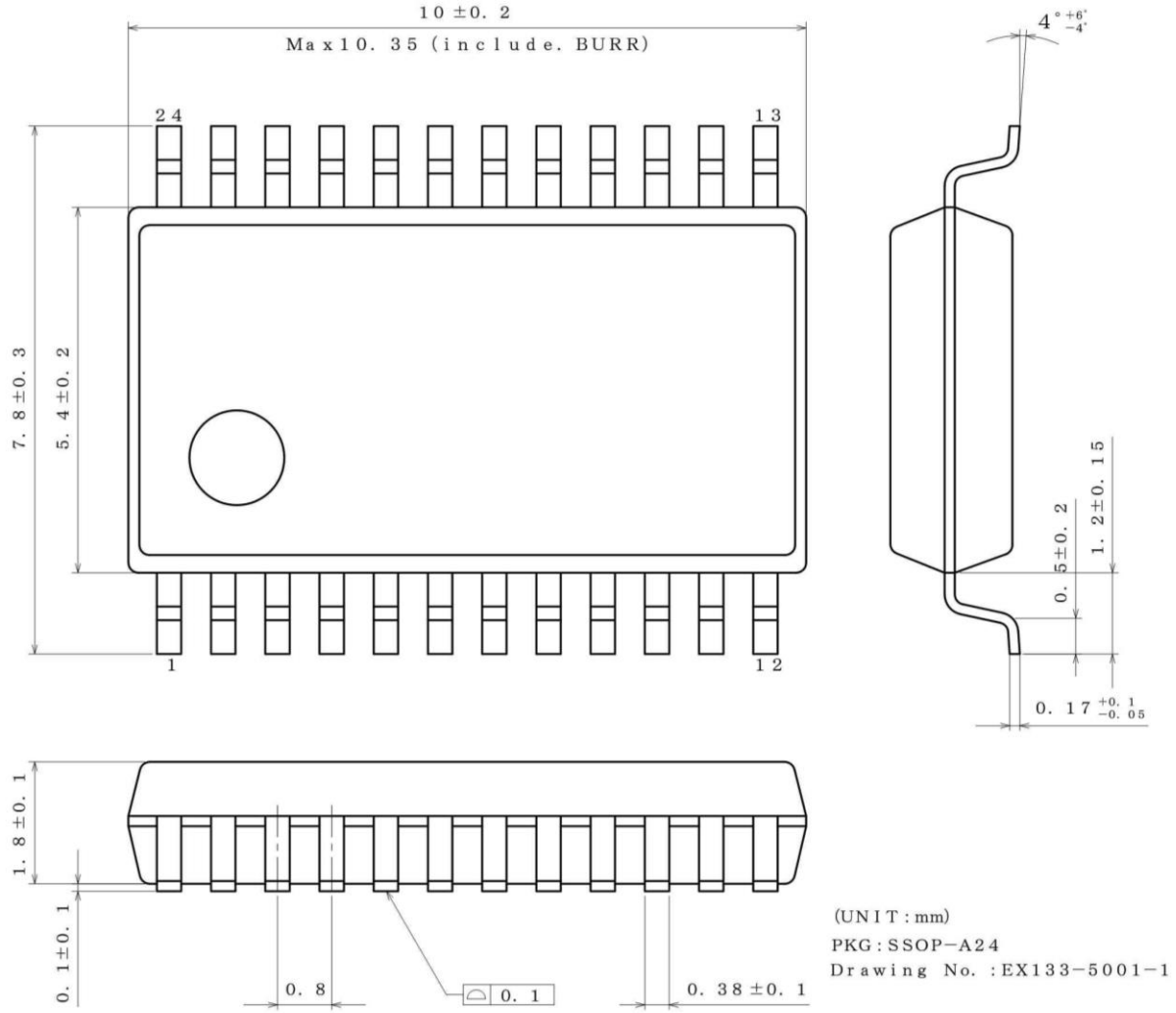
Marking Diagrams



Part Number Marking	Package	Orderable Part Number
BD9416FS	SSOP-A24	BD9416FS-E2

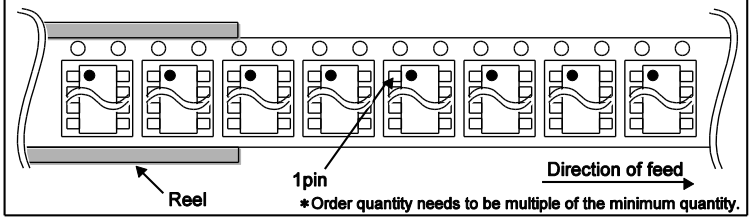
Physical Dimension, Tape and Reel Information

Package Name	SSOP-A24



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
08.Apr.2017	Rev.001	New Release
24.May.2023	Rev.002	Deleted reference to BD9416F from the datasheet (TSZ02201-0T5T0C100020-1-2) as BD9416F is being discontinued.

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

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3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

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General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

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