



# 4-Kb Microwire Serial CMOS EEPROM

## FEATURES

- High speed operation: 2MHz
- 1.8V to 5.5V supply voltage range
- Selectable x8 or x16 memory organization
- Sequential read
- Software write protection
- Power-up inadvertant write protection
- Low power CMOS technology
- 1,000,000 Program/erase cycles
- 100 year data retention
- Industrial and Extended temperature ranges
- RoHS-compliant 8-pin PDIP, SOIC, TSSOP and 8-pad TDFN packages



## PIN CONFIGURATION

	PDIP (L)	SOIC (V, X)	TSSOP (Y)	TDFN (VP2, ZD4)*		SOIC (W)*		
CS	1	8	V <sub>CC</sub>		NC	1	8	ORG
SK	2	7	NC		V <sub>CC</sub>	2	7	GND
DI	3	6	ORG		CS	3	6	DO
DO	4	5	GND		SK	4	5	DI

\* TDFN 3x3mm (ZD4) and SOIC (W) rotated pin-out packages are available only for Die Rev E (not recommended for new designs)

## PIN FUNCTION

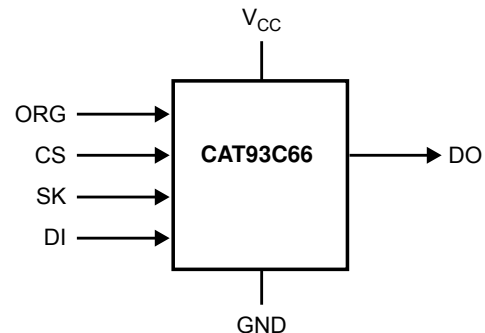
Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V <sub>CC</sub>	Power Supply
GND	Ground
ORG	Memory Organization
NC	No Connection

## DESCRIPTION

The CAT93C66 is a 4-Kb CMOS Serial EEPROM device which is organized as either 256 registers of 16 bits (ORG pin at V<sub>CC</sub>) or 512 registers of 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C66 features sequential read and self-timed internal write with auto-clear. On-chip Power-On Reset circuitry protects the internal logic against powering up in the wrong state.

For Ordering Information details, see page 15.

## FUNCTIONAL SYMBOL



Note: When the ORG pin is connected to V<sub>CC</sub>, the x16 organization is selected. When it is connected to ground, the x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x16 organization

**Absolute Maximum Ratings<sup>(1)</sup>**

Parameters	Ratings	Units
Storage Temperature	-65 to +150	°C
Voltage on Any Pin with Respect to Ground <sup>(2)</sup>	-0.5 to +6.5	V

**Reliability Characteristics<sup>(3)</sup>**

Symbol	Parameter	Min	Units
NEND <sup>(4)</sup>	Endurance	1,000,000	Program/ Erase Cycles
TDR	Data Retention	100	Years

**D.C. OPERATING CHARACTERISTICS (New Product, Die Rev. G)**

$V_{CC} = +1.8V$  to  $+5.5V$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$  unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Max	Units
$I_{CC1}$	Power Supply Current (Write)	$f_{SK} = 1MHz$ , $V_{CC} = 5.0V$		1	mA
$I_{CC2}$	Power Supply Current (Read)	$f_{SK} = 1MHz$ , $V_{CC} = 5.0V$		500	$\mu A$
$I_{SB1}$	Power Supply Current (Standby) (x8 Mode)	$V_{IN} = GND$ or $V_{CC}$ , $CS = GND$ ORG = GND	$T_A = -40^\circ C$ to $+85^\circ C$	2	$\mu A$
			$T_A = -40^\circ C$ to $+125^\circ C$	4	
$I_{SB2}$	Power Supply Current (Standby) (x16 Mode)	$V_{IN} = GND$ or $V_{CC}$ , $CS = GND$ ORG = Float or $V_{CC}$	$T_A = -40^\circ C$ to $+85^\circ C$	1	$\mu A$
			$T_A = -40^\circ C$ to $+125^\circ C$	2	
$I_{LI}$	Input Leakage Current	$V_{IN} = GND$ to $V_{CC}$	$T_A = -40^\circ C$ to $+85^\circ C$	1	$\mu A$
			$T_A = -40^\circ C$ to $+125^\circ C$	2	
$I_{LO}$	Output Leakage Current	$V_{OUT} = GND$ to $V_{CC}$ , $CS = GND$	$T_A = -40^\circ C$ to $+85^\circ C$	1	$\mu A$
			$T_A = -40^\circ C$ to $+125^\circ C$	2	
$V_{IL1}$	Input Low Voltage	$4.5V \leq V_{CC} < 5.5V$	-0.1	0.8	V
$V_{IH1}$	Input High Voltage	$4.5V \leq V_{CC} < 5.5V$	2	$V_{CC} + 1$	V
$V_{IL2}$	Input Low Voltage	$1.8V \leq V_{CC} < 4.5V$	0	$V_{CC} \times 0.2$	V
$V_{IH2}$	Input High Voltage	$1.8V \leq V_{CC} < 4.5V$	$V_{CC} \times 0.7$	$V_{CC} + 1$	V
$V_{OL1}$	Output Low Voltage	$4.5V \leq V_{CC} < 5.5V$ , $I_{OL} = 2.1mA$		0.4	V
$V_{OH1}$	Output High Voltage	$4.5V \leq V_{CC} < 5.5V$ , $I_{OH} = -400\mu A$	2.4		V
$V_{OL2}$	Output Low Voltage	$1.8V \leq V_{CC} < 4.5V$ , $I_{OL} = 1mA$		0.2	V
$V_{OH2}$	Output High Voltage	$1.8V \leq V_{CC} < 4.5V$ , $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V

**Notes:**

- (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.
- (2) The DC input voltage on any pin should not be lower than -0.5V or higher than  $V_{CC} + 0.5V$ . During transitions, the voltage on any pin may undershoot to no less than -1.5V or overshoot to no more than  $V_{CC} + 1.5V$ , for periods of less than 20 ns.
- (3) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
- (4) Block Mode,  $V_{CC} = 5V$ ,  $25^\circ C$

**D.C. OPERATING CHARACTERISTICS (Mature Product, Die Rev. E – NOT RECOMMENDED FOR NEW DESIGNS)**
 $V_{CC} = +1.8V$  to  $+5.5V$ , unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Max	Units
$I_{CC1}$	Power Supply Current (Write)	$f_{SK} = 1MHz, V_{CC} = 5.0V$		3	mA
$I_{CC2}$	Power Supply Current (Read)	$f_{SK} = 1MHz, V_{CC} = 5.0V$		500	$\mu A$
$I_{SB1}$	Power Supply Current (Standby) (x8 Mode)	$V_{IN} = GND$ or $V_{CC}$ , $CS = GND$ $ORG = GND$		10	$\mu A$
$I_{SB2}$	Power Supply Current (Standby) (x16 Mode)	$V_{IN} = GND$ or $V_{CC}$ , $CS = GND$ $ORG = Float$ or $V_{CC}$		10	$\mu A$
$I_{LI}$	Input Leakage Current	$V_{IN} = GND$ to $V_{CC}$		1	$\mu A$
$I_{LO}$	Output Leakage Current	$V_{OUT} = GND$ to $V_{CC}$ , $CS = GND$		1	$\mu A$
$V_{IL1}$	Input Low Voltage	$4.5V \leq V_{CC} < 5.5V$	-0.1	0.8	V
$V_{IH1}$	Input High Voltage	$4.5V \leq V_{CC} < 5.5V$	2	$V_{CC} + 1$	V
$V_{IL2}$	Input Low Voltage	$1.8V \leq V_{CC} < 4.5V$	0	$V_{CC} \times 0.2$	V
$V_{IH2}$	Input High Voltage	$1.8V \leq V_{CC} < 4.5V$	$V_{CC} \times 0.7$	$V_{CC} + 1$	V
$V_{OL1}$	Output Low Voltage	$4.5V \leq V_{CC} < 5.5V, I_{OL} = 2.1mA$		0.4	V
$V_{OH1}$	Output High Voltage	$4.5V \leq V_{CC} < 5.5V, I_{OH} = -400\mu A$	2.4		V
$V_{OL2}$	Output Low Voltage	$1.8V \leq V_{CC} < 4.5V, I_{OL} = 1mA$		0.2	V
$V_{OH2}$	Output High Voltage	$1.8V \leq V_{CC} < 4.5V, I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V

**PIN CAPACITANCE**
 $T_A = 25^\circ C, f = 1MHz, V_{CC} = 5V$ 

Symbol	Test	Conditions	Min	Typ	Max	Units
$C_{OUT}^{(1)}$	Output Capacitance (DO)	$V_{OUT} = 0V$			5	pF
$C_{IN}^{(1)}$	Input Capacitance (CS, SK, DI, ORG)	$V_{IN} = 0V$			5	pF

**Notes:**

- (1) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

**A.C. CHARACTERISTICS<sup>(1)</sup> (New Product, Die Rev. G)**
 $V_{CC} = +1.8V$  to  $+5.5V$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise specified.

Symbol	Parameter	Limits		Units
		Min	Max	
$t_{CSS}$	CS Setup Time	50		ns
$t_{CSH}$	CS Hold Time	0		ns
$t_{DIS}$	DI Setup Time	100		ns
$t_{DIH}$	DI Hold Time	100		ns
$t_{PD1}$	Output Delay to 1		0.25	$\mu s$
$t_{PD0}$	Output Delay to 0		0.25	$\mu s$
$t_{HZ}^{(2)}$	Output Delay to High-Z		100	ns
$t_{EW}$	Program/Erase Pulse Width		5	ms
$t_{CSMIN}$	Minimum CS Low Time	0.25		$\mu s$
$t_{SKHI}$	Minimum SK High Time	0.25		$\mu s$
$t_{SKLOW}$	Minimum SK Low Time	0.25		$\mu s$
$t_{SV}$	Output Delay to Status Valid		0.25	$\mu s$
$SK_{MAX}$	Maximum Clock Frequency	DC	2000	kHz

**A.C. CHARACTERISTICS<sup>(1)</sup> (Mature Product, Die Rev E – NOT RECOMMENDED FOR NEW DESIGN)**

Symbol	Parameter	Limits						Units
		$V_{CC} = 1.8V - 5.5V$		$V_{CC} = 2.5V - 5.5V$		$V_{CC} = 4.5V - 5.5V$		
		Min	Max	Min	Max	Min	Max	
$t_{CSS}$	CS Setup Time	200		100		50		ns
$t_{CSH}$	CS Hold Time	0		0		0		ns
$t_{DIS}$	DI Setup Time	400		200		100		ns
$t_{DIH}$	DI Hold Time	400		200		100		ns
$t_{PD1}$	Output Delay to 1		1		0.5		0.25	$\mu s$
$t_{PD0}$	Output Delay to 0		1		0.5		0.25	$\mu s$
$t_{HZ}^{(2)}$	Output Delay to High-Z		400		200		100	ns
$t_{EW}$	Program/Erase Pulse Width		10		10		10	ms
$t_{CSMIN}$	Minimum CS Low Time	1		0.5		0.25		$\mu s$
$t_{SKHI}$	Minimum SK High Time	1		0.5		0.25		$\mu s$
$t_{SKLOW}$	Minimum SK Low Time	1		0.5		0.25		$\mu s$
$t_{SV}$	Output Delay to Status Valid		1		0.5		0.25	$\mu s$
$SK_{MAX}$	Maximum Clock Frequency	DC	250	DC	500	DC	1000	kHz

**Notes:**

- (1) Test conditions according to "A.C. Test Conditions" table.
- (2) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

**POWER-UP TIMING<sup>(1) (2)</sup>**

Symbol	Parameter	Max	Units
t <sub>PUR</sub>	Power-up to Read Operation	1	ms
t <sub>PUW</sub>	Power-up to Write Operation	1	ms

**Notes:**

- (1) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
- (2) t<sub>PUR</sub> and t<sub>PUW</sub> are the delays required from the time V<sub>CC</sub> is stable until the specified operation can be initiated.

**A.C. Test Conditions**

Input Rise and Fall Times	≤ 50 ns		
Input Pulse Voltages	0.4V to 2.4V	4.5V ≤ V <sub>CC</sub> ≤ 5.5V	
Timing Reference Voltages	0.8V, 2.0V	4.5V ≤ V <sub>CC</sub> ≤ 5.5V	
Input Pulse Voltages	0.2V <sub>CC</sub> to 0.7V <sub>CC</sub>	1.8V ≤ V <sub>CC</sub> ≤ 4.5V	
Timing Reference Voltages	0.5V <sub>CC</sub>	1.8V ≤ V <sub>CC</sub> ≤ 4.5V	
Output Load	Current Source I <sub>OLmax</sub> /I <sub>OHmax</sub> ; CL=100pF		

**DEVICE OPERATION**

The CAT93C66 is a 4096-bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93C66 can be organized as either registers of 16 bits or 8 bits. When organized as X16, seven 11-bit instructions control the reading, writing and erase operations of the device. When organized as X8, seven 12-bit instructions control the reading, writing and erase operations of the device. The CAT93C66 operates on a single power supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation. The serial communication protocol follows the timing shown in Figure 1.

The ready/busy status can be determined after the start of internal write cycle by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy “1” into the DI pin. The DO pin will enter the high impedance state on the rising edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the device is a logical “1” start bit, a 2-bit (or 4-bit) opcode, 8-bit address (an additional bit when organized X8) and for write operations a 16-bit data field (8-bit for X8 organizations). The instruction format is shown in Instruction Set table.

**INSTRUCTION SET**

Instruction	Start Bit	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A8-A0	A7-A0			Read Address AN – A0
ERASE	1	11	A8-A0	A7-A0			Clear Address AN – A0
WRITE	1	01	A8-A0	A7-A0	D7-D0	D15-D0	Write Address AN – A0
EWEN	1	00	11XXXXXXXX	11XXXXXX			Write Enable
EWDS	1	00	00XXXXXXXX	00XXXXXX			Write Disable
ERAL	1	00	10XXXXXXXX	10XXXXXX			Clear All Addresses
WRAL	1	00	01XXXXXXXX	01XXXXXX	D7-D0	D15-D0	Write All Addresses

**Read**

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C66 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay ( $t_{PD0}$  or  $t_{PD1}$ ).

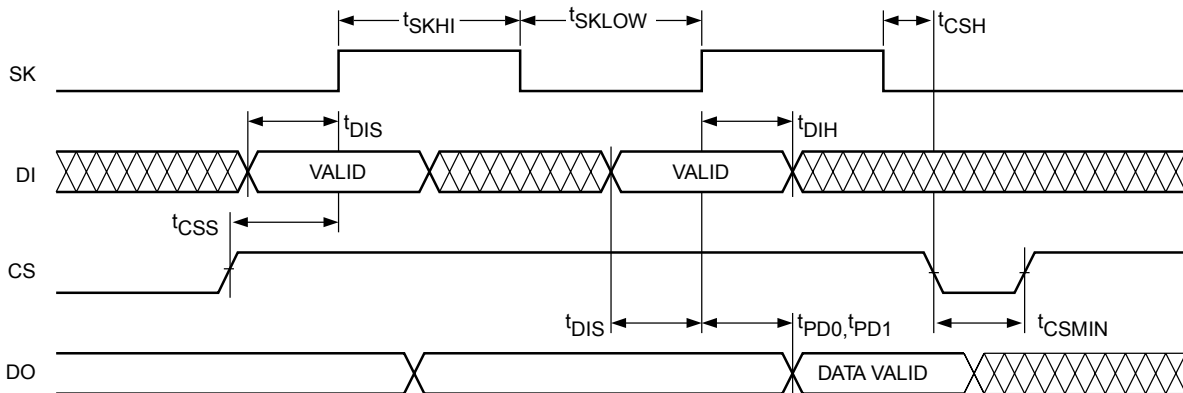
For the CAT93C66, after the initial data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the device will automatically increment to the next address and shift out the next data word in a sequential READ mode. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches to the end of the address space, then loops back to address 0. In the

sequential READ mode, only the initial data word is preceded by a dummy zero bit. All subsequent data words will follow without a dummy zero bit. The READ instruction timing is illustrated in Figure 2.

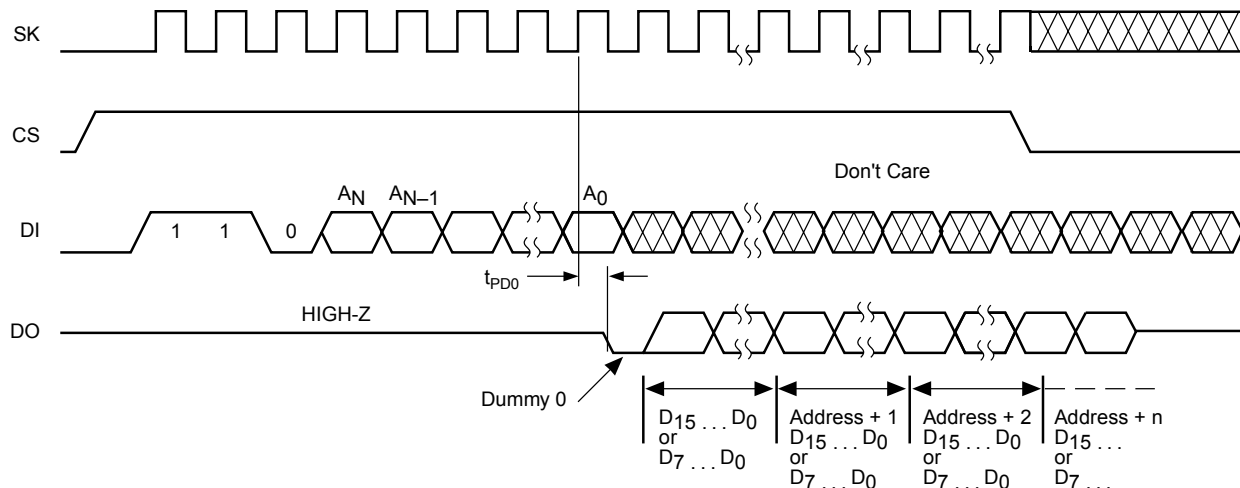
**Erase/Write Enable and Disable**

The CAT93C66 powers up in the write disable state. Any writing after power-up or after an EWDS (erase/write disable) instruction must first be preceded by the EWEN (erase/write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C66 write and erase instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status. The EWEN and EWDS instructions timing is shown in Figure 3.

**Figure 1. Synchronous Data Timing**



**Figure 2. READ Instruction Timing**



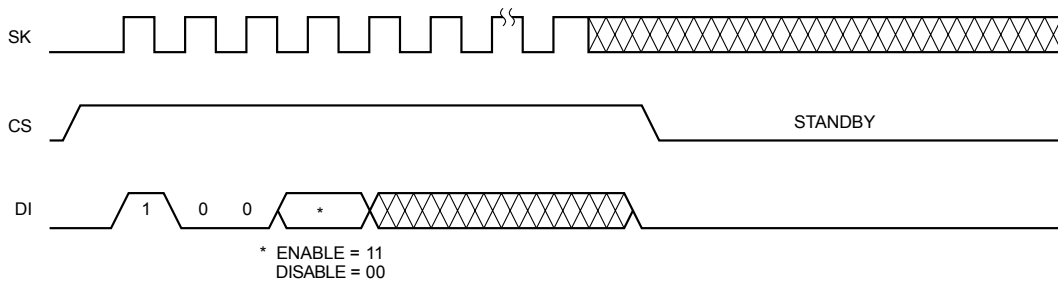
**Write**

After receiving a WRITE command (Figure 4), address and the data, the CS (Chip Select) pin must be deselected for a minimum of  $t_{CSMIN}$ . The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C66 can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before it is written into.

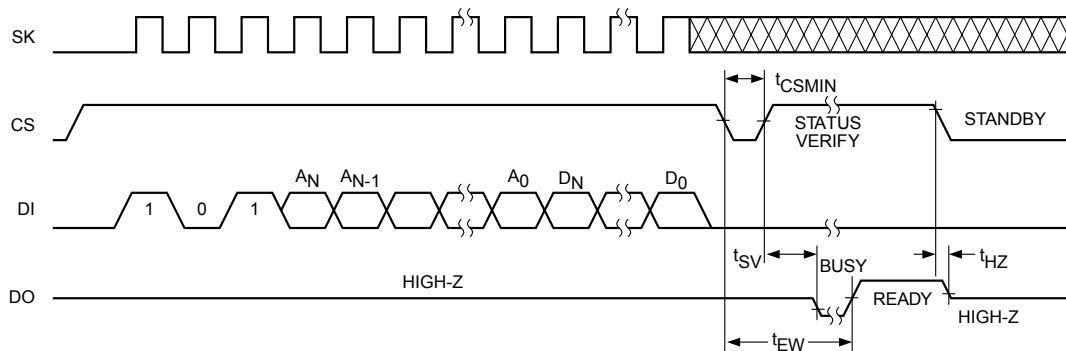
**Erase**

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of  $t_{CSMIN}$  (Figure 5). The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/ busy status of the CAT93C66 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

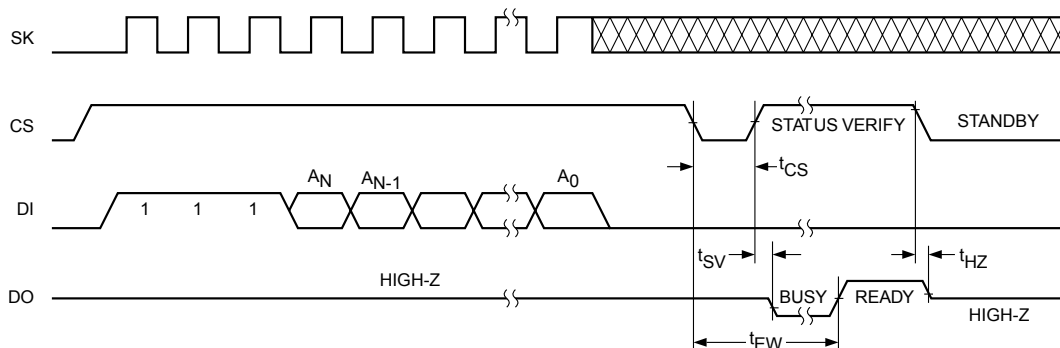
**Figure 3. EWEN/EWDS Instruction Timing**



**Figure 4. Write Instruction Timing**



**Figure 5. Erase Instruction Timing**



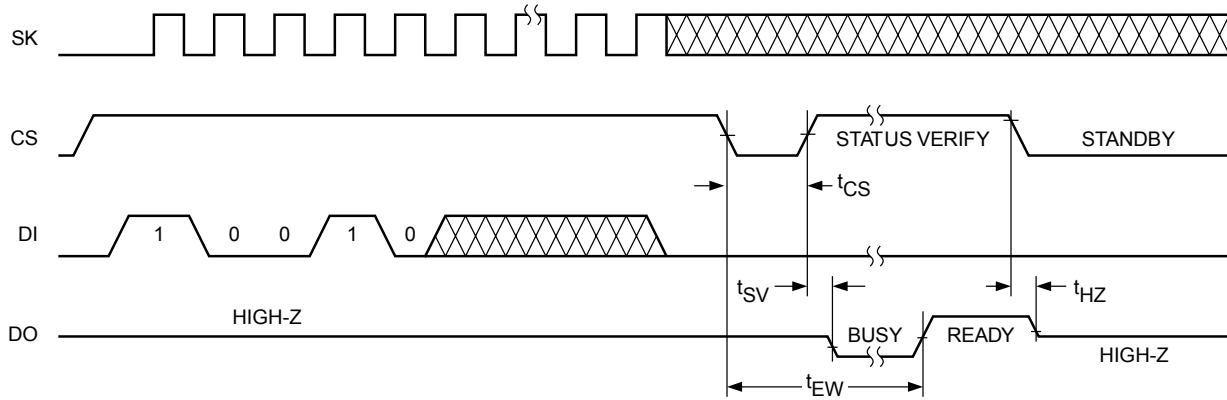
**Erase All**

Upon receiving an ERAL command (Figure 6), the CS (Chip Select) pin must be deselected for a minimum of  $t_{CSMIN}$ . The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C66 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

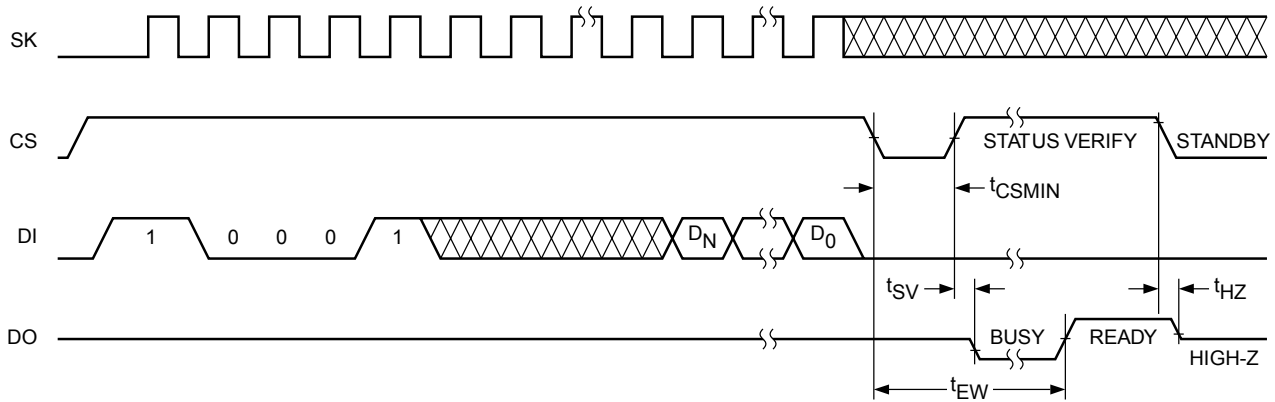
**Write All**

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of  $t_{CSMIN}$  (Figure 7). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C66 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

**Figure 6. ERAL Instruction Timing**



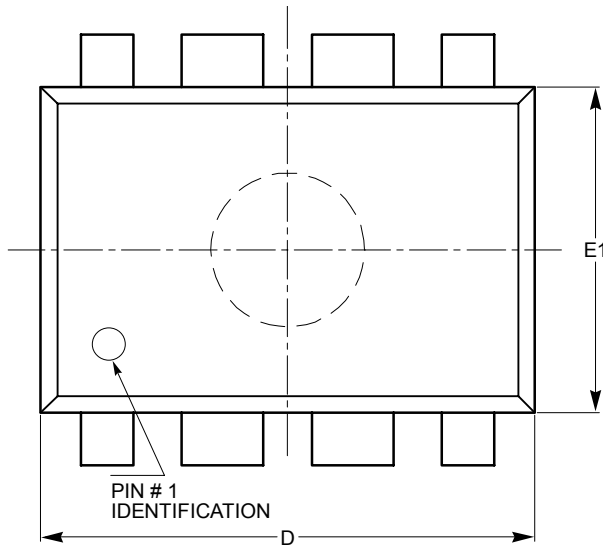
**Figure 7. WRAL Instruction Timing**





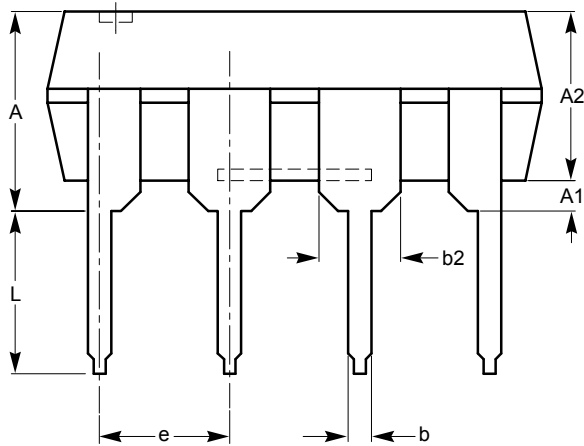
**PACKAGE OUTLINE DRAWINGS**

**PDIP 8-Lead 300mils (L)**

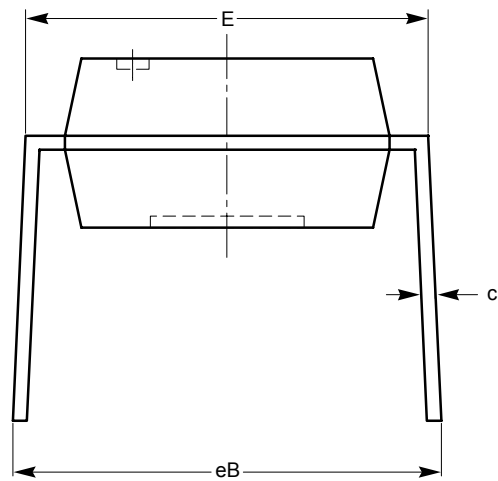


**TOP VIEW**

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
e	2.54 BSC		
E1	6.10	6.35	7.11
eB	7.87		10.92
L	2.92	3.30	3.80



**SIDE VIEW**



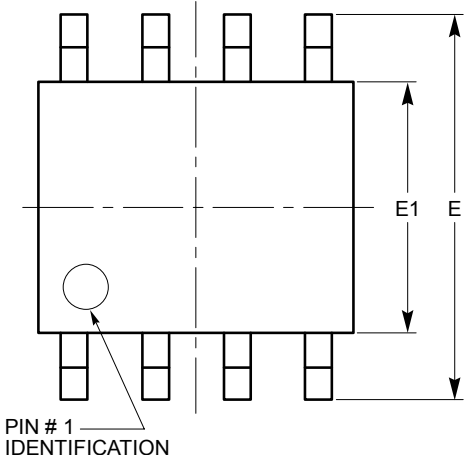
**END VIEW**

**For current Tape and Reel information, download the PDF file from:  
<http://www.catsemi.com/documents/tapeand reel.pdf>.**

**Notes:**

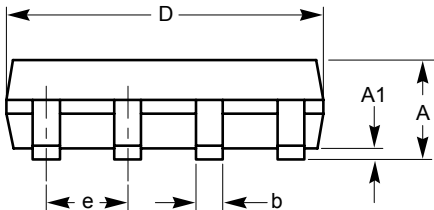
- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MS-001.

SOIC 8-Lead 150mils (V, W)

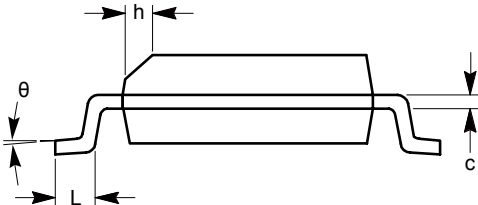


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
$\theta$	0°		8°



SIDE VIEW



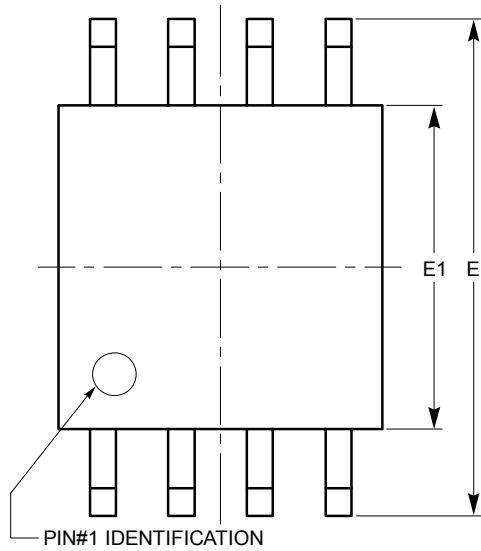
END VIEW

For current Tape and Reel information, download the PDF file from:  
<http://www.catsemi.com/documents/tapeandreel.pdf>.

Notes:

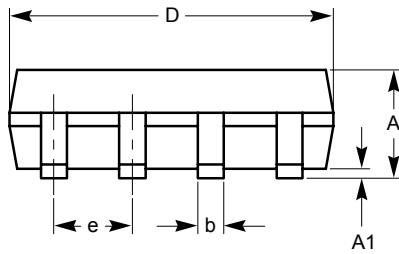
- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

**SOIC 8-Lead 208mils (X)**

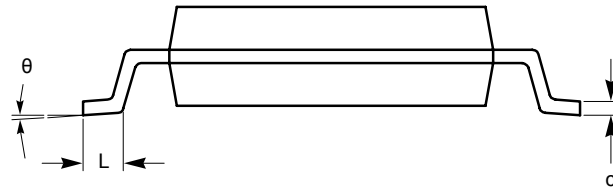


**TOP VIEW**

SYMBOL	MIN	NOM	MAX
A			2.03
A1	0.05		0.25
b	0.36		0.48
c	0.19		0.25
D	5.13		5.33
E	7.75		8.26
E1	5.13		5.38
e	1.27 BSC		
L	0.51		0.76
$\theta$	0°		8°



**SIDE VIEW**



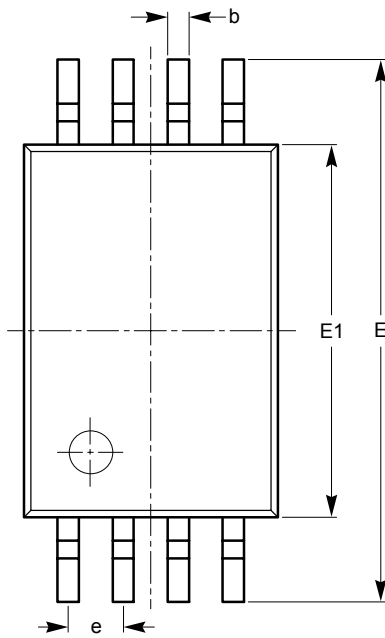
**END VIEW**

**For current Tape and Reel information, download the PDF file from:  
<http://www.catsemi.com/documents/tapeandreel.pdf>.**

**Notes:**

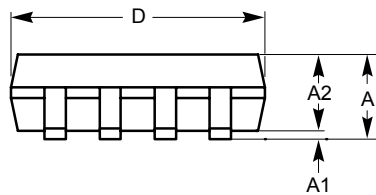
- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with EIAJ EDR-7320.

TSSOP 8-Lead 4.4mm (Y)

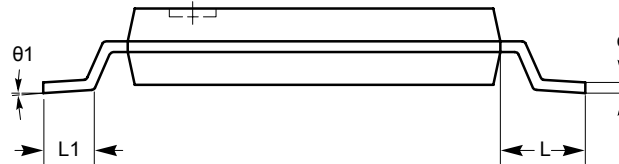


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
$\theta 1$	0°		8°



SIDE VIEW



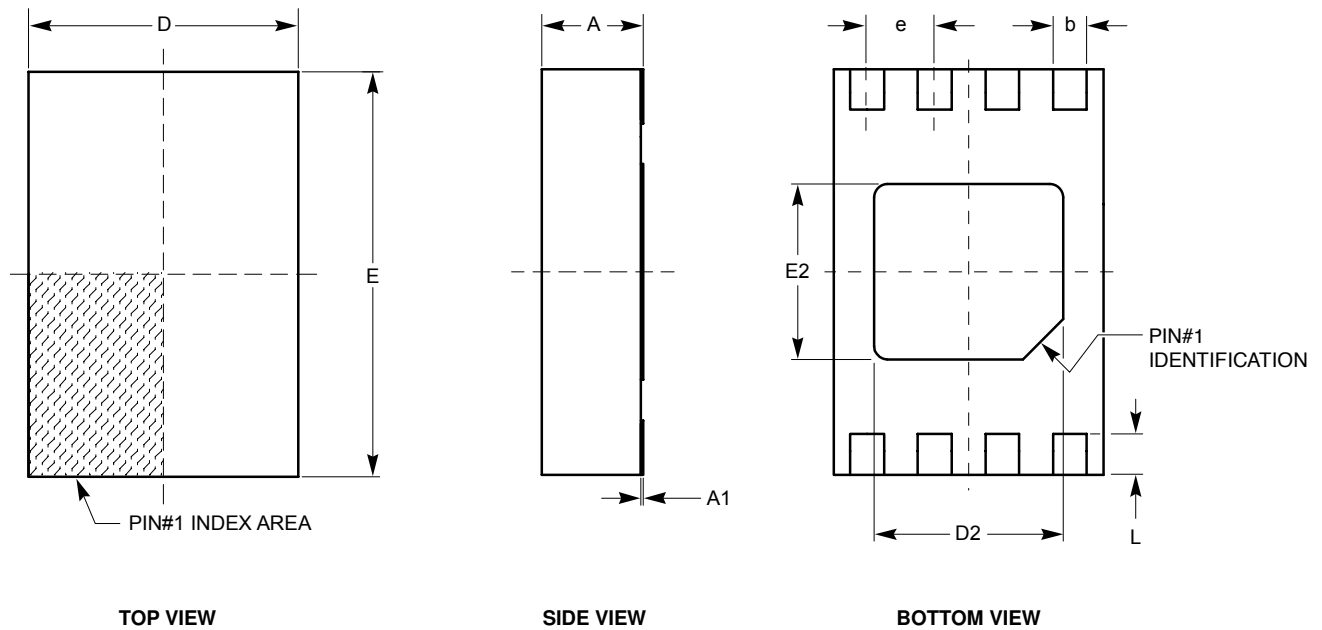
END VIEW

For current Tape and Reel information, download the PDF file from:  
<http://www.catsemi.com/documents/tapeandreel.pdf>.

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

**TDFN 8-Pad 2 x 3mm (VP2)**



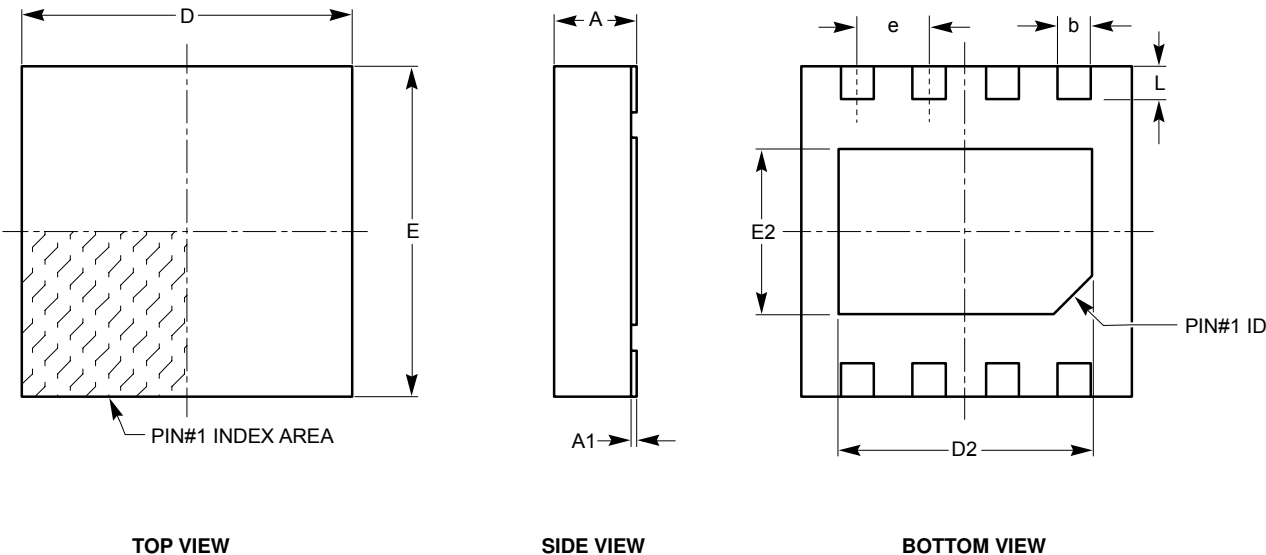
SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.45	0.55	0.65
A3	0.20 REF		
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
E	2.90	3.00	3.10
E2	1.20	1.30	1.40
e	050 TYP		
L	0.20	0.30	0.40

**For current Tape and Reel information, download the PDF file from:  
<http://www.catsemi.com/documents/tapeandreeel.pdf>.**

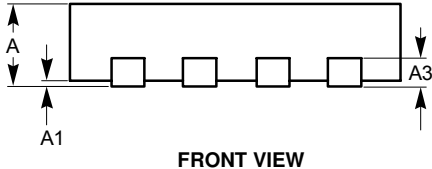
**Notes:**

- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MO-229.

TDFN 8-Pad 3 x 3mm (ZD4)



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.23	0.30	0.37
D	2.90	3.00	3.10
D2	2.20	—	2.50
E	2.90	3.00	3.10
E2	1.40	—	1.80
e	0.65 TYP		
L	0.20	0.30	0.40



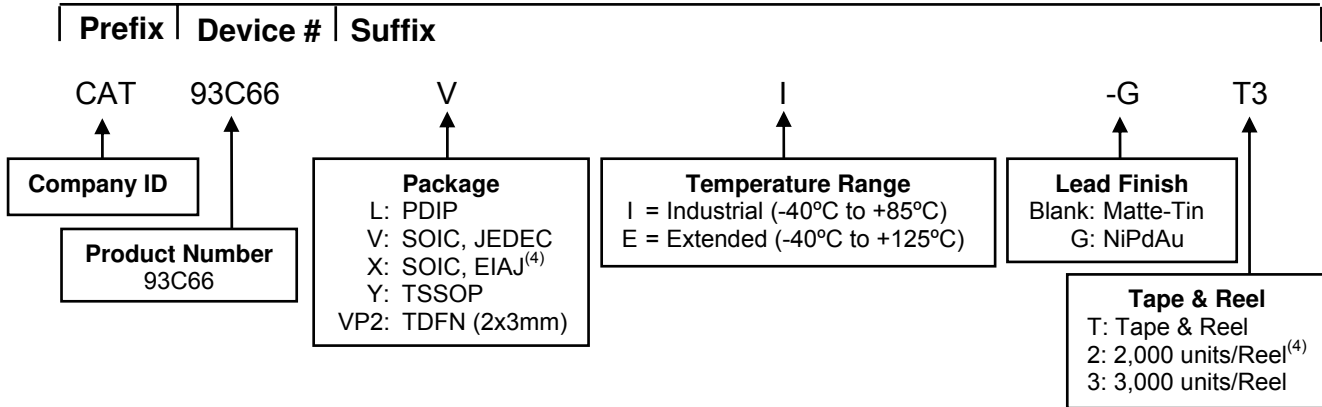
**For current Tape and Reel information, download the PDF file from:**  
<http://www.catsemi.com/documents/tapeand reel.pdf>

**Notes:**

- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MO-229.

**EXAMPLE OF ORDERING INFORMATION**

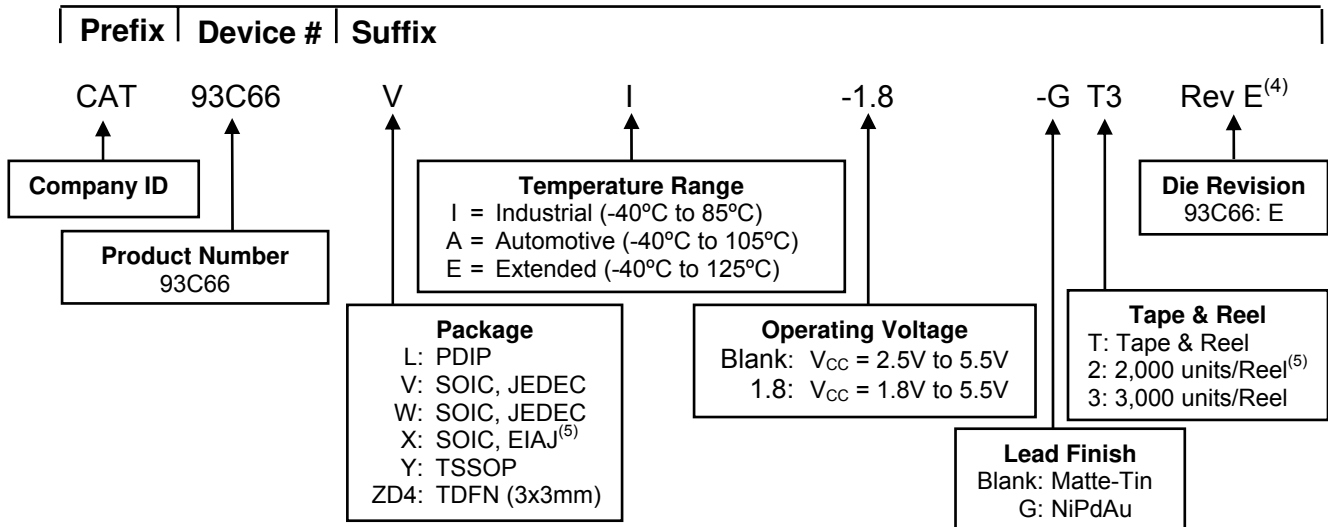
**CAT93C66, Die Rev. G (New Product)**



**Notes:**

- (1) All packages are RoHS-compliant (Lead-free, Halogen-free).
- (2) The standard lead finish is NiPdAu.
- (3) The device used in the above example is a CAT93C66VI-GT3 (SOIC, Industrial Temperature, NiPdAu, Tape & Reel, 3,000 units/Reel).
- (4) For SOIC, EIAJ (X) package the standard lead finish is Matte-Tin. This package is available in 2,000 pcs/reel, i.e. CAT93C66XI-T2.
- (5) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

**CAT93C66, Die Rev. E, Mature Product (NOT RECOMMENDED FOR NEW DESIGN)**



**Notes:**

- (1) All packages are RoHS-compliant (Lead-free, Halogen-free).
- (2) The standard finish is NiPdAu.
- (3) The device used in the above example is a CAT93C66VI-1.8-GT3 (SOIC green package, Industrial Temperature, 1.8 Volt to 5.5 Volt Operating Voltage, NiPdAu finish, Tape & Reel, 3,000 units/Reel)
- (4) Product die revision letter is marked on top of the package as a suffix to the production date code (e.g., AYWWE.) For additional information, please contact your Catalyst sales office.
- (5) For SOIC, EIAJ (X) package the standard lead finish is Matte-Tin. This package is available in 2,000 pcs/reel, i.e. CAT93C66XI-T2.
- (6) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

## REVISION HISTORY

Date	Rev.	Comments
05/14/04	L	New Data Sheet Created From CAT93C46/56/57/66/86. Parts CAT93C56, CAT93C56, CAT93C57, CAT93C66, CAT93C76 and CAT93C86 have been separated into single data sheets Add Die Revision ID Letter Update Features Update Description Update Pin Condition Add Functional Diagram Update Pin Function Update D.C. Operating Characteristics Update Pin Capacitance Update Instruction Set Update Device Operation Update Ordering Information Update Revision History Update Rev Number
10/13/06	M	Update Features Update Pin Configuration / Packages Update Functional Symbol Update Pin Functions Update D.C. Operating Characteristics ( $V_{CC}$ Range) Add Package Drawings Update Example of Ordering Information
11/17/06	N	Remove "Die Rev E" from the title Update Pin Configuration / Packages Update Absolute Maximum Rating Update Reliability Characteristics Update D.C. Operating Characteristics Added A.C. Characteristics for Die Rev G Rearrange / Format Text and Figures Added Example of Ordering Information for Die Rev G
12/07/06	O	Update separate DC Characteristics for Die Rev. G and Die Rev. E. Updated Example of Ordering Information
04/03/07	P	Update note on page 1 Update D.C. Operating Characteristics (New Product, Die Rev. G) Update Ordering Information – CAT93C66, Die Rev. G (New Product)
08/21/07	Q	Update Note on Pin Configuration Update Package Outline Drawings Update Example of Ordering Information Add MD- to document number
04/10/08	R	Add Extended Temperature Range Update Package Outline Drawings



---

*Copyrights, Trademarks and Patents*

© Catalyst Semiconductor, Inc.

Trademarks and registered trademarks of Catalyst Semiconductor include each of the following:

Adaptive Analog™, Beyond Memory™, DPP™, EZDim™, LDD™, MiniPot™, Quad-Mode™ and Quantum Charge Programmable™

I<sup>2</sup>C™ is a trademark of Philips Corporation. Catalyst Semiconductor is licensed by Philips Corporation to carry the I<sup>2</sup>C Bus Protocol.

Catalyst Semiconductor has been issued U.S. and foreign patents and has patent applications pending that protect its products.

*CATALYST SEMICONDUCTOR MAKES NO WARRANTY, REPRESENTATION OR GUARANTEE, EXPRESS OR IMPLIED, REGARDING THE SUITABILITY OF ITS PRODUCTS FOR ANY PARTICULAR PURPOSE, NOR THAT THE USE OF ITS PRODUCTS WILL NOT INFRINGE ITS INTELLECTUAL PROPERTY RIGHTS OR THE RIGHTS OF THIRD PARTIES WITH RESPECT TO ANY PARTICULAR USE OR APPLICATION AND SPECIFICALLY DISCLAIMS ANY AND ALL LIABILITY ARISING OUT OF ANY SUCH USE OR APPLICATION, INCLUDING BUT NOT LIMITED TO, CONSEQUENTIAL OR INCIDENTAL DAMAGES.*

Catalyst Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Catalyst Semiconductor product could create a situation where personal injury or death may occur.

Catalyst Semiconductor reserves the right to make changes to or discontinue any product or service described herein without notice. Products with data sheets labeled "Advance Information" or "Preliminary" and other products described herein may not be in production or offered for sale.

Catalyst Semiconductor advises customers to obtain the current version of the relevant product information before placing orders. Circuit diagrams illustrate typical semiconductor applications and may not be complete.

---



Catalyst Semiconductor, Inc.  
Corporate Headquarters  
2975 Stender Way  
Santa Clara, CA 95054  
Phone: 408.542.1000  
Fax: 408.542.1200  
www.catsemi.com

Document No: MD-1089  
Revision: R  
Issue date: 04/10/08