ZL30722

3-Input, 3-Output IEEE 1588 and SyncE Packet Clock Network Synchronizer

Product Brief

January 2016

Features

- **Packet Network Frequency and Phase Sync**
  - Frequency accuracy for GSM, WCDMA-FDD, LTE-FDD basestations and small cells
  - Frequency performance for ITU-T G.823 and G.824 synchronization interface, G.8261 PNT PEC and CES interfaces and G.8263 PEC-S-F
  - Phase synchronization performance for WCDMA-TDD, TD-SCDMA, CDMA2000, LTE-TDD and LTE-A applications
  - Client holdover and reference switching between multiple servers
  - Support for new ITU-T packet clock drafts or recs: G.8263 PEC, G.8273.2 T-BC & T-TSC w/o SyncE, and G.8273.4 T-BC-P & T-TSC-P
  - Hybrid mode for mixing SyncE and IEEE1588
- **Physical Layer Clock Synchronization**
  - ITU-T G.8262 SyncE EEC option 1 & 2
- **Low-Bandwidth DPLL**
  - Programmable bandwidth, 0.1Hz to 500Hz
  - Hitless reference switching
  - High-resolution holdover averaging
  - Numerically controlled oscillator mode
- **Input Clocks**
  - Three inputs, two differential/CMOS, one CMOS
  - Any input frequency from 8kHz to 1250MHz (8kHz to 300MHz for CMOS)
  - Per-input activity and frequency monitoring

Ordering Information

ZL30722LDG1	32 Pin QFN	Trays
ZL30722LDF1	32 Pin QFN	Tape and Reel

Matte Tin

Package size: 5 x 5 mm

-40°C to +85°C

- **Low-Jitter Fractional-N APLL and 3 Outputs**
  - Any output frequency from <1Hz to 1035MHz
  - High-resolution fractional frequency conversion with 0ppm error
  - Encapsulated design requires no external VCXO or loop filter components
  - Output jitter as low as 0.25ps RMS (12kHz-20MHz integration band)
  - Outputs are CML or 2xCMOS, can interface to LVDS, LVPECL, HSTL, SSTL and HCSL
  - Per-output supply pin with CMOS output voltages from 1.5V to 3.3V
  - Precise output alignment circuitry and per-output phase adjustment
  - Per-output enable/disable and glitchless start/stop (stop high or low)
- **General Features**
  - Automatic self-configuration at power-up from internal EEPROM; up to four configurations
  - Input-to-output alignment with external feedback
  - SPI or I^2C processor Interface
  - Easy-to-use evaluation software

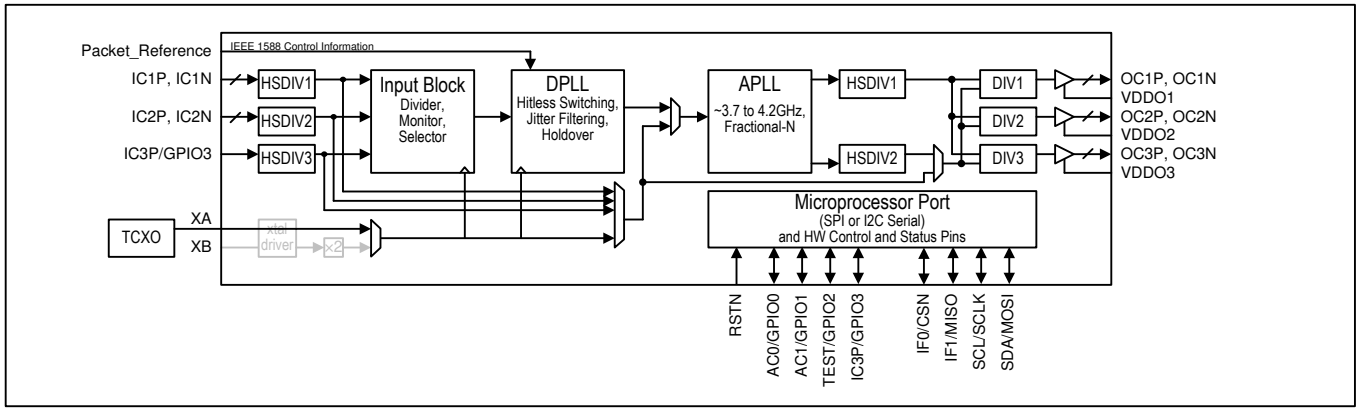

Figure 1 - Functional Block Diagram

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1. Detailed Features

1.1 Time Synchronization Algorithm

- External algorithm controls software digital PLL to adjust frequency and phase alignment
- Frequency, phase and time synchronization over IP, MPLS and Ethernet packet networks
- Frequency accuracy performance for GSM, WCDMA-FDD, LTE-FDD femtocell, small cell (residential, urban, rural, enterprise), picocell and macrocell applications, with target performance less than ±15 ppb
- Frequency performance for ITU-T G.8263 for PEC-S-F (Packet Equipment Clock - Slave - Frequency)
- Frequency performance for ITU-T G.823 and G.824 synchronization interface, as well as G.8261 PNT EEC, PNT PEC and CES interface specifications
- Phase synchronization performance for WCDMA-TDD, Mobile WiMAX, TD-SCDMA, CDMA2000, LTE-TDD and LTE-A femtocell, small cell (residential, urban, rural, enterprise), picocell and macrocell applications with target performance less than ± 1µs phase alignment.
- hase performance for ITU-T packet clock drafts or recommendations in development
  - ITU-T G.8273.2 T-BC & T-TSC, when not using SyncE input
  - ITU-T G.8273.4 T-BC-P & T-TSC-P
- Supports hybrid mode for mixing SyncE and IEEE1588 inputs
- Time Synchronization for TAI, UTC-traceability and GNSS/GPS replacement.
- Client reference switching between multiple servers
- Client holdover when server packet connectivity is lost
- Client synchronization to best server with monitoring of secondary server references

1.2 Input Clock Features

- Three input clocks, two differential or single-ended, one single-ended
- Input clocks can be any frequency from 8kHz up to 1250MHz (differential) or 300MHz (single-ended)
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN, wireless
- Inputs constantly monitored by programmable activity monitors and frequency monitors
- Fast activity monitor can disqualify the selected reference after a few missing clock cycles
- Frequency measurement and monitoring with 1ppm resolution and accept/reject hysteresis
- Optional input clock invalidation on GPIO assertion to react to LOS signals from PHYs

1.3 Electrical Clock Engine Features

- Very high-resolution DPLL architecture
- State machine automatically transitions between tracking and freerun/holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 0.1Hz to 500Hz
- Less than 0.1dB gain peaking
- Programmable phase-slope limiting
- Programmable tracking range (i.e. hold-in range)
- Truly hitless reference switching with <200ps output clock phase transient
  - Physical-clock-to-physical-clock reference switching
  - Physcial-clock-to-packet-timing reference switching
  - Packet-timing-to-physcial-clock reference switching
  - Packet-timing-to-packet-timing reference switching
- Support for SyncE and SONET/SDH equipment clock specifications
  - ITU-T G.8262 option 1 EEC
  - ITU-T G.8262 option 2
  - ITU-T G.813 option 1 SEC
  - IUT-T G.813 option 2
- Output phase adjustment in 10ps steps
- High-resolution frequency and phase measurement
- Fast detection of input clock failure and transition to holdover mode
- Holdover frequency averaging with programmable averaging time and delay time

1.4 APLL Features

- Very high-resolution fractional scaling (i.e. non-integer multiplication)
- Any-to-any frequency conversion with 0ppm error
- Two high-speed dividers (integers 4 to 15, half divides 4.5 to 7.5)
- Easy-to-configure, completely encapsulated design requires no external VCXO or loop filter components
- Bypass mode supports system testing

1.5 Output Clock Features

- Three low-jitter output clocks
- Each output can be one differential output or two CMOS outputs
- Output clocks can be any frequency from 1Hz to 1035MHz (250MHz max for CMOS and HSTL outputs)
- Output jitter as low as 0.25ps RMS (12kHz to 20MHz)
- In CMOS mode, an additional divider allows the OCxN pin to be an integer divisor of the OCxP pin (Example 1: OC3P 125MHz, OC3N 25MHz. Example 2: OC2P 25MHz, OC2N 1Hz)
- Outputs easily interface with CML, LVDS, LVPECL, HSTL, SSTL, HCSL and CMOS components
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN
- Sophisticated output-to-output phase alignment
- Per-output phase adjustment with high resolution and unlimited range
- Per-output enable/disable
- Per-output glitchless start/stop (stop high or low)

1.6 General Features

- SPI or I^2C serial microprocessor interface
- Automatic self-configuration at power-up from internal EEPROM memory; pin control to specify one of four stored configurations
- Numerically controlled oscillator (NCO) behavior allows system software to steer DPLL frequency with resolution better than 0.01ppb
- Input-to-output alignment with external feedback
- Four general-purpose I/O pins each with many possible status and control options
- Output frame sync signals: 2kHz or 8kHz (SONET/SDH), 1Hz (IEEE 1588) or other frequency
- Internal compensation for local oscillator frequency error

1.7 API Software

- Interfaces to 1588-capable PHYs and switches with integrated timestamping
- Abstraction layer for independence from OS and CPU, from embedded SoC to home-grown
- Fits into centralized, highly integrated “pizza box” architectures as well as distributed architectures with multiple line cards and timing cards

2. Applications

- ITU-T G.8262 system timing cards for Synchronous Ethernet systems
- System timing cards which support ITU-T G.781 SETS (SDH Equipment Timing Source)
- Integrated basestation reference synchronization for air interfaces for
  - GSM, WCDMA, TD-SCDMA, LTE and LTE-A
  - FDD or TDD mobile technology
  - Femtocells, small cells (residential, urban, rural, enterprise), picocells and macrocells
- Mobile Backhaul NID, cell-site router, edge switch/router, microwave or access aggregation node
- EPON/GPON OLT and ONU/ONT
- DSLAM and RT-DSLAM
- 10G, 40G and 100G line cards
- SONET/SDH, Fibre Channel, XAUI

3. Pin Diagram

The device is packaged in a 5x5mm 32-pin QFN.

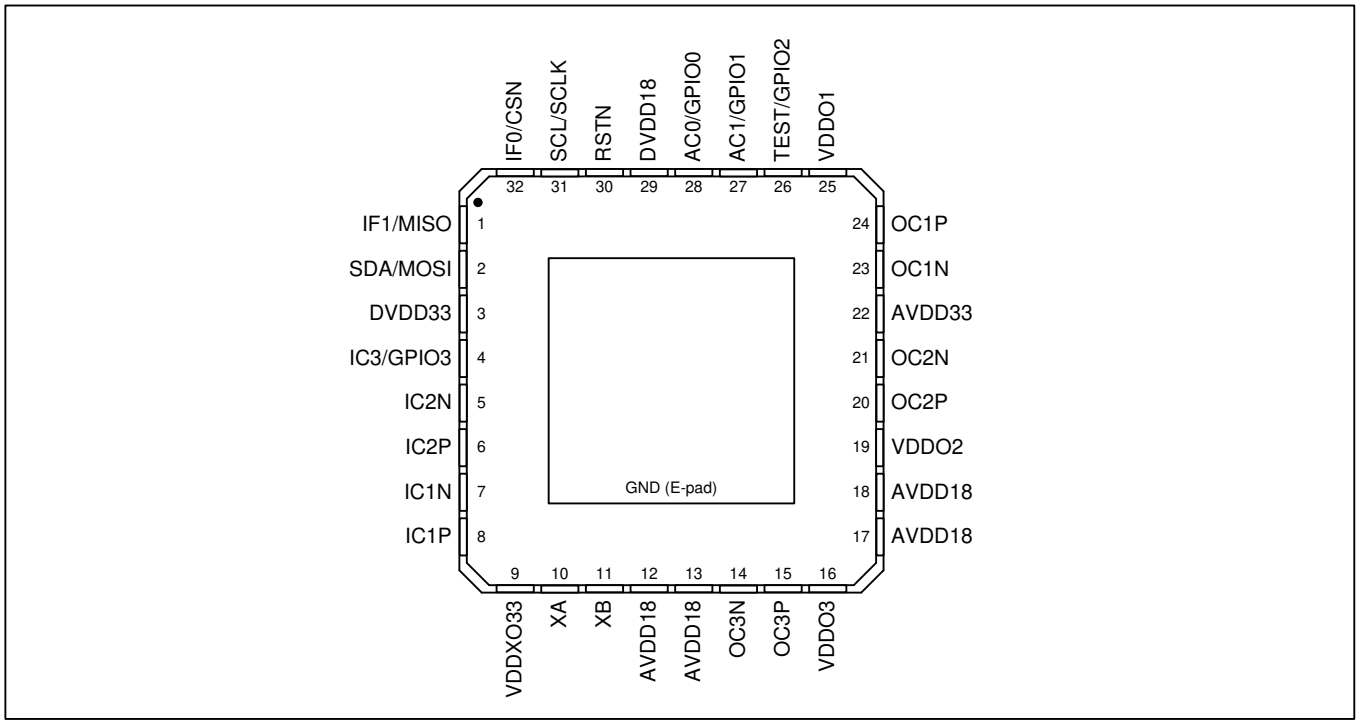

Figure 2 - Pin Diagram

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