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PICOCAP®

Data Sheet

PCapØ2A

Single-chip Solution for Capacitance Measurement
Volume 1: General Data and Front-end Description

May 29, 2014, Version 1.6
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Content

1 Overview

PCapØ2Y is a capacitance-to-digital converter (CDC) with integrated digital signal processor (DSP) for on-chip data post-processing. Its front end is based on acam's patented **PICO**CAP® principle. This conversion principle offers outstanding flexibility with respect to power consumption, resolution and speed. This datasheet describes PCapØ2A, in its basic converter functionality. The DSP description is reduced to the standard firmware that calculates pure capacitance ratios. A detailed DSP and memory description is given in datasheet volume 2. PCapØ2 can be used for single and differential sensors in grounded and floating application. Compensation of internal and external stray capacitance is implemented as well as for parallel resistance. Additionally, the temperature can be measured by means of internal thermistors or external sensors.

1.1 Features

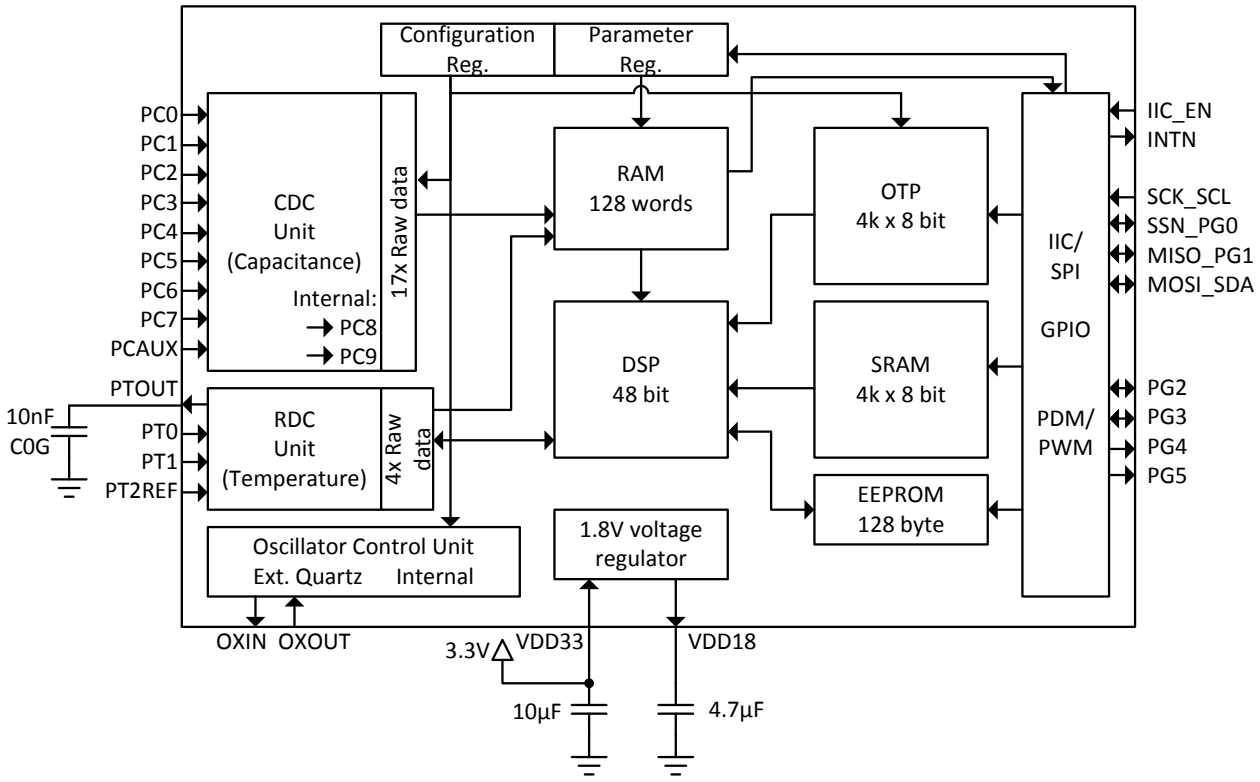
- Digital measuring principle in CMOS technology
- Up to 8 capacitances in grounded mode
- Up to 4 capacitances in floating mode (potential- free and with zero bias voltage)
- Integrated reference capacitance 1 pF to 31 pF
- Integrated discharge resistors up to 1 MOhm
- Compensation of internal (grounded) and external parasitic capacities (floating)
- Pre-charge option for slow charging
- Self-test capability for differential sensors
- High resolution: up to 15 aF at 2.5 Hz and 10 pF base capacitance or, 17 bit resolution at 5 Hz with 100 pF base capacitance and 10 pF excitation
- High measurement rate: up to 500 kHz
- Extremely low current consumption possible: Down to 2.5 µA at 2.5 Hz with 13.1 bit resolution
- High stability with temperature, low offset drift (down to 20 aF per Kelvin), low gain drift when all compensation options are activated.
- Dedicated ports for precision temperature measurement (with Pt1000 sensors, the resolution is 0.005 K)
- Serial interface (SPI or IIC compatible)
- Two 10/12/14/16 bit PDM/PWM outputs for analog interfaces
- Self-boot capability
- Single power supply (2.1 to 3.6 V), integrated 1.8 V regulator for improved PSRR.
- Integrated voltage measurement
- No need for a clock
- RISC processor core using Harvard architecture:
- 128 x 48/24 bit RAM Data (80x48 free)
- 4k x 8 bit SRAM program memory for high-speed operation (40 to 85 MHz)
- 4k (+4k for ECC)x 8 bit OTP (one-time programmable) program memory for normal speed operation (up to 40 MHz)
- 128 byte EEPROM for calibration data and user data (serial number etc.)

1.2 Applications

- Humidity sensors
- Position sensors
- Pressure sensors
- Force sensors
- Acceleration sensors
- Inclination sensors
- Tilt sensors
- Angle sensors
- Wireless applications
- Level sensors
- Microphones
- MEMS sensors

1.3 Blockdiagram

Figure 1-1 Blockdiagram



2 Characteristics & Specifications

2.1 Electrical Characteristics

2.1.1 Absolute Maximum Ratings

Supply voltage V_{DD}-to-GND	- 0.3 to 4.0 V
Storage temperature Tstg	- 55 to 150 °C
ESD rating (HBM), each pin	> 2 kV
Junction temperature (Tj)	max. 125 °C
OTP Data Retention Period	10 years at 95 °C temperature
EEPROM Data Retention Period	10 years at 95 °C temperature

2.1.2 Recommended Operating Conditions

Table 2-1 Operating conditions

Quantity	Symbol	Remarks	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		2.1		3.6	V
Digital port voltage	$V_{io\_digital}$	Relative to ground	- 0.6	3.3	V_{DD} +0.6 ≤ 3.6	V
Digital ports switching level		HIGH → LOW LOW → HIGH		0.3 * V_{DD} 0.7 * V_{DD}		
Analog port voltage	V_{io_analog}		- 0.6		V_{DD} +0.6 ≤ 3.6	V
OTP Programming voltage	V_{OTP}	Between "VPP_OTP" port and ground. Do not expose other ports to programming voltage.		6.5	7.0	V
SPI bus frequency	$f_{SPI\text{-}bus}$	Clock frequency for the 4-wire SPI bus operation	0		20	MHz
I²C bus frequency		Speed (data rate) of the 2-wire I²C bus operation	0		100	kHz
OTP Bit hold time		Bit hold time for OTP write	30		500	µs
GPIO input rise time		Rise time of the input signal put to general-purpose I/O			500	ns
GPIO output rise time		Rise time of the output signal from a general-purpose I/O		6	t.b.d.	ns
CDC discharge time		MR1	0		40	µs

RDC discharge time			0		100	µs
Junction Temperature	T_j	Junction temperature must not exceed +125 °C	- 40		+ 125	°C
Ambient Temperature	T_a	At VDD = 2.4V -/+ 0.3V	- 40		+ 125	°C

2.2 CDC Precision

2.2.1 RMS Noise and Resolution vs. Output Data Rate

Table 2-2 Typical capacitive noise & resolution vs. output data rate, 10 pF base + 1 pF span, fast settle, MR1, V = 3.0 V

Output Data Rate [Hz]	FLOATING Fully compensated			GROUNDED Internally compensated		
	RMS Noise [aF]	Eff. Resolution 10 pF base [Bits]	Eff. Resolution 1 pF span [Bits]	RMS Noise [aF]	Eff. Resolution 10 pF base [Bits]	Eff. Resolution 1 pF span [Bits]
2.5	15	19.3	16.0			
5	23	18.7	15.4	15	19.3	16.0
10	35	18.1	14.8	23	18.7	15.4
25	48	17.7	14.4	50	17.6	14.3
100	134	16.2	12.9	81	16.9	13.6
250	172	15.8	12.5	116	16.4	13.1
1,000	330	14.9	11.6	147	16.0	12.7
2,000	438	14.5	11.2	230	15.4	12.1
4,000	603	14.0	10.7	327	14.9	11.6
10,000	838	13.5	10.2	566	14.1	10.8
25,000				817	13.6	10.3

The table gives the root mean-square (RMS) noise in aF as a function of output data rate in Hz, measured at 3.0 V supply voltage using the maximum possible sample size for in-chip averaging at the minimum possible cycle time. Bit values are calculated as a binary logarithm of noise over the span (BITs = ln(span/noise)/ln(2)). The measurements have been done with the PCapØ2 evaluation board, with fixed COG ceramic capacitors.

Both, sensor and reference are connected “floating” or “grounded”, as indicated. When floating, compensation mechanisms for both internal and external stray capacitances are activated, when grounded, internal ones only.

2.2.2 RMS Noise vs. Supply Voltage

Figure x RMS Noise vs. Supply Voltage – to follow

Note: Buffer capacitors of sufficient capacitance are mandatory for good measurement quality. We recommend to use minimum 10 µF COG for VDD33 and 4.7 µF for VDD18_OUT.

2.2.3 Voltage-Dependent Offset and Gain Error (PSRR)

Figure x Gain Error in % vs. Supply Voltage (Power Supply Rejection Ratio) – to follow

2.2.4 Temperature-Dependent Offset and Gain Error

Values typical at 3V:

Gain drift: 10 ppm / K
Offset drift: 20 aF / K

Gain and offset drift have been determined with a 10 pF base capacitance (COG), both reference and sensor, connected in floating mode. Temperature range was from -20°C to +60°C.

2.3 RDC Precision

Table 2-3 Thermoresistive coefficients Tk at 20 °C

Material	Tk
Internal poly-silicon reference	-1.1 ppm/K
Internal aluminum thermistor	2830 ppm/K
External PT1000 sensor	3830 ppm/K

Table 2-4 Noise with internal Al/PolySi at 20 °C

Measurement Conditions	R2/Rref typ.	RMS noise R2/Rref	Typical RMS noise (*) Temperature
No averaging, 2 fake measurements	0.825	50 ppm	25 mK
16-fold averaging, 8 fake measurements	0.823	10 ppm	5 mK

(*) after linearization in post-processing software

Linearity error internal temperature sensor: typ. 100mK

2.4 Oscillators

2.4.1 Internal RC-Oscillator

The integrated RC-Oscillator can be set in the range between 10 kHz and 200 kHz, in which 50 kHz is the standard setting (see Register 3 description) and section 5.3.

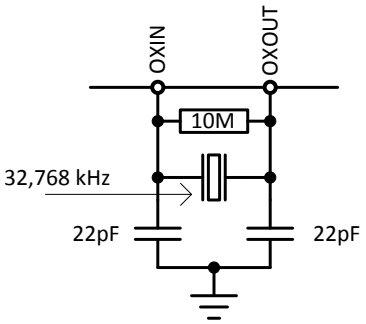
The nominal frequency e.g. 50 kHz has a standard deviation of +/-20 % over parts.

More than that, the internal oscillator depends on voltage and temperature.

2.4.2 External Oscillators

Alternatively, the PCapØ2 can be operated with a precise and stable clock by applying an external 32.768 kHz quartz oscillator. Further, the PDM outputs provide a precise frequency-modulated signal for a measured value (e.g., humidity or pressure). The frequency range is set by the offset and slope in the parameter registers.

Figure 2-1

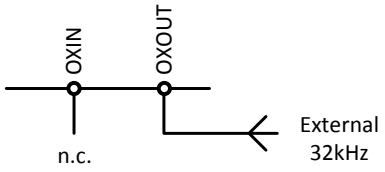


Configuration:

OX_CLK32KHZ_EN = 1	Register 3, Bit[1]	
OX_DIS = 1	Register 4, Bit[7]	(disable the OX clock)
OX_AMP_TRIM = 0	Register 4, Bit[6]	(only relevant for 4 MHz)
OHF_CLK_SEL = 4	Register 6, Bit[2:0]	(external OX)
OX_AUTOSTOP_DIS = 1	Register 4, Bit[4]	
OX_RUN = 1	Register 4, Bit[2:0]	(permanent)

It is also possible to provide an external low-frequency square wave clock signal at the OXOUT pin (3.6 V max.). Pin OXIN has to be connected to GND.

Figure 2-2



2.5 Power Consumption

Table 2-5 Total current I [µA] as a function of conversion rate (CONV_TIME) and resolution (C_AVRG) in triggered mode

OLF Freq. [kHz]	CONV_ TIME	Measure rate [Hz]	I [µA] C_AVRG (RMS resolution [Bits])					
			1	4	16	64	256	1024
			13.1	14.2	15.1	16.0	16.6	17.5
50	10000	2.5	2.5	2.7	2.9	3.9	8.5	33
50	2500	10	3.1	3.3	3.7	8.3	20	32
50	1250	20	3.9	5	7	15	26	
50	625	40	5.6	7	11	29		
50	250	100	11	13	24			
50	125	200	19	27				
50	50	500	43	57				
50	25	1000	84					
50	12	2080	172					
200	24	4160	348					
200	12	9320	689					

Temperature measurement in addition to capacitive measurement will add between 2 and 10 µA approximately, depending on speed. Total consumption values below 30 µA may be obtained only when driving the on-chip 1.8 volts core supply generator in an energy-saving mode; ultimate microampere savings also demand to slow down the DSP.

2.6 Package Information

2.6.1 Dice - Pad Layout

Die dimensions: 2.01 mm x 2.01 mm with pad pitch 120 µm, pad opening is 85 µm x 85 µm, Thickness 290 µm.

Figure 2-3 Pad positions on die

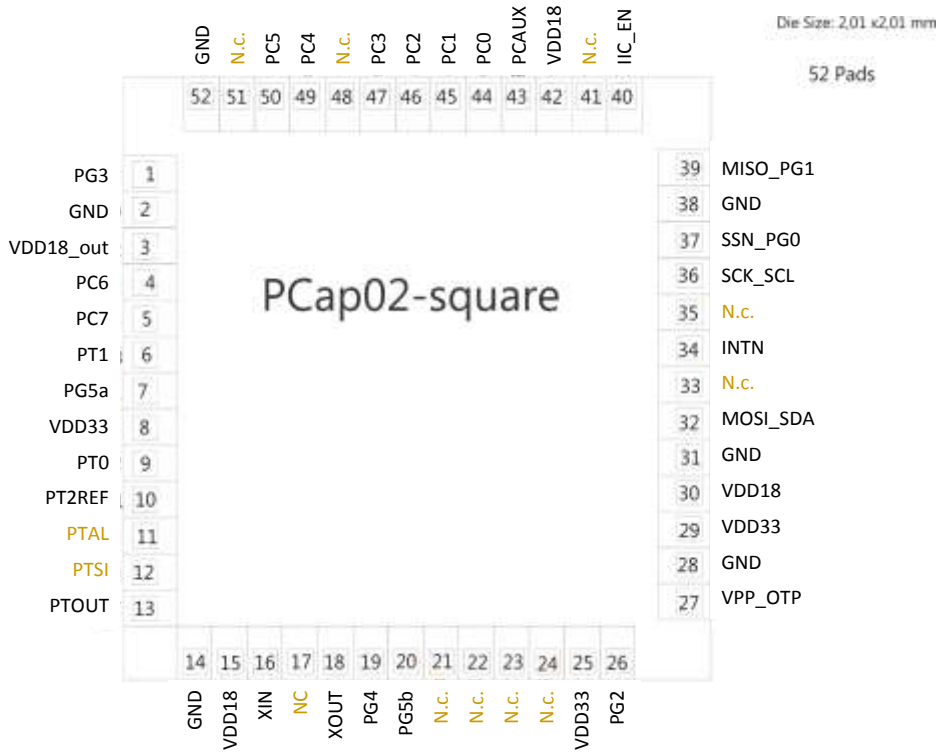


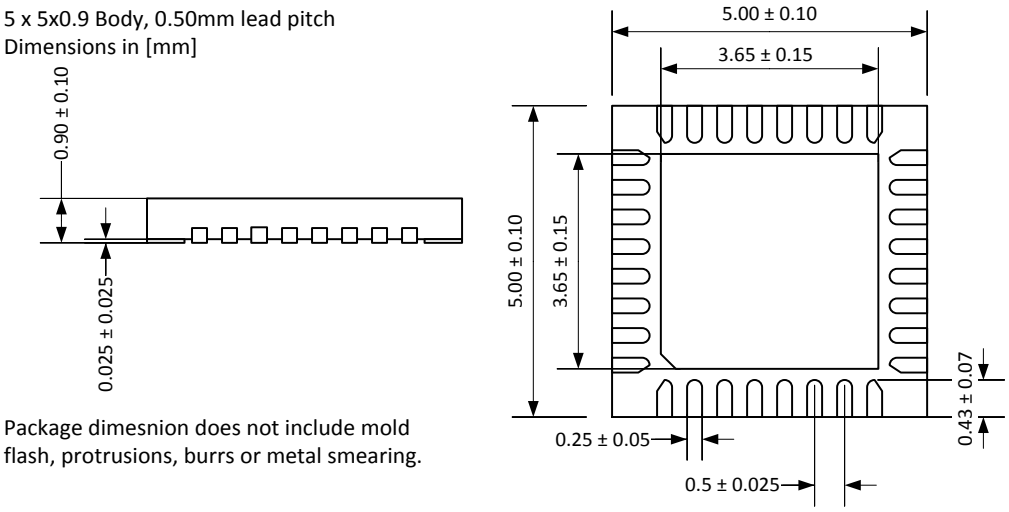
Table 2-6 Pad description

Pad	Name	X-Pos(µm)	Y-Pos(µm)	Type
1	PG3	44.5	1680.0	
2	GND	44.5	1560.0	
3	VDD18_out	44.5	1440.0	
4	PC6	44.5	1320.0	
5	PC7	44.5	1200.0	
6	PT1	44.5	1080.0	
7	PG5a	44.5	960.0	
8	VDD33	44.5	840.0	
9	PT0	44.5	720.0	
10	PT2REF	44.5	600.0	
11	PTAL	no pad	no pad	
12	PTSI	no pad	no pad	
13	PTOUT	44.5	240.0	
14	GND	270.0	44.5	
15	VDD18	390.0	44.5	
16	XIN	510.0	44.5	
17	n.c.	no pad	no pad	

Pad	Name	X-Pos(µm)	Y-Pos(µm)	Type
18	XOUT	750.0	44.5	
19	PG4	870.0	44.5	
20	PG5	990.0	44.5	
21	TEST0	1170.0	44.5	
22	TEST1	1290.0	44.5	
23	TEST2	1410.0	44.5	
24	TEST3	1530.0	44.5	
25	VDD33	1650.0	44.5	
26	PG2	1770.0	44.5	
27	VPP_OTP	1965.5	240.0	
28	GND	1965.5	360.0	
29	VDD33	1965.5	480.0	
30	VDD18	1965.5	600.0	
31	GND	1965.5	720.0	
32	MOSI_SDA	1965.5	840.0	
33	TEST4	1965.5	960.0	
34	INTN	1965.5	1080.0	
35	TEST5	1965.5	1200.0	
36	SCK_SCL	1965.5	1320.0	
37	SSN_PG0	1965.5	1440.0	
38	GND	1965.5	1560.0	
39	MISO_PG1	1965.5	1680.0	
40	IIC_EN	1770.0	1965.5	
41	TEST6	1650.0	1965.5	
42	VDD18	1530.0	1965.5	
43	PCAUX	1350.0	1965.5	
44	PC0	1230.0	1965.5	
45	PC1	1110.0	1965.5	
46	PC2	990.0	1965.5	
47	PC3	870.0	1965.5	
48	TTES7	750.0	1965.5	
49	PC4	630.0	1965.5	
50	PC5	510.0	1965.5	
51	TEST8	390.0	1965.5	
52	GND	270.0	1965.5	

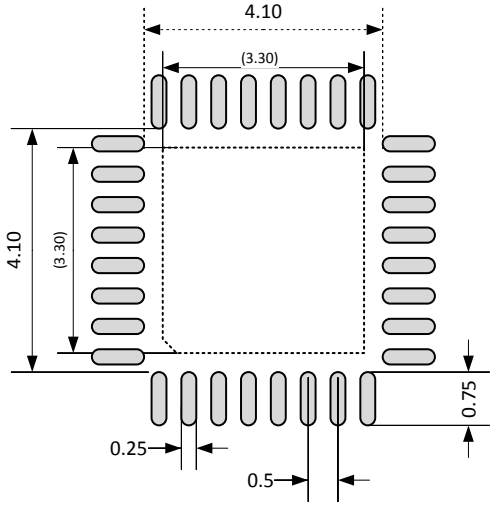
2.7 QFN Packages

Figure 2-4 QFN32 package dimensions



Dimensioning and tolerances acc. to ASME Y14.5M-1994

Landing pattern (dimensions in [mm]):



Caution: Center pad is internally connected to GND. No wires other than GND are allowed underneath.

It is recommended to not use the center pad. Too much solder paste could reduce solder quality.

Suitable socket:

e.g. Plastronics 32QN50S15050D

Thermal resistance: Roughly 28 K/W (value just for reference).

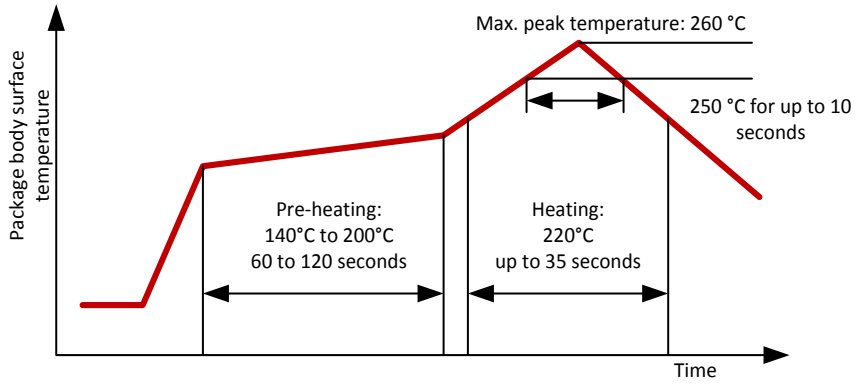
Environmental: The package is RoHS compliant and does not contain any critical materials according to REACH regulation (EG) No. 1907/2006.

Moisture Sensitive Level (MSL): Based on JEDEC 020 Moisture Sensitivity Level definition the PCapØ2 is classified as MSL 3.

Soldering Temperature Profile

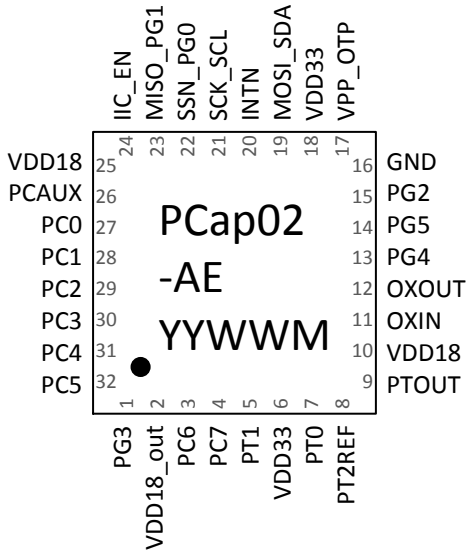
The temperature profile for infrared reflow furnace (in which the temperature is the resin's surface temperature) should be maintained within the range described below.

Figure 2-8: Soldering profile



2.7.1 Pin-Out QFN32

Figure 2-5 QFN32 Pin-out



The center pad on the bottom of the QFN package is internally connected to GND.

Connecting to ground on the PCB is not mandatory, and for reliable soldering it should not be connected.

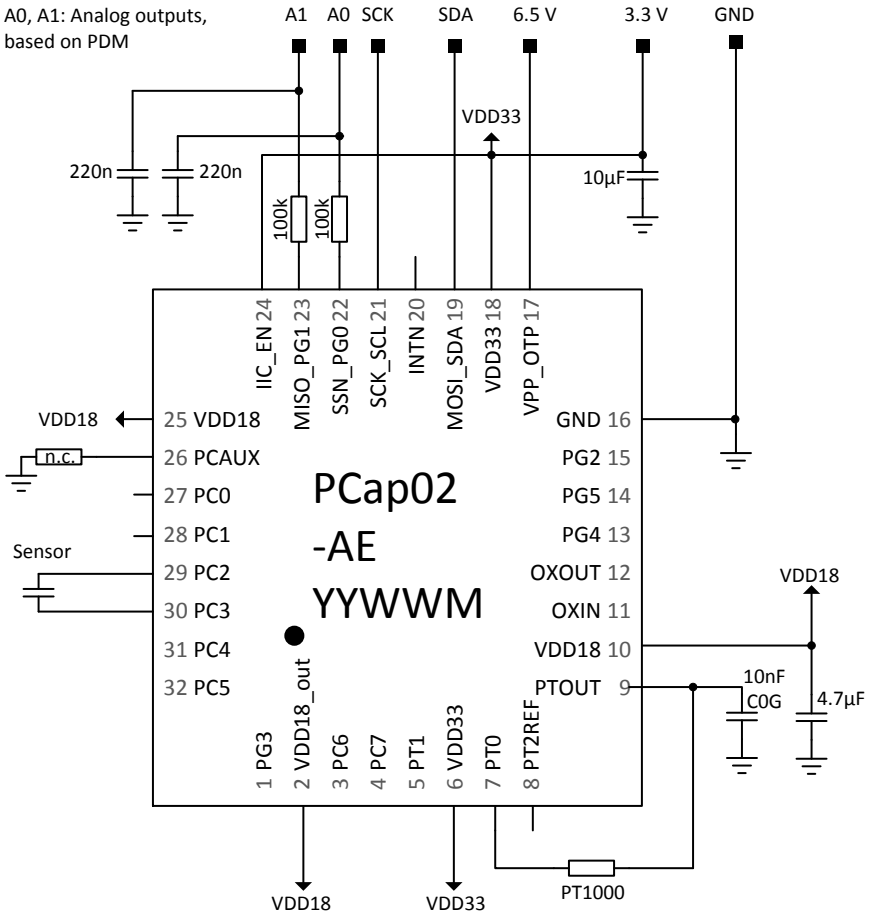
2.7.3 Pin/Pad Assignment

Table 2-7 Pin Description

Pin	Description	Comment	Pin#
PG3	General purpose I/O port		1
VDD18_out			2
PC6	Capacitance port		3
PC7	Capacitance port		4
PT1	Resistance port (temperature sensor)		5
VDD33			6
PT0	Resistance port (temperature sensor)		7
PT2REF	Resistance port (temp. sensor, refer.)		8
PTOUT	Port to connect 10 nF discharge capacitor for resistance measurement		9
VDD18			10
OXIN	Oscillator port		11
OXOUT	Oscillator port		12
PG4	General purpose I/O port		13
PG5	General purpose I/O port		14
PG2	General purpose I/O port		15
GND			16
VPP_OTP			17
VDD33			18
MOSI_SDA	Master out/Slave in when SPI is used. Otherwise, Serial data out for IIC		19
INTN	Interrupt, Low active		20
SCK_SCL	Serial clock for SPI/IIC		21
SSN_PG0	Serial Select Line (Serial reset). Otherwise, general purpose I/O port		22
MISO_PG1	Master in/Slave out when SPI is used. Otherwise, general purpose I/O port		23
IIC_EN	0 = SPI enable, 1 = IIC enable		24
VDD18			25
PCAUX	Capacitance port		26
PC0	Capacitance measurement port		27
PC1	Capacitance measurement port		28
PC2	Capacitance measurement port		29
PC3	Capacitance measurement port		30
PC4	Capacitance measurement port		31
PC5	Capacitance measurement port		32

2.7.4 Typical Schematics

Figure 2-6 Typical schematics, I²C interface, internal references.



3 Converter Frontend

The device uses “discharge time measurement” as a principle for measuring either capacitance (CDC unit) or resistance (RDC unit). It addresses all ports (PC...,PT...) in time multiplex, CDC and RDC measurements possibly running in parallel. The time measurement is done by means of a high-resolution TDC (time-to-digital converter).

3.1 CDC, Capacitance-to-Digital Converter

3.1.1 Measuring Principle

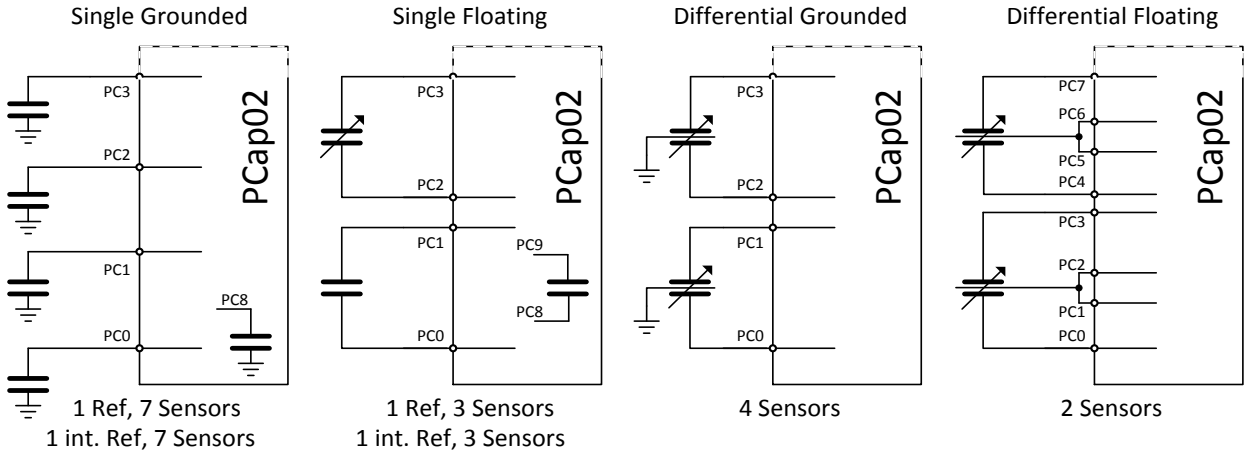
In PCapØ2 capacitance measurement is done by measuring discharge times of RC-networks. The measurements are radiometric. This means the capacitors are compared to a fixed reference or, like in differential sensors, to capacitors with change in opposite direction. Thanks to the short time intervals and special compensation methods, the ratio of discharge times is directly proportional to the ratio of capacitors. The discharge time is defined by the capacitor and the selected discharge resistor.

$$\frac{\tau_N}{\tau_{ref}} = \frac{C_N}{C_{ref}} \qquad \tau = k * R * C$$

3.1.2 Connecting Sensors

PCapØ2 can handle single and differential sensors in grounded or floating connection. Additionally to the known PCapØ1 options, PCapØ2 has integrated reference capacitors. Those can be used with single sensors. They are programmable in a range from 1 to 31pF in steps of 1 pF.

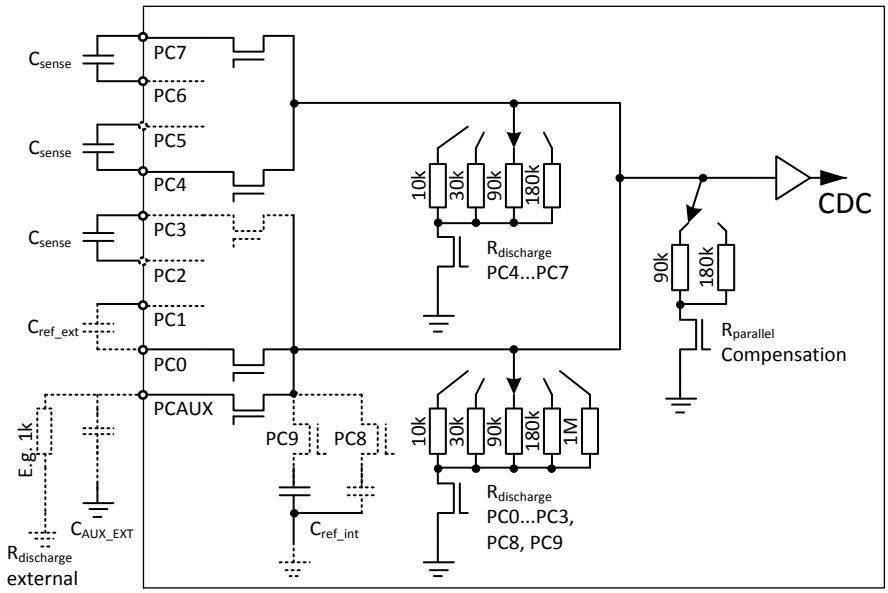
Figure 3-1 Connecting sensors



3.1.3 Discharge Resistors

The PCapØ2A has two sets of discharge resistors already integrated. One resistor set (10k, 30k, 90k, 180k, 1000k) is for measurements on port PC0 to PC3 and the internal reference ports PC8 and PC9. The other resistor set (10k, 30k, 90k, 180k) is for ports PC4 to PC7. This way, it is possible to measure different sensors with strongly deviated capacitance like pressure and humidity with one and the same chip. The resistors are selected by parameters RCHG_xxx.

Figure 3-2 Integrated discharge resistors



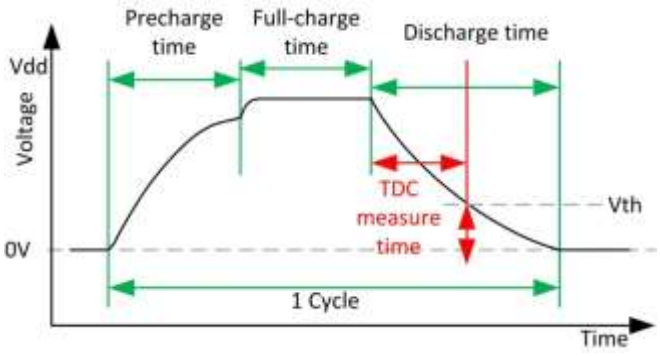
Some applications like humidity sensors may demand a very slow discharge. For this reason the 1 MOhm discharge resistor is integrated. It is selected by RDCHG_1MEG_EN.

For big capacitances there is the possibility to use an external discharge resistor.

3.1.4 Cycle

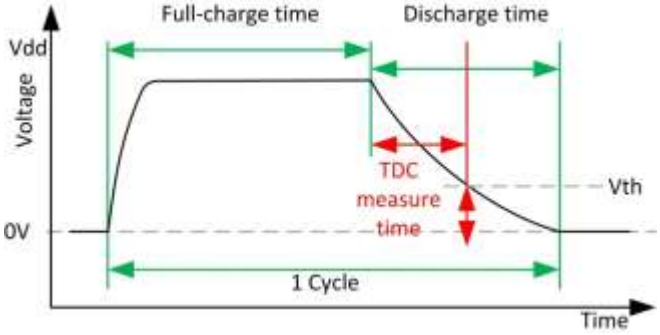
In PCapØ2 the measuring principle was greatly improved by introducing a pre-charge phase. In the very first step, the capacitor is charged up via a series resistor to a level close to Vdd. The resistor reduces the charge current and reduces the mechanical stress on the sensing capacitor. This can be necessary in some MEMS applications. In a second step, the capacitor is charged up finally to Vdd without a series resistor. Then, in the third step, the capacitor is discharged via the discharge resistor down to OV. The CDC measures the time interval until a trigger level is reached. All this is called a single “cycle”.

Figure 3-3 Single Cycle Timing



In applications that don't need the slow charge up but high conversion rate, it is possible to disable the pre-charge option and to start charge up directly without any series resistor.

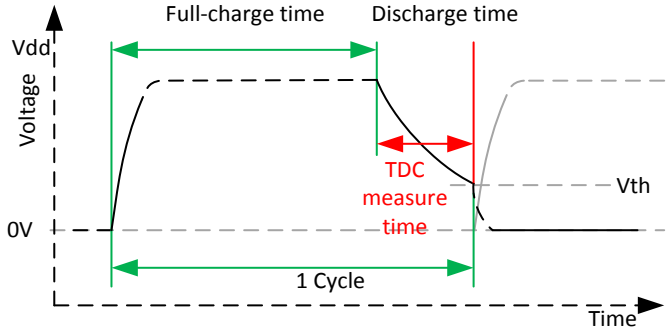
Figure 3-4 Single Cycle, fast charge



In both cases the capacitors are discharged for the full discharge time period and then connected to GND.

Finally, there is an option to operate the chip in PCapØ1 compatible mode. This means, as soon as the trigger level of the discharge time measurement is reached, the current port is immediately connected to GND and the next port will be charged up to Vdd.

Figure 3-5 Single Cycle, PCapØ1compatible



3.1.5 Sequence

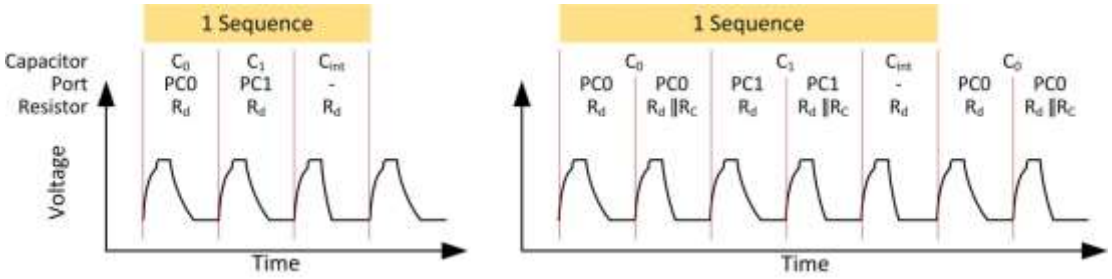
A "sequence" is made of a set of cycles, namely those for the various active ports as well as combinations of them as given by the compensation measurements. The number and kind of single cycles depends on the way of connecting the sensors, the number of capacitors and the selected compensation options.

For **grounded** sensors, the sequence starts always with PCO (reference) and then one or more of the other 7 ports. Normally, internal compensation is activated. So the sequence ends with the measurement C_{int} of the internal stray capacitance/delays. For compensating internal parasitic capacitance and the comparator delay the CDC measures the discharge time with all ports being off (C_{int}).

For compensating parallel resistances to the capacitors, the CDC measures the discharge time for each capacitor a second time.

The following figure shows the sequence for a grounded sensor with internal compensation and in case of parallel resistance compensation.

Figure 3-6 Sequence for 1 reference & 1 sensor in grounded connection, compensated for internal capacitance, and – one the right side – compensation for parallel resistances



For **floating** sensors, the sequence starts always with PCO/PC1 (reference), followed by one to three pairs of ports for the sensors. Normally, full compensation (internal and external) is activated.

For compensation of external parasitic capacitances the CDC makes a measurement for each capacitor with both ports being opened. So, for each capacitor 3 measurements are made, e.g. PCO, PC1 and PCO+PC1. In case of parallel-resistance compensation there are 5 measurements for each capacitor. The sequence ends with the internal compensation measurement C_{int}. The following figures show the sequence for 1 floating sensor with full compensation.

Figure 3-7 Sequence for 1 reference & 1 sensor in floating connection, fully compensated for parasitic capacitances

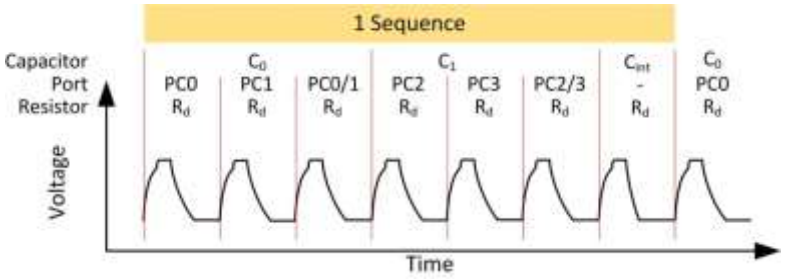
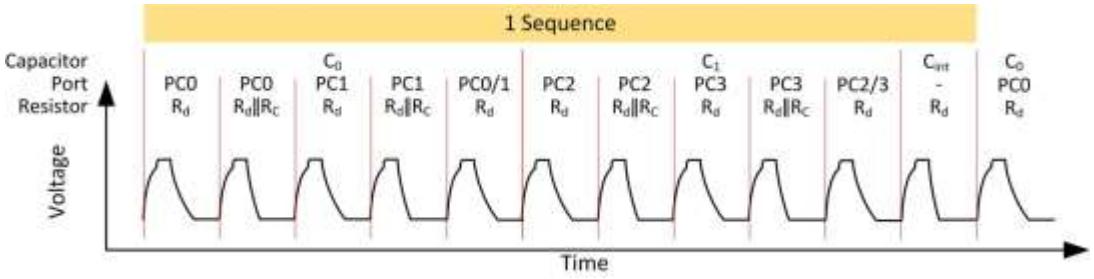


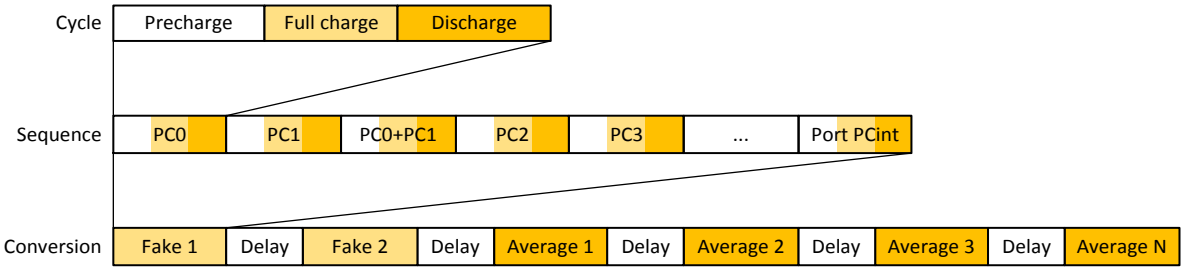
Figure 3-8 Sequence for 1 reference & 1 sensor in grounded connection, fully compensated for parasitic capacitances and for parallel resistances



3.1.6 Conversion

Finally, the combination of various sequences and delays in between the sequences define a single “conversion”. At the end of a conversion the measurement results are ready for further processing and readout. The end of the conversion is indicated by flag to the DSP and also the RDC unit.

Figure 3-9 Cycle – Sequence – Conversion



A conversion is triggered from outside the CDC unit:

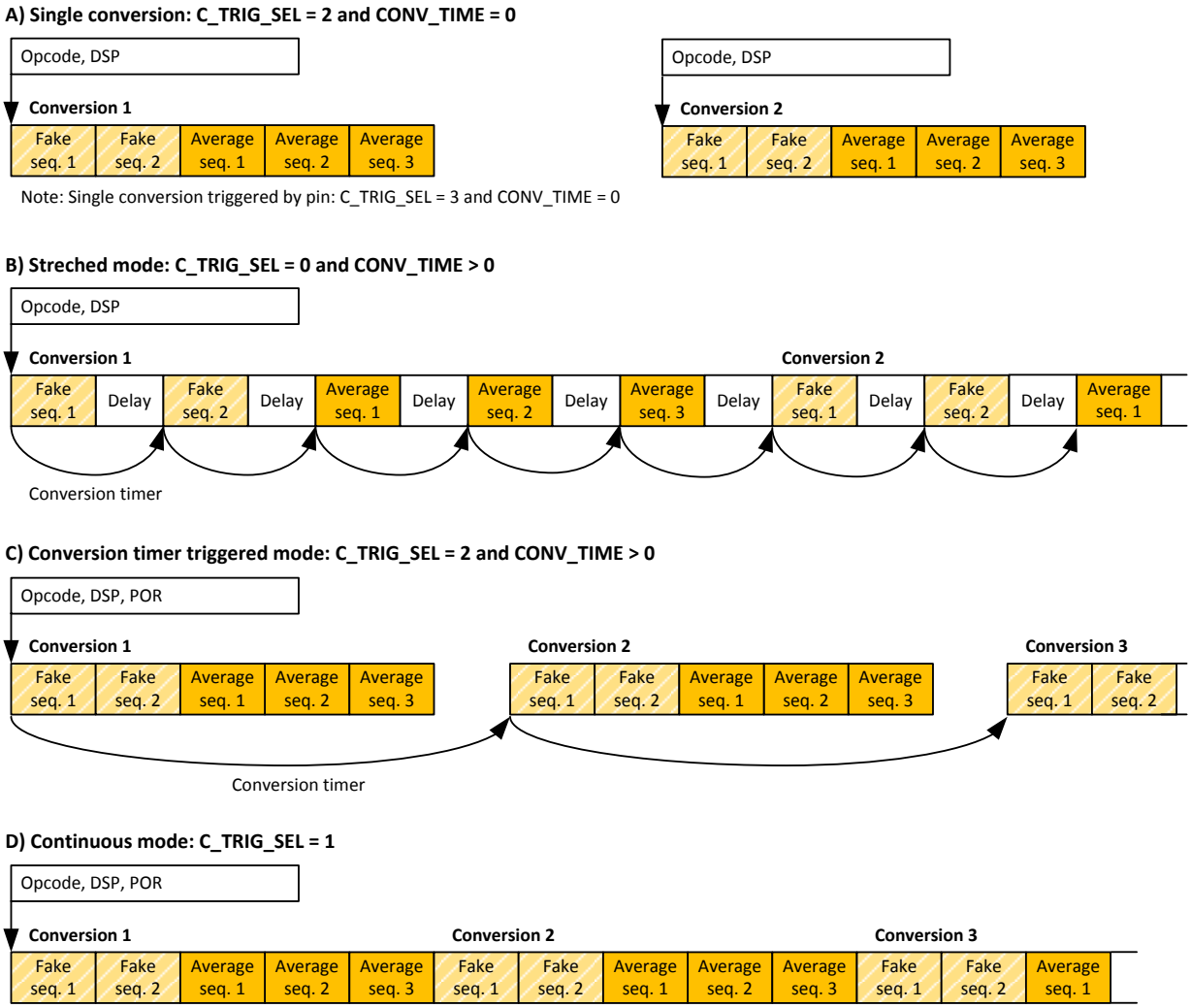
- By the conversion timer
- Pin triggered
- By the DSP
- By serial interface (opcode).

Once triggered, a conversion is automatically completed, including all fake measurements and all real measurements defined by sample size for averaging. The end of the conversion is indicated to the master (DSP, timer, µP).

The way conversions follow each other is described by four principal operating modes:

Single conversion, Stretched mode, Conversion timer triggered mode and Continuous mode.

Figure 3-10 Conversion trigger and succession



By setting Flag 1 in the PARA8 register, DSP_TRIG_CDC, the CDC can be triggered by the end of the DSP. This has to be implemented in the firmware and is already part in the standard firmware.

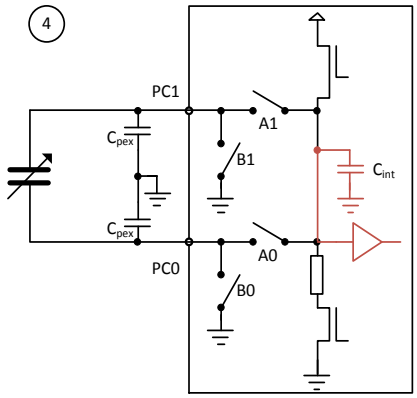
3.2 CDC Compensation Options

3.2.1 Internal Compensation

For the internal compensation measurement, both switches A1 and A0 are open. Only the internal parasitic capacitance and the comparator propagation delay will thus be measured.

It is recommended to have internal compensation active in any application.

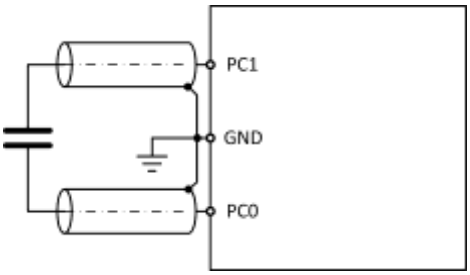
Figure 3-11 Internal compensation measurement



3.2.2 External Compensation

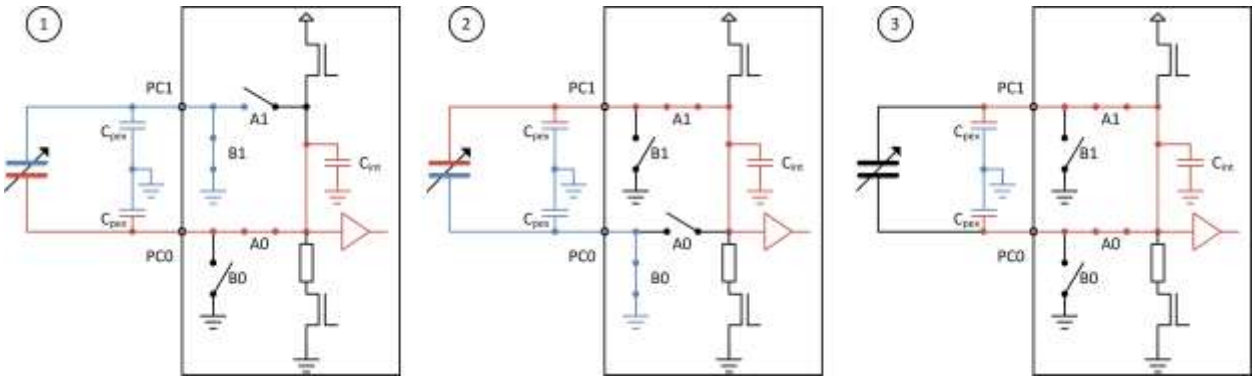
With floating capacitors we have the additional option to compensate external parasitic capacitances against ground. On the PCB, the wire capacitance typically refers to ground. For long wires, it is recommended to use shields which should be grounded at their PCB side.

Figure 3-12 How to connect shielded cables for compensation of the external parasitic capacitances.



Three measurements are necessary for each capacitor in case of floating sensors; this is shown in Figure 3-13.

Figure 3-13 Floating capacitors, external compensation measurements, the three measurements that are made for each floating capacitor.



3.2.3 Parallel Resistance

In some applications the sensor might see a parallel resistance. This resistance is typically caused by dirt or condensation and is changing slowly. In PCapØ2A a compensation method is implemented to get rid of this.

3.2.4 Force Compensation & Self-test

For differential sensors, mainly MEMS, a force compensation method is available. In this mode the inactive electrode is connected to a dummy charge circuit and therefore always has a potential similar to that of the active electrode. The center electrode therefore is almost force free. Because the capacitances are different, the voltage is not the same upon reaching the trigger threshold, so there is a residual force.

This mode can be used for self-test, too. If force compensation is toggled, means measurements with and without compensation are made, then the force on the active electrode varies. The user should see an obvious difference between the measurement results with and without compensation. If not, then the sensor is most likely broken.

3.2.5 DC Balance

When driving floating sensors then the sensors' supply is typically DC free.

With parallel resistance compensation this symmetry would be broken. Therefore, PCapØ2 has the possibility to add dummy measurements so that even with parallel resistance compensation the sensors are operated DC free (set by C_DC_BALANCE).

In applications with grounded sensors the sensors can`t be DC fee by principle.

3.2.6 Gain Correction

Comparable to classical A/D converters, the PCapØ2 shows a gain error. But in case of PCapØ2 the gain error is mainly given by internal parasitic capacitances and the propagation delay of the internal comparator. With internal compensation being active this delay is subtracted from the original measurement. The temperature drift can be approximated linearly and corrected mathematically just by a gain factor. In the standard firmware parameter 8 is reserved for the gain correction factor. The correction factor depends on the discharge time and therefore the RC combination. The firmware has to take this factor into account, like the cdc.h library does. The factor is stored in parameter register 7 as Gain_Corr. It has to be evaluated individually for every single application. E.g., with 22 pF and 30 kOhm the correction factor is 1.25.

Empirical method to find the right gain correction factor:

Replace the sensor with a temperature stable capacitor of the same size (ceramic COG) as your reference capacitor. (Therefore: quotient = 1, gain = 0). Set the gain correction factor to 1.0. Put the system (PCapØ2 on PCB) into a temperature chamber and measure the offset drift over temperature. Add an additional temperature stable capacitor to simulate your gain. Measure the gain drift. Increase the gain correction factor and measure the gain drift again. With a gain correction factor >1.0 the gain drift will decrease. If the gain correction factor is set too big then you will see a negative gain drift due to over compensation. The right gain correction factor is found, if the drift is reduced to what you measured at the initial offset drift measurement. Write back the new Gain_Corr value into parameter 7 register.

3.3 CDC Important Parameters

3.3.1 Cycle clock

The basic period t_{cycle} that defines the cycle time can be derived from the low frequency oscillator or the high frequency oscillator. It is selected as in PCapØ1 by configuration parameters CY_CLK_SEL (register 11).

Table 3-1 Configure cycle clock, for details see register **11**

CY_CLK_SEL	Cycle time base	
'b00	$t_{cycle} = t_{OLF}$	t_{OLF} = period low-frequency oscil.
'b10	$t_{cycle} = 4 * t_{OHF}$	t_{OHF} = period high-frequency oscil.
'b11	$t_{cycle} = t_{OHF}$	t_{OHF} = period high-frequency oscil.

3.3.2 Cycle time

The pre-charge, full-charge and discharge times of a single cycle are defined in multiples of t_{cycle}. Those are selected by:

Table 3-2 Configure cycle time, for detailsd see register **23-26**

Reg.	Configuration Parameter	Description
25, 26	PRECHARGE_TIME	Time to charge via resistor for current limitation. 0 = no pre-charge phase 1 to 1023: $t_{precharg}$ = PRECHARGE_TIME*t_{cycle}
27, 28	FULLCHARGE_TIME	Time for final charge without current limitation. 0 = no full-charge phase 1 to 1023: $t_{fullcharge}$ = (FULLCHARGE_TIME + 2) · t_{cycle}
23, 24	DISCHARGE_TIME	Time to discharge the capacitor. 0 = not allowed 1 to 1023: $t_{discharge}$ = (DISCHARGE_TIME + 1) · t_{cycle}

In case that PRECHARGE_TIME = FULLCHARGE_TIME = 0 the timing is similar to PCapØ1. Note: while in PCapØ1 the times are set in 2's complement, in PCapØ2 the times are set linearly and therefore can be set in finer steps.

3.3.3 Sequence

The length of a sequence depends on the kind and number of sensors, the selected compensation methods and the averaging sample size. The following parameters affect the sequence:

Table 3-3 Configure sequence, for details see registers **10** - **12**

Reg.	Configuration Parameter	Description
12	C_PORT_EN	Bitwise enable of the capacitance ports PC0 to PC7 0 = Port disabled 1 = Port active
10	C_REF_INT	Switches between external and internal reference capacitors. Can not be used with differential sensors. 0 = external, PC0 or PC0 & PC1 1 = internal, PC8 or PC8 & PC9
10	C_DIFFERENTIAL	Switches between single and differential sensors 0 = single 1= differential
10	C_FLOATING	Switches between grounded and floating sensors 0 = grounded 1 = floating
10	C_COMP_INT	Turns on compensation of internal capacitances/delays 0 = off 1 = on, recommended
10	C_COMP_EXT	Turns on compensation of external parasitic capacitances. Available only with floating sensors. 0 = off 1 = on, recommended
10	C_COMP_R	Turns on compensation of parallel resistances 0 = off 1 = on
11	C_DC_BALANCE	Turns on an additional measurement for DC balance. Introduces one additional measurement per capacitor. Effective in modes other than single grounded. 0 = off 1 = on
10	C_COMP_FORCE	Turns on force compensation for differential sensors 0 = off, inactive electrode HiZ 1 = on, inactive electrode connected to dummy charge

3.3.4 Conversion

The duration of a full conversion has a lower limit given by the number of fake measurements, the averaging and eventually an inter-sequence delay:

Table 3-4 Configure conversion, for details see registers **13**ff, **26**

Reg.	Configuration Parameter	Description
26	C_FAKE	Number of fake measurements (cycles with results being ignored) 0 = No dummy cycles 1 = 1 dummy cycle … 15 = 15 dummy cycles
13, 14	C_AVRG	Sample size for averaging within one conversion. 0 = 1 = no averaging … 8191 = maximum sample size 1st configuration bank, set by DSP_SEL_CFG_BANK = 0
15, 16	C_AVRG_ALT	Second sample size for averaging within one conversion. 0 = 1 = no averaging … 8191 = maximum sample size 2nd configuration bank, set by DSP_SEL_CFG_BANK = 1. The DSP may switch between C_AVRG and C_AVRG_ALT values to have two operating modes selected by software.

The Start of the next conversion depends on the selection of the measurement trigger. In continuous mode the next conversion follows immediately the previous one. In stretched mode the time interval between two conversions is defined by the conversion timer. Finally, in single conversion mode or pin trigger mode the single conversions are started individually, by serial opcode, by DSP command or by a trigger at a pin. New in PCapØ2 is the possibility that the DSP can select between to configuration settings for averaging, trigger select and conversion timer. This way it can switch between e.g. a scan mode and a measurement mode.

Table 3-5 Configure conversion, for details see registers **17** - **24**

Reg.	Configuration Parameter	Description
24	C_TRIG_SEL	First trigger selection for CDC trigger 0 = Off when CONV_TIMEx = 0 0 = Stretched when CONV_TIMEx > 0 1 = Continuous mode when CONV_TIMEx > 0 1 = Single conversion when CONV_TIMEx = 0 2 = Conversion timer triggered 3 = Pin triggered 1st configuration bank, set by DSP_SEL_CFG_BANK = 0
24	C_TRIG_SEL_ALT	Second trigger selection for CDC trigger 0 = Off when CONV_TIMEx = 0 0 = Streched when CONV_TIMEx > 0 1 = Continuous mode when CONV_TIMEx > 0

		1 = Single conversion when CONV_TIMEx = 02 = Conversion timer triggered 3 = Pin triggered 2nd configuration bank, set by DSP_SEL_CFG_BANK = 1. The DSP may switch between C_TRIG_SEL and C_TRIG_SEL_ALT values to have two operating modes selected by software.
24	C_STARTONPIN	Selects the GPIO that triggers the CDC measurement
17,18, 19	CONV_TIME	Sets the conversion time in multiples of twice the period of the low-frequency clock. t_{conv} = 2*CONV_TIMEO*t_{ofl} 1st configuration bank, set by DSP_SEL_CFG_BANK = 0
20,21, 23	CONV_TIME_ALT	Second setting for conversion time. t_{conv} = 2*CONV_TIMEO*t_{ofl} 2nd configuration bank, set by DSP_SEL_CFG_BANK = 1. The DSP may switch between CONV_TIME and CONV_TIME_ALT values to have two operating modes selected by software.

3.4 RDC Resistance-to-Digital Converter

3.4.1 Measuring Principle

In PCapØ2 resistance measurement is done by measuring discharge times. The measurements are ratiometric. This means the temperature-sensitive resistances are compared to fixed references. The ratio of discharge times is directly proportional to the ratio of capacitors. The discharge time is defined by the resistors and the load capacitance.

$$\frac{\tau_N}{\tau_{ref}} = \frac{R_\theta}{R_{ref}} \qquad \tau = k * R * C$$

3.4.2 Connecting Sensors

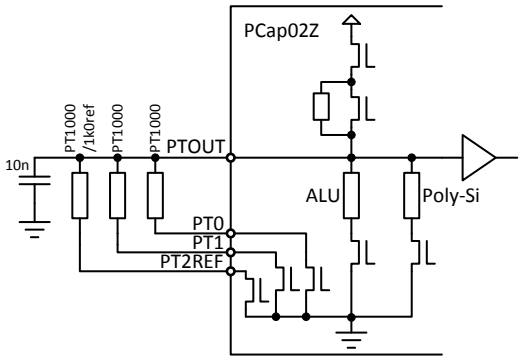
The chip device has two on-chip resistor elements for the measurement of temperature, an aluminum strip with TK ≈ 2800 ppm/K as a sensor and a poly-silicon resistor with TK “close to zero” as a reference. In the range 0°C to 100°C the aluminum sensor can be well approximated by a linear function of temperature.

As an alternative, it is possible to connect up to three external sensors. One of those can be used as external reference alternately. External and internal thermometers/reference may be mixed, e.g. an external PT1000 may be compared to the internal Poly-Si resistor.

In any case, it is mandatory to connect an external 10 nF capacitor, because the temperature measurement, too, is discharge time based. 10 µs discharge time are

sufficient. For the capacitor, COG ceramics yields best performance, while X7R material yields fair results.

Figure 3-14 Connecting temperature sensors

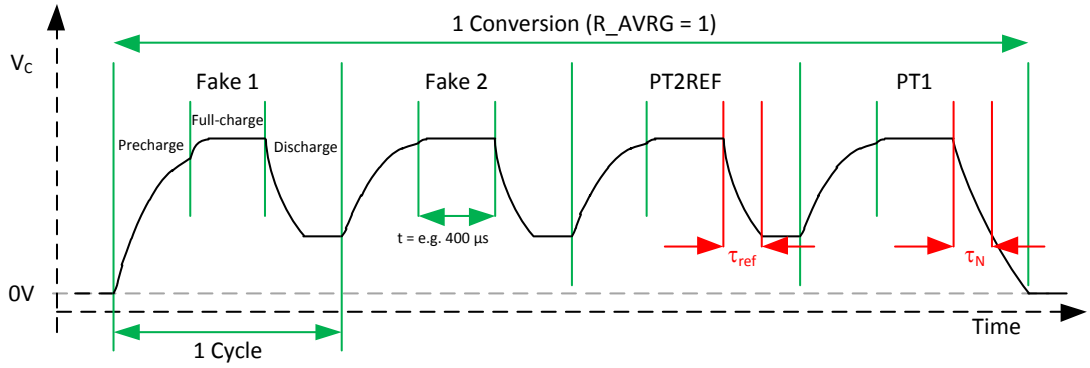


Note: The RDC measurement is based on a AC principle. So long cables with their parasitic capacitance and resistance will disturb and it is recommended to have short cables (≤ 0.5m), ideally twisted and shielded.

3.4.3 Cycle & Conversion

In PCapØ2 the resistance measurement is now running in three phases, like in capacitance measurement: Precharge – Full charge – Discharge. The timing is based on the internal low-frequency oscillator (OLF). The duration of the three phases can be 1 or 2 periods of this reference. The conversion starts with 2 or 8 fake measurements to improve the stability of data. For each single conversion the averaging can be selected with sample size 1, 4, 8 or 16.

Figure 3-15 RDC conversion (R_AVRG = 1, Reference and sensor, 2 fake measurements)



3.4.4 Trigger

There are various possibilities to trigger a resistance measurement:

- Serial Interface command, PIN or DSP

- CDC end of conversion
- Low-frequency oscillator (OLF)

For CDC and OLF options the RDC measure rate can be reduced by setting a divider (R_TRI_PREDIV).

In case of the CDC option there are three ways of how the DSP is triggered:

- Parallel: The CDC end of conversion triggers RDC and CDC in parallel
- Sequentially, synchronous: The DSP is triggered by the RDC end of conversion. Assuming that RDC rate is less than the CDC rate, the inactive RDC conversions are replaced by a delay.
- Sequentially, asynchronous: The DSP is triggered by the RDC end of conversion. If RDC rate is less than CDC rate the DSP is triggered directly from the CDC for inactive RDC conversions.

Figure 3-16 RDC Timing parallel mode

(R_TRIG_PREDIV = 3,R_TRIG_SEL = 3'b101, DSP_START_EN: CDC_TRIG_EN = 1, RDC_TRIG_EN = 0)

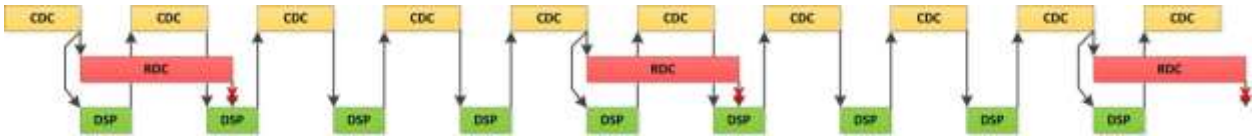


Figure 3-17 RDC Timing sequential, synchronous mode

(C_TRIG_SEL = 2, CONV_TIMER = 0, DSP_TRIG_CDC = 1, R_TRIG_PREDIV = 3, R_TRIG_SEL = 3'b110, DSP_START_EN: CDC_TRIG_EN = 0, RDC_TRIG_EN = 1)

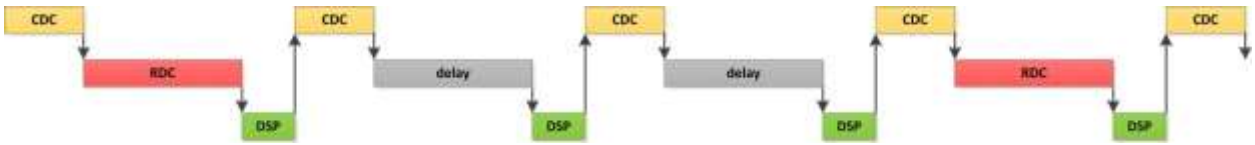
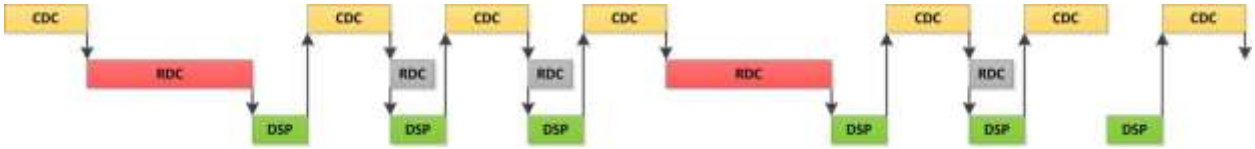


Figure 3-18 RDC Timing sequential, asynchronous mode

(C_TRIG_SEL = 2, CONV_TIMER = 0, DSP_TRIG_CDC = 1, R_TRIG_PREDIV = 3, R_TRIG_SEL = 3'b101, DSP_START_EN: CDC_TRIG_EN = 0, RDC_TRIG_EN = 1)



3.5 RDC Important Parameters

3.5.1 Cycle Clock

The base frequency for the temperature measurement is the low frequency oscillator. By setting divider R_OLF_DIV the user can ensure that the period is 100µs or 80µs. A further bit, R_CY, specifies whether 1 or 2 periods define the length of precharge phase and discharge phase.

Table 3-6 Configure cycle clock, see also register **35**

OLF Frequency	R_OLF_DIV	$t_{precharge} = t_{fullcharge} = t_{discharge}$	
		R_CY = 0	R_CY = 1
10 kHz	1	100 µs	200 µs
50 kHz	4	80 µs	160 µs
100 kHz	8	80 µs	160 µs
200 kHz	16	80 µs	160 µs

Both parameters are set in register 35.

3.5.2 Sequence

The major settings for the sequence are the number of ports, the fakes, the reference averaging.

Table 3-7 Configure sequence, for details see registers **33**, **34**

Reg.	Configuration Parameter	Description
34	R_PORT_EN	Enable ports PT0, PT1, PT2REF
34	R_PORT_EN_IREF	Enable the internal reference resistor
34	R_PORT_EN_IMES	Enable the internal temperature sensor
34	R_REF_SEL	0 = PT2REF is used for reference time (external) 1 = IREF is used for reference (internal)
34	R_3EXT_SEL	0 = less than 3 external sensors + external reference 1 = 3 external sensors
32	R_AVRG	Set averaging for T measurement
33	R_FAKE	Set number of fake measurements

3.5.3 Conversion

Table 3-8 Configure conversion, for details see registers **29**, **30**

Reg.	Configuration Parameter	Description
29	R_TRIG_SEL	Selection of trigger source for RDC unit (1st configuration bank, set by DSP_SEL_CFG_BANK = 0)
29	R_TRIG_SEL_ALT	Alternative selection of trigger source for RDC unit (2nd configuration bank set by DSP_SEL_CFG_BANK = 1)
30,31, 32	R_TRIG_PREDIV	Predivider to set the RDC rate as fraction of the CDC rate but also to the OLF_CLK when OLF_CLK is selected as RDC Trigger 0 = 1 = RDC conversion with each CDC conversion 2 = RDC conversion every second CDC conversion … 2^21
29	R_STARTONPIN	Start RDC conversion on pin trigger. Not recommended

4 Interfaces (Serial & PDM/PWM)

4.1 Serial Interfaces

Two types of serial interfaces are available for communication with a microcontroller and for programming the device: SPI and IIC. Only one interface is available at a time, selected by pin IIC_EN. On both interfaces the PCapØ2 can operate as slave only.

IIC_EN = GROUND	4-wire SPI interface General-purpose I/O pins PG0 and PG1 are not available
IIC_EN = VDD	2-wire I²C interface All general-purpose I/O pins are available

IIC_EN may not be floating. If no controller interface is needed connect IIC_EN to VDD.

Note:

Besides the case of reading the result registers, it is recommended to deactivate the converter for any communication to configuration registers, EEPROM, OTP or SRAM. This is done by setting the RunBit configuration register 77 to '0'. After the communication process the RunBit needs to be set back to '1'.

4.1.1 Opcodes

Table 4-1 PCapØ2 Opcodes

Description	Byte2								Byte1		Byte0
Write to OTP	1	0	1	add<12…0>							data<7…0>
Read from OTP	0	0	1	add<12…0>							data<7…0>
Write to SRAM	1	0	0	1	add<11…0>						data<7…0>
Read from SRAM	0	0	0	1	add<11…0>						data<7…0>
Block write EEPROM	1	1	1	0	0	0	0	1	data<7…0>		
Erase EEPROM	1	1	1	0	0	0	1	0	0	add<6…0>	[dummy byte]
Write configuration	1	1	0	0	0	0	0	0	0	add<6…0>	data<7…0>
Read result	0	1	0	0	0	0	0	0	0	add<6…0>	data<7…0>
Write EEPROM	1	1	1	0	0	0	0	0	0	add<6…0>	data<7…0>
Read EEPROM	0	1	1	0	0	0	0	0	0	add<6…0>	data<7…0>
Block erase EEPROM	1	1	1	0	0	0	1	1			
POR (Power-on Reset)	1	0	0	0	1	0	0	0			
Initialize	1	0	0	0	1	0	1	0			
CDC Start conversion	1	0	0	0	1	1	0	0			
RDC Start conversion	1	0	0	0	1	1	1	0			
Terminate write OTP	1	0	0	0	0	1	0	0			

All commands for write or read to memory or configuration / read registers may use explicit addressing or address auto-increment.

The serial interface is tested most easily by writing an arbitrary data to the SRAM and read this back.

4.2 I²C Compatible Interface

The present paragraph outlines the PCapØ2 device specific use of the I²C interface. The external I²C master begins the communication by creating a start condition, a falling edge on the SDA line while SCL is HIGH. It stops the communication by a stop condition, a rising edge on the SDA line while SCK is high. Data bits are transferred with the rising edge of SCK.

On I²C buses, every slave holds an individual 7-bit device address. This address has always to be sent as the first byte after the start condition, the eighth bit indicating the direction of the following data transfer (R=read=1 and W=write=0).

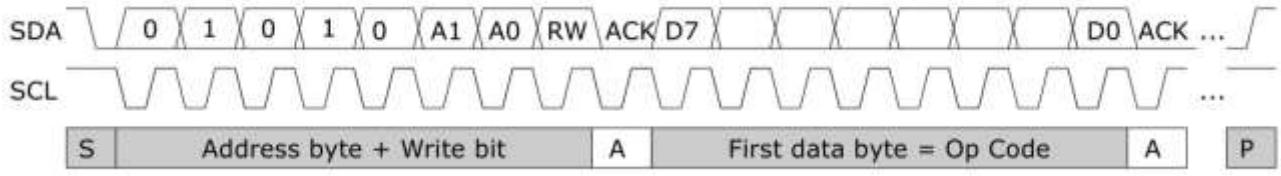
Address byte:

MSB							LSB
0	1	0	1	0	A1	A0	R/W
fixed					variable		key

Default address: 40 (A1 = A0 = 0)

The address byte is followed by the opcode and eventually the payload. Each byte is followed by an acknowledge bit (= 0, when a slave acknowledges).

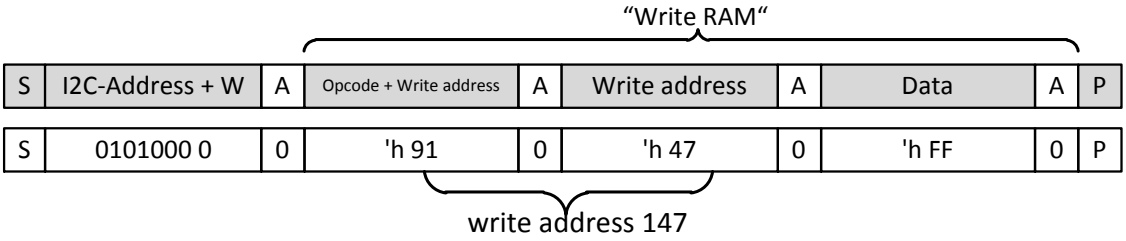
Figure 4-1 I²C principle sequence



4.2.1 I²C Write

During write transactions, the master alone sends data, the addressed slave just sends the acknowledge bits. The master first sends the slave address plus the write bit. Then it sends the PCapØ2 specific opcode including the register address in the slave. Finally it sends the payload ("Data").

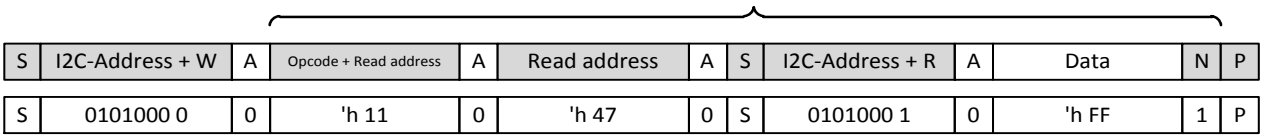
Figure 4-2 I²C Write procedure; an example (“write 'hFF as a datum to the SRAM at address 'h147.)



4.2.2 I²C Read

During read transactions, the direction of communication has to be commuted. Therefore, the master creates again a start condition and sends the slave address plus the read bit to switch into read mode. Figure 4-6 shows an example with op code “read from SRAM“.

Figure 4-3 I²C Read example. “Read from SRAM address ‘h147”, we find ‘hFF having been programmed before



After arrival of the first (or any) data byte, the master may either signal

- Not-Acknowledge = N = 1 to indicate “end read“, “stop sending“ to the slave, or
- Acknowledge = A = 0 to indicate “continue in automatic address-increment mode” and thus receive many bytes in a row. As one can see, automatic address increment is particularly useful and efficient with the I²C interface.

4.3 SPI interface

Clock Polarity, Clock Phase and Bit Order: The following choices are necessary for successful operation.

Table 4-2 SPI Clock Polarity, Clock Phase and Bit Order

SPI - Parameter	Description	Setting
CPOL	Clock polarity	0
CPHA	Clock phase	1
Mode	SPI Mode	1
DORD	Bit sequence order	0, MSB first

Figure 4-4 SPI Write

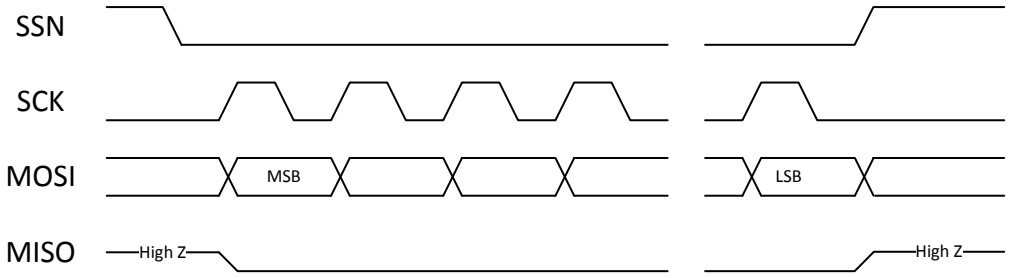


Figure 4-5 SPI Read

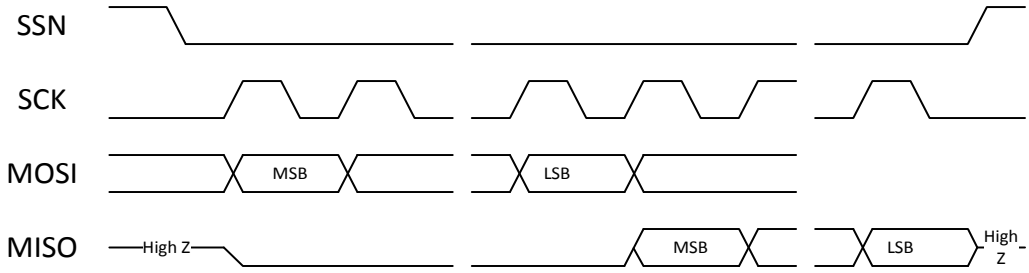


Table 4-3 SPI timing parameters

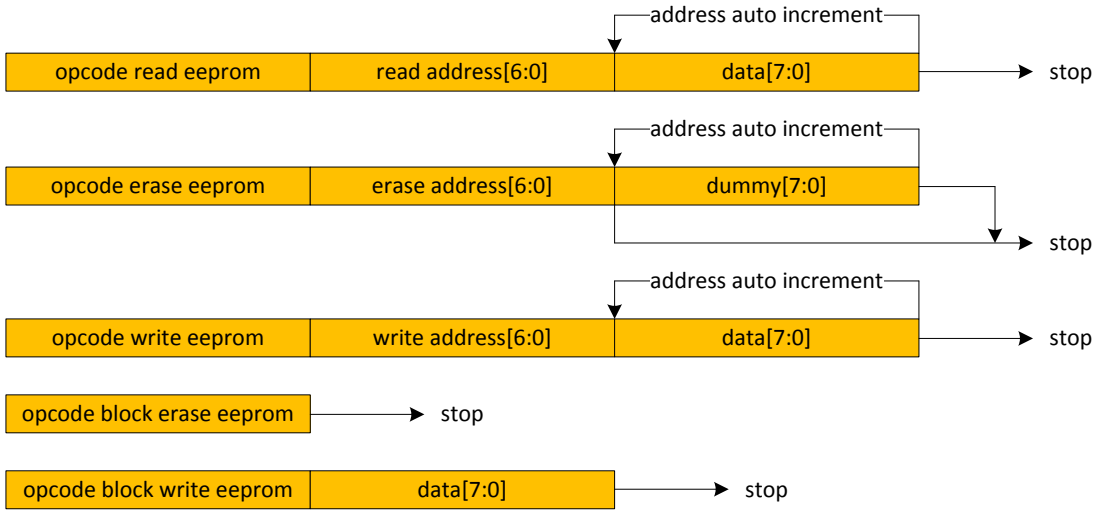
Name	Symbol	VDD=2.2 V	VDD=3.0 V	VDD=3.6 V	Units
Serial clock frequency	fSPI-bus	10	17	20	MHz
Serial clock pulse width HI state	tpwh	50	30	25	ns
Serial clock pulse width LO state	tpwl	50	30	25	ns
SSN enable-to-valid latch	tsussn	10	8	7	ns
SSN pulse width between write cycles	tpwssn	50	30	25	ns
Data setup time prior to clock edge	tsud	7	6	5	ns
Data hold time after clock edge	thd	5	4	3	ns
Data valid after clock edge	tvd	40	26	16	ns

4.4 Special Timings

4.4.1 EEPROM Timings

Here we describe the necessary timing for communication with the EEPROM via serial interface. Only 1's can be written to the EEPROM. Therefore, it is necessary to erase the EEPROM cells before writing new data. EEPROM communication may use address auto-increment. In case of "Erase EEPROM" the incremental write is achieved by sending additional dummy bytes (e.g. ´hE2_03_00 will erase EEPROM cells 3 and 4).

Figure 4-6 EEPROM communication



Before writing to the EEPROM following conditions need to be fulfilled:

OCF frequency =5 kHz (e.g. OLF_CTUNE= 2 (50 kHz), OLF_FTUNE ~5, OCF_TIME=5)
BG_TRIM1 = 7
EE_DISABLE = 0
Either: EE_SINGLE_WR_EN = 1 or: EE_WR_EN = 1 & EE_ON = 1

The EEPROM wakeup can be done explicitly or automatically (EE_ON or EE_ON_DSP). It is mandatory to take care of the setup timings, for each individual byte:

	EE_WAKEUP_MODE		
t_{rdsu}	0	1.5*t_{OCF}	300 µs
	1		10 µs
t_{rd}	X		600 ns
t_{wrsu}	0	1*t_{OCF}	200 µs
	1		10µs
t_{wr}	0	34*t_{OCF}	6.8 ms

Figure 4-7 EEPROM power controlled by user: Write/ Erase/ Block write/ Block erase

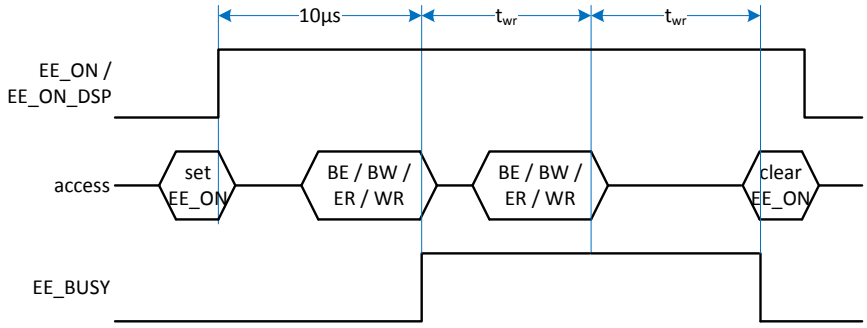


Figure 4-8 EEPROM power controlled by user: Read

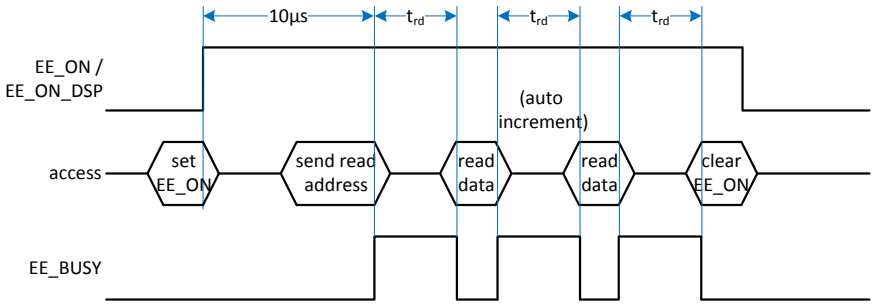


Figure 4-9 EEPROM power controlled automatically: Write/ Erase/ Block write/ Block erase

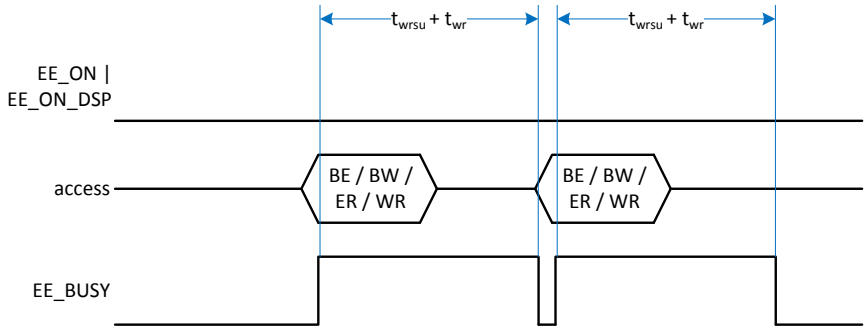
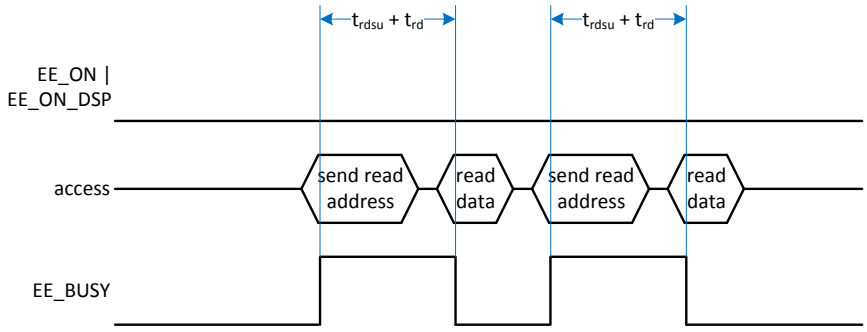


Figure 4-10 EEPROM power controlled automatically: Read



4.5 OTP Timings

In the un-programmed state the OTP cells' content is 'hFF. Once programmed to '0', the bits can't be set back to '1'. Writing to the OTP demands an external programming voltage of 6.5 volts at pin VPP_OTP. After setting the programming voltage it is mandatory to wait for 1 ms. After each data byte sent it is mandatory to wait for min. 30 µs (max. 1000µs) before sending the next data or to terminate the OTP write.

Note:

Before reading the OTP make sure that in configuration register 1 the correct ECC_MODE is configured.

Figure 4-11 OTP timing for programming by SPI

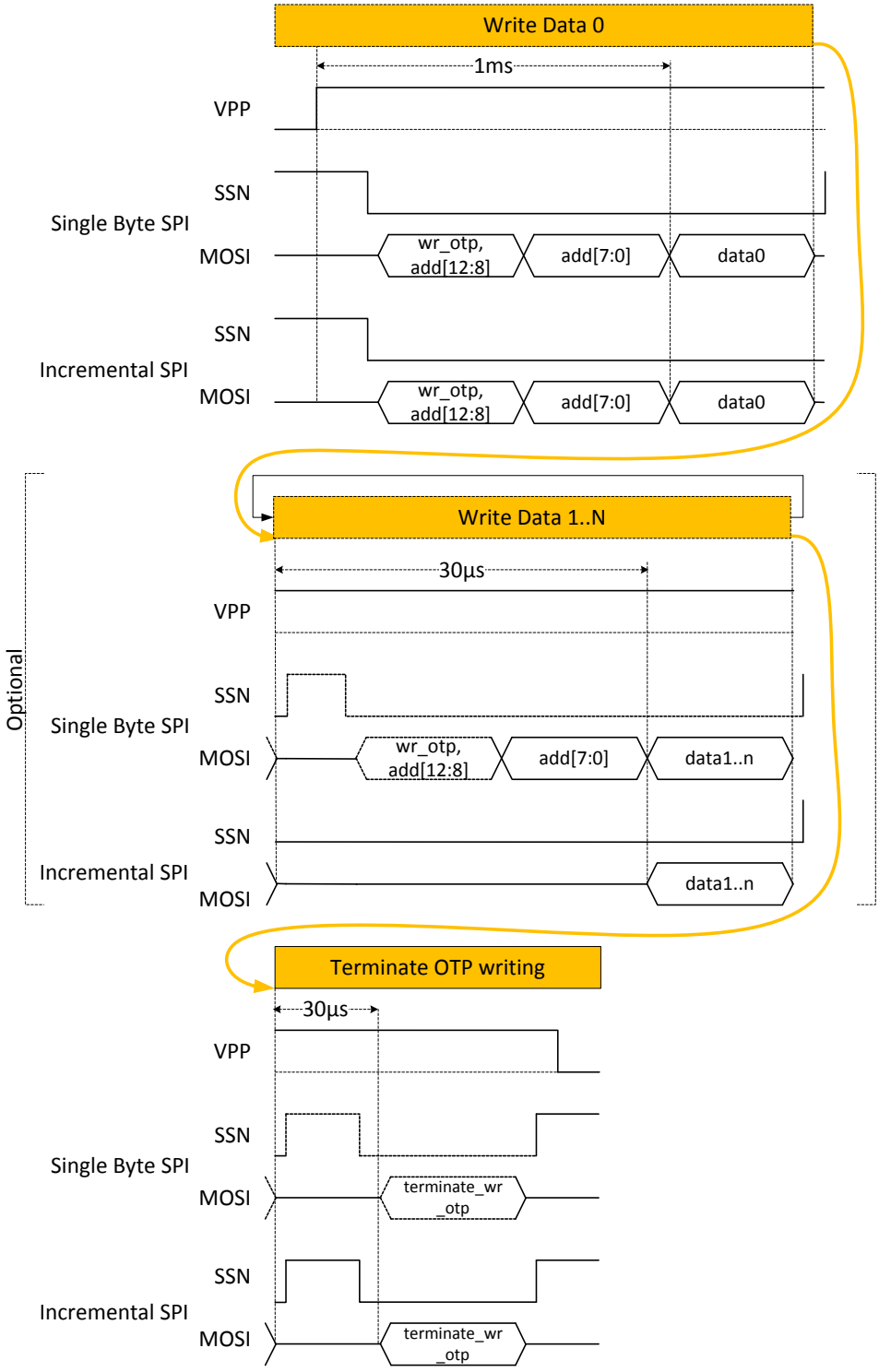
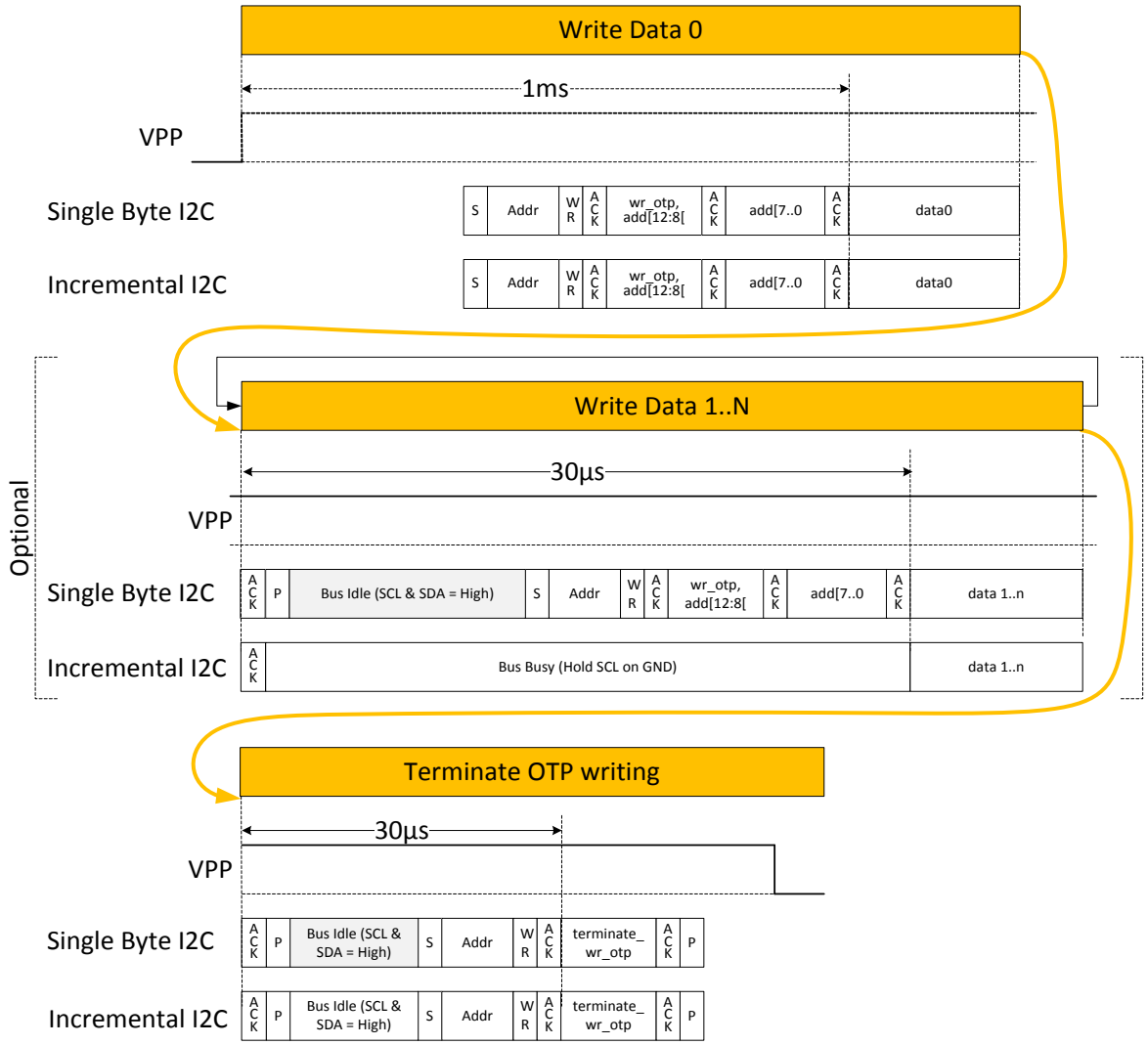


Figure 4-12 OTP timing for programming by I²C



4.6 GPIO and PDM/PWM

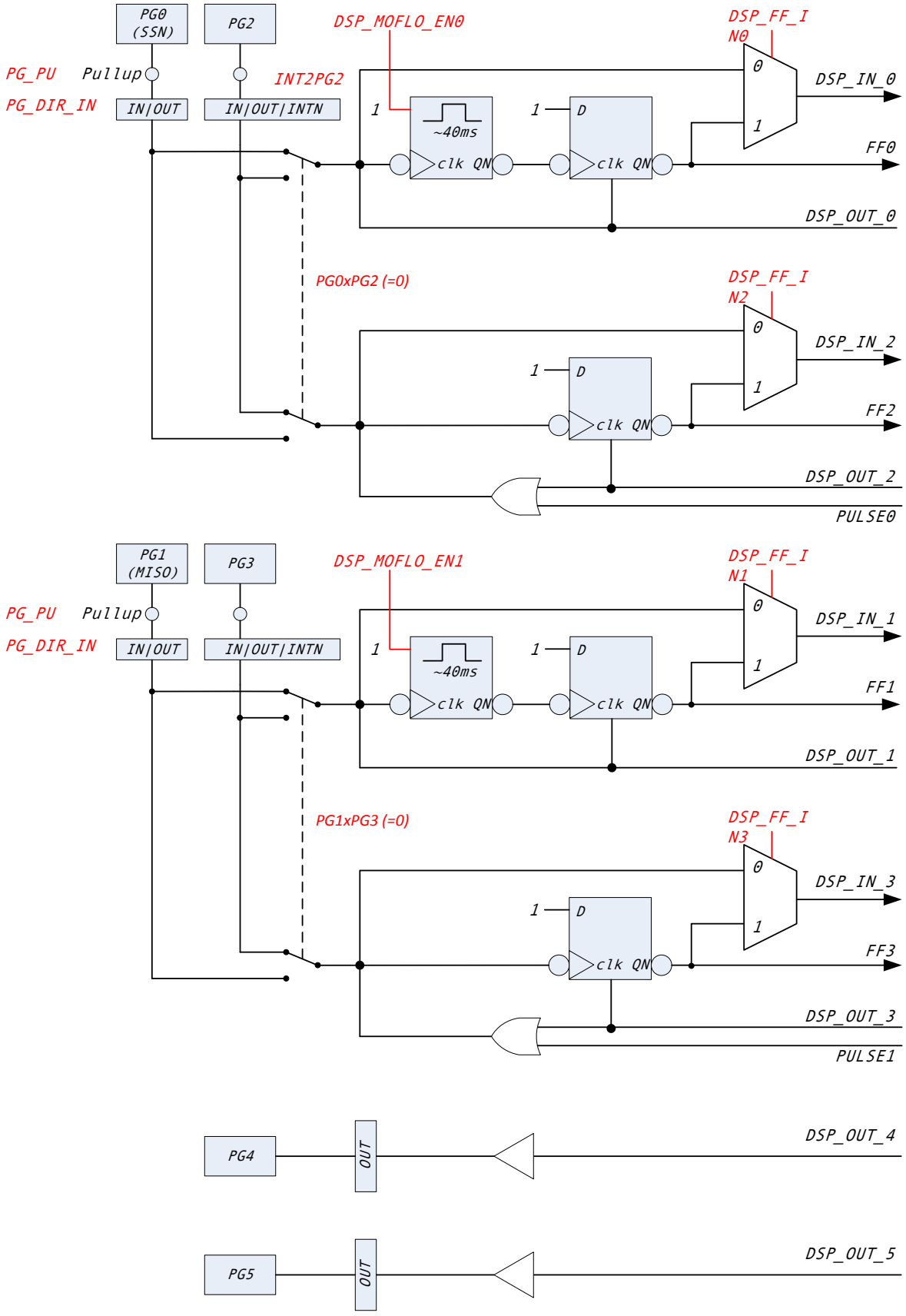
This section is about the general purpose ports and their use as Pulse-Density / Pulse Width Modulated outputs (PDM/PWM). Like PCapØ1, PCapØ2 is very flexible with assignment of the various GPIO pins to the DSP inputs/outputs. The following table shows the 5 general purpose ports and their possible assignment.

Table 4-4 General-Purpose Port Assignment

External Port Name	Description	Direction in or out
PG0	SSN (in SPI-Mode), serial select	in
	DSP_x_0 or DSP_x_2, I/O for the DSP	in(1) / out
	FF0 or FF2, I/O for the DSP with Flip-Flop	in(1)
	Pulse0, PDM or PWM output	out
PG1	MISO (in SPI-Mode)	out
	DSP_x_1 or DSP_x_3, I/O for the DSP	in(1) / out
	FF1 or FF3, I/O for the DSP with Flip-Flop	in(1)
	Pulse1, PDM or PWM output	out
PG2	DSP_x_0 or DSP_x_2, I/O for the DSP	in(1) / out
	FF0 or FF2, I/O for the DSP with Flip-Flop	in(1)
	Pulse0, PDM or PWM output	out
	INTN	out
PG3	DSP_x_1 or DSP_x_3, I/O for the DSP	in(1) / out
	FF1 or FF3, I/O for the DSP with Flip-Flop	in(1)
	Pulse1, PDM or PWM output	out
PG4	DSP_OUT_4 (output only)	out
PG5	DSP_OUT_5 (output only)	out

(1) These ports provide an optional debouncing filter and an optional pull-up resistor.

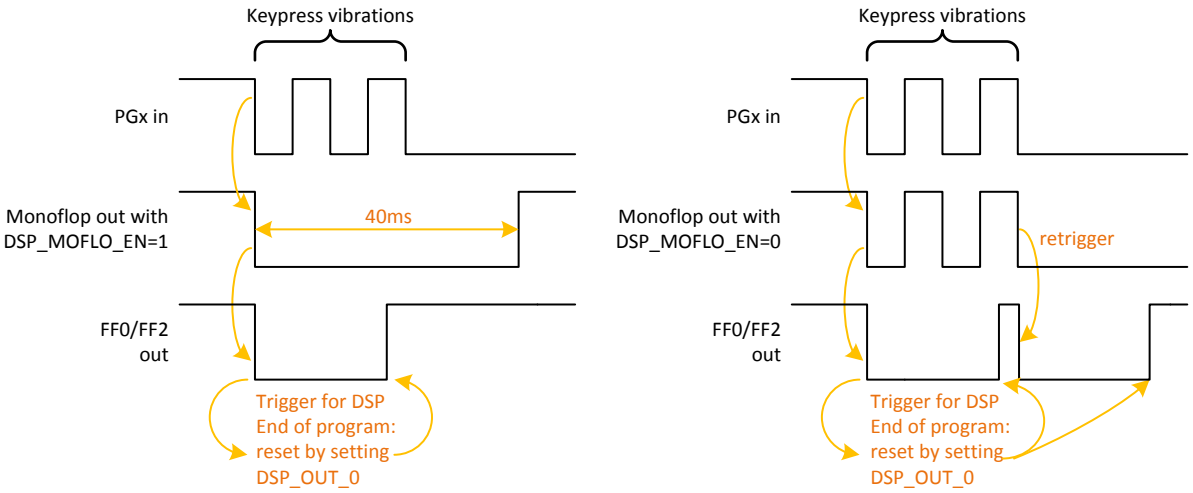
Figure 4-13 GPIO assignment



4.6.1 Debouncing filter

There is a possibility to activate a 40 ms debounce filter ("monoflop") for the ports in case these are used as push button inputs. This might be useful especially in case the DSP is started by the pins (signals FF0, FF2). Figure 2-3 shows the effect of the monoflop filter.

Figure 4-14 Port trigger timing

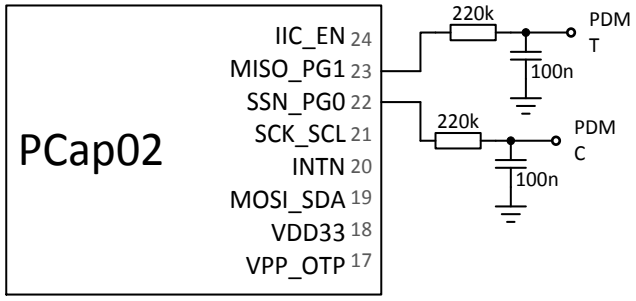


4.6.2 PDM/PWM

There is a possibility to generate two pulse width modulated or pulse density modulated output signals. In general, PDM is preferred because of better noise behavior. The output is based on the content of RAM registers PI0_REF, PI1_REF (DSP write addresses 98, 99. Width 16 bit each). The content of those RAM cells depends on the firmware. The description in this datasheet is based on the standard firmware, which writes the capacitance ration to PI0_REF, the Resistance ratio to PI1_REF.

The pulse interfaces can be switched on individually. The resolution can be programmed from 10 to 16 bit. There is a broad range of clock signals that can be selected as base for the pulse interfaces, derived from the 50 kHz low-frequency oscillator, the 4 MHz high-frequency oscillator or an internal ring oscillator with up to 20MHz or the cycle time. The output pins may be PG0 or PG2 and PG1 or PG3.

Figure 4-15



Filter configuration instructions:

The resistor should be >= 50 kOhm

The internal DC resistance of the output buffer is typ. 100 Ohm

1.Settling time (for PDM and PWM)

If the output value changes, the settling time to reach 90% is 2.3 x Tau

Tau=R x C

Example: 200k x 100nF x 2.3 = 50 ms

The smaller is Tau the faster is the settling but the higher is the ripple.

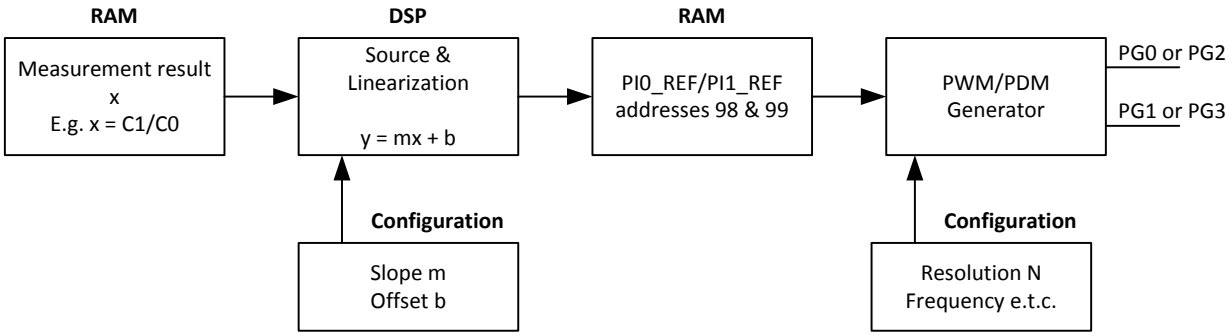
2.Voltage Ripple

Calculation method: T.b.d.

The output signal can be converted into an analog voltage through a low-pass filter. For the PDM output a first-order filter made of 220 kΩ / 100 nF is sufficient. The PWM output needs a filter with a lower cutoff frequency.

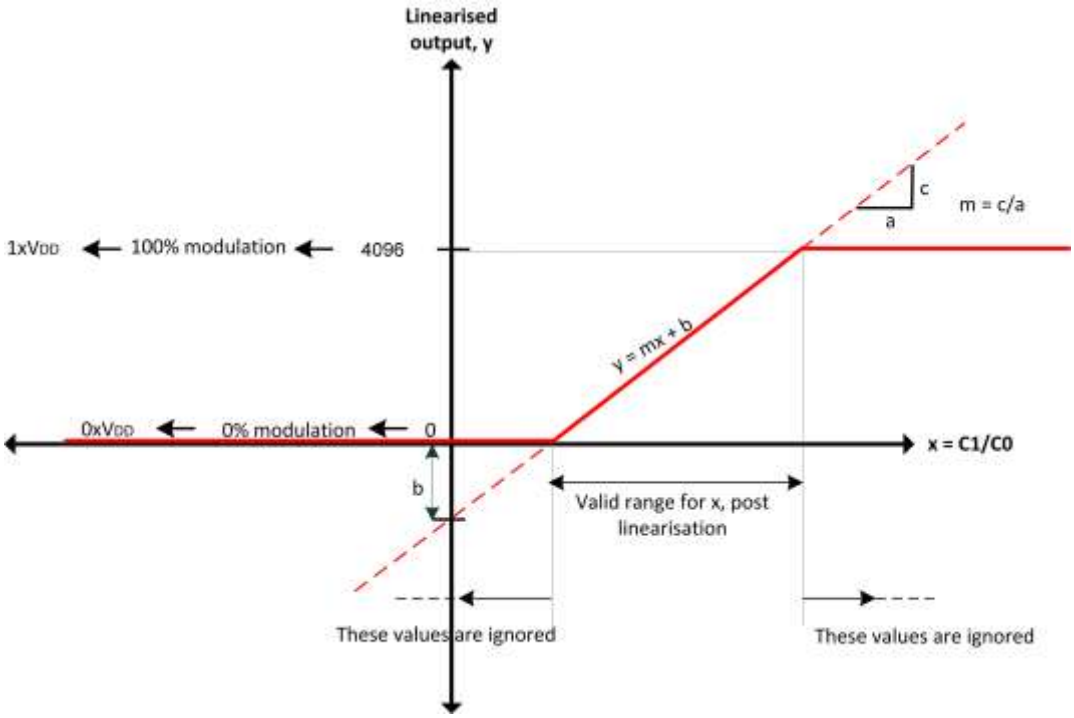
In the standard firmware, the result of measurement from capacitance or temperature is a 24-bit value. The DSP linearizes this 24 bit result to a 12 bit value (assuming '12 bit resolution' setting). The parameters Slope (m) and Offset (b) of the linear function are configurable in parameter registers 59 – 70. Both, offset and slope can be set to either positive or negative values. The setting of the slope and offset limits the range of the output signal and hence determines the voltage range of the filtered analog signal. A 12-bit resolution thus limits the result value between 0 and 4096. For lower-bit resolutions, the range reduces accordingly. The following figure depicts how the result is processed to generate the pulsed output.

Figure 4-16 PWM-PDM pulse generation



The following figure shows a sample linear function and its parameters graphically. In this graph, the result C1/C0 has been taken on the x-axis, assuming that this result is to be pulse modulated. Here the value of m is positive and b is negative. A 12 bit resolution has been configured.

Figure 4-17 PWM-PDM linearization



By setting the value of m and b, the linearization function limits the range of the output x as shown. Values outside these limits are ignored. Thereby knowing the range in which the results might change, the parameters of the linearization function can be fed accordingly. The lower limit of the valid range corresponds to 0% modulation (all bits are 0), The upper limit of the valid range corresponds to 100% modulation (all bits are 1), and this is the maximum possible value of output. 12 bit resolution implies that this maximum value is 4096. For lower-bit resolutions, this maximum value will come down accordingly. In terms of voltage, the two limits correspond to 0V and VDD.

Applications:

- A typical case would be outputting capacitance results through PG0 and temperature results through PG1. Calculation and transfer to the output registers will be performed by firmware.
- Main application will be when an analog interface is demanded by the final customer.
- Other applications concern maybe an impossibility to use the serial interface (speed limitations or other concerns).
- Finally, a temperature-coded pulse stream could be low-pass filtered and then directly used for temperature control.

Please note that the entire linearization task as described here is performed by firmware, especially the standard firmware.

4.7 Interfaces Parameters

4.7.1 GPIO Settings

Table 4-5

Reg.	Configuration Parameter	Description
40	DSP_MOFLO_EN	Activates anti-bouncing filters on PG0/PG1
40	PG0xPG2	Swaps PG0 and PG2 functionality
40	PG1xPG3	Swaps PG1 and PG3 functionality
42	DSP_FF_IN	Activates latching FLIFLOPs at ports PG0 to PG3
43	INT2PG2	Permits rerouting the interrupt signal to the PG2 port. If INT2PG2 =1 then all other settings for PG2 are ignored. Useful with QFN24 packages, where no INTN pin is available.
46	PG_DIR_IN	Toggles outputs to inputs 0 = output; 1 = input
46	PG_PU	Turn on pull-up resistors for ports PG0 to PG3

4.7.2 PDM/PWM Settings

Table 4-6

<table>
<tr><th>Reg.</th><th>Configuration Parameter</th><th>Description</th></tr>
<tr><td>44</td><td>PIO_CLK_SEL
PI1_CLK_SEL</td><td>Select clock sources for pulse code generators.
0 = pulse interface off
<table>
<tr><th></th><th>Clock source</th><th>Factor</th><th>Frequency</th></tr>
<tr><td>0</td><td colspan="3">Off</td></tr>
<tr><td>1</td><td rowspan="3">Cycle time</td><td>1</td><td>1 / (cycle time)</td></tr>
<tr><td>2</td><td>2</td><td>2 / (cycle time)</td></tr>
<tr><td>3</td><td>4</td><td>4 / (cycle time)</td></tr>
<tr><td>4</td><td rowspan="4">HF, High-frequency clock (e.g. 4 MHz)</td><td>2</td><td>8 MHz</td></tr>
<tr><td>5</td><td>1</td><td>4 MHz</td></tr>
<tr><td>6</td><td>0.5</td><td>2 MHz</td></tr>
<tr><td>7</td><td>0.25</td><td>1 MHz</td></tr>
<tr><td>8</td><td rowspan="4">LF, High-frequency clock (e.g. 50 kHz)</td><td>2</td><td>100 kHz</td></tr>
<tr><td>9</td><td>1</td><td>50 kHz</td></tr>
<tr><td>10</td><td>0.5</td><td>25 kHz</td></tr>
<tr><td>11</td><td>0.25</td><td>12.5 kHz</td></tr>
<tr><td>12</td><td rowspan="3">Internal Ring Oscillator (not recommended)</td><td>1</td><td>20 MHz</td></tr>
<tr><td>13</td><td>0.5</td><td>10 MHz</td></tr>
<tr><td>14</td><td>0.25</td><td>5 MHz</td></tr>
</table></td></tr>
<tr><td>45</td><td>PI_EN</td><td>Switch on pulse outputs
‘bxx01 = PWM at PIO
‘bxx10 = PDM at PIO
‘b01xx = PWM at PI1
‘b10xx = PDM at PI1</td></tr>
<tr><td>45</td><td>PIO_RES,
PI1_RES</td><td>Resolution of pulse interfaces
0 = 10 bit
1 = 12 bit
2 = 14 bit
3 = 16 bit</td></tr>
</table>

5 Configuration & Read Registers

5.1 Configuration registers

The PCapØ2 offers 78 write registers, 51 registers for configuring the hardware (CDC, RDC, clocks, PDM/PWM, DSP) and 27 registers for making parameters available to the DSP (to be interpreted by firmware). All of these 78 registers are one byte large.

A 78th register contains nothing but one single bit, the RunBit, which enables/disables the front-end and the DSP. Register 77 has to be written every time the configuration has been modified.

Note: Before writing into the configuration registers the RunBit in register 77 has to be set to 0. Then, as a last step, configuration register 77 is written again with RunBit = 1.

Table 5-1 Configuration register map

Reg	7	6	5	4	3	2	1	0
0	AUTOBOOT_DIS 3			0	MEM_LOCK_DIS 3			0
1	ECC_MODE 7							0
2		SPI_COLL AVOID_EN	I2C_ADD 1	0	MEM_CMP_LENGTH 1	0	OTP_RO_SPEED 1	0
3	OLF_CTUNE 1	0	OLF_FTUNE 3			0	OX_CLK32 KHZ_EN	OLF_CLK_ SEL
4	OX_DIS	OX_AMP_ TRIM	OX_DIV4	OX_AUTO STOP_DIS	OX_STOP	OX_RUN 2		0
5			OCF_TIME 5					0
6						OHF_CLK_SEL[2:0] 2		0
7				DCHG_ DUM_DIS	SCHMITT_ CDUM_EN	C_SENSE_ INVERT	SCHMITT_SEL[1:0] 1	0
8	RDCHG_INT_H[1:0] 1	0	RDCHG_INT_L[1:0] 1	0	RDCHG_ INT_EN		RDCHG_ EXT_EN	RDCHG_ 1MEG_EN
9		AUX_PD_ DIS	AUX_CINT	RDCHG_EA RLY_OPEN	RDCHG_ PERM_EN	RDCHG_ EXT_PERM	RCHG_SEL[1:0] 1	0
10	C_REF_INT	COMP_R_ SEL	C_COMP_ EXT	C_COMP_ INT	C_COMP_R	C_COMP_ FORCE	C_DIFFER ENTIAL	C_FLOAT ING
11			C_PORT_ PAT	C_SELFTEST	CY_CLK_SEL		CY_PRE_ LONG	C_DC_ BALANCE
12	C_PORT_EN 7							0

13	7			C_AVRG				0
14				12				8
15	7			C_AVRG_ALT				0
16				12				8
17	7							0
18	15			CONV_TIME				8
19		22						16
20	7							0
21	15			CONV_TIME_ALT				8
22		22						16
23	7			DISCHARGE_TIME				0
24	C_STARTONPIN 1	0	C_TRIG_SEL_ALT 1	0	C_TRIG_SEL 1	0	DISCHARGE_TIME 9	8
25	7			PRECHARGE_TIME				0
26			C_FAKE 3			0	PRECHARGE_TIME 9	8
27	7			FULLCHARGE_TIME				0
28	EE_SINGLE_WR_EN	EE_WR_EN	EE_DISABLE	EE_IFC_PRIO	EE_WAKE UP_MODE	EE_ON	FULLCHARGE_TIME 9	8
29	R_STARTONPIN 1	0	R_TRIG_SEL_ALT 2	0	R_TRIG_SEL 2			0
30	7			R_TRIG_PREDIV				0
31	15							8
32	R_AVRG 1	0	21					16
33	R_SENSE_INVERT	R_FAKE	R_QHA_SEL 5					0
34		R_REF_SEL	R_3EXT_SEL	R_PT1_EN	R_PT0_EN	R_PT2REF_EN	R_PORT_EN_IMES	R_PORT_EN_IREF
35	C_REF_SEL 4				0	R_CY	R_OLF_DIV 1	0
36				RTC_CLK_SEL	RTC_EN	LBD_CLK_SEL	TDC_NOISE_CY_DIS	
37	TDC_MUPU_NO 5					0	TDC_FIN_ADJ 1	0
38	TDC_QHA_SEL 5					0		
39		TEBU_SEL 1	0	EE_VEE2_ENA	EE_VEE1_ENA	EE_EETEST_ENA	TDC_CALWIDTH 1	0
40	DSP_MOFLO_EN 1	0	DSP_CLK_MODE 1	0	DSP_SPEED 1	0	PG1xPG3	PG0xPG2
41	7			WD_TIME				0
42	DSP_STARTONPIN 3			0	DSP_FF_IN 3			0
43	INT2PG2	DSP_SPRAM_SEL	DSP_START	DSP_START_EN 4				0
44	PI1_CLK_SEL 3			0	PI0_CLK_SEL 3			0

45	PI_EN								PI1_RES				PI0_RES			
	3							0	1			0	1			0
46	PG_DIR_IN								PG_PU							
	3							0	3							0
47					BG_PERM				BG_TRIM0							
									4							0
48	TDC_NOISE_DIS		TDC_MUPU_SPEED				TDC_MR2		BG_TRIM1							
			1			0			3							0
49	TDC_ALUPER MOPEN		TDC_ALU SLOW		TDC_CHAN_EN				TDC_CAL AVG		TDC_CAL_DELAY					
					1			0			1			0		
50	7															0
51	15						Parameter0									8
52	23															16
53	7															0
54	15						Parameter1									8
55	23															16
56	7															0
57	15						Parameter2									8
58			22													16
59	7															0
60	15						Parameter3									8
61	23															16
62	7															0
63	15						Parameter4									8
64	23															16
65	7															0
66	15						Parameter5									8
67	23															16
68	7															0
69	15						Parameter6									8
70	23															16
71	7															0
72	15						Parameter7									8
73	23															16
74	7															0
75	15						Parameter8									8
76	23															16
77															RUNBIT	

Firmware specific

5.2 Configuration Registers in Detail

Reg	7	6	5	4	3	2	1	0
0	AUTOBOOT_DIS				MEM_LOCK_DIS			
	3			0	3			0

Name	Description	Settings
AUTOBOOT_DIS[3:0]	Automatic self-boot from OTP	'h0 := stand-alone operation, the device boots itself from the OTP memory 'hF := slave operation, the device requires to be booted via the serial interface
MEM_LOCK_DIS[3:0]	Program-memory Read-out blocker (OTP and SRAM against the serial interface)	'h0 := activating the read-out blocker, which prevents the firmware from being read and thus helps protecting your intellectual property 'hF := memory remains unblocked

Reg	7	6	5	4	3	2	1	0
1	ECC_MODE							
	7							0

Name	Description	Settings
ECC_MODE[7:0]	OTP-internal error detection and repair mechanism	'h00 := disabled ("direct/simple") 'h0F := "double" mode 'hF0 := "quad" mode (with memory size halved down to 1963 bytes, see section 6.2)

Reg	7	6	5	4	3	2	1	0
2		SPI_COLL AVOID_EN	I2C_ADD		MEM_COMP_LENGTH		OTP_RO_SPEED	
			1	0	1	0	1	0

Name	Description	Settings
SPI_COLLAVOID_EN	Avoids collisions of DSP and SPI register access	1 = recommended
I2C_ADD	Complement to the I²C-address	see chapter 4
MEM_COMP_LENGTH[1:0]	Controls the SRAM-to-OTP comparison mechanism	0 := disable 1 := exit after comparison

		of 5 bytes 2 := exit after every 33 bytes 3 := exit after every 257 bytes
OTP_RO_SPEED	Speed of OTP oscillator	1 = fastest, recommended

Reg	7	6	5	4	3	2	1	0
3	OLF_CTUNE 1 0		OLF_FTUNE 3 0				OX_CLK32 KHZ_EN	OLF_CLK_ SEL

Name	Description	Settings
OLF_CTUNE[1:0]	Coarse-tune the low-frequency clock	0 := 200kHz 1 := 100kHz 2 := 50kHz recommended 3 := 10kHz
OLF_FTUNE[3:0]	Fine-tune the low-frequency clock	0:= minimum recommended 15:= maximum
OX_CLK32KHZ_EN	Switches external Oscillatorpad from 4MHz to 32 kHz clock generator	0:= external oscillator set to 4MHz resonator 1:= external oscillator set to 32 kHz quartz
OLF_CLK_SEL	Select the low-frequency clock source	0:= on-chip clock source for OLF 1:= 32 kHz quartz serves as OLF

see remarks in section 5.4

Reg	7	6	5	4	3	2	1	0
4	OX_DIS	OX_AMP_ TRIM	OX_DIV4	OX_AUTO STOP_DIS	OX_STOP	OX_RUN 2		0

Name	Description	Settings
OX_DIS	Disable the OX clock	0:= clock generator on, 1:= off
OX_AMP_TRIM	Trim the OX clock feedback gain	0:= low gain, 1:= high gain
OX_DIV4	OX clock frequency := raw freq./4	0:= no division; 1:= division by 4
OX_AUTOSTOP_DIS	acam internal bits	default := 0
OX_STOP	acam internal bits	default := 0
OX_RUN[2:0]	Control the permanency or the latency for pulsed mode of the OX generator. Latency means an oscillator warm-up time before a measurement starts	0:= generator off 6:= OX latency = 1 / f_{OLF} 3:= OX latency = 2 / f_{OLF} 2:= OX latency = 31 / f_{OLF} 1:= OX runs in permanence

see remarks in section 5.4

Reg	7	6	5	4	3	2	1	0
5			OCF_TIME					
			5					0

Name	Description	Settings
OCF_TIME[5:0]	Controls the OCF frequency, serving the EEPROM, must be adjusted so that f_{OCF} := 3..5 kHz. OCF is derived from OLF via a counter.	0:= maximum possible OCF frequency ($f_{OCF} = f_{OLF} / 1$) 63:= minimum possible OCF frequency ($f_{OCF} = f_{OLF} / 126$) $OCF\_TIME = \frac{f_{OCF}}{2 \cdot f_{OLF}}$

Reg	7	6	5	4	3	2	1	0
6						OHF_CLK_SEL[2:0]		
						2		0

Name	Description	Settings
OHF_CLK_SEL[2:0]	Choice of HF clock source; if no HF quartz or ceramic oscillator is connected, nor any other off-chip HF clock signal available, choose "internal"	1 := internal clock source #1 2 := internal clock source #2 4 := external clock source

Reg	7	6	5	4	3	2	1	0
7				DCHG_DUM_DIS	SCHMITT_CDUM_EN	C_SENSE_INVERT	SCHMITT_SEL[1:0]	
							1	0

Name	Description	Settings
DCHG_DUM_DIS	Dummy charge/discharge symmetry for differential capacitors	0:= for differential capacitors, 1:= for ordinary capacitors
SCHMITT_CDUM_EN	Even better symmetry	0:= default 1:= recommended with differential sensors and dummy mode active
C_SENSE_INVERT	Invert levels between trigger and converter	1:= recommended when using one of the on-chip Schmitt triggers
SCHMITT_SEL[1:0]	Selection of internal Schmitt trigger	0 = recommended

Reg	7	6	5	4	3	2	1	0
8	RDCHG_INT_H[1:0] 1	0	RDCHG_INT_L[1:0] 1	0	RDCHG_ INT_EN		RDCHG_ EXT_EN	RDCHG_ 1MEG_EN

Name	Description	Settings
RDCHG_INT_H[1:0]	Choice of one out of 4 on-chip discharge resistors for the CDC ports PC4 – PC7	0:= 180 kΩ 1:= 90 kΩ 2:= 30 kΩ 3:= 10 kΩ
RDCHG_INT_L[1:0]	Same, but for ports PC0 – PC3 plus special ports PC8 – PC9	
RDCHG_INT_EN	Enable internal discharge resistors	0:= off 1:= internal on
RDCHG_EXT_EN	Enable external discharge resistors	0:= off 1:= external on
RDCHG_1MEG_EN	Replace the kilo-ohm discharge resistors by a 1-MΩ-resistor in the PC0-PC3 and PC8-PC9 paths, only. The PC4-PC7 path is unaffected.	0:= 10 ... 180 kΩ 1:= 1 MΩ

Reg	7	6	5	4	3	2	1	0
9		AUX_PD_ DIS	AUX_CINT	RDCHG_EA RLY_OPEN	RDCHG_ PERM_EN	RDCHG_ EXT_PERM	RCHG_SEL[1:0] 1	0

Name	Description	Settings
AUX_PD_DIS	Activate the auxiliary port PC_AUX by disabling the pull-down resistors built-in for its protection	0 = off 1 = active
AUX_CINT		
RDCHG_EARLY_OPEN	Early open the chip-internal discharge resistor	0 = off 1 = on
RDCHG_PERM_EN	Keep the chip-internal discharge resistor permanently connected.	0 = off 1 = on
RDCHG_EXT_PERM	Enable the external discharge resistor.	0 = off 1 = on
RCHG_SEL[1:0]	Choice of one out of 4 on-chip charging resistors for the CDC, permitting to limit the charging current, avoiding transients	0:= 180 kΩ 1:= 90 kΩ 2:= 30 kΩ 3:= 10 kΩ

Reg	7	6	5	4	3	2	1	0
10	C_REF_INT	COMP_R_ SEL	C_COMP_ EXT	C_COMP_ INT	C_COMP_R	C_COMP_ FORCE	C_DIFFER ENTIAL	C_FLOAT ING

Name	Description	Settings
C_REF_INT	Use on-chip reference capacitor at CDC special ports PC8 and PC9	0:= external reference at PC0/GND or PC0/PC1) 1:= internal reference
COMP_R_SEL	Choice of an on-chip auxiliary resistor used for compensating slowly-varying parasitic parallel resistivity	0 := 90 kΩ 1 := 180 kΩ
C_COMP_EXT	Activate the compensation mechanism for off-chip parasitic capacitances	0:= idle 1:= active; must be avoided when C_FLOATING==0
C_COMP_INT	Activate the compensation mechanism for on-chip parasitic capacitances and gain compensation	0:= idle 1:= active
C_COMP_R	Activate the compensation mechanism for slowly-varying parasitic parallel resistivity	0 := idle 1 := active
C_COMP_FORCE	Compensation for mechanical forces on differential sensors. The outer electrodes have nearly the same potential. Can be used only with differential modes.	0 := off 1 := active
C_DIFFERENTIAL	Select between single or differential sensors	0:= ordinary 1:= differential
C_FLOATING	Select between grounded or floating sensors	0:= grounded 1:= floating

Reg	7	6	5	4	3	2	1	0
11			C_PORT_PAT	C_SELFTEST	CY_CLK_SEL		CY_PRE_LONG	C_DC_BALANCE

Name	Description	Settings
C_PORT_PAT	The order of the measured ports will be reversed after each sequence Do not use in combination with ("PCapØ2-Mode" && Conversion Timer && AVRG!=0), See bug report 7.1.1	0 := normal 1 := alternating order of ports
C_SELFTEST	For differential sensors only. See 3.2.4	0 := off 1 := inverts value of C_COMP_FORCE.
CY_CLK_SEL	Clock source for CDC:	'b00 := OLF_CLK 'b01 := inhibit 'b10 := OHF_CLK/4 'b11 := OHF_CLK

CY_PRE_LONG	Adds safety delay between internal clock paths	0 := off, recommended 1 := on
C_DC_BALANCE	helps keeping the sensor DC free (charge-free on the average); only applicable with single floating or with differential capacitors.	0:= idle 1:= active

Reg	7	6	5	4	3	2	1	0
12	C_PORT_EN							
	7							0

Name	Description	Settings
C_PORT_EN[7:0]	Enables bitwise the CDC ports from PC0 to PC7, bit #0 for port PC0, #1 for PC1 etc.	'h00:= all closed, the CDC will not work 'h01:= only port PC0 is activated etc. 'hFF:= all ports activated

Reg	7	6	5	4	3	2	1	0
13	7			C_AVRG				0
14				12				8
15	7			C_AVRG_ALT				0
16				12				8

Name	Description	Settings
C_AVRG[12:0]	Sample size for averaging (calculating the mean value) over CDC measurements	0=1:= no averaging 2:= averaging over 2 values 3:= averaging over 3 values etc. 8191:=maximum sample size
C_AVRG_ALT[12:0]	Second sample size for averaging 2nd configuration bank, set by DSP_SEL_CFG_BANK = 1. The DSP may switch between C_AVRG and C_AVRG_ALT values to have two operating modes selected by software.	

Reg	7	6	5	4	3	2	1	0
17	7							0
18	15			CONV_TIME				8
19		22						16

Reg	7	6	5	4	3	2	1	0
20	7							0
21	15				CONV_TIME_ALT			8
22		22						16

Name	Description	Settings
CONV_TIME[22:0]	Conversion trigger period or: sequence period (in stretched mode)	Concerning CDC, a particular period for triggering the measurements $T_{conv./seq}$= 2 * CONV_TIME[..] / f_{OLF}
CONV_TIME_ALT[22:0]	2nd configuration bank, set by DSP_SEL_CFG_BANK = 1. The DSP may switch between C_AVRG and C_AVRG_ALT values to have two operating modes selected by software.	

Reg	7	6	5	4	3	2	1	0
23	DISCHARGE_TIME							
	7							0

Name	Description
DISCHARGE_TIME[7:0] Leading bits at next address.	Sets CDC discharge time $t_{discharge}$. Time interval reserved for discharge time measurement. $t_{discharge}$ = (DISCHARGE_TIME + 1) * $T_{cycleclock}$ 0 := $t_{discharge}$ = 1 * $T_{cycleclock}$

Reg	7	6	5	4	3	2	1	0
24	C_STARTONPIN		C_TRIG_SEL_ALT		C_TRIG_SEL		DISCHARGE_TIME	
	1	0	1	0	1	0	9	8

Parameter	Description	Settings	
C_STARTONPIN[1:0]	Selection of the GPIO port that permits triggering a CDC start	0:= PG0, 1:= PG1, 2:= PG2, 3:= PG3	
C_TRIG_SEL_ALT[1:0]	Same, but written to an alternative register bank under DSP control (the DSP is free to toggle between those two banks)	0:= stretched mode 1:= immediate loop-back ("continuous run") 2:= conversion trigger timer 3:= rising edge at one of the GPIO ports	0 to 3: op code 'h8C is always a possible trigger for the CDC
C_TRIG_SEL[1:0]	Selection of the trigger source accepted for starting the CDC		

DISCHARGE_TIME[9:8]	Leading bits to preceding address		

Reg	7	6	5	4	3	2	1	0
25	PRECHARGE_TIME							
	7							0
26			C_FAKE				PRECHARGE_TIME	
			3			0	9	8

Name	Description
PRECHARGE_TIME[9:0] Leading bits at next address.	Sets CDC precharge time $t_{precharge}$. $t_{precharge}$ =(PRECHARGE_TIME + 1) * $T_{cycleclock}$ 0 := no precharge
C_FAKE[3:0]	Number of ”fake“ or ”warm-up” measurements for the CDC, performed just before the “real” ones; the “fake” values do not count

Reg	7	6	5	4	3	2	1	0
27	FULLCHARGE_TIME							
	7							0
28	EE_SINGLE_WR_EN	EE_WR_EN	EE_DISABLE	EE_IFC_PRIO	EE_WAKE UP_MODE	EE_ON	FULLCHARGE_TIME	
							9	8

Name	Description	Settings
FULLCHARGE_TIME [9:0]	Sets the fullcharge time $t_{fullcharge}$, the time interval to charge up fully to maximum voltage. $t_{fullcharge}$ = (FULLCHARGE_TIME + 1) * $T_{cycleclock}$ 0 := no fullcharge	
EE_SINGLE_WR_EN	EEPROM Single write protection: Does not affect EEPROM read access!	0 := no single write action is allowed 1 := if EE_WR_EN == 1 a single write is allowed
EE_WR_EN	EEPROM Write protection bit. Does not affect EEPROM read access!	0 := no write/erase to EEPROM is possible 1 := write/erase access to EEPROM is allowed
EE_DISABLE	EEPROM disable	0 := EEPROM enabled 1 := EEPROM completely disabled, no read access possible
EE_IFC_PRIO	acam internal bits	default := 0
EE_WAKEUP_MODE	select read and write setup time for EEPROM	0 := 1.5 *t_{OCF} 1 := 10µs
EE_ON	EE_ON wakes up the	0 := wakes up the EEPROM

	EEPROM permanently. If EE_ON=0, every access to the EEPROM wakes up the EEPROM and sends it to sleep immediately afterwards. That consumes time. With EE_ON=1 faster access is possible for frequent EEPROM operations. With EE_ON=1 the current consumption rises by appr. 20µA	only during access 1 := EEPROM is awake permanently

Reg	7	6	5	4	3	2	1	0
29	R_STARTONPIN		R_TRIG_SEL_ALT			R_TRIG_SEL		
	1	0	2		0	2		0

Parameter	Description	Settings
R_STARTONPIN[1:0]	Use not recommended	0
R_TRIG_SEL_ALT[2:0]	Same, but for the alternative register bank	0 := off 1 := OLF_CLK 3 := Pin triggered 5 := CDC asynchronous (recommended) 6 := CDC synchronous end-of-CDC-conversion-run
R_TRIG_SEL[2:0]	Trigger source selection for the RDC	

Reg	7	6	5	4	3	2	1	0
30	7			R_TRIG_PREDIV				0
31	15							8
32	R_AVRG							
	1	0	21					16

Parameter	Description	Settings
R_TRIG_PREDIV[21:0]	Predivider, permits to make less temperature measurements than capacitance measurements. This is a factor between measurement rates of CDC over RDC. It is used also as OLF clock divider if OLF is used as trigger source.	0=1:= every signal triggers 2:= every 2nd signal triggers 3:= every 3rd signal triggers etc. 2^{21} := maximum factor (~2M)
R_AVRG[1:0]	Sample size for the mean value calculation (averaging) in the RDC part	0:= not averaged 1:= 4-fold averaged 2:= 8-fold averaged 3:= 16-fold averaged

Reg	7	6	5	4	3	2	1	0
33	R_SENSE_INVERT	R_FAKE	R_QHA_SEL 5					0

Parameter	Description	Settings
R_SENSE_INVERT		0 := recommended setting
R_FAKE	Number of "fake" or "warm-up" measurements for the RDC, performed just before the "real" ones; the "fake" values do not count	0:= 2 fake cycles per average value 1:= 8 fake cycle per average value
R_QHA_SEL	acam internal bits	mandatory :=0

Reg	7	6	5	4	3	2	1	0
34		R_REF_SEL	R_3EXT_SEL	R_PT1_EN	R_PT0_EN	R_PT2REF_EN	R_PORT_EN_IMES	R_PORT_EN_IREF

Parameter	Description	Settings
R_REF_SEL	Choice of reference for the RDC part	0:= external at port PT0 1:= internal polysilicon strip
R_3EXT_SEL	Permits to measure 3 external sensors, if and only if the internal refe-rence is used	0:= fewer than 3 external sensors, external reference possible 1:= three external sensors; the internal reference is to be used
R_PT1_EN	Port activation for the RDC part	0:= disabled 1:= activates port PT1
R_PT0_EN	Port activation for the RDC part	0:= disabled 1:= activates port PT0
R_PT2REF_EN	Port activation for the RDC part	activates port PT2REF
R_PORT_EN_IMES	Port activation for internal aluminum temperature sensor	0:= disabled 1:= enabled
R_PORT_EN_IREF	Port activation for internal reference resistor	0:= disabled 1:= enabled

Reg	7	6	5	4	3	2	1	0
35	C_REF_SEL 4				0	R_CY	R_OLF_DIV 1	0

Parameter	Description	Settings
C_REF_SEL[4:0]	Setting the on-chip reference capacitor for the	0:= minimum 1:= approx.1 pF

	CDC Note: step width varies from 0.3pF to 1.5pF	31:= maximum (approx. 31 pF)
R_CY	Cycle-time for the RDC part	0:= 140 µs 1:= 280 µs
R_OLF_DIV[1:0]	Clock divider for the RDC part. Depends on the OLF_CTUNE (and OLF_FTUNE). Target frequency is about 10kHz for the RDC part.	0:= /1 (for OLF = 10kHz) 1:= /4 (for OLF = 50kHz) 2:= /8 (for OLF = 100kHz) 3:= /16 (for OLF = 200kHz)

Reg	7	6	5	4	3	2	1	0
36				RTC_CLK_SEL	RTC_EN	LBD_CLK_SEL	TDC_NOISE_CY_DIS	

Parameter	Description	Settings
RTC_CLK_SEL	Clock source selection for the real-time clock (RTC), External 32-kHz quartz required. The internal OLF is not precise enough.	0 := OLF clock 1 := ext. HF
RTC_EN	Activate the real-time clock (RTC)	
LBD_CLK_SEL	Clock source selection for the low-battery detection	0 := OLF clock 1 .= OLF clock / 16
TDC_NOISE_CY_DIS	acam internal bits	mandatory := 0

Reg	7	6	5	4	3	2	1	0
37	TDC_MUPU_NO						TDC_FIN_ADJ	
	5					0	1	0

Parameter	Description	Settings
TDC_MUPU_NO	acam internal bits	mandatory := 0
TDC_FIN_ADJ	acam internal bits	mandatory := 0

Reg	7	6	5	4	3	2	1	0
38	TDC_QHA_SEL							
	5					0		

Parameter	Description	Settings
TDC_QHA_SEL	acam internal bits	mandatory := 13

Reg	7	6	5	4	3	2	1	0
39		TEBU_SEL 1 0		EE_VEE2_ ENA	EE_VEE1_ ENA	EE_EETEST_ ENA	TDC_CALWIDTH 1	0

Parameter	Description	Settings
TEBU_SEL	acam internal bits	mandatory := 0
EE_VEE2_ENA	acam internal bits	mandatory := 0
EE_VEE1_ENA	acam internal bits	mandatory := 0
EE_EETESTR_ENA	acam internal bits	mandatory := 0
TDC_CALWIDTH	acam internal bits	mandatory := 0

Reg	7	6	5	4	3	2	1	0
40	DSP_MOFLO_EN 1 0		DSP_CLK_MODE 1 0		DSP_SPEED 1 0		PG1xPG3	PG0xPG2

Name	Description	Settings
DSP_MOFLO_EN[1:0]	Enable the mono-flop (antibouncing filter)" in the GPIO pulse line.	0 = off 3 = on
DSP_CLK_MODE	Select the clock source for the DSP	0 = ring oscillator 1 = LF clock 3 = HF clock
DSP_SPEED	DSP speed	0 = fastest 3 = slowest
PG1xPG3	Switch PG1/PG3 wiring to/from DSP	0 = pulse output at PG3 1 = pulse output at PG1
PG0xPG2	Switch PG0/PG2 wiring to/from DSP	0 = pulse output at PG2 1 = pulse output at PG0

Reg	7	6	5	4	3	2	1	0
41	WD_TIME 7							0

Name	Description	Settings
WD_TIME[7:0]	Watch-dog timer, normally in multiples of 50 milliseconds, if OCF is tuned to 5 kHz as it should. Watchdog is started together with DSP and designed to be reset by a DSP command before the	$t_{watchdog}$ = WD_TIME * 50 ms

	watchdog time is reached. Otherwise a power-up reset is initiated.

Reg	7	6	5	4	3	2	1	0
42	DSP_STARTONPIN				DSP_FF_IN			
	3			0	3			0

Name	Description	Settings
DSP_STARTONPIN	Pin mask for starting the DSP" - This mask permits assigning one or more GPIO pins to start the DSP	Bitwise PG0 to PG3
DSP_FF_IN	Pin mask for flip-flop activation	Bitwise DSP_IN_0 to DSP_IN_3

Reg	7	6	5	4	3	2	1	0
43	INT2PG2	DSP_ SPRAM_SEL	DSP_START	DSP_START_EN				
				4				0

Name	Description	Settings
INT2PG2	Define PG2 as an additional interrupt port (useful for small packages with no dedicated INTN pin)	0 := INTN port only 1 := INTN and PG2 in parallel
DSP_SPRAM_SEL	Selects between SRAM and OTP memory as a program memory, where the DSP is to be controlled from	0 := OTP memory 1 := SRAM
DSP_START	Trigger DSP directly by Interface. Remark, DSP_START must be set to 0 by user.	1 := Trigger DSP
DSP_START_EN[4:0]	Mask for activating various trigger sources for starting the DSP	

Bit	Trigger condition
#0	End-of-CDC-conversion-run
#1	timer
#2	End-of-RDC-conversion-run
#3	INT_TRIG_EN (rising edge of INT)
#4	Error in front-end

Reg	7	6	5	4	3	2	1	0
44	PI1_CLK_SEL				PI0_CLK_SEL			
	3			0	3			0

Name	Description	Settings	
PI1_CLK_SEL[3:0] PI0_CLK_SEL[3:0]	Base frequency for the pulse-code interfaces, based on OLF or OHF, separately for the pulse paths 0 and 1	4 := OHF * 2 5 := OHF 6 := OHF / 2 7 := OHF / 4 8 := OLF * 2 9 := OLF	10 := OLF / 2 11 := OLF / 4 12 := RO 13 := RO / 2 14 := RO / 4

Reg	7	6	5	4	3	2	1	0
45	PI_EN				PI1_RES		PI0_RES	
	3			0	1	0	1	0

Name	Description	Settings
PI_EN[3:0]	Enables pulse-code generation, either pulse-density or pulse-width, separately for the pulse paths 0 and 1	b'xx01 := PWM at path 0 b'xx10 := PDM at path 0 b'01xx := PWM at path 1 b'10xx := PDM at path 1
PI1_RES[1:0] PI0_RES[1:0]	Resolution of the pulse-code interfaces	0 := 10 bit 1 := 12 bit 2 := 14 bit 3 := 16 bit

Reg	7	6	5	4	3	2	1	0
46	PG_DIR_IN				PG_PU			
	3			0	3			0

Name	Description	Settings	
PG_DIR_IN[3:0]	Toggles general-purpose port direction between input and output	0 := output 1 := input	#0 and #4: PG0 #1 and #5: PG1 #2 and #6: PG2 #3 and #7: PG3
PG_PULLUP[3:0]	Activates protective pull-up resistors at general-purpose ports	0 := idle 1 := active	

Reg	7	6	5	4	3	2	1	0
47			BG_PERM	BG_TRIM0				
				4				0

Name	Description	Settings
BG_PERM	activate Bandgap permanently . With BG_PERM = 1 the current consumption rises by appr. 20µA	1 := Bandgap permanent enabled 0 := Bandgap pulsed
BG_TRIM0[4:0]	Trim the internal bandgap / core-powersupply for normal operating	'h00 := 1.68V ... 'h07 := 1.8V ... 'h1F := 2.2V

Reg	7	6	5	4	3	2	1	0
48	TDC_NOISE_DIS	TDC_MUPU_SPEED		TDC_MR2	BG_TRIM1			
		1	0		3			0

Name	Description	Settings
TDC_NOISE_DIS	acam internal bits	mandatory := 0
TDC_MUPU_SPEED	TDC specific speed select	mandatory := 1
TDC_MR2	TDC specific measure range select	0 := MR1 1 := MR2
BG_TRIM1[3:0]	Trim the internal bandgap / core-powersupply for Low-Bat-Detection (LBD) and EEPROM writing	recommended := 'h07

Reg	7	6	5	4	3	2	1	0
49	TDC_ALUPERMOPEN	TDC_ALUSLOW	TDC_CHAN_EN		TDC_CALAVG	TDC_CAL_DELAY		
			1	0		1	0	

Name	Description	Settings
TDC_ALUPERMOPEN	acam internal bits	mandatory := 0
TDC_ALUSLOW	acam internal bits	mandatory := 0
TDC_CHAN_EN	acam internal bits	mandatory := 3
TDC_CALAVG	acam internal bits	mandatory := 0
TDC_CAL_DELAY	acam internal bits	mandatory := 0

Reg	7	6	5	4	3	2	1	0
50	7							0
51	15			Parameter0				8
52	23							16
53	7							0
54	15			Parameter1				8
55	23							16
56	7							0
57	15			Parameter2				8
58	(mandatory=0)	22						16
59	7							0
60	15			Parameter3				8
61	23							16
62	7							0
63	15			Parameter4				8
64	23							16
65	7							0
66	15			Parameter5				8
67	23							16
68	7							0
69	15			Parameter6				8
70	23							16
71	7							0
72	15			Parameter7 (e.g. Gain_Corr)				8
73	23							16
74	7				DSP_TRIG_CDC	CDC_TRIG_BG	DSP_TRIG_CDC	CDC_TRIG_BG 0
75	15			Parameter8				8
76	23							16

Reg	7	6	5	4	3	2	1	0
77								RUNBIT

Parameter	Description	Settings
RUNBIT	on/off switch for front-end and DSP: It should be "off" during programming and any registry modification, thus protecting the chip from any undesirable/unspecified states	0 := off = the chip system is idle and protected 1 := on = the protection is removed, and the system may run

The RunBit is most useful for debugging and test. A basic thing like testing the interface should include toggling the RunBit. It is mirrored to Read_Address24, bit #0.

5.3 Oscillator Configuration

OLF_CLK Frequency variation over samples ± 20%, OLF_CLK temperature drift ± 5%,

OLF_CLK vs. VDD ± 2%

OLF_CLK-Trimming:

OLF_CTUNE	OLF_FTUNE	OLF Frequency
3 := (10kHz)	1	5 kHz
3 := (10kHz)	7	10 kHz
2 := (50kHz)	0	28 kHz
2 := (50kHz)	3	48 kHz
1 := (100kHz)	4	100 kHz
0 := (200kHz)	5	200 kHz

The several clock sources are available to control the various units of the chip:

OLF_CLK	Description:	Internal low frequency oscillator. It is always running and can't be turned off. It can be configured for frequency range 5 to 200 kHz.
	Sources:	Internal low power oscillator or external 32 kHz quartz
	Application:	May be clock source for pulse interface, CDC, RDC, Real time counter (RTC), DSP, low-battery detection (LBD).
	Parameters:	OLF_CLK_SEL, OLF_CTUNE, OLF_FTUNE, OX_CLK32KHZ_EN
OHF_CLK	Description:	High frequency clock
	Sources:	External or internal HF oscillators (1..20 MHz, typical 4 MHz)
	Application:	Measure range 2, pulse interfaces
	Parameters:	OX_DIS, OX_RUN, OHF_CLK_SEL, OX_AMP_TRIM, OX_DIV4, OX_AUTOSTOP_DIS, OX_STOP
OCF_CLK	Description:	Constant clock, needs to be set to 5 kHz
	Sources:	OLF_CLK
	Application:	EEPROM, Watchdog
	Parameters:	OCF_TIME

RTC_CLK	Description:	Clock for real time counter (RTC)
	Sources:	OFL_CLK (possible but not recommended) or external HF oscillator (32 kHz)
	Application:	RTC
	Parameters:	RTC_CLK_SEL, RTC_EN

5.3.1 RTC (Real Time Counter)

There is a real time counter which can be used to have long-term timing information. The use demands an external 32.768 kHz oscillator. The RTC is a Gray-counter with 2^{17} pre-divider, which gives a base period of 4 seconds and a measurement range of 3 days and 49 minutes. The count is given in Gray-code. It can be interpreted only by the DSP.

The RTC is turned on by setting configuration bit RTC_EN = 1.

The base clock is selected by parameter RTC_CLK_SEL.

5.4 Low Battery Detection (LBD)

PCapØ2 has the capability to monitor the voltage. The voltage measurement is started by setting DSP output bit TRIG_LBD (Bit 14). This bit is set back to 0 automatically. The end of the voltage measurement is indicated by DSP input bit LBD_BUSY (Bit 8) which indicates whether the process is still running. At the end, the voltage information can be read back from RAM address 92: LBD_DATA. The result is a 6 bit integer. The calculation of the voltage depends on the trim of the bandgap. The relevant configuration parameter is BG_TRIM1 in configuration register 48. The recommended setting is BG_TRIM1 = 7.

With this setting the voltage is calculated according to:

Voltage = 2.026 V + LBD_DATA * 24.4 mV

With LBD_CLK_SEL the base clock for the low battery detection measurement is selected between OLF and OLF/16, But this has no effect on the result. Voltage conversion needs 17 respectively 17x16 OLF clk cycles.

5.5 Read Registers

PCapØ2 has 44 byte of RAM for read access, combined as triples of 3 byte.

Table 5-2 Read registers

Reg	7	6	5	4	3	2	1	0
0	7							0
1	15				**Res0**			8
2	23							16
3	7							0
4	15				**Res1**			8
5	23							16
6	7							0
7	15				**Res2**			8
8	23							16
9	7							0
10	15				**Res3**			8
11	23							16
12	7							0
13	15				**Res4**			8
14	23							16
15	7							0
16	15				**Res5**			8
17	23							16
18	7							0
19	15				**Res6**			8
20	23							16
21	7							0
22	15				**Res7**			8
23	23							16
24	7							0
25	15				**Status**			8
26	23							16
27	31							24
28	39				**Res0**			32
29	47							40
30	31							24
31	39				**Res1**			32
32	42							40
33	7							0
34	15				**Res8**			8
35	23							16
36	7							0
37	15				**Res9**			8
38	23							16
39	7							0
40	15				**Res10**			8
41	23							16
42	7							0
43	15				**Res11**			8
44	23							16

The read registers are made of 11 result registers. Res0 and Res1 may have 48 bit, even, whereas the higher 24 bit are at addresses 27 to 32. Addresses 24 to 26 contain the status register.

5.5.1 Result Registers

The content of the results registers depends on the firmware. The following describes the result registers as they are used by the standard firmware.

Table 5-3 Result registers with standard firmware

<table>
<tr><th>Name</th><th>Length</th><th>Format</th><th>Meaning</th></tr>
<tr><td>Res0</td><td rowspan="12">24 bits</td><td>Integer</td><td>For debugging only. The CDC discharge time, see note below.</td></tr>
<tr><td>Res1</td><td rowspan="10">Unsigned fixed-point number:
3 bits integer
21 bits fractional

min = ‘h0 =
= 0.0000000

max = ‘hFFFFFF =
= 7.9999995</td><td><table><tr><th></th><th>ordinary C</th><th>differential C</th></tr><tr><td>Res1</td><td>ratio C1 / C0</td><td>ratio C1 / C0</td></tr><tr><td>Res2</td><td>C2 / C0</td><td>C3 / C2</td></tr><tr><td>Res3</td><td>C3 / C0</td><td>C5 / C4</td></tr><tr><td>Res4</td><td>C4 / C0</td><td>C7 / C6</td></tr><tr><td>Res5</td><td>C5 / C0</td><td>zero</td></tr><tr><td>Res6</td><td>C6 / C0</td><td>zero</td></tr><tr><td>Res7</td><td>C7 / C0</td><td>zero</td></tr></table></td></tr>
<tr><td>Res2</td><td></td></tr>
<tr><td>Res3</td><td></td></tr>
<tr><td>Res4</td><td></td></tr>
<tr><td>Res5</td><td></td></tr>
<tr><td>Res6</td><td></td></tr>
<tr><td>Res7</td><td></td></tr>
<tr><td>Res8</td><td>Res8 not assigned</td></tr>
<tr><td>Res9</td><td>Res9 not assigned</td></tr>
<tr><td>Res10</td><td rowspan="2">Res10 and Res11:
ratio R_temperature / R_reference, depending on the particular setting of the RDC front-end, see there</td></tr>
<tr><td>Res11</td></tr>
</table>

The user is free to assign any data to the results registers in his own firmware.

Note: The integer value Res0, multiplied by the TDC bin size (≈21 picosecond best case, typically 22...23 ps) yields the discharge time at port PC0, useful for debugging and design.

5.5.3 Status Register Details

Table 5-4 Address 24, STATUS_0

Bit #	Name	Explanation
0	RunBit	The RunBit from write register 77 is mirrored here
1	CDC active	Warning: traffic on interface may enhance noise in measurement
2	RDC ready	
3	EEPROM busy	
4	AutoBoot busy	
5	POR_Flag_SRAM	A memory mismatch error from an SRAM-to-OTP comparison has been detected and has provoked a power-up reset
6	POR_Flag_Config	same, but inside Configuration registry rather than SRAM-to-OTP
7	POR_Flag_Wdog	A watchdog overflow has been detected and has provoked a power-up reset. Perhaps the firmware has hung up in an unwanted endless loop or, more likely, a CDC/RDC trigger signal has been lost.

#5, #6 and #7 may signal erratic states provoked by stochastic disturbances.

Table 5-5 Address 25, STATUS_1

Bit #	Name	Explanation
0	Comb_Err	All error bits, from here onward, disjunctively combined (using bit-or)
1	Err_Ovfl	An overflow error occurred when the CDC unit was busy
2	Mup_Err	A particular kind of TDC error occurred when the CDC unit was busy
3	RDC_Err	Some kind of error occurred when the RDC unit was busy
4 - 7	n.c.	test bits (no error bits)

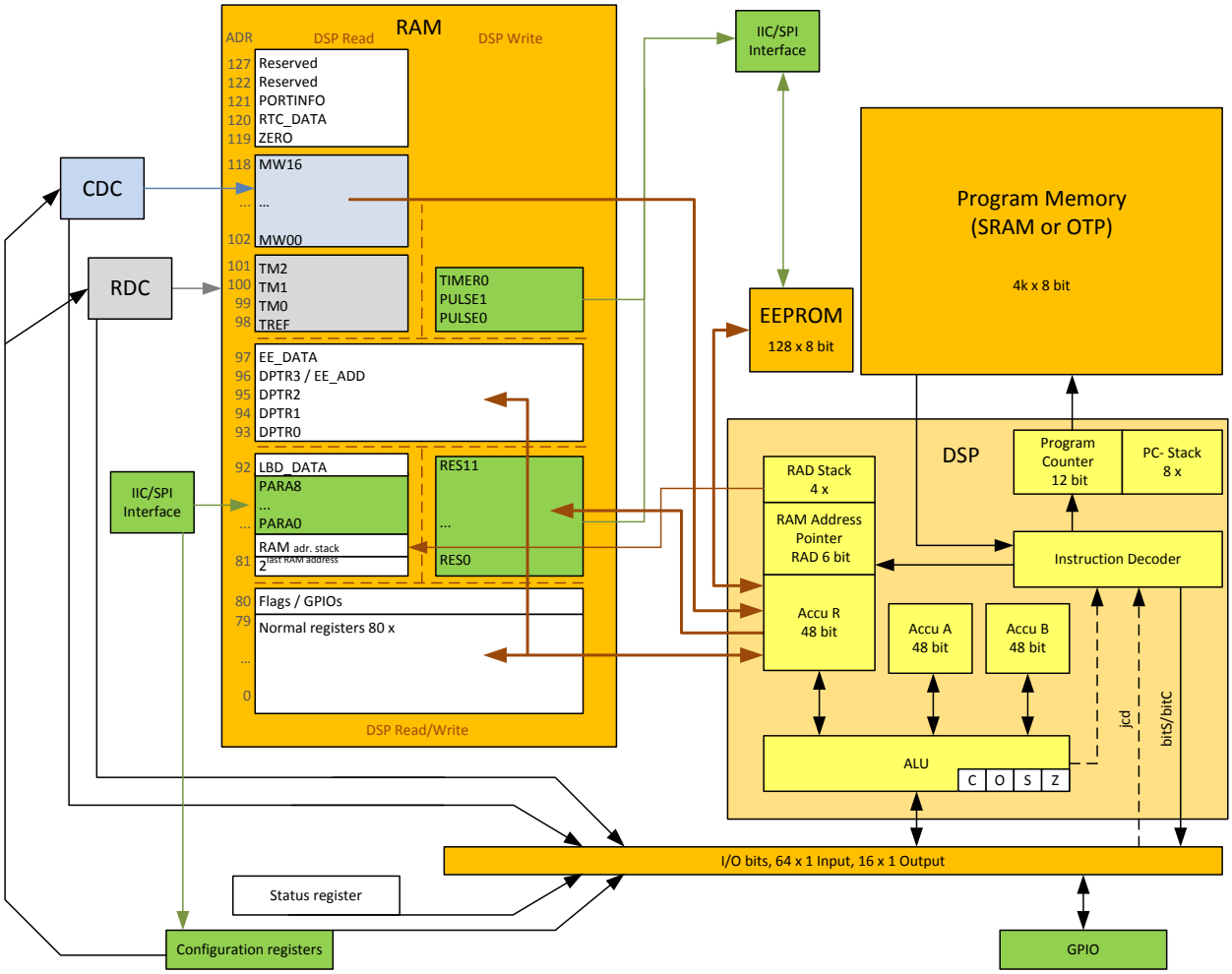
Table 5-6 Address 26, STATUS_2

Bit #	Name	Port con-cerned	Explanation
0	C_PortError0	PC0	In the CDC unit, one or several ports are affected by some error like a short-circuit to ground. May also be a charge/ discharge resistivity too big, a capacitance too big, or an ill-defined precharge/fullcharge/discharge time.
1	C_PortError1	PC1	
…	…	…	
7	C_PortError7	PC7	

6 DSP & Memory

A digital signal processor (DSP) in Harvard architecture has been integrated. It is programmable and responsible for the content of all the result registers – with the exception of the hard-wired status register. The software, called “firmware”, is either available ready-made from acam or can be written by the user himself. In this datasheet we describe only the standard firmware as provided by acam. This firmware writes the compensated capacitance ratios and the resistance ratios to the result registers, signals an interrupt (INTN) and does a first-order linearization and scaling for the pulse-code outputs. However, it does no higher-order linearization, filtering or any other data processing, even though this is largely possible and library elements are available for user-programming.

Figure 6-1 DSP & Memory



This Harvard DSP for 48 bit wide parallel data processing is coupled to a 128 x 48 bit RAM, 80 x 48 bit thereof free accessible. The DSP is internally clocked at approximately 55 MHz. The clock generator is stopped through a firmware command, so as to save power. The DSP starts again upon a GPIO signal or an “end of measurement run” condition.

The DSP is acam proprietary, designed for low-power tasks as well as very high data rates. It is programmable in Assembler (there is no high-level language available). A user-friendly assembler software providing a graphical interface, help text pop-ups and sample code sustain programming efforts. Subroutines are possible down to the seventh order.

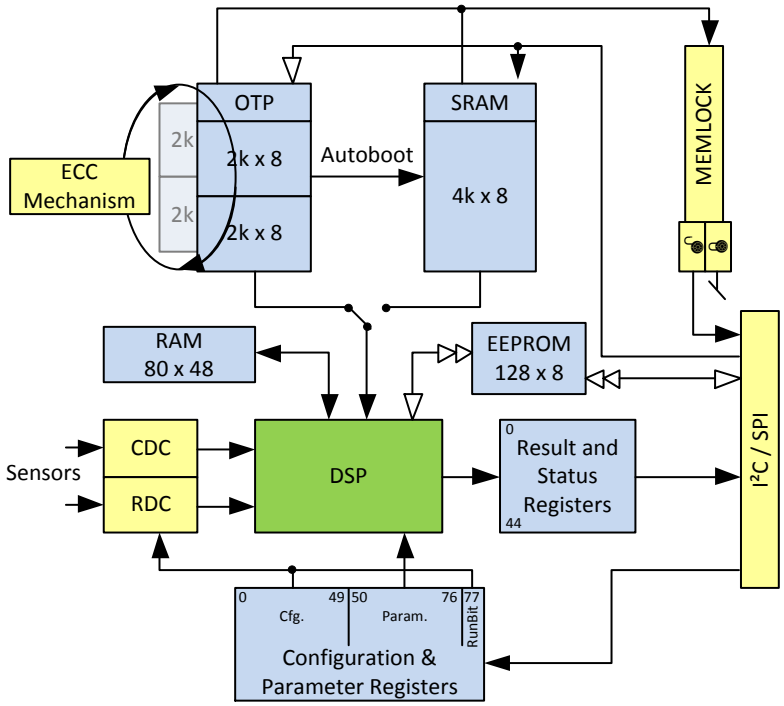
6.1 Memory Map

Table 6-1 Memory Map

Address		SRAM (volatile)		OTP (permanent: non-volatile, non-erasable)					
				direct/single		double		quad	
dec.	hex.	Contents	Length (byte)	Contents	Length (byte)	Contents	Length (byte)	Contents	Length (byte)
4095 … 4016	FFF … FB0	Program code	4096	Config. & Param.	80	Config.& Param.	80	Config.& Param.	80
4015 … 4011	FAF … FAB			not for use	5	not for use	5	not for use	5
4010 … 2048	FAA … 800h			Program code	4011	Program code	4011	Program code	1963
2047 … 1968	7FF … 7B0							Config.& Param.	80
1967 … 1963	7AF … 7AB							not for use	5
1962 … 0	7AA … 000							Program code	1963

6.2 Memory Management

Figure 6-2 Memory management



6.2.1 SRAM Data Integrity

The DSP can be operated either from SRAM (for maximum speed) or from OTP (for low power). When operated from SRAM, an SRAM-to-OTP data integrity monitor can be activated through parameter MEMCOMP in register 0, but must (!) be deactivated for operation directly from OTP.

When the MEMCOMP option is activated, the DSP compares the content of the SRAM with the OTP content at regular intervals if the following conditions are fulfilled:

- Configuration is set for copying OTP content to SRAM and the program runs from the SRAM (DSP_SRAM_SEL=1 in Reg. 43) , AND
- DSP runs on the ring oscillator clock.

The DSP executes the comparison during those times when it is not running other tasks or firmware. When a mismatch occurs during comparison, a power-on reset is generated, and the data is copied freshly from the OTP to the SRAM again, and the execution starts again. Thus data integrity is ensured using this mechanism.

6.2.2 Memory integrity using ECC

The memory integrity mechanism in PCap surveys the OTP contents internally and corrects faulty bits as far as possible. Data validity in the OTP memory is ensured using a built-in ECC mechanism. There are three possible ECC modes configurable in Register 1

(ECC_MODE). Depending on the mode selected, the maximum size of the program code is limited, and the method of redundancy implemented varies.

In general, the ECC mechanism is a bit error detection and automatic correction. The following are the different mechanisms depending on the ECC_MODE bits.

ECC_MODE = 'h00 in Configuration register 1:

Direct / single: In this setting, no error detection/correction is performed. Thus the maximum allowed programmable space of 4kB is available for program code.

ECC_MODE = 'h0F in Configuration register 1:

Double: When this option is set, the data integrity is achieved by redundancy in the form of parity generation. For the 4 kB program code (maximum), 4kB of parity is generated and programmed in the chip. For every single byte of program code read from the chip, the parity byte is immediately checked and if erroneous, the code byte is automatically corrected.

Note: When you want to program the OTP on your own (without using acam's PCap Frontpanel software), then the generator matrix to generate the parity bytes can be made available to you. Please contact support@acam.de in that case.

ECC_MODE = 'hF0 in Configuration register 1:

Quad: When this option is configured, data integrity is achieved by pure mirroring, i.e. by storing the same program code 4 times as identical copies in the memory. This limits the maximum size of the program code to 2 kB. So, when a single byte of program code is read, actually, the same byte is read from all the four banks and a logical bitwise AND of the four results is performed and given out as the correct byte.

Note: Un-programmed bits in the OTP are '1'.

6.2.3 Memory Read Protection

Clearing the MEM_LOCK_DIS bits in Configuration register 2 activates the memory read-out protection mechanism. Once set, the contents of the OTP and the SRAM (if executing from it) cannot be read out anymore, thus securing your intellectual property from unauthorized access. MEMLOCK gets active earliest after it has been written to the OTP and the chip has got a power-on reset.

6.3 Getting started

For principal operation PCapØ2 needs two things:

- Configuration
- Firmware

When working the first time with the chip the OTP is blank. There is no firmware in the chip and the chip is not configured. First, the configuration registers have to be set correctly. Then, as a starting point, the standard firmware (PCapØ2_standard.hex) should be written to the SRAM. With this firmware the chip works as simple CDC that provides pure capacitance ratios and resistance ratios.

Once a custom specific firmware is written and approved, this firmware can be written into the OTP, together with the configuration. Then, after a power-on reset, the firmware and configuration can be loaded automatically and the chip is ready for measurement, even in stand-alone operation.

6.3.1 Using the Standard Firmware

1. ‘hC0 4D 00 ; Write configuration, Disable converter: RunBit = 0
2. ‘hC0 00 0F 00 01 94 80 05 01 04 A8 00 30 00 0F 01 00 00 00 D0 07 00 00 00 00 02 08 01 00 02 00 05 05 00 00 00 43 05 00 00 34 00 00 00 00 44 00 00 FF 00 07 30 01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 01 00 00 00 00 20 01 ; Write config. registers 0 to 76, PCa02_standard.cfg
3. ‘h90 00 00 00 00 7A C0 CF FF F0 D2 43 7A D0 34 62 63 00 65 7A C4 D1 43 7A D0 33 AB 47 42 5C 48 … 6A C9 7A C0 C0 C0 C9 D2 43 7A DD 44 6A F2 44 6A F3 44 7A ; Write SRAM, PCapØ2_standard.hex firmware
4. ‘hC0 4D 01 ; Write configuration, Enable converter: RunBit = 1
5. ‘h8A ; Send partial reset
6. ‘h8C ; Start measurement
7. ‘h40 24 00 00 00 ; Read status, addresses 24, 25, 26
8. ‘h40 03 00 00 00 ; Read Res1, addresses 3, 4, 5. Res1 is expected to be in the range of 2,000,000 or ’h2000XX if the two capacitors are of same size. Res1 has the format of a fixed point number with 3 integer digits and 21 fractional digits. So, dividing the 2,000,000 by 2^{21} gives a factor of about 1 for the ratio C1/C0.

7 Miscellaneous

7.1 Bug Report

7.1.1 Port Pattern

Description:

With parameter C_PORT_PAT = 1 the order of the measured ports will be reversed after each sequence. This does not work in combination with PCapØ2 mode & conversion timer & AVRG != 0.

Workaround:

Don't use the critical combination of parameters.

7.2 I²C Bug with POR directly after rd/wr OTP/SRAM

Description:

The bug refers to configurations that combine autoboot == 1 && DSP_SRAM == 1 && I2C_EN == 1. If a power-on reset is sent directly after a write to OTP or write to SRAM had been sent then all data will be manipulated when being copied from OTP to SRAM. They will be set to data = data or ´h10. This does not happen in SPI communication mode.

The error behavior is not critical in stand-alone applications because in such applications there is no write access to OTP or SRAM.

Workaround:

Before sending the POR command send a "read from OTP" command.

7.3 Limitation of Parameter2

Description:

Under certain circumstances, a '1' in bit 23 of Parameter2 causes that no results can be read out.

Workaround:

Don't use the highest bit of register 58[7], (Parameter2[23]), but set it to 'O'.

7.4 History

- 22.08.2012 First draft version
- 11.10.2012 release version v0.2 including bug report
- 19.01.2013 Version 1.0 for final silicon PCapØ2A
- 05.02.2013 Section 5, Reg 2, 7, 33, 34 description and settings
- 14.02.2013 Section 1, 2.2.2 buffer capacitors. 5.4 Low battery detection, 2.6.4
- 16.07.2013 New section 2.4 Internal RC-Oscillator; 7.3 Limitation of Parameter2 section 4.6 GPIO table expanded
- 06.12.2013 section 6.3.1 corrected RunBit register address (reg. 77 = 'h4D)
- 13.03.2014 Section 3.4.4 RDC Trigger
- 19.05.2014 Section 2.2.4 Temperature-dependent Gain and Offset error
- 29.05.2014 New section 2.4 Oscillators,internal and external

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