



150-mW STEREO AUDIO POWER AMPLIFIER

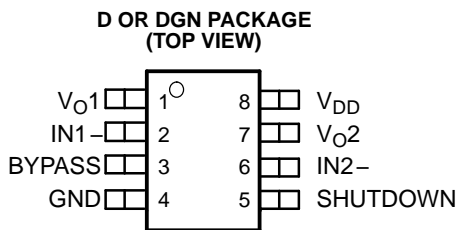
FEATURES

- 150-mW Stereo Output
- PC Power Supply Compatible
 - Fully Specified for 3.3-V and 5-V Operation
 - Operation to 2.5 V
- Pop Reduction Circuitry
- Internal Midrail Generation
- Thermal and Short-Circuit Protection
- Surface-Mount Packaging
 - PowerPAD™ MSOP
 - SOIC
- Pin Compatible With LM4880 and LM4881 (SOIC)

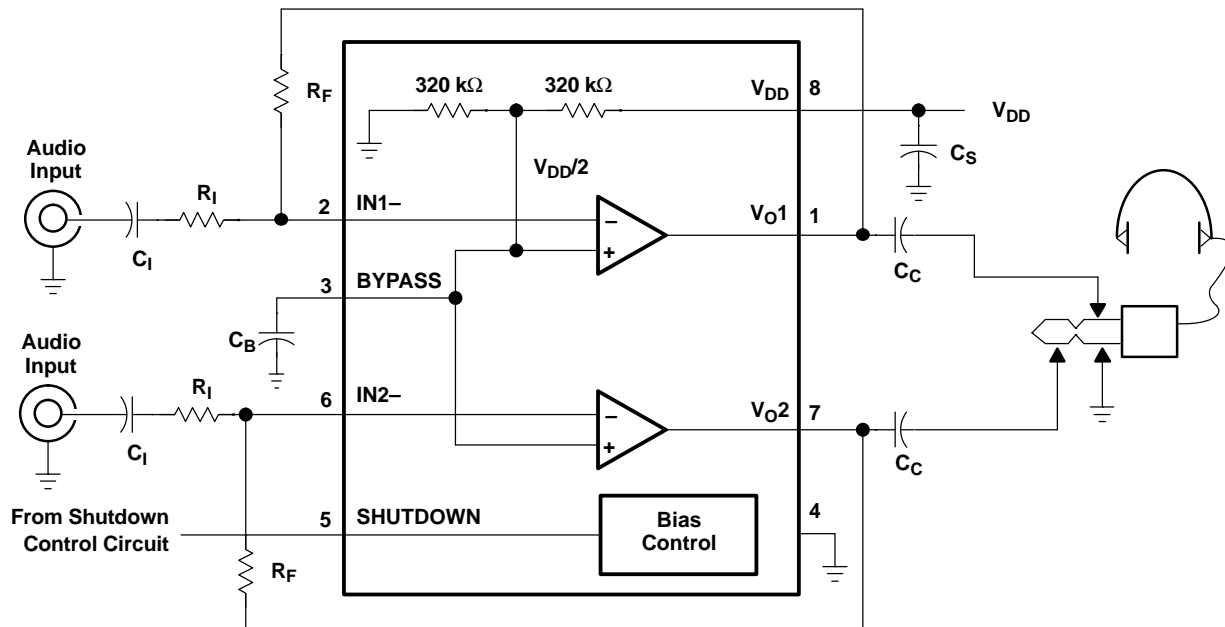
DESCRIPTION

The TPA122 is a stereo audio power amplifier packaged in either an 8-pin SOIC, or an 8-pin PowerPAD™ MSOP package capable of delivering 150 mW of continuous RMS power per channel into 8-Ω loads. Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 1 to 10.

THD+N when driving an 8-Ω load from 5 V is 0.1% at 1 kHz, and less than 2% across the audio band of 20 Hz to 20 kHz. For 32-Ω loads, the THD+N is reduced to less than 0.06% at 1 kHz, and is less than 1% across the audio band of 20 Hz to 20 kHz. For 10-kΩ loads, the THD+N performance is 0.01% at 1 kHz, and less than 0.02% across the audio band of 20 Hz to 20 kHz.



TYPICAL APPLICATION CIRCUIT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

T _A	PACKAGED DEVICES		MSOP SYMBOLIZATION
	SMALL OUTLINE ⁽¹⁾ (D)	MSOP ⁽¹⁾ (DGN)	
–40°C to 85°C	TPA122D	TPA122DGN	TI AAE

(1) The D and DGN packages are available in left-ended tape and reel only (e.g., TPA122DR, TPA122DGNR).

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
BYPASS	3	I	Tap to voltage divider for internal mid-supply bias supply. Connect to a 0.1 μF to 1 μF low ESR capacitor for best performance.
GND	4	I	GND is the ground connection.
IN1-	2	I	IN1- is the inverting input for channel 1.
IN2-	6	I	IN2- is the inverting input for channel 2.
SHUTDOWN	5	I	Puts the device in a low quiescent current mode when held high
V _{DD}	8	I	V _{DD} is the supply voltage terminal.
V _{O1}	1	O	V _{O1} is the audio output for channel 1.
V _{O2}	7	O	V _{O2} is the audio output for channel 2.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	UNIT
V _{DD} Supply voltage	6 V
V _I Input voltage	–0.3 V to V _{DD} + 0.3 V
Continuous total power dissipation	Internally limited
T _J Operating junction temperature range	–40°C to 150°C
T _{stg} Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
DGN	2.14 W ⁽¹⁾	17.1 mW/°C	1.37 W	1.11 W

(1) See the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* of that document.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V _{DD}	Supply voltage	2.5	5.5	V
T _A	Operating free-air temperature	–40	85	°C
V _{IH}	High-level input voltage, (SHUTDOWN)	0.80 × V _{DD}		V
V _{IL}	Low-level input voltage, (SHUTDOWN)	0.40 × V _{DD}		V

DC ELECTRICAL CHARACTERISTICS

at T_A = 25°C, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OO}	Output offset voltage			10	mV
PSRR	Power supply rejection ratio	V _{DD} = 3.2 V to 3.4 V		83	dB
I _{DD}	Supply current	V _{DD} = 2.5, SHUTDOWN = 0 V		1.5	3 mA
I _{DD(SD)}	Supply current in SHUTDOWN mode	V _{DD} = 2.5, SHUTDOWN = V _{DD}		10	50 μA
Z _I	Input impedance			> 1	MΩ

AC OPERATING CHARACTERISTICS

V_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P _O	Output power (each channel)	THD ≤ 0.1%		70 ⁽¹⁾	mW
THD+N	Total harmonic distortion + noise	P _O = 70 mW, 20 Hz–20 kHz		2%	
B _{OM}	Maximum output power BW	G = 10, THD < 5%		> 20	kHz
	Phase margin	Open loop		58°	
	Supply ripple rejection	f = 1 kHz		68	dB
	Channel/channel output separation	f = 1 kHz		86	dB
SNR	Signal-to-noise ratio	P _O = 100 mW		100	dB
V _n	Noise output voltage			9.5	μV(rms)

(1) Measured at 1 kHz

DC ELECTRICAL CHARACTERISTICS

at T_A = 25°C, V_{DD} = 5.5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OO}	Output offset voltage			10	mV
PSRR	Power supply rejection ratio	V _{DD} = 4.9 V to 5.1 V		76	dB
I _{DD}	Supply current	SHUTDOWN = 0 V		1.5	3 mA
I _{DD(SD)}	Supply current in SHUTDOWN mode	SHUTDOWN = V _{DD}		60	100 μA
I _{IH}	High-level input current (SHUTDOWN)	V _{DD} = 5.5 V, V _I = V _{DD}		1	μA
I _{IL}	Low-level input current (SHUTDOWN)	V _{DD} = 5.5 V, V _I = 0 V		1	μA
Z _I	Input impedance			> 1	MΩ

AC OPERATING CHARACTERISTICS $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 8\ \Omega$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD \leq 0.1%		70 ⁽¹⁾		mW
THD+N	Total harmonic distortion + noise	$P_O = 150\text{ mW}$, 20 Hz–20 kHz		2%		
B_{OM}	Maximum output power BW	$G = 10$, THD < 5%		> 20		kHz
	Phase margin	Open loop		56°		
	Supply ripple rejection ratio	$f = 1\text{ kHz}$		68		dB
	Channel/channel output separation	$f = 1\text{ kHz}$		86		dB
SNR	Signal-to-noise ratio	$P_O = 150\text{ mW}$		100		dB
V_n	Noise output voltage			9.5		$\mu\text{V(rms)}$

(1) Measured at 1 kHz

AC OPERATING CHARACTERISTICS $V_{DD} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 32\ \Omega$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD \leq 0.1%		40 ⁽¹⁾		mW
THD+N	Total harmonic distortion + noise	$P_O = 30\text{ mW}$, 20 Hz–20 kHz		0.5%		
B_{OM}	Maximum output power BW	$G = 10$, THD < 2%		> 20		kHz
	Phase margin	Open loop		58°		
	Supply ripple rejection	$f = 1\text{ kHz}$		68		dB
	Channel/channel output separation	$f = 1\text{ kHz}$		86		dB
SNR	Signal-to-noise ratio	$P_O = 100\text{ mW}$		100		dB
V_n	Noise output voltage			9.5		$\mu\text{V(rms)}$

(1) Measured at 1 kHz

AC OPERATING CHARACTERISTICS $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 32\ \Omega$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD \leq 0.1%		40 ⁽¹⁾		mW
THD+N	Total harmonic distortion + noise	$P_O = 60\text{ mW}$, 20 Hz–20 kHz		0.4%		
B_{OM}	Maximum output power BW	$G = 10$, THD < 2%		> 20		kHz
	Phase margin	Open loop		56°		
	Supply ripple rejection	$f = 1\text{ kHz}$		68		dB
	Channel/channel output separation	$f = 1\text{ kHz}$		86		dB
SNR	Signal-to-noise ratio	$P_O = 150\text{ mW}$		100		dB
V_n	Noise output voltage			9.5		$\mu\text{V(rms)}$

(1) Measured at 1 kHz

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Frequency	1, 2, 4, 5, 7, 8, 10, 11, 13, 14, 16, 17, 34, 36
		vs Output power	3, 6, 9, 12, 15, 18
	Supply ripple rejection	vs Frequency	19, 20
V_n	Output noise voltage	vs Frequency	21, 22
	Crosstalk	vs Frequency	23-26, 37, 38
	Mute attenuation	vs Frequency	27, 28
	Open-loop gain and phase margin	vs Frequency	29, 30
	Output power	vs Load resistance	31, 32
	Phase	vs Frequency	39-44
I_{DD}	Supply current	vs Supply voltage	33
SNR	Signal-to-noise ratio	vs Voltage gain	35
	Closed-loop gain	vs Frequency	39-44
	Power dissipation/amplifier	vs Output power	45, 46

**TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY**

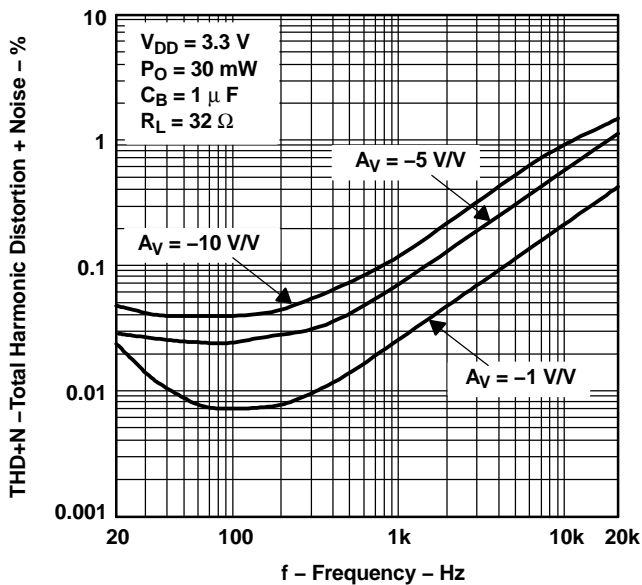


Figure 1.

**TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY**

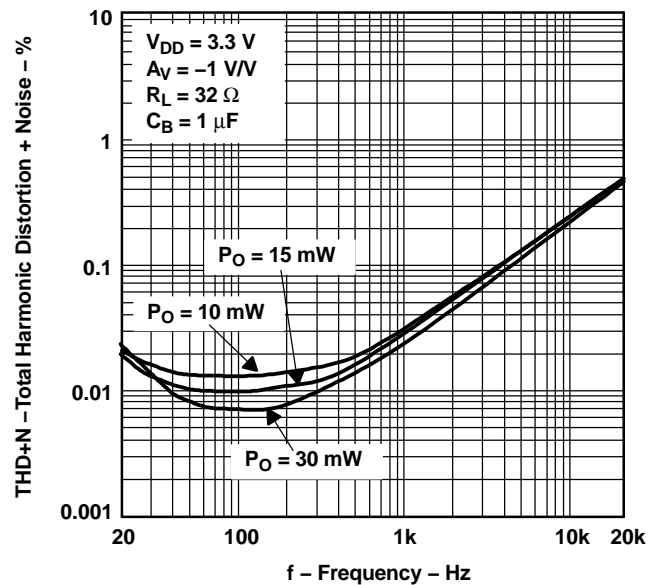


Figure 2.

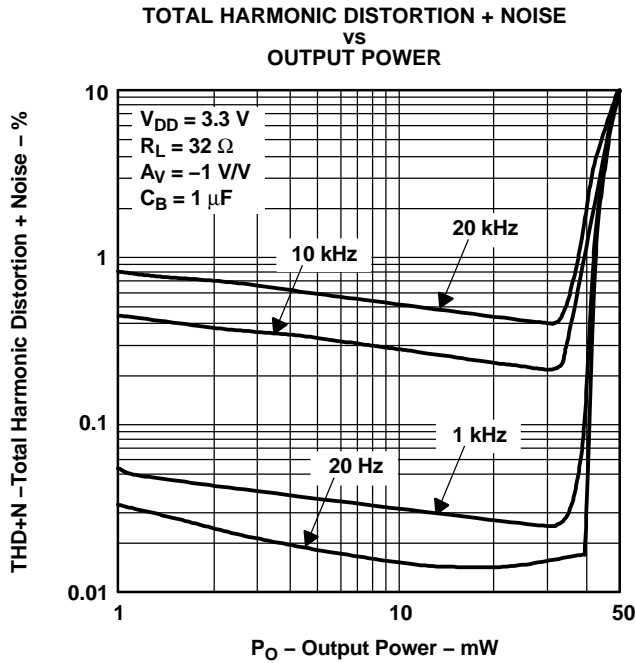


Figure 3.

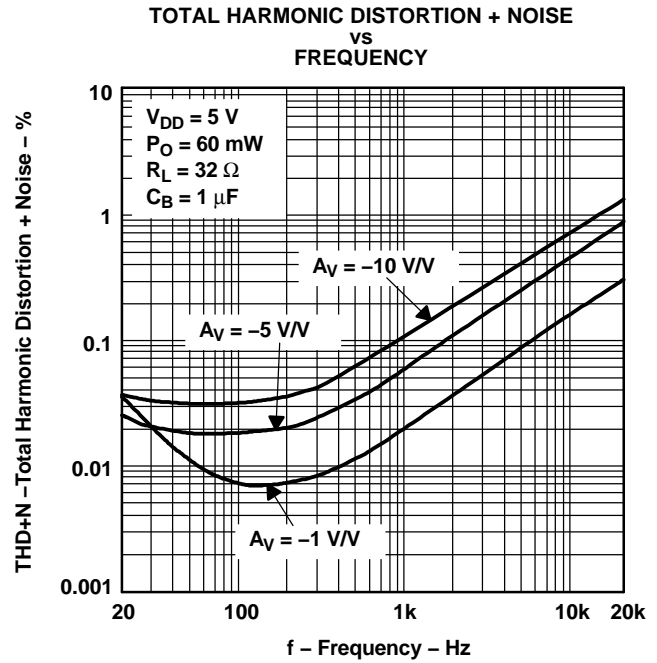


Figure 4.

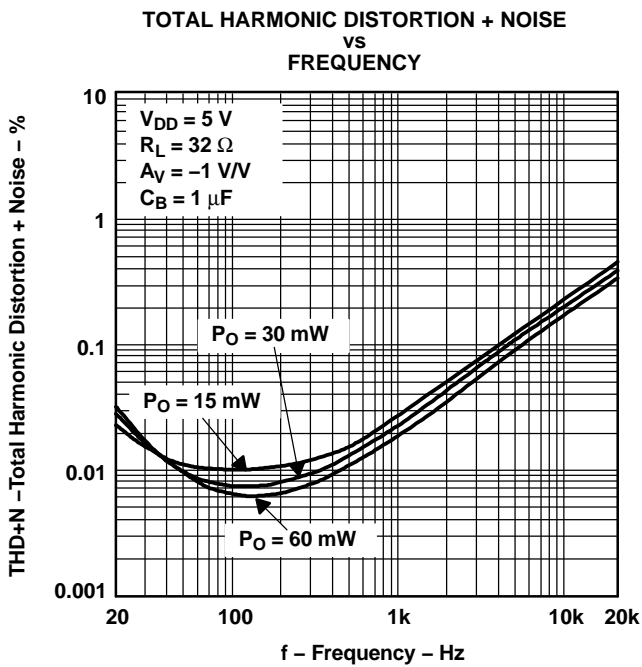


Figure 5.

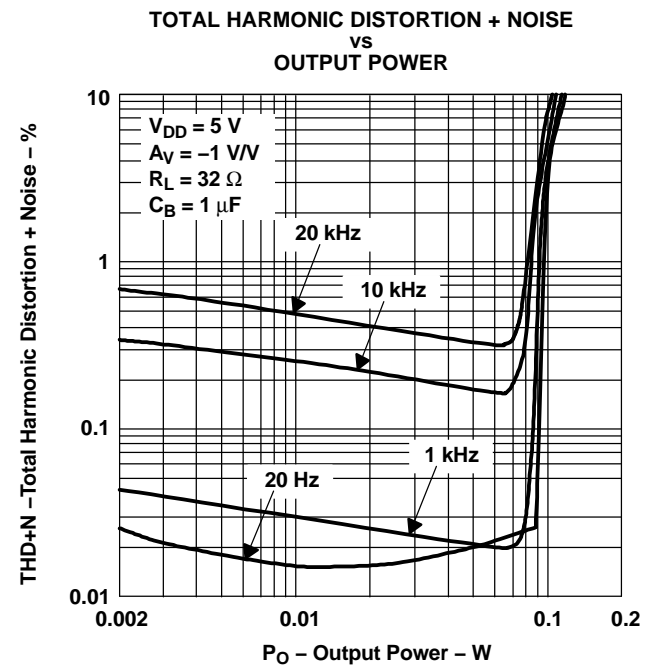


Figure 6.

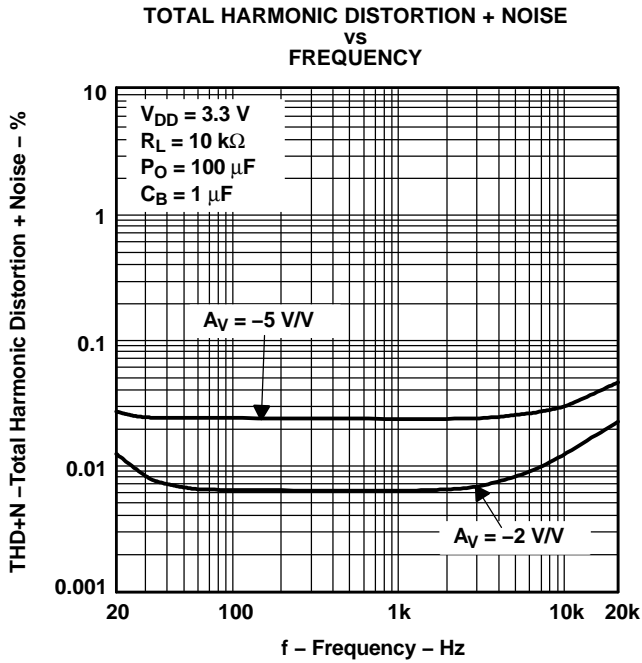


Figure 7.

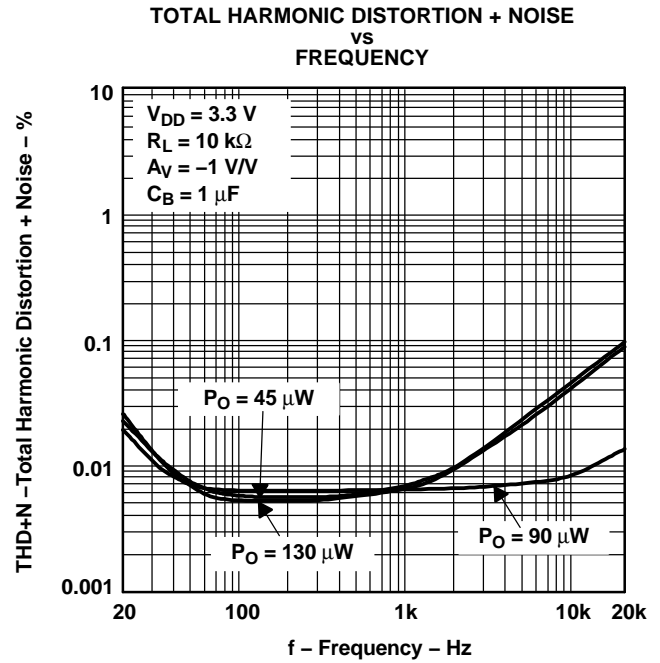


Figure 8.

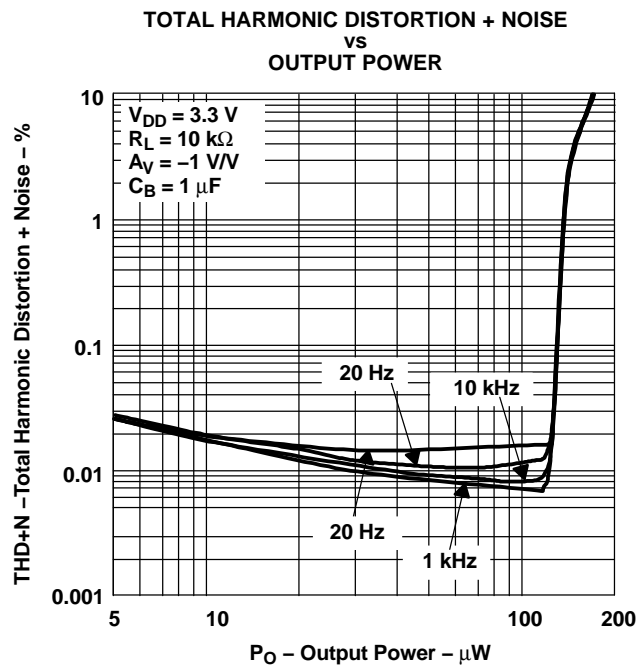


Figure 9.

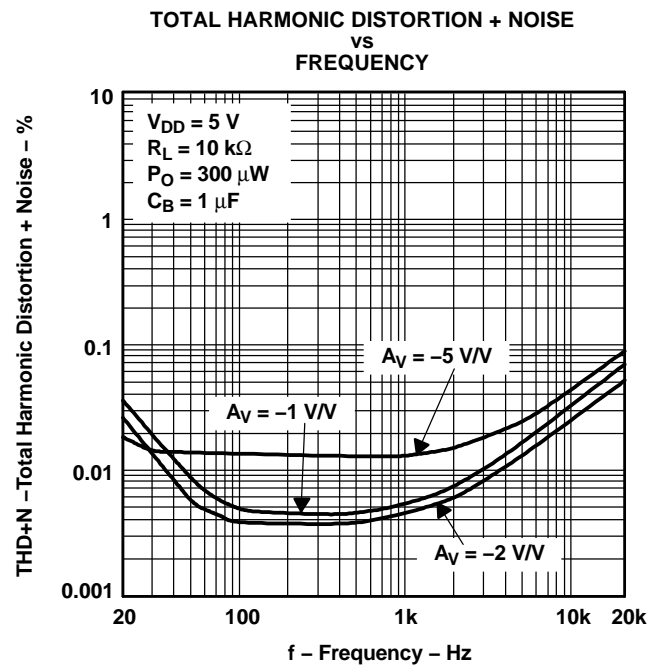


Figure 10.

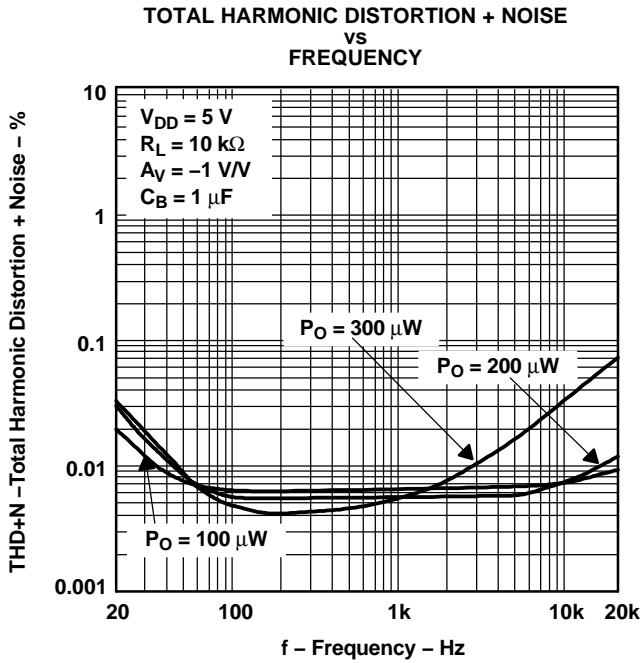


Figure 11.

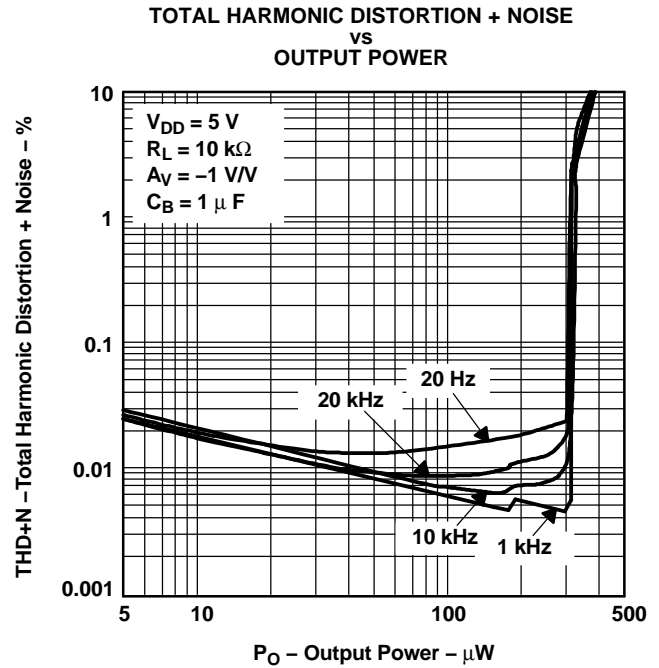


Figure 12.

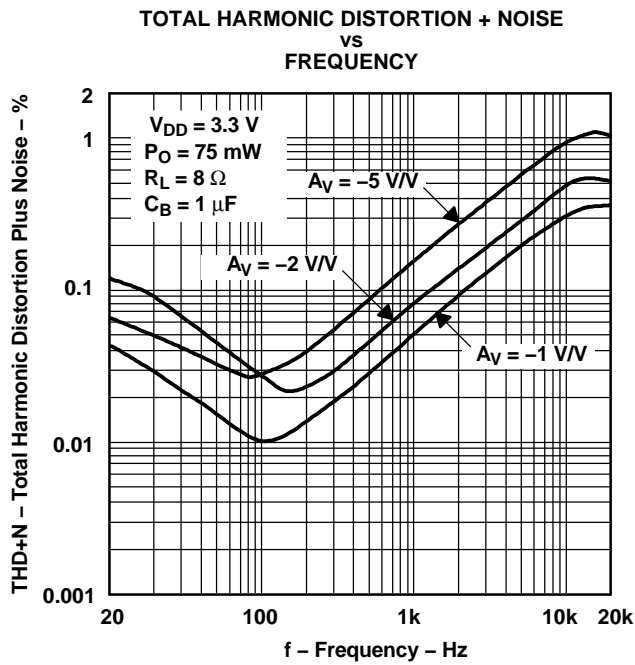


Figure 13.

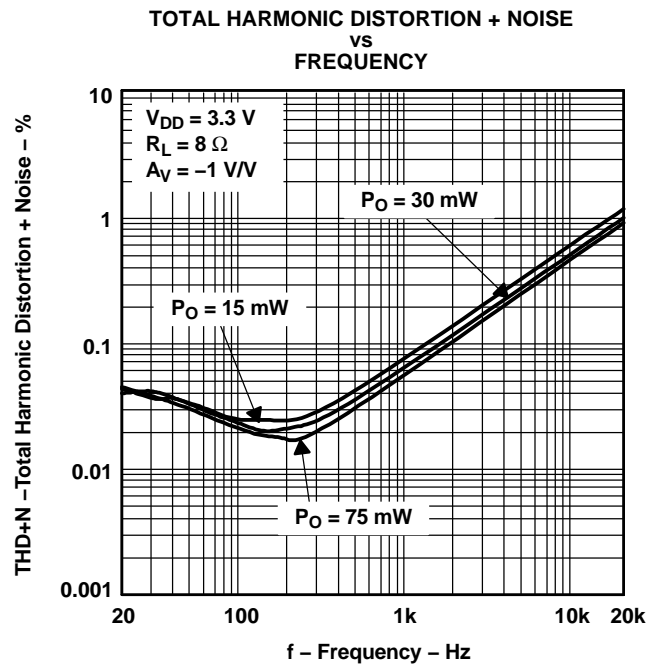


Figure 14.

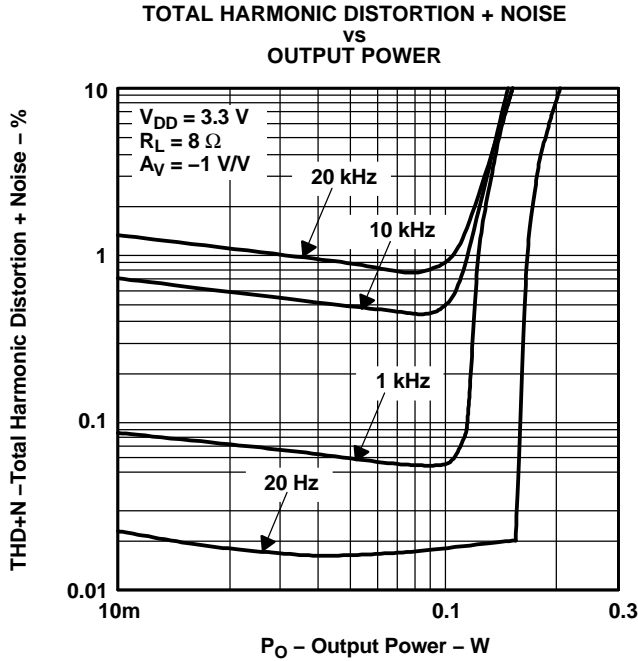


Figure 15.

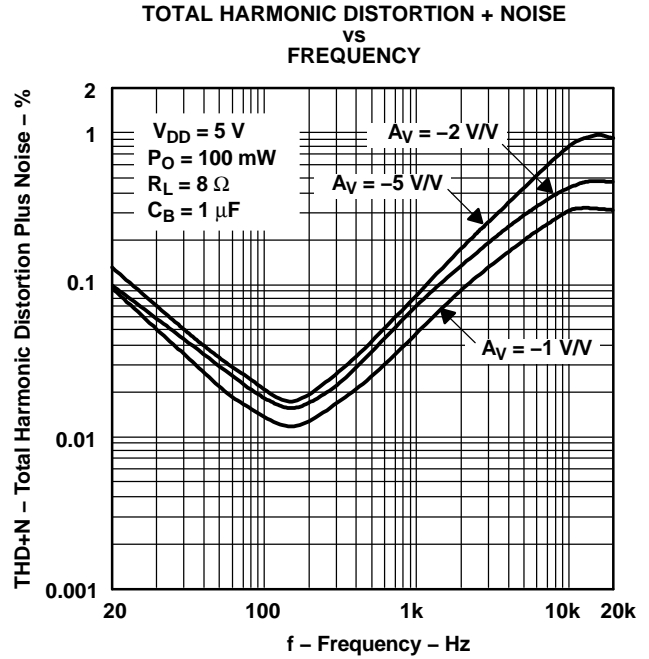


Figure 16.

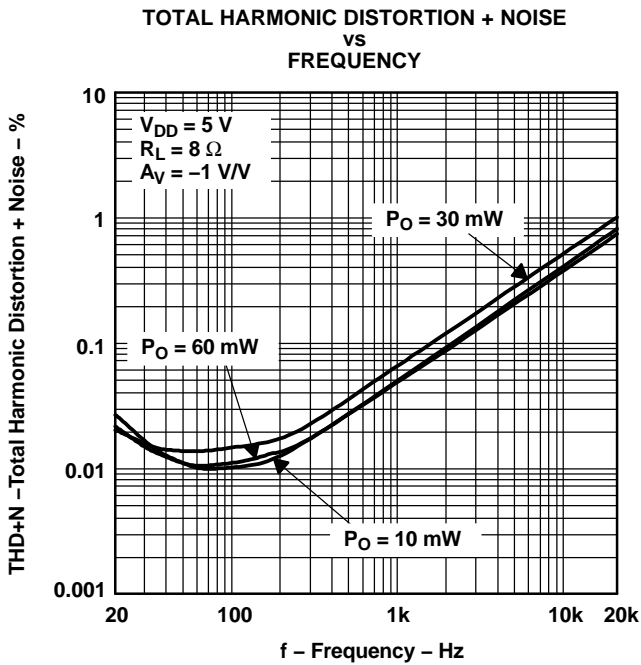


Figure 17.

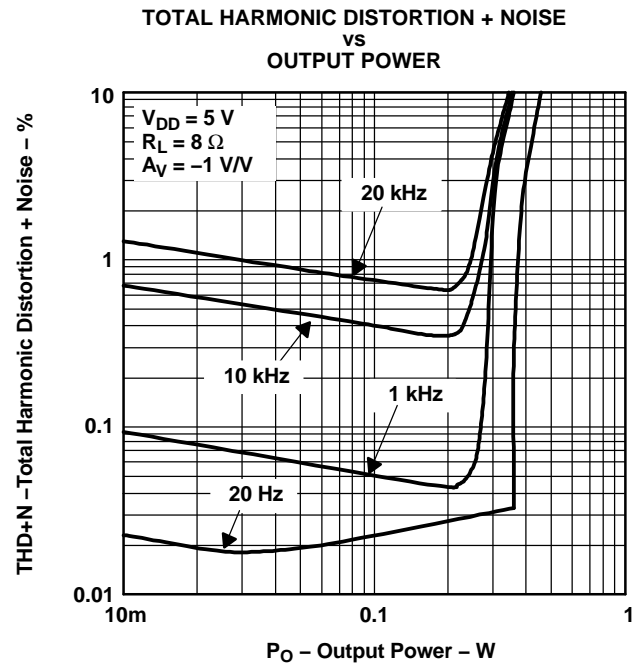


Figure 18.

SUPPLY RIPPLE REJECTION RATIO
VS
FREQUENCY

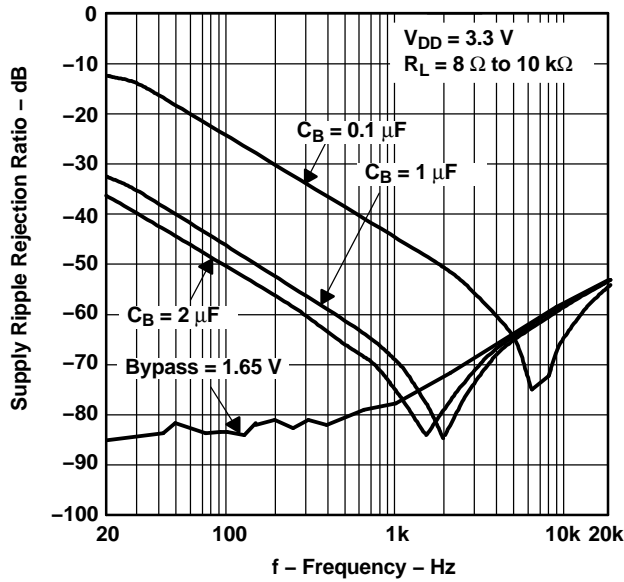


Figure 19.

SUPPLY RIPPLE REJECTION RATIO
VS
FREQUENCY

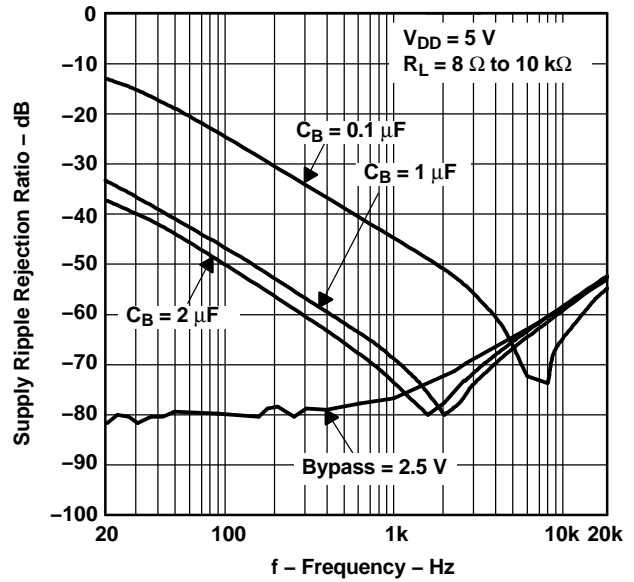


Figure 20.

OUTPUT NOISE VOLTAGE
VS
FREQUENCY

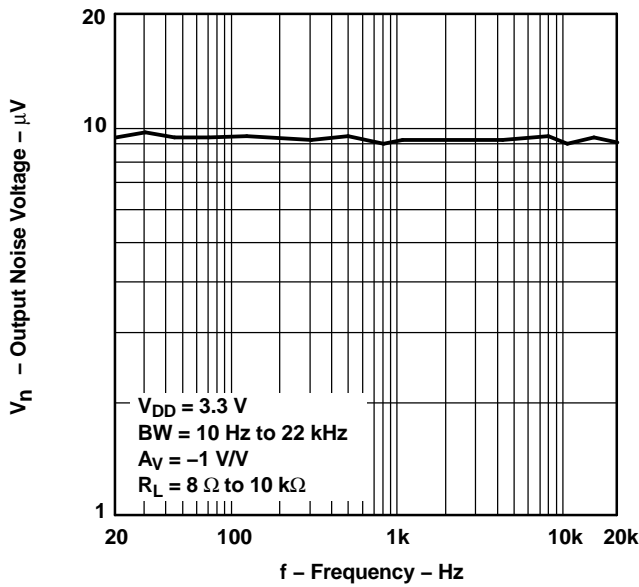


Figure 21.

OUTPUT NOISE VOLTAGE
VS
FREQUENCY

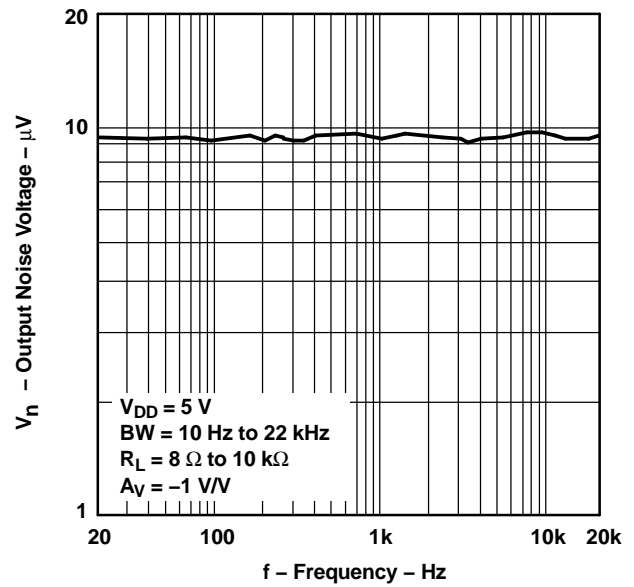


Figure 22.

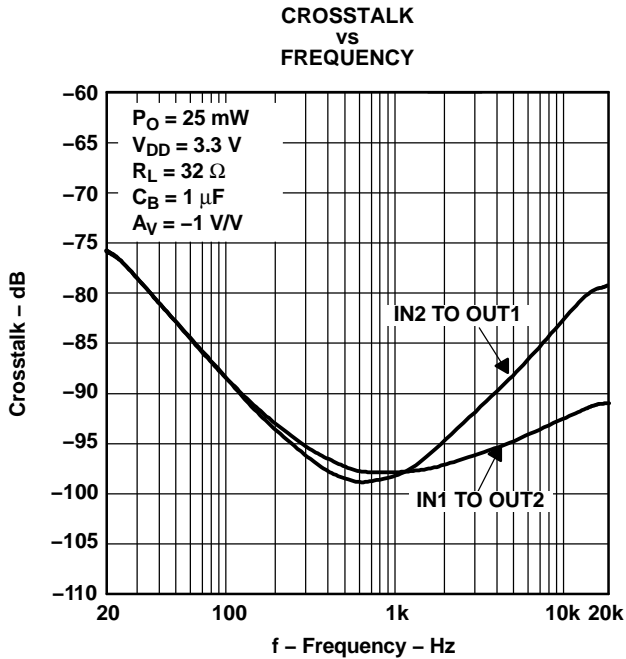


Figure 23.

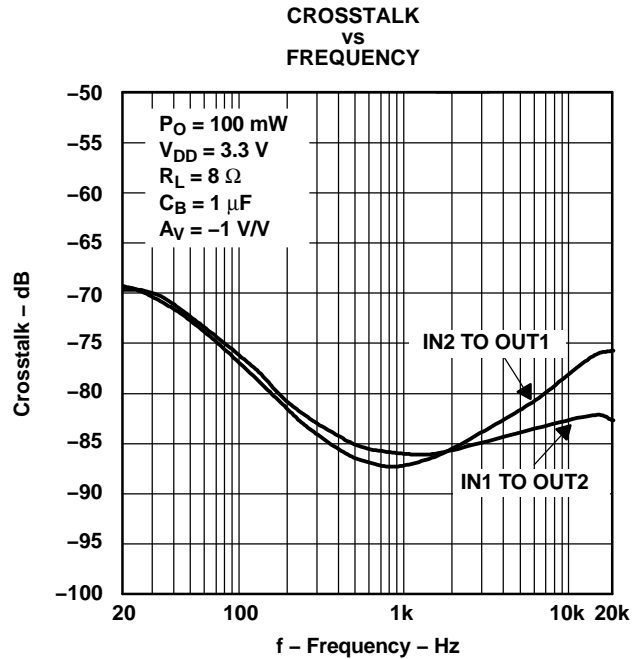


Figure 24.

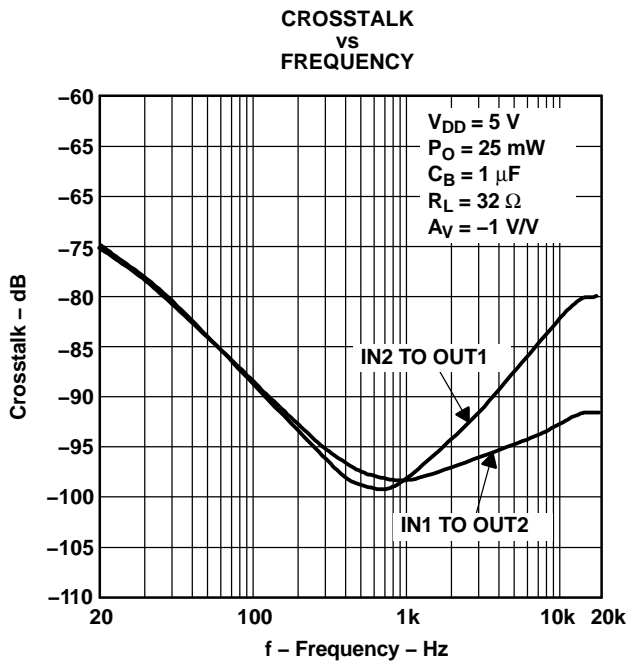


Figure 25.

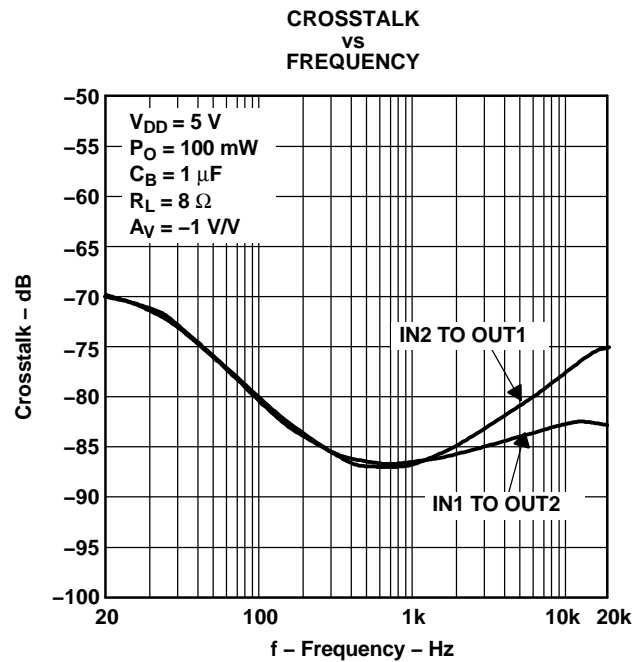


Figure 26.

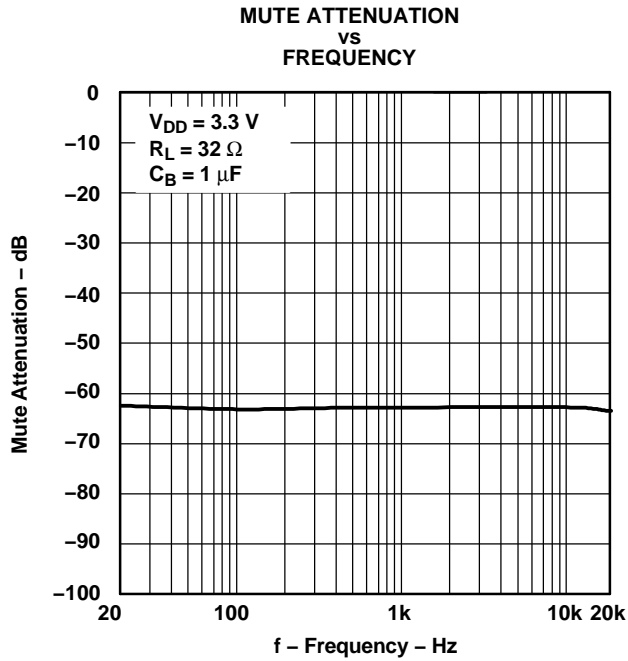


Figure 27.

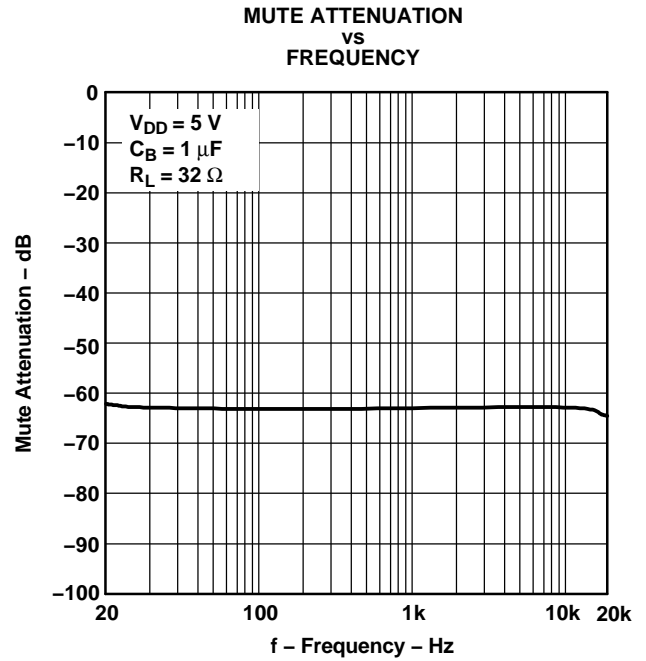


Figure 28.

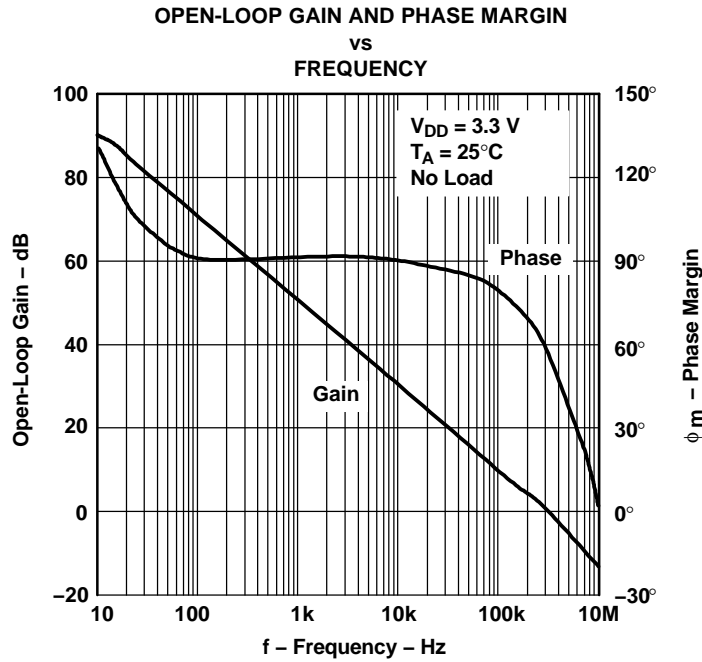


Figure 29.

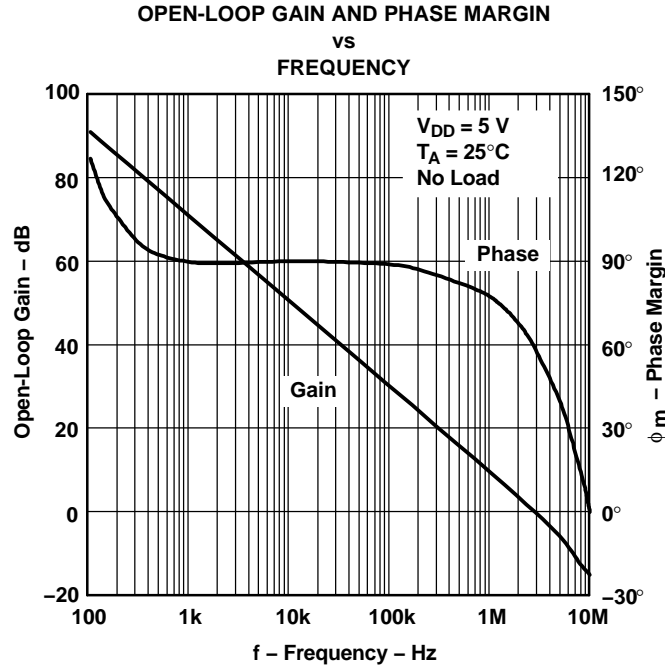


Figure 30.

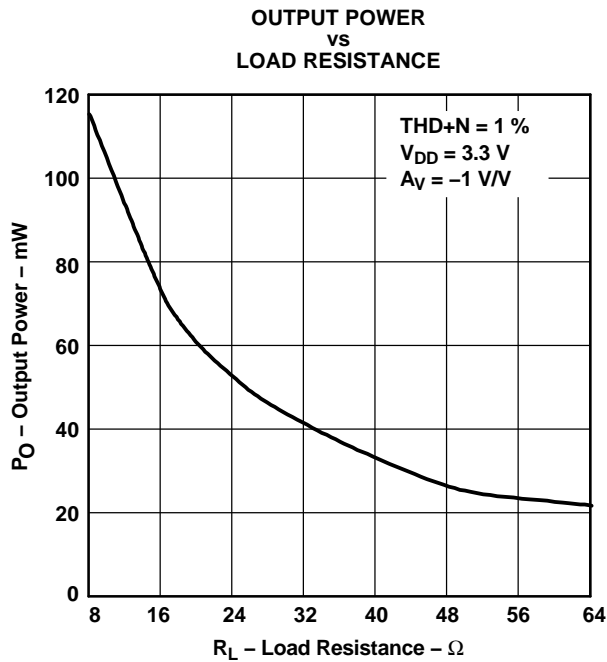


Figure 31.

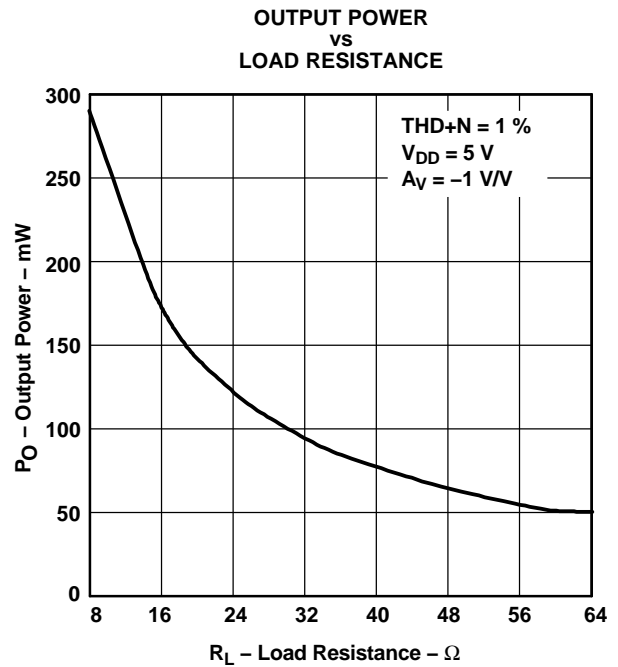


Figure 32.

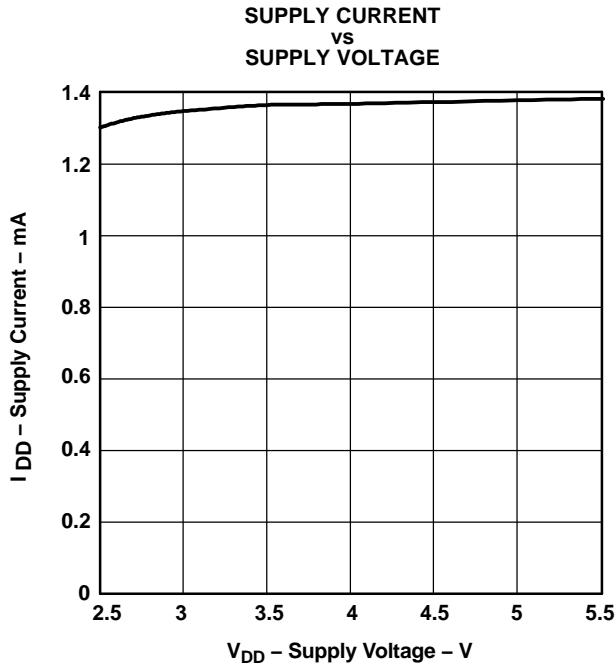


Figure 33.

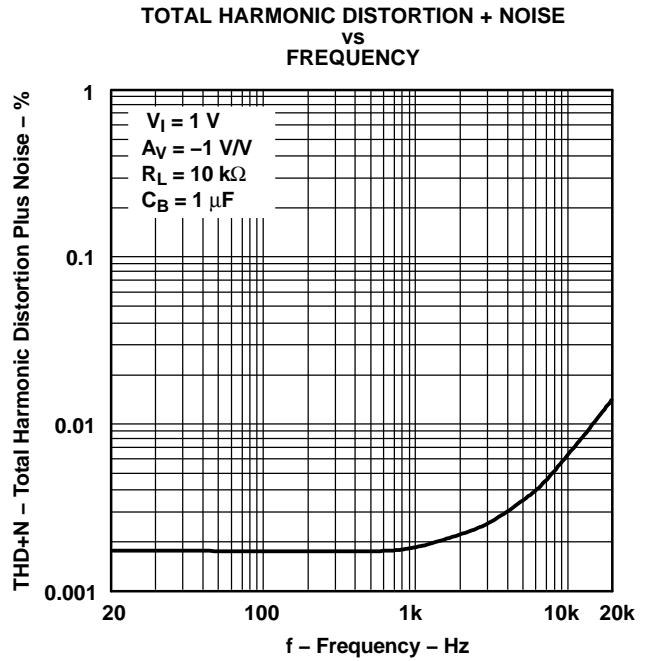


Figure 34.

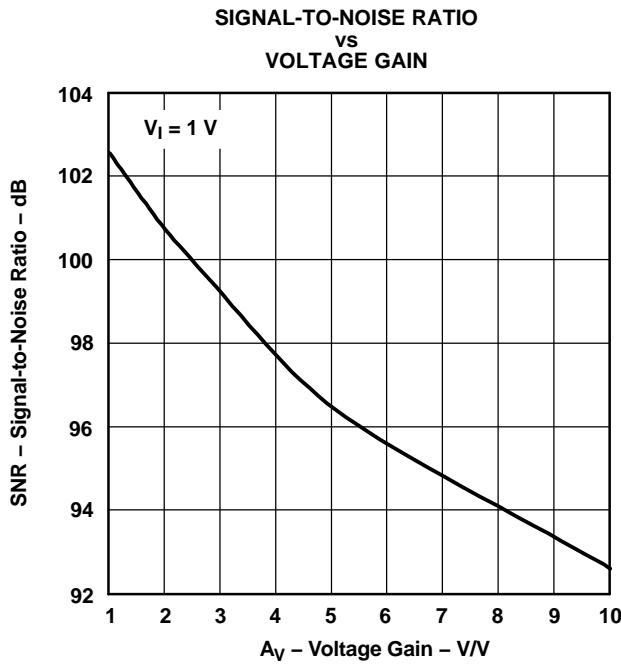


Figure 35.

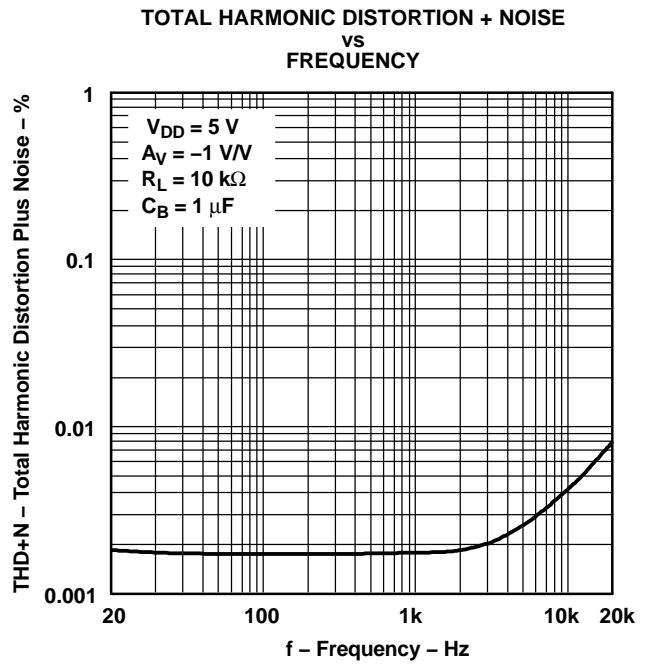


Figure 36.

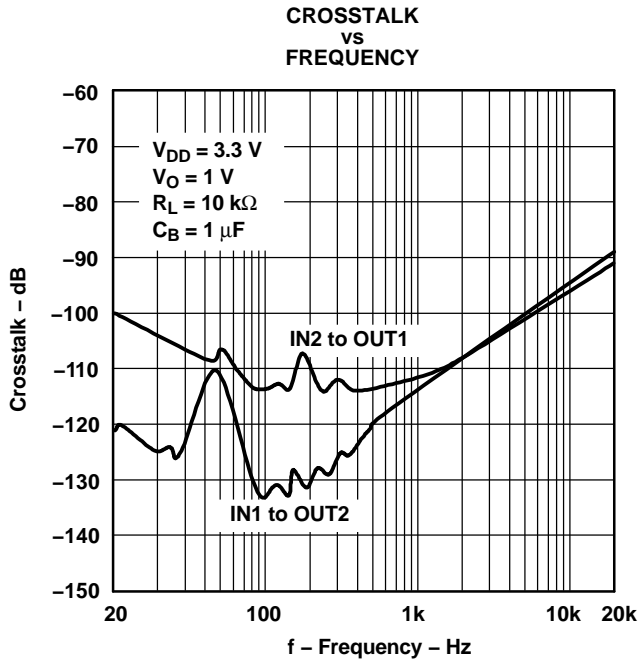


Figure 37.

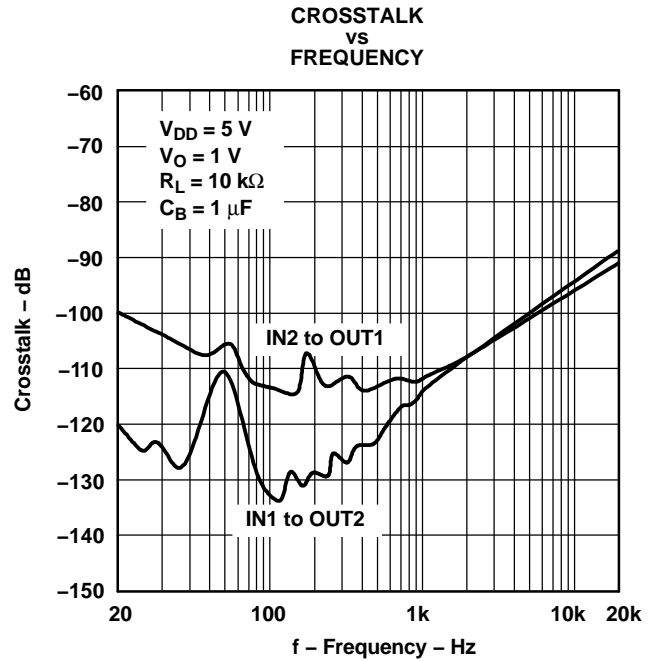


Figure 38.

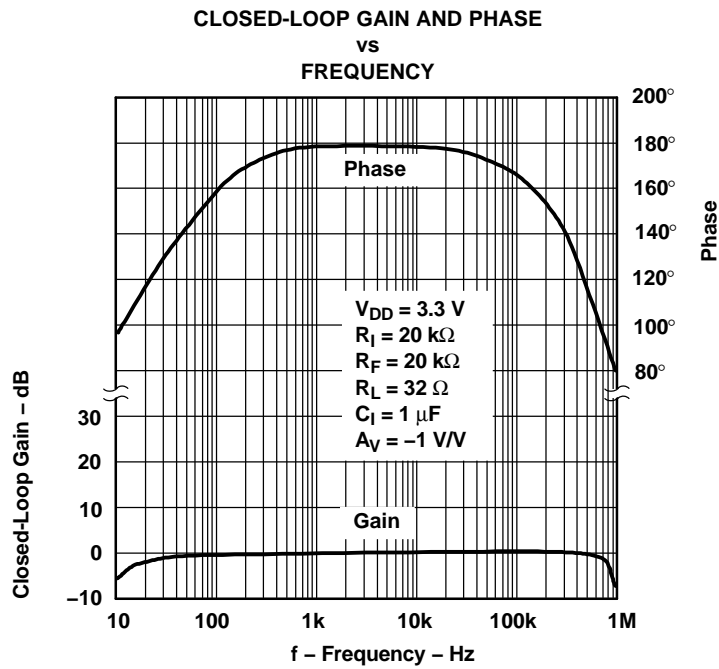


Figure 39.

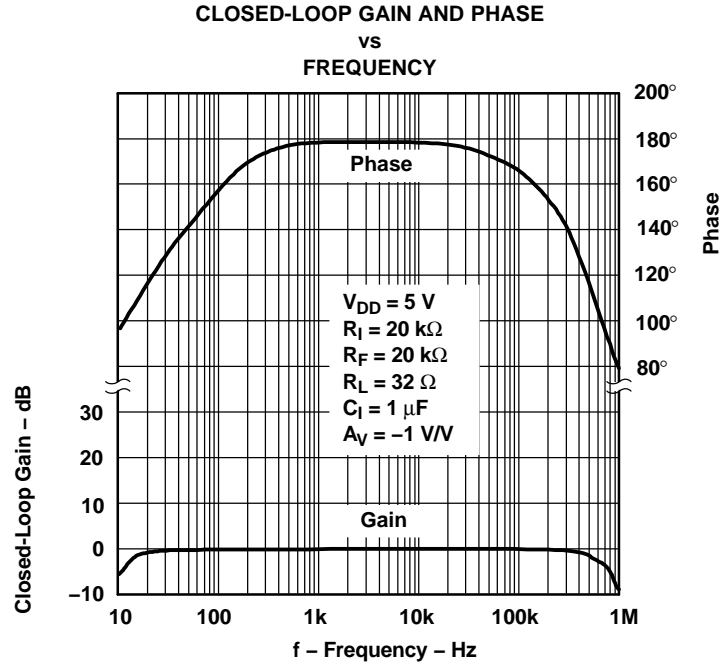


Figure 40.

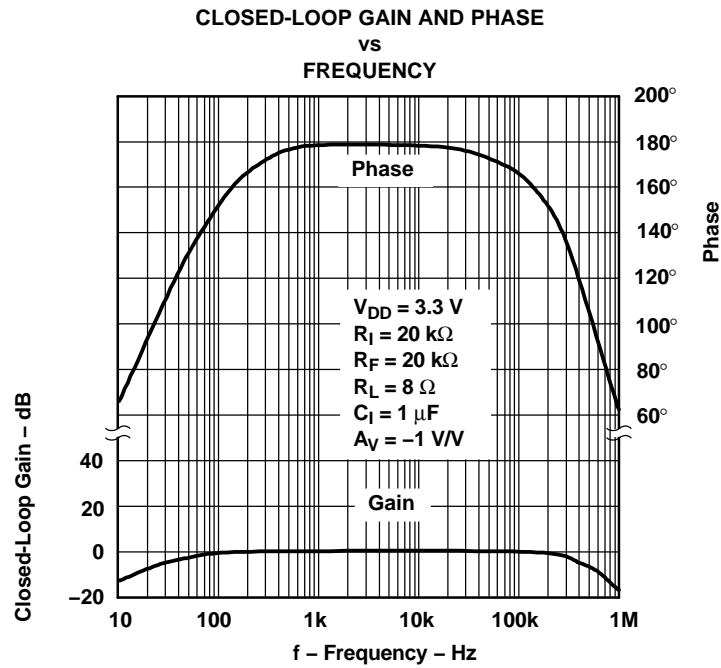


Figure 41.

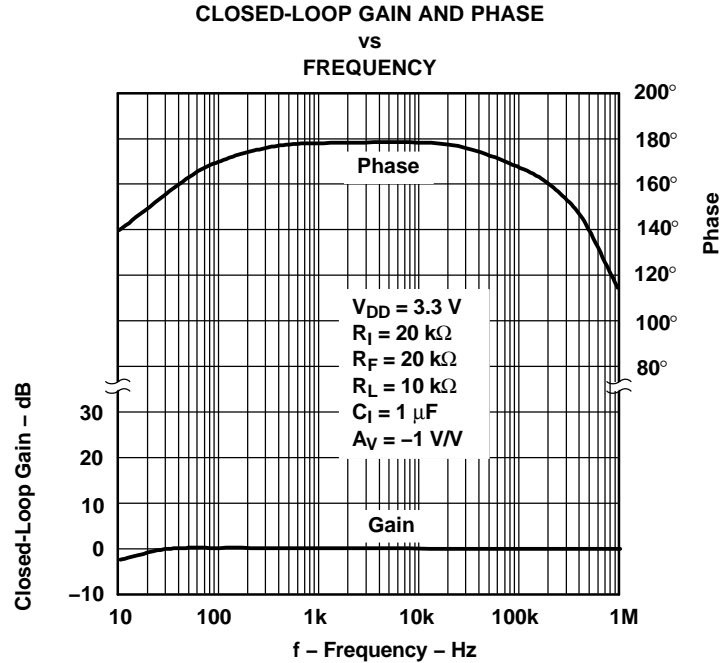


Figure 42.

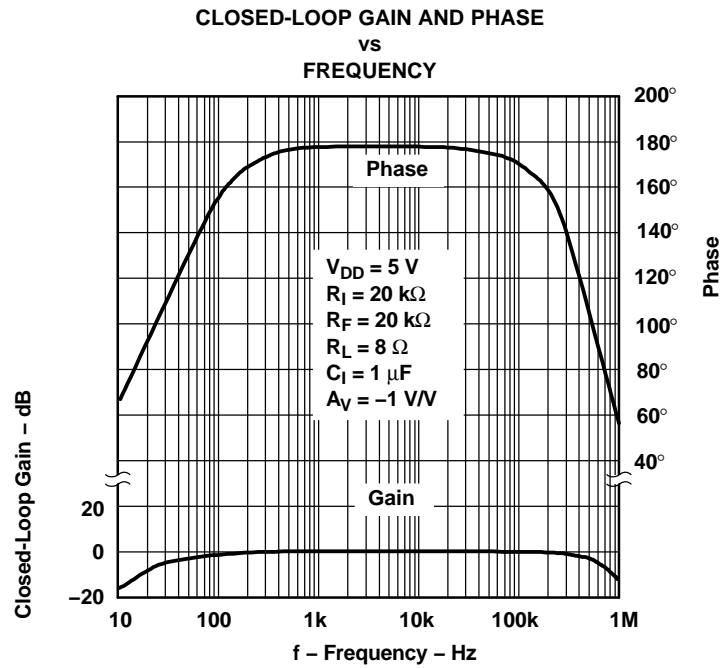


Figure 43.

CLOSED-LOOP GAIN AND PHASE
vs
FREQUENCY

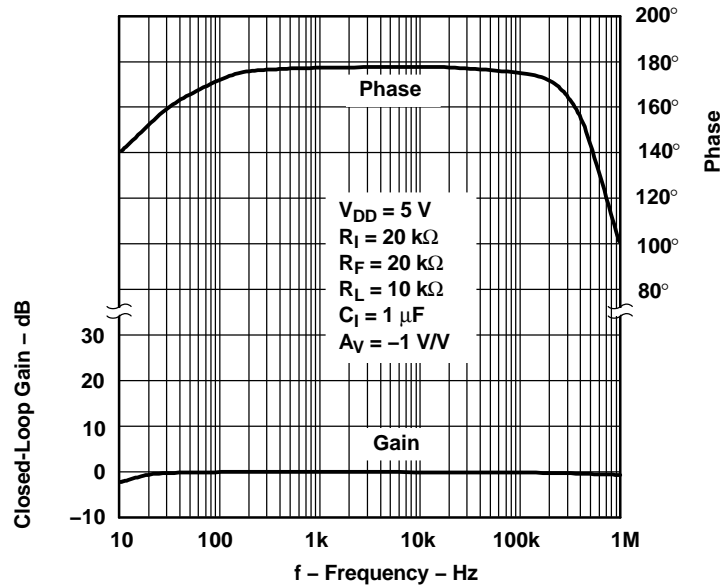


Figure 44.

POWER DISSIPATION/AMPLIFIER
vs
OUTPUT POWER

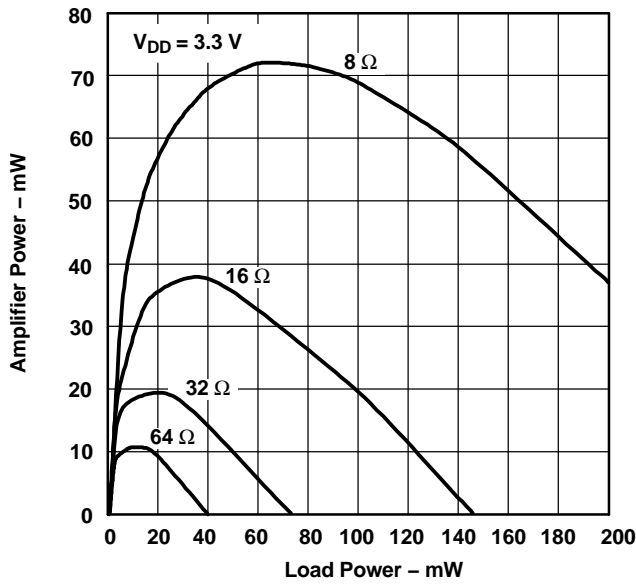


Figure 45.

POWER DISSIPATION/AMPLIFIER
vs
OUTPUT POWER

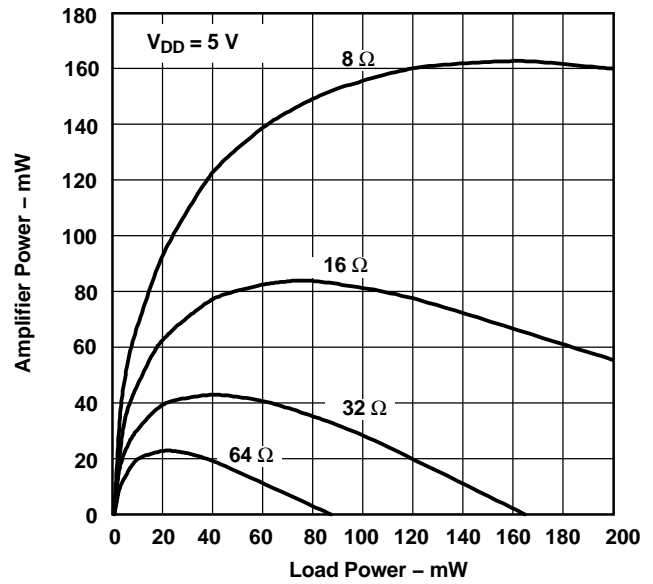


Figure 46.

APPLICATION INFORMATION

GAIN SETTING RESISTORS, R_F and R_I

The gain for the TPA122 is set by resistors R_F and R_I according to Equation 1.

$$\text{Gain} = - \left(\frac{R_F}{R_I} \right) \quad (1)$$

Given that the TPA122 is an MOS amplifier, the input impedance is high. Consequently, input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper start-up operation of the amplifier. Taken together, it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 k Ω and 20 k Ω . The effective impedance is calculated in Equation 2.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \quad (2)$$

As an example, consider an input resistance of 20 k Ω and a feedback resistor of 20 k Ω . The gain of the amplifier would be -1 and the effective impedance at the inverting terminal would be 10 k Ω , which is within the recommended range.

For high-performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 k Ω , the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F . In effect, this creates a low-pass filter network with the cutoff frequency defined in Equation 3.

$$f_{c(\text{lowpass})} = \frac{1}{2\pi R_F C_F} \quad (3)$$

For example, if R_F is 100 k Ω and C_F is 5 pF, then $f_{c(\text{lowpass})}$ is 318 kHz, which is well outside the audio range.

INPUT CAPACITOR C_I

In the typical application, an input capacitor, C_I , is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in Equation 4.

$$f_{c(\text{highpass})} = \frac{1}{2\pi R_I C_I} \quad (4)$$

The value of C_I is important to consider, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where R_I is 20 k Ω and the specification calls for a flat bass response down to 20 Hz. Equation 4 is reconfigured as Equation 5.

$$C_I = \frac{1}{2\pi R_I f_{c(\text{highpass})}} \quad (5)$$

In this example, C_I is 0.4 μF , so one would likely choose a value in the range of 0.47 μF to 1 μF . A further consideration for this capacitor is the leakage path from the input source through the input network (R_I , C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (> 10). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

APPLICATION INFORMATION (continued)

POWER SUPPLY DECOUPLING, C_S

The TPA122 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF , placed as close as possible to the device V_{DD} lead, works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the power amplifier is recommended.

MIDRAIL BYPASS CAPACITOR, C_B

The midrail bypass capacitor, C_B , serves several important functions. During start-up, C_B determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so low it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 160-k Ω source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in Equation 6 should be maintained.

$$\frac{1}{(C_B \times 160 \text{ k}\Omega)} \leq \frac{1}{(C_I R_I)} \quad (6)$$

As an example, consider a circuit where C_B is 1 μF , C_I is 1 μF , and R_I is 20 k Ω . Inserting these values into Equation 6 results in: $6.25 \leq 50$ which satisfies the rule. Bypass capacitor, C_B , values of 0.1- μF to 1- μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

OUTPUT COUPLING CAPACITOR, C_C

In the typical single-supply, single-ended (SE) configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 7.

$$f_c = \frac{1}{2\pi R_L C_C} \quad (7)$$

The main disadvantage, from a performance standpoint, is that the typically small load impedances drive the low-frequency corner higher. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 68 μF is chosen and loads vary from 32 Ω to 47 k Ω . Table 1 summarizes the frequency response characteristics of each configuration.

Table 1. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
32 Ω	68 μF	73 Hz
10,000 Ω	68 μF	0.23 Hz
47,000 Ω	68 μF	0.05 Hz

As Table 1 indicates, headphone response is adequate and drive into line level inputs (a home stereo for example) is good.

The output coupling capacitor required in single-supply, SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

$$\frac{1}{(C_B \times 160 \text{ k}\Omega)} \leq \frac{1}{(C_I R_I)} \ll \frac{1}{R_L C_C} \quad (8)$$

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

5-V VERSUS 3.3-V OPERATION

The TPA122 was designed for operation over a supply range of 2.5 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation because these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability. The most important consideration is that of output power. Each amplifier in the TPA122 can produce a maximum voltage swing of $V_{DD} - 1$ V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)} = 2.3$ V, as opposed to $V_{O(PP)} = 4$ V for 5-V operation. The reduced voltage swing subsequently reduces maximum output power into the load before distortion begins to become significant.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA122D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPA122	Samples
TPA122DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAE	Samples
TPA122DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAE	Samples
TPA122DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPA122	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

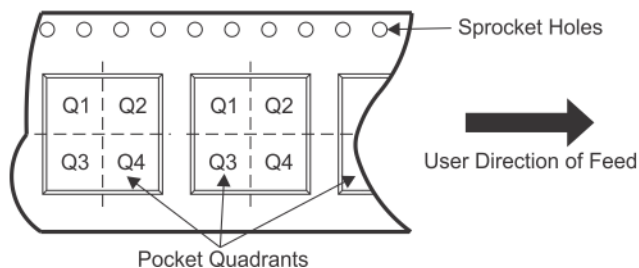
(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA122DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA122DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA122DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPA122DR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPA122D	D	SOIC	8	75	505.46	6.76	3810	4

GENERIC PACKAGE VIEW

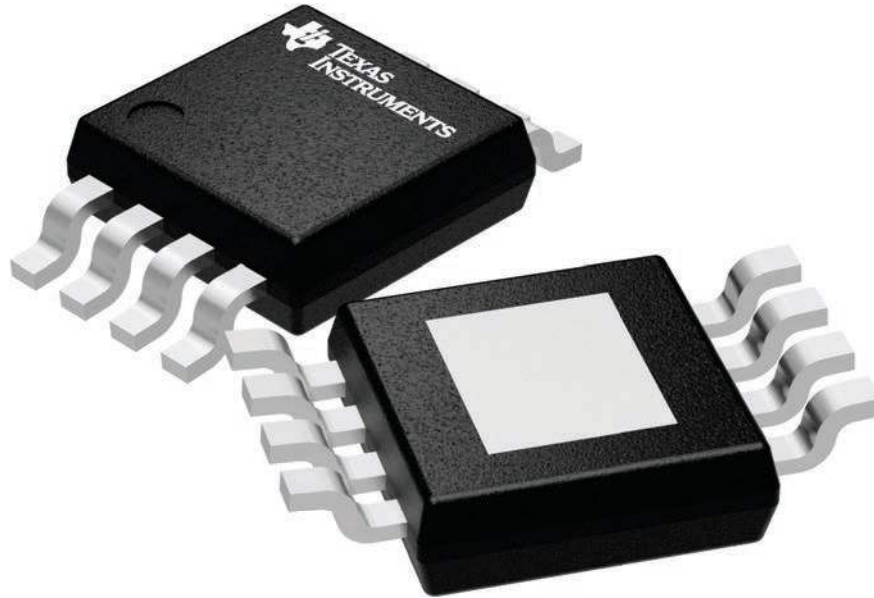
DGN 8

PowerPAD VSSOP - 1.1 mm max height

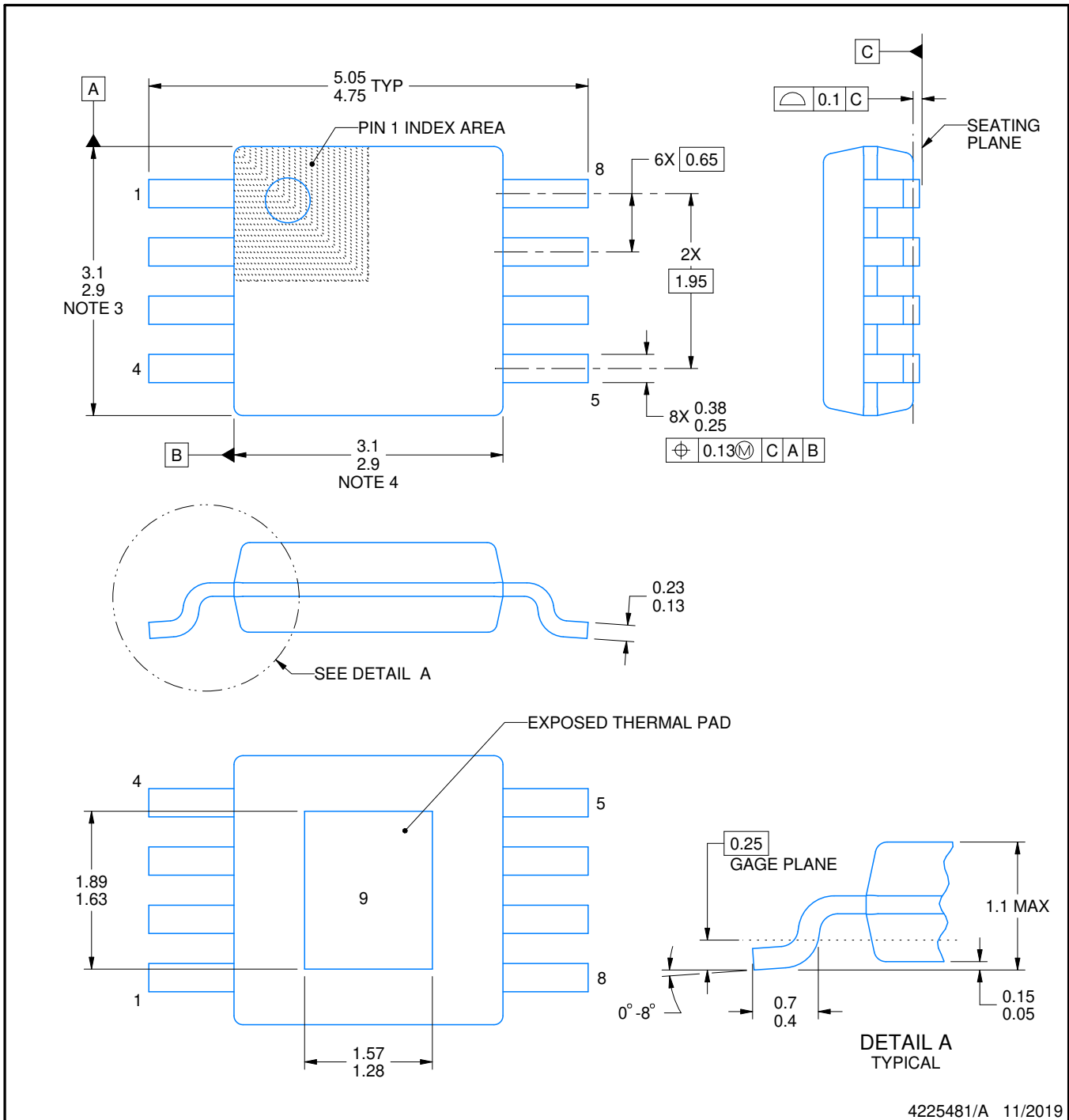
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A



4225481/A 11/2019

PowerPAD is a trademark of Texas Instruments.

NOTES:

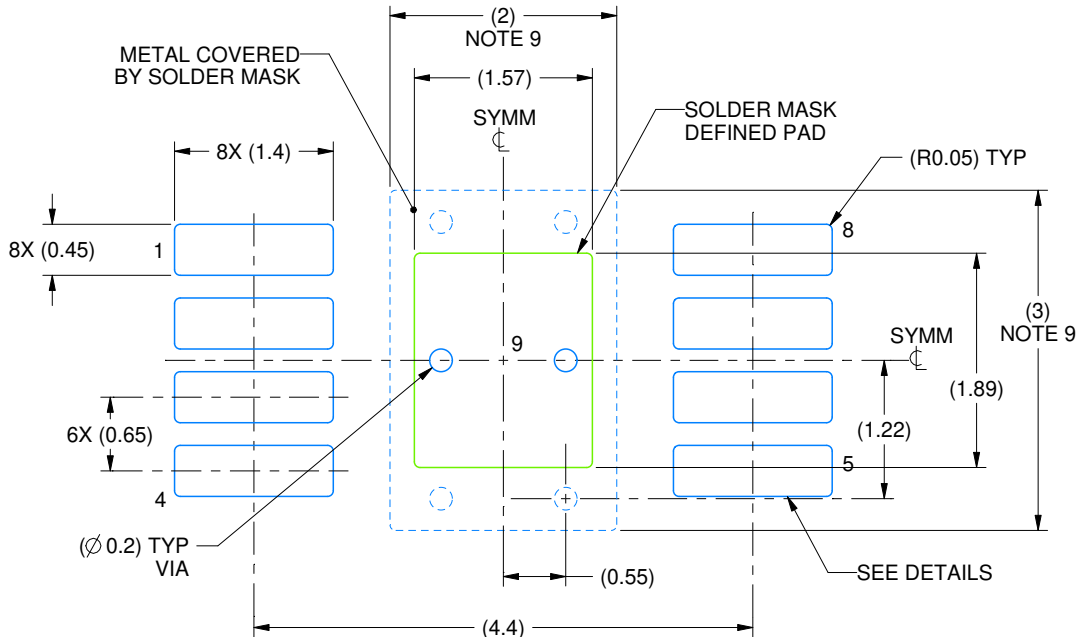
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

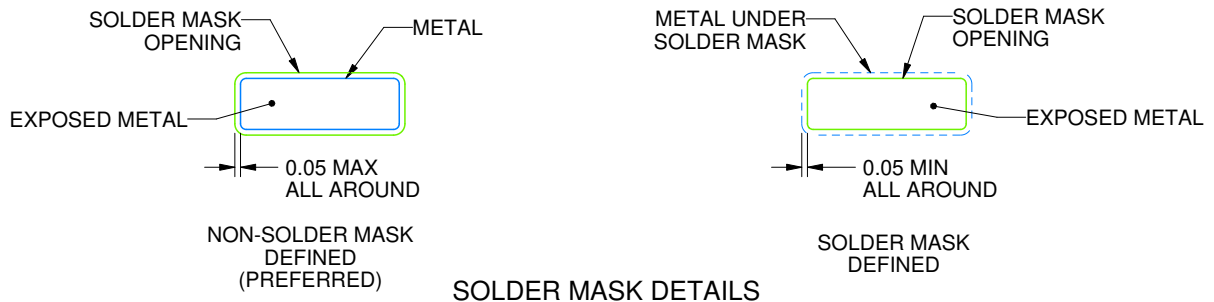
DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



4225481/A 11/2019

NOTES: (continued)

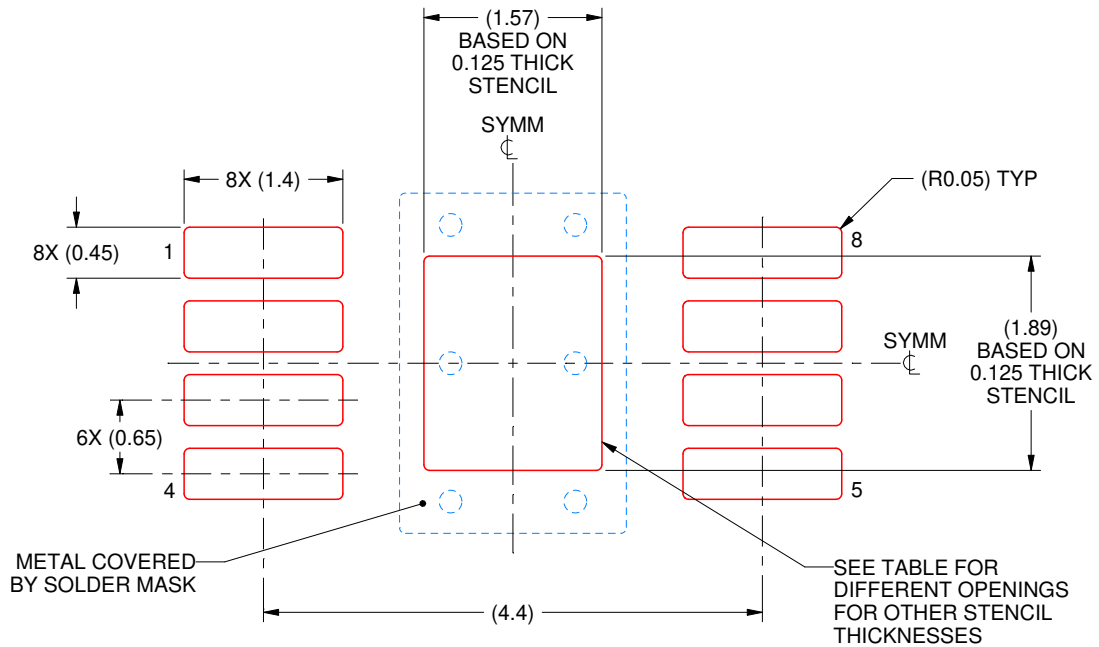
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

D0008A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

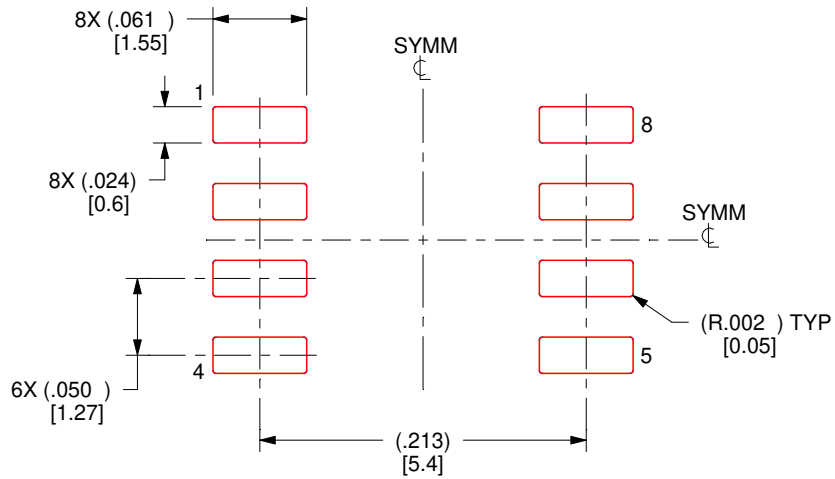
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated