DC to 40 GHz MMIC Medium Power Voltage Controlled Attenuator

Features
- Wideband operation: DC to 40 GHz
- Low Insertion Loss (<3 dB)
- Good Input/Output Match
- Medium Attenuation (max. 17 dB)
- Size: 1640 x 920 mm

Description
The MMS005AA is a medium-power DC-40 GHz PHEMT FET attenuator. The performance of the device is controlled by two bias voltages, Vseries and Vshunt. The bias voltages control the match and attenuation of the device when varied between -1V and +0.5V DC. For additional information please refer to the tables of recommended bias settings optimized for flat insertion loss and flat attenuation.

Application
The MMS005AA MMIC voltage controlled attenuator is ideal for high frequency and broadband applications in test equipment, commercial and military systems. The attenuator is especially suited for applications needing a moderate amount of adjustable attenuation and fast attenuation control from DC to millimeter frequencies. The device is also useful as a general purpose building block in communications systems.

Key Characteristics: $Z_o = 50\Omega$

| Parameter	Description	Min	Typ	Max
Attenuation (dB)	DC to 40 GHz	0	-	17
Flatness (±dB)	DC to 40 GHz	-	1	-
Insertion Loss (dB	DC to 40 GHz	-	-	3
S11 (dB)	DC to 40 GHz	-	-10	-8
S22 (dB)	DC to 40 GHz	-	-10	-8
P1dB (dBm)	1dB Gain Compression 0 to 15 dB Attenuation	8	-	-

Optimized for Flat Attenuation (Typical)

MMS005AA Attenuation
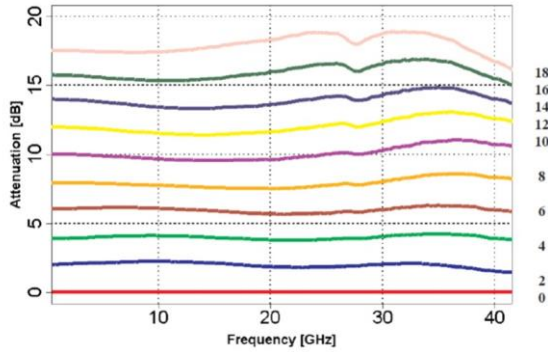
Typical on wafer measured performance

| Vseries (V)	Vshunt (V)	Att. (dB)*
-0.625	0.343	18.3
-0.625	-0.287	15.9
-0.625	-0.1	13.6
-0.616	-0.456	11.6
-0.608	-0.501	9.6
-0.601	-0.544	7.5
-0.595	-0.583	5.7
-0.569	-0.622	3.8
-0.55	-0.7	1.8
0.5	-1	0

Optimized for Flat Insertion Loss (Typical)

MMS005AA Insertion Loss
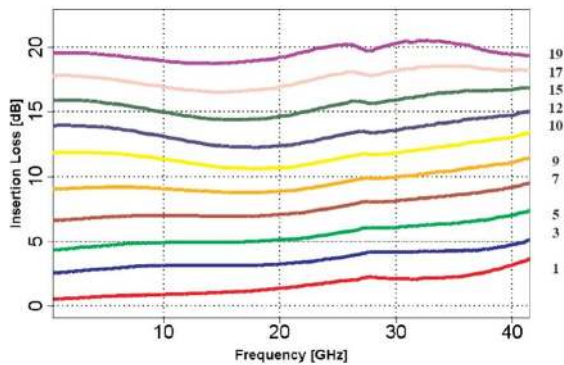
Typical on wafer measured performance

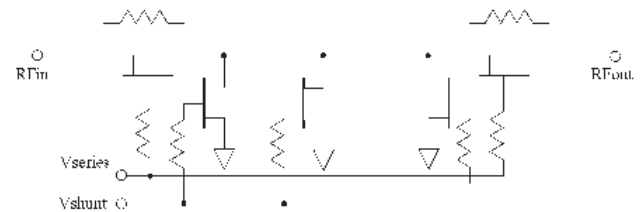| Vseries (V)	Vshunt (V)	Att. (dB)*
-650	0	19.2
-0.65	-0.312	16.9
-0.65	-0.413	14.6
-0.65	-0.475	12.4
-0.641	-0.513	10.7
-0.618	-0.549	8.9
0.595	-0.583	7.1
-0.568	-0.624	5.1
-0.55	-0.7	3.3
0.5	-1	1.4

Note: (*) Midband
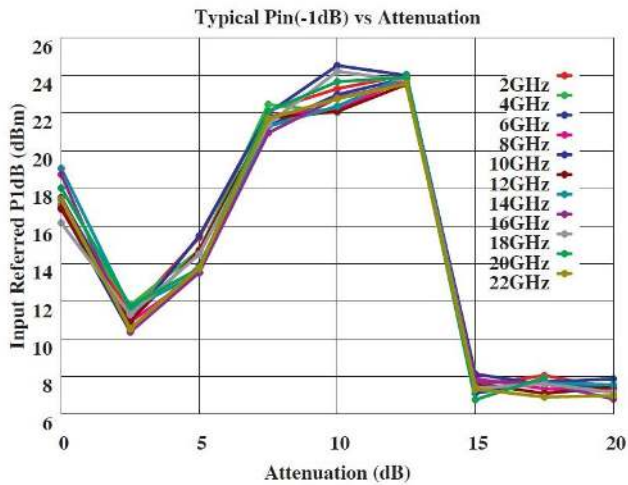
MMS005AA S11
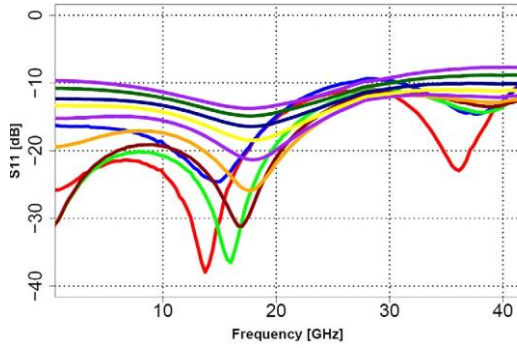
Typical on wafer measured performance

MMS005AA S22
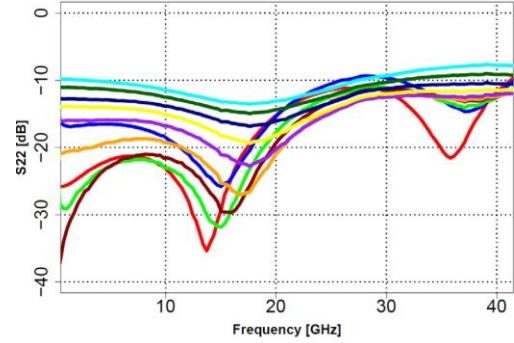
Typical on wafer measured performance

Table 1: Supplemental Specifications

Parameter	Description	Min	Typ	Max
Vseries	Attenuation Control Voltage	-2V	-	0.5V
Vshunt	Attenuation Control Voltage	-2V	-	0.5V
Dcin	DC feedback circuit input	0 V	0.25 V	1 V
Dcout	DC feedback circuit output	0 V	0.25 V	1 V
GND	Backside Ground Plane	-	-	22dBm
Tch	Channel Temperature	-	-	150°C
Θch	Thermal Resistance (Tcase=85°C)	-	60o C/Watt	-

Typical Pin (1dB) vs Attenuation

Typical on evaluated package measured performance

MMS005AA Simplified Schematic Diagram

Pick-up and Chip Handling:

This MMIC has exposed air bridges on the top surface. **Do not pick up chip with vacuum on the die center;** handle from edges or use a collet.

ESD Handling and Bonding:

This MMIC is ESD sensitive; preventive measures should be taken during handling, die attach, and bonding.

Epoxy die attach is recommended. Please review our application note MM-APP-0001 handling and die attach recommendations, on our website for more handling, die attach and bonding information.

DC Feedback Circuit for Variable Attenuator:

The following feedback circuit does a good job of providing the series and shunt biases to the variable attenuator for a user-selected amount of attenuation.

The circuit references a 1/3 scale version of the microwave attenuator, which is used for the DC feedback loop. Because the devices are 1/3 the size of the unscaled attenuator, the reference impedence is 3 times larger (150W instead of 50W).

The circuit uses two ordinary opamps to provide the bias control voltages to the attenuator. Opamp OA1 senses the input impedance of the attenuator and adjusts the series FET gate voltage Vseries so that the impedance looking into the attenuator is 150W. The input impedance can be adjusted with the potentiometer shown in the schematic (Figure 8). When this feedback loop is at DC equilibrium the voltage at DCin will be Vref/2.

The second opamp OA2 adjusts the shunt FET gate voltage so that the DC output voltage DCout is equal to the voltage at the opamp negative input terminal. When 0V is applied to the negative input terminal of OA2, the attenuation is maximized.
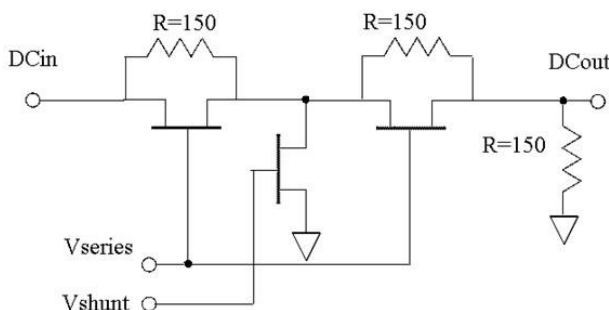
Conversely, if Vref/2 is applied at the negative input of OA2 then the attenuation is minimized.

A voltage divider with the shunt resistor terminated by the voltage Vref makes for a convienient conversion of voltage to attenuation.   If the input to the divider Vatten is set to 0 volts then the negative input of OA2 will have a value of Vref/2 and the attenuator will have minimum attenuation.
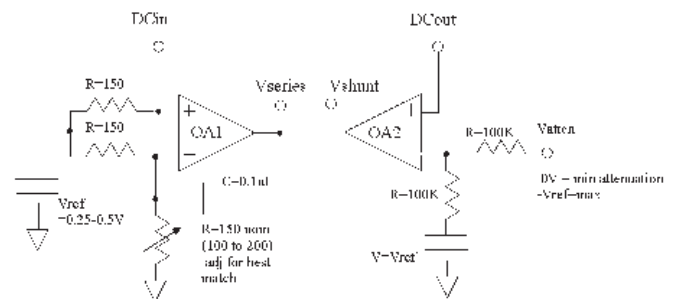
Conversely, if Vatten is set to –Vref then the negative input of OA2 is set 0V and the attenuator will have maximum attenuation. This makes the calculation of Vatten easy and requires a minimum number of parts.
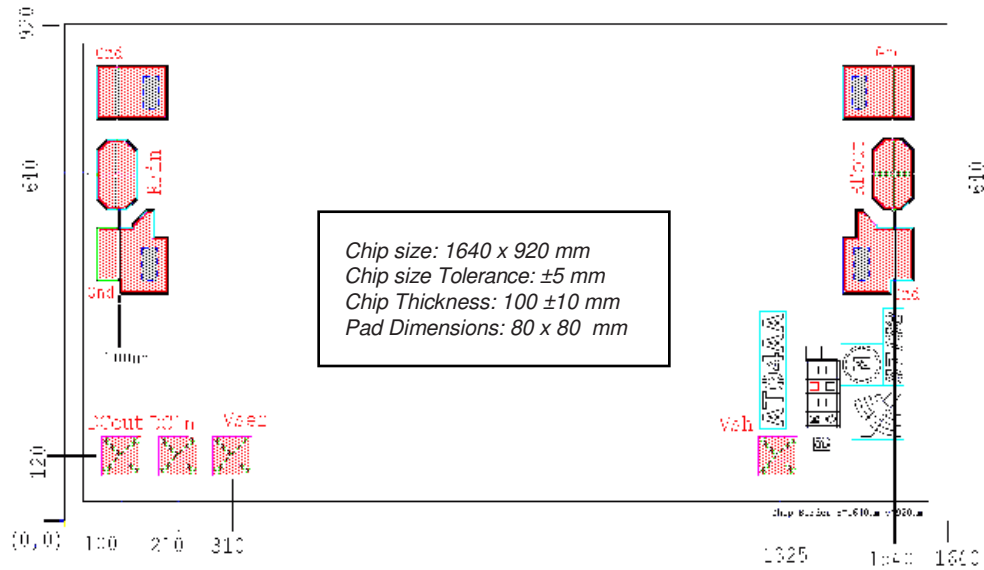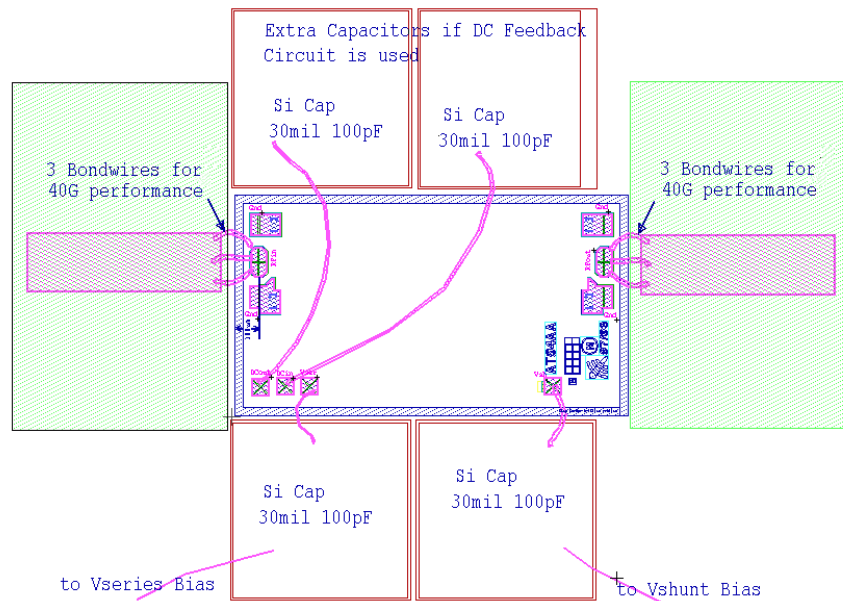
Scaled DC Attenuator

Circuit (1/3 scale attenuator)

The DC feedback circuit to adjust the attenuator

Physical Characteristics of MMS005AA

Chip size: 1640 x 920 mm
Chip size Tolerance: ±5 mm
Chip Thickness: 100 ±10 mm
Pad Dimensions: 80 x 80 mm

Assembly Diagram of MMS005AA

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