EL4583A

Sync Separator, 50% Slice, S-H, Filter, HOUT

FN7503
Rev 2.00
November 12, 2010

The EL4583A extracts timing from video sync in NTSC, PAL, and SECAM systems, and non-standard formats, or from computer graphics operating at higher scan rates. Timing adjustment is via an external resistor. Input without valid vertical interval (no serration pulses) produces a default vertical output.

Outputs are: composite sync, vertical sync, filter, burst/back porch, horizontal, no signal detect, level, and odd/even output (in interlaced scan formats only).

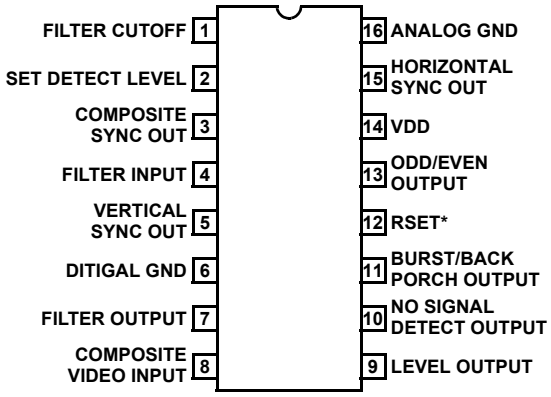
The EL4583A sync slice level is set to the mid-point between sync tip and the blanking level. This 50% point is determined by two internal sample and hold circuits that track sync tip and back porch levels. It provides hum and noise rejection and compensates for input levels of 0.5V to 2.0V_{P-P}.

A built in filter attenuates the chroma signal to prevent color burst from disturbing the 50% sync slice. Cut off frequency is set by a resistor to ground from the Filter Cut Off pin. Additionally, the filter can be by-passed and video signal fed directly to the Video Input.

The level output pin provides a signal with twice the sync amplitude which may be used to control an external AGC function. A TTL/CMOS compatible No Signal Detect Output flags a loss or reduction in input signal level. A resistor sets the Set Detect Level.

Pinout

EL4583A
(16-PIN SO)
TOP VIEW



* R_{SET} MUST BE A 1% REGISTER

Features

- NTSC, PAL, and SECAM sync separation
- Single supply, +5V operation
- Precision 50% slicing
- Built-in programmable color burst filter
- Decodes non-standard vertical
- Horizontal sync output
- Sync pulse amplitude output
- Low-power CMOS
- Detects loss of signal
- Resistor programmable scan rate
- Few external components
- Available in 16-pin SO (0.150”) packages
- Pb-Free plus anneal available (RoHS compliant)

Applications

- Video special effects
- Video test equipment
- Video distribution
- Multimedia
- Displays
- Imaging
- Video data capture
- Video triggers

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL4583AIS	16-Pin SO (0.150”)	-	MDP0027
EL4583AIS-T7	16-Pin SO (0.150”)	7”	MDP0027
EL4583AIS-T13	16-Pin SO (0.150”)	13”	MDP0027
EL4583AISZ (See Note)	16-Pin SO (0.150”) (Pb-free)	-	MDP0027
EL4583AISZ-T7 (See Note)	16-Pin SO (0.150”) (Pb-free)	7”	MDP0027
EL4583AISZ-T13 (See Note)	16-Pin SO (0.150”) (Pb-free)	13”	MDP0027

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = 25°C)

V_{CC} Supply 7V
Storage Temperature . . . . . .-65°C to +150°C
Pin Voltages . . . . . -0.5V to V_{CC} +0.5V

Operating Temperature Range . . . . . .-40°C to +85°C
Power Dissipation . . . . . See Curves
Die Junction Temperature . . . . . .150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

V_{DD} = 5V, T_A = 25°C, R_{SET} = 681kΩ, R_F = 33kΩ, R_{LV} = 82kΩ, unless otherwise specified.

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
I_{DD}	V_{DD} = 5V (Note 1)		2.5	4	mA
Clamp Voltage	Pins 4, 8, unloaded	1.3	1.55	1.8	V
Discharge Current	Pins 4, 8, with Signal (V_{IN} = 2V)	3	6	12	µA
Discharge Current	Pins 4, 8, no Signal (Note 2)		10		µA
Clamp Charge Current	Pins 4, 8, V_{IN} = 1V	2	3	4	mA
Ref. Voltage V_{REF}	Pin 12, V_{DD} = 5V (Note 3)	1.5	1.75	2	V
Filter Reference Voltage, V_{FR}	Pin 1	0.60	0.75	0.90	V
Level Reference Current	Pin 2 (Note 4)	1.5	2.5	3.5	µA
V_{OL} Output Low Voltage	I_{OL} = 1.6mA		350	800	mV
V_{OH} Output High Voltage	I_{OH} = -40µA	4			V
	I_{OH} = -1.6mA	2.4	4		V

NOTES:

1. No video signal, outputs unloaded
2. At loss of signal (pin 10 high) the pull down current source switches to a value of 10µA
3. Tested for V_{DD} 5V ±5%
4. Current sourced from pin 2 is V_{REF}/R_{SET}

DC Electrical Specifications

R_F = 33kΩ, R_{SET} = 681kΩ, V_{DD} = 5V, Video Input = $1V_{P-P}$, T_A = 25°C, C_L = 15pF, I_{OH} = -1.6mA, I_{OL} = 1.6mA, unless otherwise specified.

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Horizontal Pulse Width, Pin 15, t_H	(Note 1)	3.8	5	6.2	µs
Vertical Sync Width, Pin 5, t_{VS}	(Note 2)		195		µs
Burst/Back Porch Width, Pin 11, t_B	(Note 1)	2.7	3.7	4.7	µs
Filter Attenuation	F_{IN} = 3.6MHz (Note 3)		16		dB
Comp. Sync Prop. Delay, t_{CS}	V_{IN} (Pin 4)—Comp Sync		250	400	ns
Input Dynamic Range	p-p NTSC Signal	0.4		2	V
Slice Level	Input Voltage = $1V_{P-P}$	40	50	60	%
	V_{SLICE}/V_{BLANK}	40	50	60	%
Level Out, Pin 9	Input Voltage = $1V_{P-P}$, Pin 4	500	600	700	mV
Vertical Sync Default Time, t_{VSD}	(Note 4)	27	36	57	µs
Loss of Signal Time-Out	Pin 10	400	600	800	µs
Burst/Back Porch Delay, t_{BD}	(See Figure 4)		250	400	ns

NOTES:

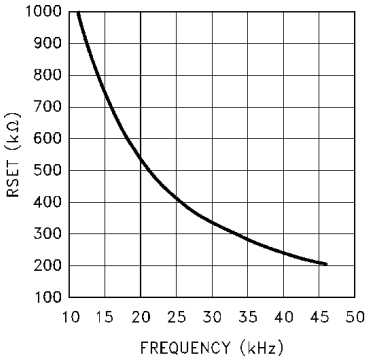
1. Width is a function of R_{SET}
2. c/s, Vertical, Back porch and H are all active low, V_{OH} = 0.8V; vertical is 3H lines wide of NTSC signal
3. Attenuation is a function of R_F; see filter typical characteristics
4. Vertical pulse width in absence of serrations on input signal

Pin Descriptions

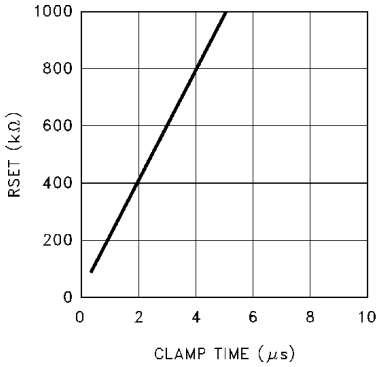
PIN NUMBER	PIN NAME	PIN FUNCTION
1	Filter Cut-Off	A resistor R_F connected between this input and ground determines the input filter characteristic. Increasing R_F increases the filter 3.58MHz color burst attenuation. See the typical performance characteristics.
2	Set Detect Level	A resistor R_{LV} connected between pin 2 and ground determines the value of the minimum signal which triggers the loss of signal output on pin 10. The relationship is $V_P MIN = 0.75RLV/R_{SET}$, where $V_P MIN$ is the minimum detected sync pulse amplitude applied to pin 4. See the typical performance characteristics.
3	Composite Sync Output	This output replicates all the sync inputs on the input video.
4	Filter Input	The filter is a 3 pole active filter with a gain of 2, designed to produce a constant phase delay of nominally 260ns with signal amplitude. Resistor RF on pin 1 controls the filter cut-off. An internal clamp sets the minimum voltage on pin 4 at 1.55V when the input becomes low impedance. Above the clamp voltage, an input current of 1µA charges the input coupling capacitor. With loss of signal, the current source switches to a value of 10µA, for faster signal recovery.
5	Vertical Sync Output	The vertical sync output is synchronous with the first serration pulse rising edge in the vertical interval of the input signal and ends on the trailing edge of the first equalizing Output pulse after the vertical interval. It will therefore be slightly more than 3H lines wide.
6	Digital Ground	This is the ground return for digital buffer outputs.
7	Filter Output	Output of the active 3 pole filter which has its input on pin 4. It is recommended to ac couple the output to pin 8.
8	Video Input	This input can be directly driven by the signal if it is desired to bypass the filter, for example, in the case of strong clean signals. This input is 6dB less sensitive than the filter input.
9	Level Output	This pin provides an analog voltage which is nominally equal to twice the sync pulse amplitude of the video input signal applied to pin 4. It therefore provides an indication of signal strength.
10	No Signal Detect Output	This is a digital output which goes high when either a) loss of input signal or b) the input signal level falls below a predetermined amplitude as set by R_{LV} on pin 2. There will be several horizontal lines delay before the output is initiated.
11	Burst/Back Porch Output	The start of back porch output is triggered on the trailing edge of normal H sync, and on the rising edge of serration pulses in the vertical interval. The pulse is timed out internally to produce a one-shot output. The pulse width is a function of R_{SET}. This output can be used for d.c. restore functions where the back porch level is a known reference.
12	R_{SET}	The current through the resistor R_{SET} determines the timing of the functions within the I.C. These functions include the sampling of the sync pulse 50% point, back porch output and the 2H eliminator. For faster scan rates, the resistor needs to be reduced inversely. For NTSC 15.7kHz scan rate R_{SET} is 681k 1%. R_{SET} must be a 1% resistor.
13	Odd/Even Output	Odd-even output is low for even field and high for odd field. The operation of this circuit has been improved for rejecting spurious noise pulses such as those present in VCR signals.
14	V_{DD} 5V	The internal circuits are designed to have a high immunity to supply variations, although as with most I.C.s a 0.1µF decoupling capacitor is advisable.
15	Horizontal Sync Output	This output produces only true H pulses of nominal width 5µs. The leading edge is triggered from the leading edge of the input H sync, with the same prop. delay as the composite sync The half line pulses present in the input signal during vertical blanking are eliminated with an internal 2H eliminator circuit.
16	Analog Ground	This is the ground return for the signal paths in the chips, R_{SET}, R_F and R_{LV}.

Typical Performance Curves

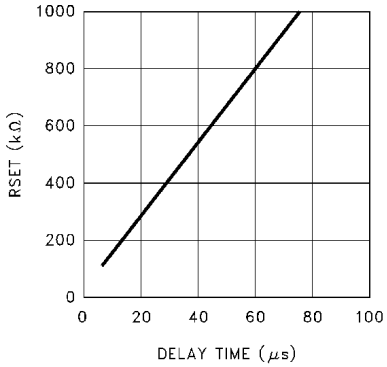
R_{SET} vs HORIZONTAL FREQUENCY



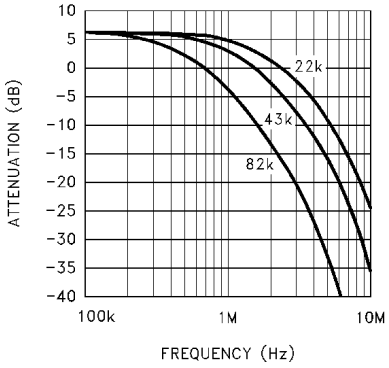
BACK PORCH CLAMP ON TIME vs R_{SET}



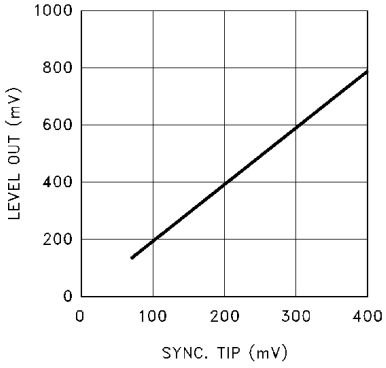
VERTICAL DEFAULT DELAY TIME vs R_{SET}



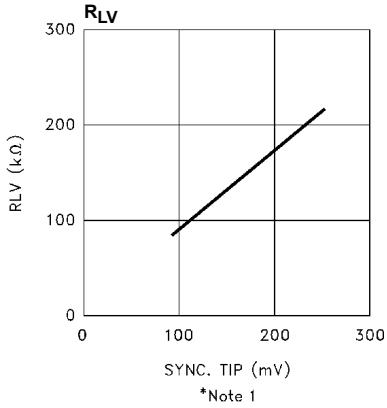
FILTER 3dB BW vs R_F



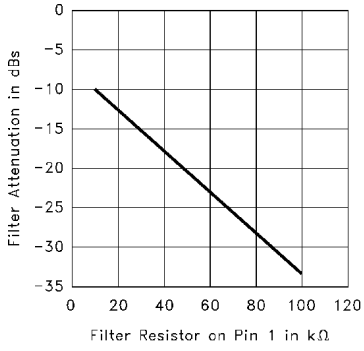
LEVEL OUT (PIN 9) vs SYNC TIP AMPLITUDE



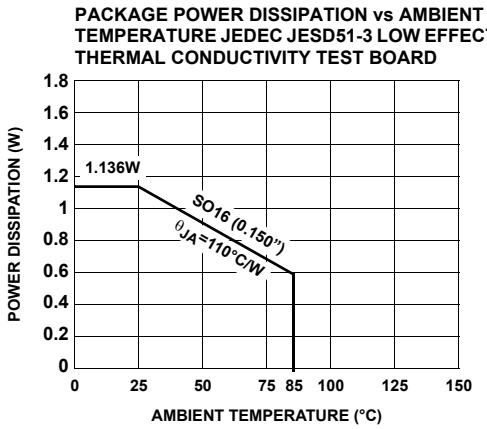
MINIMUM SIGNAL DETECT vs R_{LV}

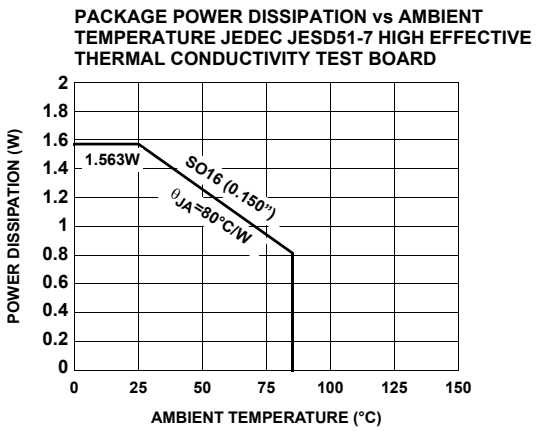


FILTER ATTENUATION vs R_F @ f = 3.58MHz

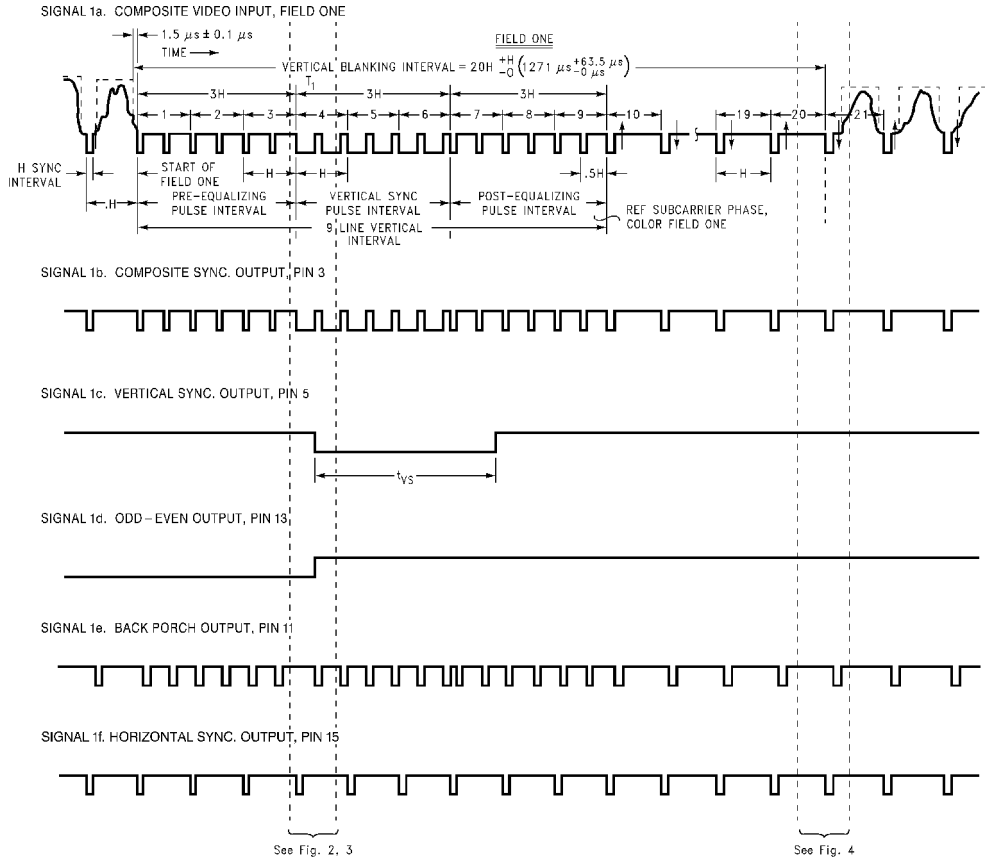


NOTE: For R_{LV} < 1000kΩ, no signal detect output (pin 10) will default high at minimum signal sensitivity specification, or at complete loss of signal.





Timing Diagram



NOTES:

b. The composite sync output reproduces all the video input sync pulses, with a propagation delay.
c. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.
d. Odd-even output is low for even field, and high for odd field.
e. Back porch goes low for a fixed pulse width on the trailing edge of video input sync pulses. Note that for serration pulses during vertical, the back porch starts on the rising edge of the serration pulse (with propagation delay).
f. Horizontal sync output produces the true “H” pulses of nominal width of 5µs. It has the same delay as the composite sync.

FIGURE 1.

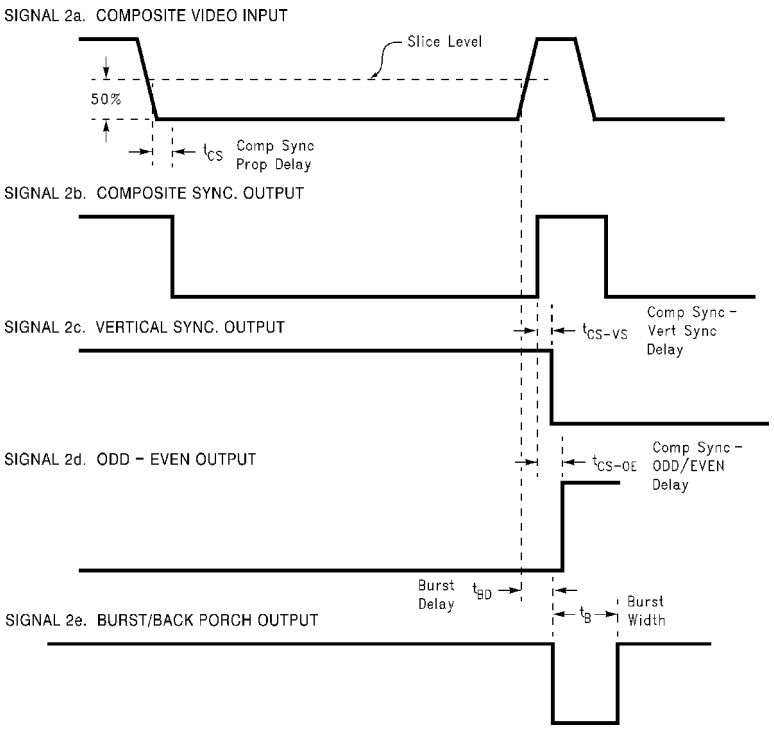


FIGURE 2.

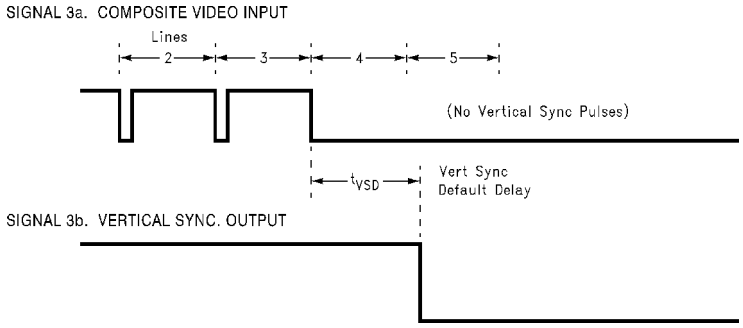


FIGURE 3.

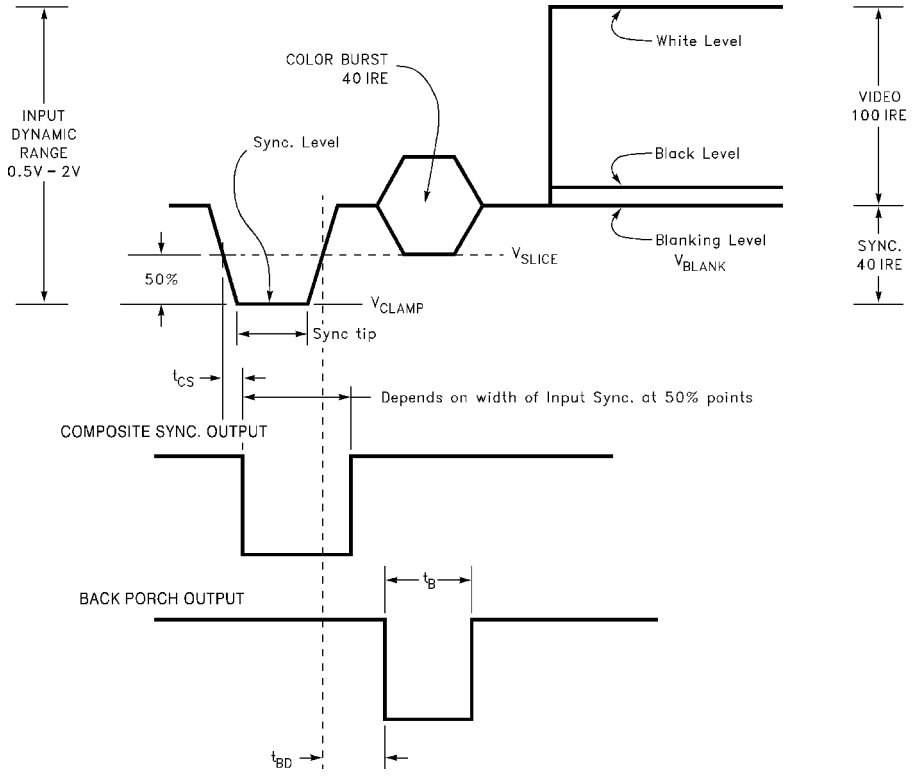


FIGURE 4. STANDARD (NTSC INPUT) H. SYNC DETAIL

Description of Operation

A simplified block schematic is shown in Figure 1. The following description is intended to provide the user with sufficient information to understand the effects of the external components and signal conditions on the outputs of the integrated circuit.

The video signal is AC coupled to pin 4 via the capacitor C_1, nominally 0.1µF. The clamp circuit A1 will prevent the input signal on pin 4 going more negative than 1.5V, the value of reference voltage V_{R1}. Thus the sync tip, the most negative part of the video waveform, will be clamped at 1.5V. The current source I_1, nominally 6µA, charges the coupling capacitor during the remaining portion of the H line, approximately 58µs for a 15.75kHz timebase. From I • t = C • V, the video time-constant can be calculated. It is important to note that the charge taken from the capacitor during video must be replaced during the sync tip time, which is much shorter, (ratio of x 12.5). The corresponding current to restore the charge during sync will therefore be an order of magnitude higher, and any resistance in series with C_I will cause sync tip crushing. For this reason, the internal series resistance has been minimized and external high resistance values in series with the input coupling capacitor should be avoided. The user can exercise some control over the value of the input time constant by introducing an external pull-up resistance from pin 4 to the 5V supply. The maximum voltage across the resistance will be V_{DD} less 1.5V, for black level. For a net discharge current greater than zero, the resistance should be greater than 450k. This will have the effect of increasing the time constant and reducing the degree of picture tilt. The current source I_1 directly tracks reference current I_{TR} and thus increases with scan rate adjustment, as explained later.

The signal is processed through an active 3 pole filter (F1) designed for minimum ripple with constant phase delay. The filter attenuates the color burst by 12dB and eliminates fast transient spikes without sync crushing. An external filter is not necessary. The filter also amplifies the video signal by 6dB to improve the detection accuracy. The filter cut-off frequency is controlled by an external resistor from pin 1 to ground.

Internal reference voltages (block V_{REF}) with high immunity to supply voltage variation are derived on the chip. Reference V_{R4} with op-amp A2 forces pin 12 to a reference voltage of 1.7V nominal. Consequently, it can be seen that the external resistance R_{SET} will determine the value of the reference current I_{TR}. The internal resistance R3 is only about 6kΩ, much less than R_{SET}. All the internal timing

functions on the chip are referenced to I_{TR} and have excellent supply voltage rejection.

To improve noise immunity, the output of the 3 pole filter is brought out to pin 7. It is recommended to AC couple the output to pin 8, the video input pin. In case of strong clean video signal, the video input pin, pin 8, can be driven by the signal directly.

Comparator C2 on the input to the sample and hold block (S/H) compares the leading and trailing edges of the sync pulse with a threshold voltage V_{R2} which is referenced at a fixed level above the clamp voltage V_{R1}. The output of C2 initiates the timing one-shots for gating the sample and hold circuits. The sample of the sync tip is delayed by 0.8µs to enable the actual sample of 2µs to be taken on the optimum section of the sync pulse tip. The acquisition time of the circuit is about three horizontal lines. The double poly CMOS technology enables long time constants to be achieved with small high quality on-chip capacitors. The back porch voltage is similarly derived from the trailing edge of sync, which also serves to cut off the tip sample if the gate time exceeds the tip period. Note that the sample and hold gating times will track R_{SET} through I_{OT}.

The 50% level of the sync tip is derived through the resistor divider R1 and R2, from the sample and held voltages V_{TIP} and V_{BP} and applied to the plus input of comparator C1. This comparator has built in hysteresis to avoid false triggering. The output of C2 is a digital 5V signal which feeds the C/S output buffer B1, the vertical, back porch and odd/even functions.

The vertical circuit senses C/S edges and initiates an integrator which is reset by the shorter horizontal sync pulses but times out with the longer vertical sync pulse widths. The internal timing circuits are referenced to I_{OT} and V_{R3}, the timeout period being inversely proportional to the timing current. The vertical output pulse is started on the first serration pulse in the vertical interval and is then self-timed out. In the absence of a serration pulse, an internal timer will default the start of vertical.

The Horizontal circuit senses C/S edges and produces the true horizontal pulses of nominal width 5µs. The leading edge is triggered from the leading edge of the input H sync, with the same prop. delay as composite sync. The half line pulses present in the input signal during vertical blanking are removed with an internal 2H eliminator circuit. The 2H eliminator initiates a time out period after a horizontal pulse is generated. The time out period is a function of I_{OT} which is set by R_{SET}.

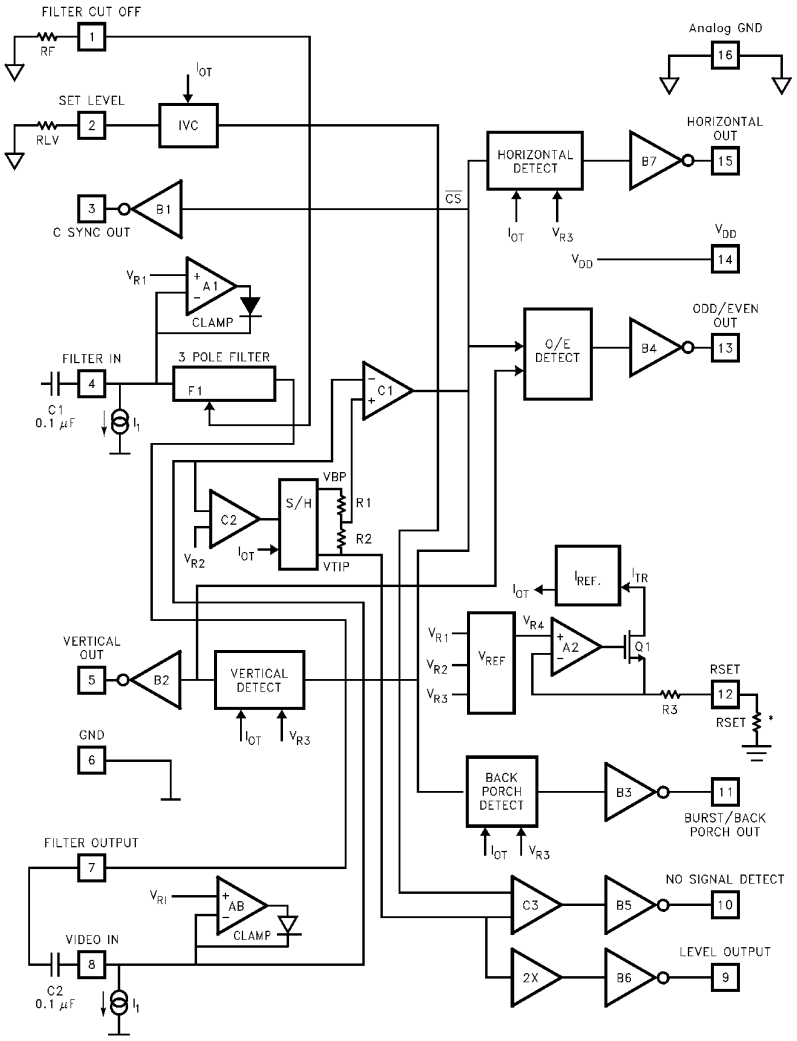
The back porch is triggered from the sync tip trailing edge and initiates a one-shot pulse. The period of this pulse is again a function of I_{OT} and will therefore track the scan rate set by RESET.

The odd/even circuit (O/E) tracks the relationship of the horizontal pulses to the leading edge of the vertical output and will switch on every field at the start of vertical. Pin 13 is high during an odd field.

Loss of video signal can be detected by monitoring the No Signal Detect Output pin 10. The VTIP voltage held by the sample and hold is compared with a voltage level set by R_{LV} on pin 2. Pin 10 output goes high when the VTIP falls below R_{LV} set value.

VTIP voltage is also passed through an amplifier with gain of 2 and buffed to pin 9. This provides an indication of signal strength. This signal (Level Output) can be used for AGC applications.

Block Diagram



* Note: R_{SET} must be a 1% resistor

FIGURE 5. STANDARD (NTSC INPUT) H. SYNC DETAIL

© Copyright Intersil Americas LLC 2004-2010. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com