VCU129 Evaluation Board

User Guide

UG1318 (v1.0) August 12, 2019

XILINX®

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
08/12/2019 Version 1.0	
Initial release.	N/A

Table of Contents

XILINX

Chapter 1

Introduction

Overview

The VCU129 evaluation board enables the evaluation and development of 56G PAM4 applications. Key applications include 56G backplane, 400 GbE and other 56G applications. The VCU129 board for the Xilinx® Virtex® UltraScale+™ FPGA provides a hardware environment for designs targeting the UltraScale+ XCVU29P-L2FSGA2577E device. The VCU129 evaluation board is equipped with various board-level features needed for design development, such as:

- DDR4 DIMM memory
- RLD-3 component memory
- QSFP28 small form-factor pluggable (SFP) interfaces
- QSFP-DD small form-factor pluggable interfaces
- Ganged small form-factor pluggable (SFP28) interfaces
- Ganged small form-factor pluggable (SFP56) interfaces
- Octal small form-factor pluggable (OSFP) interfaces
- PCIe® endpoint cable interfaces (Gen3 x1, x2, x4, x8)
- Ethernet PHY
- General purpose I/O
- UART interface

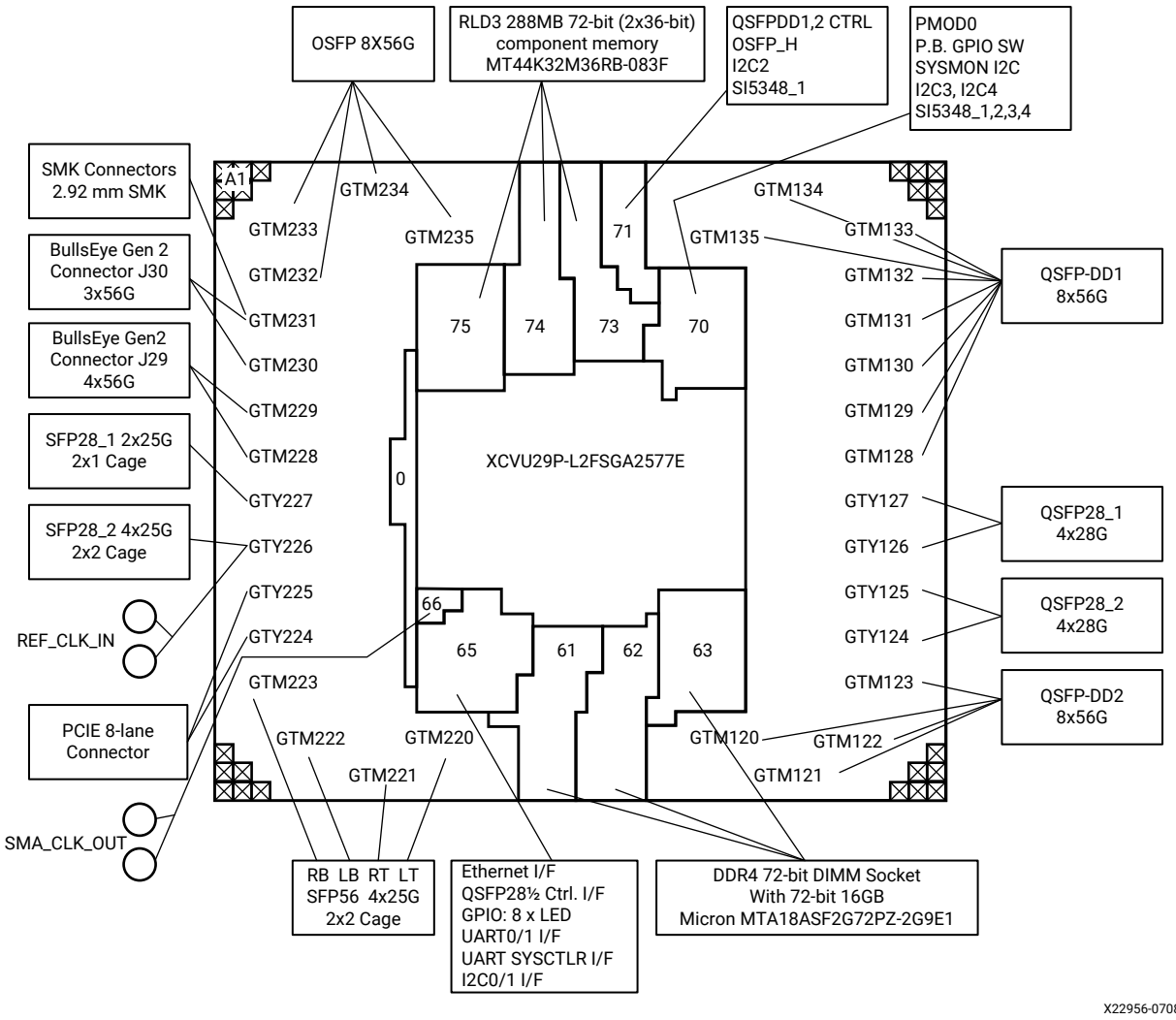
Additional Resources

See Appendix C: Additional Resources and Legal Notices for references to documents, files, and resources relevant to the VCU129 evaluation board.

Block Diagram

A block diagram of the VCU129 evaluation board is shown in the following figure.

Figure 1: **VCU129 Evaluation Board Block Diagram**



Board Features

The VCU129 evaluation board features are listed here. Detailed information for each feature is provided in Chapter 3: Board Component Descriptions.

- Virtex UltraScale+ XCVU29P-L2FSGA2577E device

- 2 Gb Quad SPI flash configuration memory
- 2x QSFP56-DD module interface
- OSFP module interface
- SFP56
- DDR4 DIMM socket (72-bit) with 16 GB DIMM installed
- 288 MB 72-bit RLD3 component memory interface (2 x [1.125 Gb x 36])
- 2x QSFP28 module interface
- 4x QSFP28 100 Gb/s Optical Interface
- SFP28
- 2x BullsEye Gen2
- USB JTAG interface (FTDI FT4232HL with a micro-AB USB connector)
- Clock sources:
  - Memory I/F clocks:
    - 2x Si570 (DDR4 300 MHz, RLD3 100 MHz) LVDS oscillators
  - QSFP clocks:
    - Four 7-output Si5348 I2C program clock oscillators (156.25 MHz default)
    - External SMA different clock input to GTY226 for QSFP
  - PCIe connector I/F clock:
    - Fixed 100 MHz HCSL clock from PCIe connector input to 1 to 2 clock buffer wired to GTY224 and GTY225
  - System Controller clock:
    - SiT8008A 33.33 MHz single-ended clock oscillator
  - GPIO clocks:
    - External SMA different clock I/O to Bank 66
- 32 GTY transceivers (eight Quads)
  - 2x28 Gb/s QSFP28 connectors (eight GTY transceivers)
  - 4x28 Gb/s SFP28 (2x2) connector (four GTY transceivers)
  - 2x28 Gb/s SFP28 (2x1) connector (two GTY transceivers)
  - PCIe 8-lane endpoint connector (eight GTY transceivers)
  - Not used (10 GTY transceivers)

- 48 GTM transceivers (24 Duals)
  - 2x28 Gb/s 2x QSFP-DD interfaces (sixteen GTM transceivers)
  - 25 Gb/s SFP56 (2x2) interfaces (four GTM transceivers)
  - 2x Bulls Eye (Gen 2) interfaces (seven GTM transceivers)
  - SMK connector (one GTM transceiver)
  - OSFP interfaces (eight GTM transceivers)
  - Not used (twelve GTM transceivers)
- PCI Express endpoint interfaces
  - Gen1 (x1, x2, x4, x8)
  - Gen2 (x1, x2, x4, x8)
  - Gen3 (x1, x2, x4, x8)
- Ethernet PHY SGMII interface with RJ-45 connector
- USB JTAG UART bridge with micro-B USB connector (shared FTDI FT4232HL)
- I2C bus
- Status LEDs
- User I/O (6 x P.B. switch, 4-pole DIP switch, 8 x LED, male PMOD, female PMOD)
- Power management with I2C monitoring (TI Fusion GUI, system controller SCUI)
- Configuration options:
  - Quad SPI flash memory
  - USB JTAG I/F (FTDI FT4232HL)
  - Platform cable USB II interface 2x7 2 mm keyed connector
- Zynq®-7000 SoC XC7Z010 based system controller

Board Specifications

Dimensions

Rectangular Form-factor

- **Height:** 11.50 inch (29.21 cm)

- **Length:** 15.00 inch (38.10 cm)
- **Thickness (±5%):** 0.125 inch (0.3175 cm)

***Note*:** A 3D model of this board is not available.

Environmental

- **Temperature:** Operating: 0°C to +45°C, Storage: -25°C to +60°C
- **Humidity:** 10% to 90% non-condensing

Operating Voltage

+12 V_{DC}

Chapter 2

Board Setup and Configuration

Electrostatic Discharge Caution

CAUTION! *ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.*

To prevent ESD damage:

- Use an ESD wrist or ankle strap and ensure that it makes skin contact. Connect the equipment end of the strap to an unpainted metal surface on the chassis.
- Avoid touching the adapter against your clothing. The wrist strap protects components from ESD on the body only.
- Handle the adapter by its bracket or edges only. Avoid touching the printed circuit board or the connectors.
- Put the adapter down only on an antistatic surface such as the bag supplied in your kit.
- If you are returning the adapter to Xilinx® Product Support, place it back in its antistatic bag immediately.

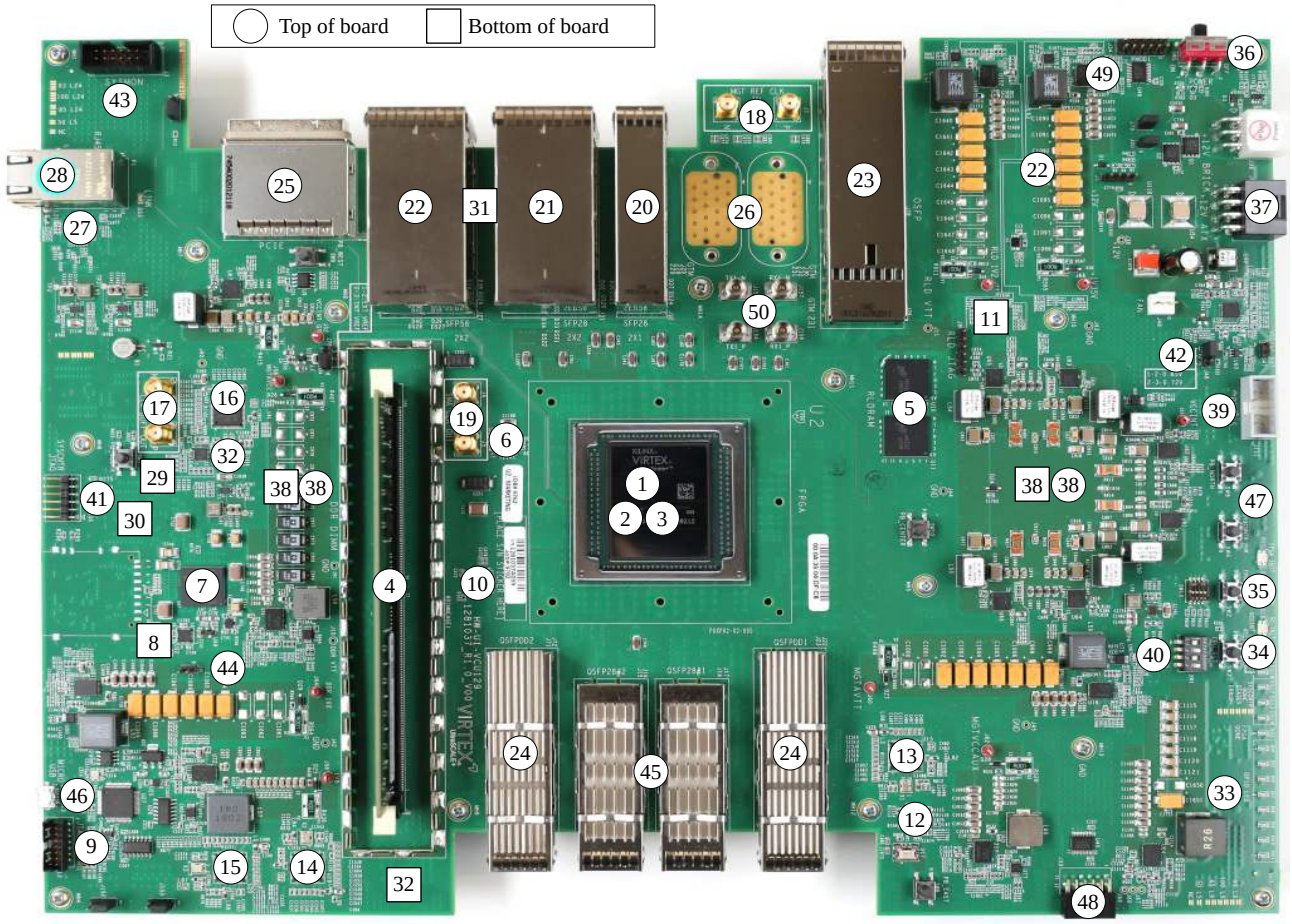
Board Component Location

The figure below shows the VCU129 board component locations. Each numbered component shown in the figure is keyed to VCU129 Board Component Descriptions. VCU129 Board Component Descriptions identifies the components, references the respective schematic page numbers, and links to a detailed functional description of the components and Chapter 3: Board Component Descriptions.

IMPORTANT! *Figure 2 is for visual reference only and might not reflect the current revision of the board.*

IMPORTANT! *There could be multiple revisions of this board. The specific details concerning the differences between revisions are not captured in this document. This document is not intended to be a reference design guide and the information herein should not be used as such. Always refer to the schematic, layout, and XDC files of the specific VCU129 version of interest for such details.*

Figure 2: **VCU129 Evaluation Board Component Locations**



X23059-073019

VCU129 Board Component Descriptions

Table 1: **VCU129 Board Component Descriptions**

Callout	Feature (U#) = Top [U#] = Bottom	Notes	Schematic Page Number
1	Virtex UltraScale+ XCVU29P-L2FSGA2577E Device (U2), (with fan-sink on soldered FPGA)	XCVU29P-L2FSGA2577E with Cofan 30-6090-01	
2	GTY Transceivers (32 GTY within eight quads)	Embedded within FPGA U2	10, 14
3	GTM Transceivers (48 GTM within twenty-four duals)	Embedded within FPGA U2	9, 11-13, 15-16

Table 1: **VCU129 Board Component Descriptions** *(cont'd)*

Callout	Feature (U#) = Top [U#] = Bottom	Notes	Schematic Page Number
4	DDR4 DIMM Memory socket, 72-bit I/F, (J8) with 16 GB DIMM installed	FCI 10124677-0001001LF Micron MTA18ASF2G72PZ-2G9E1	24
5	RLD3 Component Memory, RLD3 72-bit component memory I/F (U10, U11)	2 x Micron MT44K32M36RB-083F	29-30
6	Quad SPI Flash Memory (U1)	Micron MT25QU02GCBB8E12-0SIT	3
7	System Controller, Zynq-7000 SoC (U47)	XC7Z010CLG225	45-48
8	Quad SPI Flash Memory [U51]	Micron MT25QU128ABA	47
9	JTAG cable connector 2x7 2 mm shrouded & keyed (J12)	Molex 87832-1420	31
10	DDR4 DIMM Memory I/F clock, 300 MHz LVDS (U14)	Silicon Labs SI570BAB000313DG (default 300 MHz)	27
11	RLD3 Interface Clock I/F clock, 100 MHz LVDS [U16]	Silicon Labs SI570BAB002038DG (default 100 MHz)	27
12	12.8 MHz Ref. Clk. TCXO (U17) and 1 to 4 buffer (U18) for 4 x SI5348	Conner-Winnfield T200F-012.8M and SiLabs SI53306-B-GM	27
13	SI5348 I2C (7-output) Program Clock, LVDS (U15)	Silicon Labs SI5348A-D09879-GM (default 156.250 MHz)	27
14	SI5348 I2C (7-output) Program Clock, LVDS (U19)	Silicon Labs SI5348A-D09879-GM (default 156.250 MHz)	28
15	SI5348 I2C (7-output) Program Clock, LVDS (U20)	Silicon Labs SI5348A-D09879-GM (default 156.250 MHz)	29
16	SI5348 I2C (7-output) Program Clock, LVDS (U21)	Silicon Labs SI5348A-D09879-GM (default 156.250 MHz)	30
17	SI5348 (U21) CH6 output clk SMA J75 (P)/J76 (N)	Rosenberger 32K10K-400L5	30
18	User QSFP SMA Connector Clocks pair J7 (P)/J6 (N) input to XCVU29P U2 GTY226	Rosenberger 32K10K-400L5	12
19	User SMA Connector Clocks pair J5 (P)/J4 (N) direct connect to XCVU29P U2 Bank 66	Rosenberger 32K10K-400L5	5
20	(2 x 1) SFP28 Module Connector, SFP28A-B (J32A, J32B) wired to VCU129 GTY Interface Connections 227, with cage (J32C)	Amphenol UE86-3G1620-10361 with cage (1 wide x 2 high)	42 12 (GTY)
21	(2 x 2) SFP28 Module Connector, SFP28_2_LT, RT, LB, RB (J31A-D), wired to VCU129 GTY Interface Connections 226, with cage (J31E)	2 x 2 Amphenol UE86-3G2620-10361 with cage (2 wide x 2 high)	41 12 (GTY)
22	2 x 2 SFP56 Module Connector, SFP56_LT, RT, LB, RB (J27A-D), wired to VCU129 GTM Interface Connections 220-223, with cage (J27E)	2 x 2 Amphenol UE86-3G2620-10361 with cage (2 wide x 2 high)	43 11 (GTM)

Table 1: **VCU129 Board Component Descriptions** *(cont'd)*

Callout	Feature (U#) = Top [U#] = Bottom	Notes	Schematic Page Number
23	OSFP Module Connector, OSFP (J26) wired to VCU129 GTM Interface Connections 232-235, with cage (J28)	Amphenol UE62-A1011-3000T with UE62-B1620-02011 cage	39 14 (GTM)
24	2 x QSFPDD Module Connector, QSFPDD1 (J22) wired to VCU129 GTM Interface Connections 128/135, QSFPDD2 (J71) wired to VCU129 GTM Interface Connections 120-123	2 x Amphenol UE36-A1010-3000T with UE36-B16200-06A2A cage w/ heatsink	38 7,9,10 (GTM)
25	PCI Express Endpoint Connectivity (J18) wired to VCU129 GTY Interface Connections 224/225, with guide housing	Connector: Molex 75586-0007 Guide Housing: Molex 74540-0201	37 12 (GTY)
26	2 x Bulls Eye Gen2 connector pads (J29, J30)	Samtec RSP-200723-XX-BEYE (optional)	40
27	10/100/1000 Mb/s Tri-Speed Ethernet PHY with RJ45, SGMII mode only, [U40], (P1)	TI DP83867ISRGZ with Wurth 7499111221A RJ45 (with magnetics)	37
28	Ethernet PHY Status LEDs, LEDs are integrated into P1 bezel	Wurth 7499111221A RJ45 with integrated status LEDs	37
29	I2C0 Bus Topology, 3 x I2C level-translator [U30, U31, U33] and port expander [U32]	3 x TI PCA9306 level-translator 1 x TI TCA6416A port expander	32
30	I2C1 Bus Topology, 2 x I2C level-translator [U35, U36] and 2 x switch [U37, U39]	2 x TI PCA9306 level-translator 2 x TI TCA9548A port switch	33
31	I2C2 Bus Topology, 2 x port expander [U91, U100]	2 x TI TCA6416A port expander	34
32	I2C3 Bus Topology, 2 x port expander [U93], (U104)	2 x TI TCA6416A port expander	34
33	User GPIO LEDs (DS4-DS11), active-High	Lumex SML-LX0603GW-TR	44
34	User GPIO Pushbutton, CPU reset (SW3), active-High	E-Switch TL3301EF100QG	44
35	Program_B Pushbutton Switch SW2, active-Low	E-Switch TL3301EF100QG	3
36	Switches, Power On/Off Slide Switch SW5	C&K 1201M2S3AQE2	49
37	Power Input Connectors, Molex 2x6 (J39) in parallel with Astron 2x4 (JP1) (use one only)	2x6 Molex 39-30-1060 2x8 Astron 6652208-T0003T-H	49
38	VCU129 Board Power System, power management system (top) and [bottom]	TI power system	49-64
39	PMBus 2x5 shrouded male pin header (J151)	Assmann AWHW10G-0202-T	52
40	FPGA U2 configuration mode DIP switch, (SW1)	4-pole CTS 218-4LPSTRF	3
41	System Controller rt-angle JTAG header, (J35)	1x6 Samtec TSW-106-22-F-S-RA	45
42	FPGA VCCINT select header, (J48)	1x3 Sullins PBC36SAAN	45
43	SYSMON header, (J3)	2x6 Molex 70246-1201	53
44	SYS CTLR RE-PROG header, (J36)	1x2 Sullins PBC36SAAN	47

Table 1: **VCU129 Board Component Descriptions** *(cont'd)*

Callout	Feature (U#) = Top [U#] = Bottom	Notes	Schematic Page Number
45	2 x QSFP28 Module Connector, QSFP1 (J14) wired to GTY126/127, QSFP2 (J15) wired to GTY124/125	2 x Amphenol FS1-Z38-20Z6-60 with U95-T171-100A cage w/ heatsink	36 8 (GTY)
46	USB micro-AB (J13) and 2mm USB JTAG Interface keyed cable connector (J12), USB UART Interface (U27)	Hirose ZX62D-AB-5P8(30) USB micro-AB Molex 87832-1420, FTDI FT4232HL	31
47	SYSCTLR_POR_B Pushbutton (SW4), active-Low	E-Switch TL3301EF100QG	47
48	PMOD0 2x6 Rt-Angle Receptacle (J33)	Sullins PPPC062LJBN-RC	
49	PMOD1 2x6 Vertical Pin Header (J34)	Sullins PBC36DAAN	44
50	SMK 2.9 mm connectors (J154, J155, J156, J157)	Molex 0732520091	40

Default Jumper and Switch Settings

Jumpers

Table 2: **VCU129 Board Default Jumper Settings**

Ref. Des.	Function	Default	Schematic Page
J2	POR_OVERRIDE	2-3	3
	1-2: Enable		
	2-3: Disable		
J1	PCIe Test Header	OPEN	3
	1: FPGA DONE test point		
	2: FPGA_INIT_B test point		
	3: PGOOD test point		
	4: GND		
J78	SYSMON VREF Selection	1-2	3
	1-2: 1.25V External VREFP connected to FPGA		
	2-3: VREFP connected to GND (Internal VREF)		
J79	SYSMON VP and I2C Address	ON	3
	OFF: SYSMON_VP_R floating		
	ON: SYSMON_VP pulled down		
J80	SYSMON VN and I2C Address	ON	3
	OFF: SYSMON_VN_R floating		
	ON: SYSMON_VN pulled down		

Table 2: **VCU129 Board Default Jumper Settings** *(cont'd)*

Ref. Des.	Function	Default	Schematic Page
J48	VCCINT Selection	1-2	45
	1-2: Configure VCCINT to 0.85V		
	2-3: Configure VCCINT to 0.72V		
J36	System Controller QSPI DQ3	OFF	47
	OFF: SYSCTLR_QSPI_IO3 pulled to 1.8V		
	ON: SYSCTLR_QSPI_IO3 pulled to GND		
J47	VCCINT Regulator Reset	OPEN	51
	OFF: VCCINT_RESET pulled up		
	ON: VCCINT_RESET pulled to GND		
J152	SYS_1V0, SYS_1V8 & UTIL_3V3 Power regulator enable through Jumper	1-2	54
	1-2: Disable the power regulators		
	2-3: Enable the power regulators		
J153	Remaining power regulators enable through Jumper	1-2	54
	1-2: Disable the power regulators		
	2-3: Enable the power regulators		

Switches

Table 3: **VCU129 Board Default Switch Settings**

Ref. Des.	Function	Default	Schematic Page
SW1	FPGA Boot Mode Selection/ SYS_CTLR Enable IO	X001	3
	Switch OFF = 1 = High; ON = 0 = Low		
	SW1[2:4] = Mode Pins[2:0] M[2:0]: 101 > JTAG 001 > Master SPI		
	SW1[1] = SYS_CTLR_EN (FW dependent)		
SW5	Power ON Switch	2-3	49
	1-2: Power ON		
	2-3: Power OFF		
SW13	User Programmable for FPGA - GPIO	XXXX	44
	Switch OFF = 1 = High; ON = 0 = Low		

FPGA Configuration

The VCU129 board supports two of the UltraScale+™ FPGA configuration modes:

- Quad SPI 2 Gb flash memory (U1)
- JTAG using:
  - USB JTAG configuration port (FT4232HL U27 + USB J13 micro-AB)
  - Xilinx® Platform Cable USB II, 2 mm, keyed flat cable header (J12)

Each configuration interface corresponds to one or more configuration modes and bus widths, as listed in the table below. The mode switches M2, M1, and M0 are on SW1 positions 2, 3, and 4, respectively. The FPGA default mode setting M[2:0] = 001 selects the master SPI configuration mode.

Table 4: **Configuration Modes**

Configuration Mode	SW1 DIP Switch Settings M[2:0]	Bus Width	CCLK Direction
Master SPI	001	x1, x2, x4	Output
JTAG	101	x1	Not Applicable

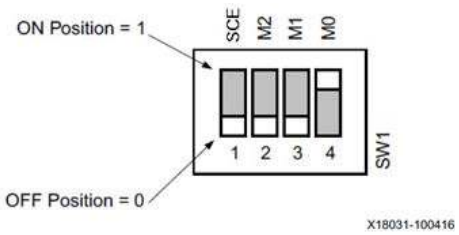
Notes:

1. DIP SW1 is active-High (connected net is pulled High when DIP switch is on/closed).

For complete details on configuring the FPGA, see *UltraScale Architecture Configuration User Guide* (UG570).

The following figure shows the configuration mode DIP switch SW1 JTAG switch positions.

Figure 3: **SW1 JTAG Mode Settings**



JTAG

Vivado®, Xilinx® SDK, or third-party tools can establish a JTAG connection to the XCVU29P FPGA device through the FTDI FT4232H USB-to-JTAG/USB UART device (U27) connected to micro-USB connector (J13). Alternatively, a JTAG cable can be connected to the keyed flat cable header (J12). JTAG initiated configuration takes priority over the configuration method selected through the FPGA mode pins M[2:0], wired to SW1 positions [2:4].

Quad SPI

To boot from the dual Quad SPI nonvolatile configuration memory:

1. Store a valid XCVU29P FPGA boot image in the 2 Gb Quad SPI flash device (U1) connected to the FPGA Bank 0 Quad SPI interface. See the VCU129 Restoring Flash Tutorial XTP563 for information on programming the QSPI.
2. Set the boot mode pins SW1 M[2:0] as indicated in Table 4: Configuration Modes for Master SPI.
3. Power-cycle the VCU129 board. Mode SW1 is callout 40 in Figure 2: VCU129 Evaluation Board Component Locations.

The Virtex UltraScale+ FPGA maximum QSPI clock frequency of 125 MHz for -2 speed devices and 100 MHz for -2L devices are listed in the *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* (DS923).

XILINX

Chapter 3

Board Component Descriptions

Overview

This chapter provides a detailed functional description of the board's components and features. VCU129 Board Component Descriptions identifies the components, references the respective schematic page numbers, and links to the corresponding detailed functional description in this chapter. Component locations are shown in Figure 2.

Component Descriptions

Virtex UltraScale+ XCVU29P-L2FSGA2577E Device

[Figure 2, callout 1]

The VCU129 board is populated with the Virtex UltraScale+ XCVU29P-L2FSGA2577E device. For more information on Virtex UltraScale+ FPGAs, see *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* (DS923).

- **Encryption Key Battery Backup Circuit:** The Seiko TS621E rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to the XCVU29P device U1 VBATT pin BB14. The battery supply current IBATT specification is 150 nA maximum when the board power is off. B1 is charged from the VCC1V8 1.8V rail through a series diode with a typical forward voltage drop of 0.38V and 4.7 KΩ current limit resistor. The nominal charging voltage is 1.42V. The XCVU29P device U2 implements bitstream encryption key technology. The VCU129 board provides an encryption key button-type battery backup circuit.
- **I/O Voltage Rails:** There are 10 I/O banks available on the XCVU29P device and the VCU129 board. The voltages applied to the FPGA banks on the VCU129 board are listed in the table below.

Table 5: **I/O Bank Voltage Rails**

FPGA (U1) Bank	Power Supply Rail Net Name	Voltage
Bank 0	VCC1V8	1.8V
HP Bank 61	DDR4_VDDQ_1V2	1.2V
HP Bank 62	DDR4_VDDQ_1V2	1.2V
HP Bank 63	DDR4_VDDQ_1V2	1.2V
HP Bank 65	VCC1V8	1.8V
HP Bank 66	VCC1V8	1.8V
HP Bank 70	VCC1V8	1.8V
HP Bank 71	VCC1V8	1.8V
HP Bank 73	RLD3_VDDQ_1V2	1.2V
HP Bank 74	RLD3_VDDQ_1V2	1.2V
HP Bank 75	RLD3_VDDQ_1V2	1.2V

DDR4 DIMM Memory

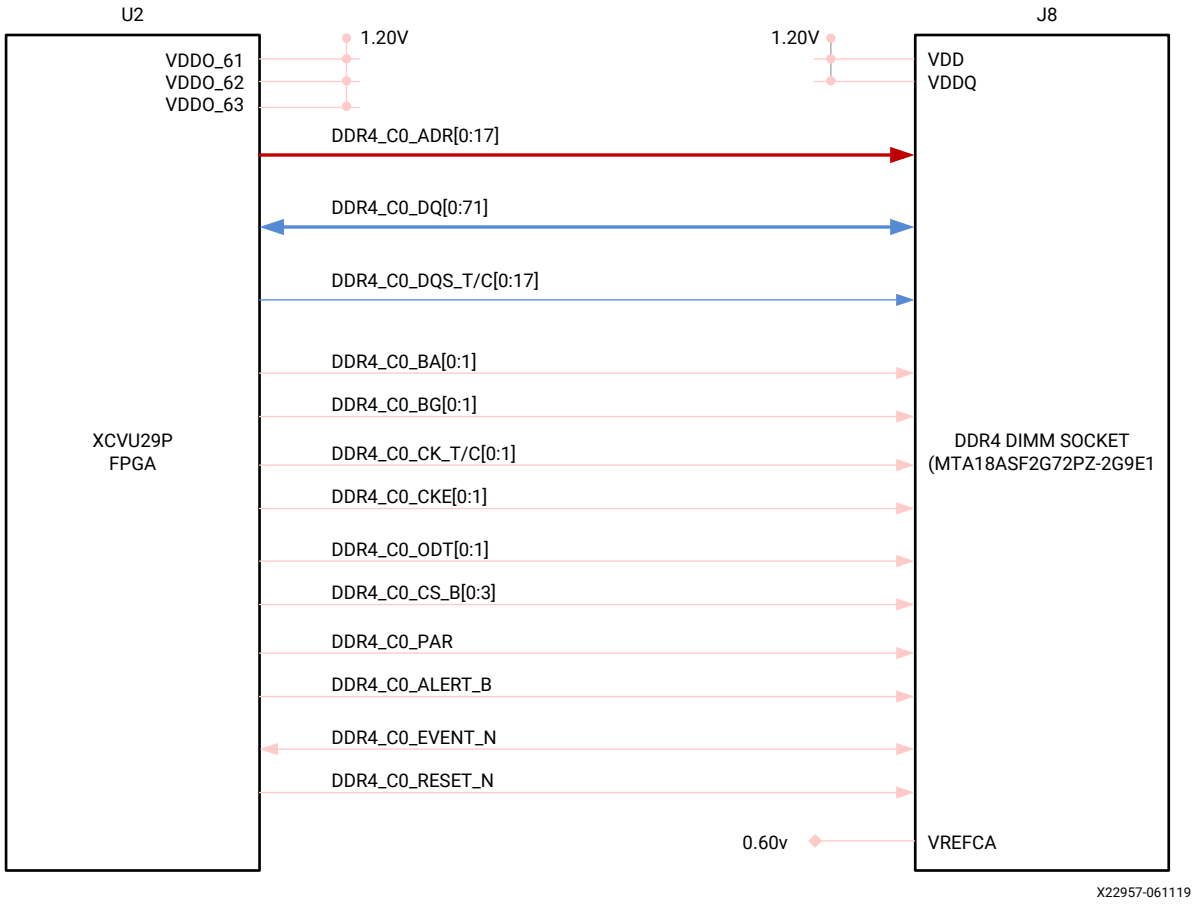
[Figure 2, callout 4]

A 72-bit wide, 288-pin DDR4 DIMM memory socket (J8) is connected to XCVU29P U2 HP banks 61, 62, and 63. The VCU129 is shipped with a DDR4 72-bit 16 GB RDIMM installed:

- Manufacturer: Micron
- Part Number: MTA18ASF2G72PZ-2G9E1
- Description:
  - 16 GB 288-pin DDR4 RDIMM
  - Single rank
  - 2 Gb 72

The VCU129 XCVU29P FPGA DDR4 interface performance is documented in the *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* (DS923).

Figure 4: **DDR4 Memory Interface**



The DDR4 0.6V V_{TT} termination voltage (net DDR4_C0_VTT) is sourced from the TI TPS51200DR linear regulator (U12). The DDR4 memory interface bank VREF pins are not connected, which, coupled with an XDC set_property INTERNAL VREF constraint, invoke the INTERNAL VREF mode.

The detailed FPGA connections for the feature described in this section are documented in the VCU129 board XDC file, referenced in Appendix A: Xilinx Design Constraints.

The VCU129 DDR4 DIMM interface adheres to the constraints guidelines documented in the "DDR3/DDR4 Design Guidelines" section of the *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150). The VCU129 board DDR4 memory component interface is a 40Ω impedance implementation.

For more information on the internal VREF, see the "Supply Voltages for the SelectIO Pins VREF" and the "Internal VREF" sections in the *UltraScale Architecture SelectIO Resources User Guide* (UG571). For more details about the Micron DDR4 DIMM memory, see the Micron MTA18ASF2G72PZ-2G9E1 data sheet at the Micron website.

RLD3 Component Memory

[Figure 2, callout 5]

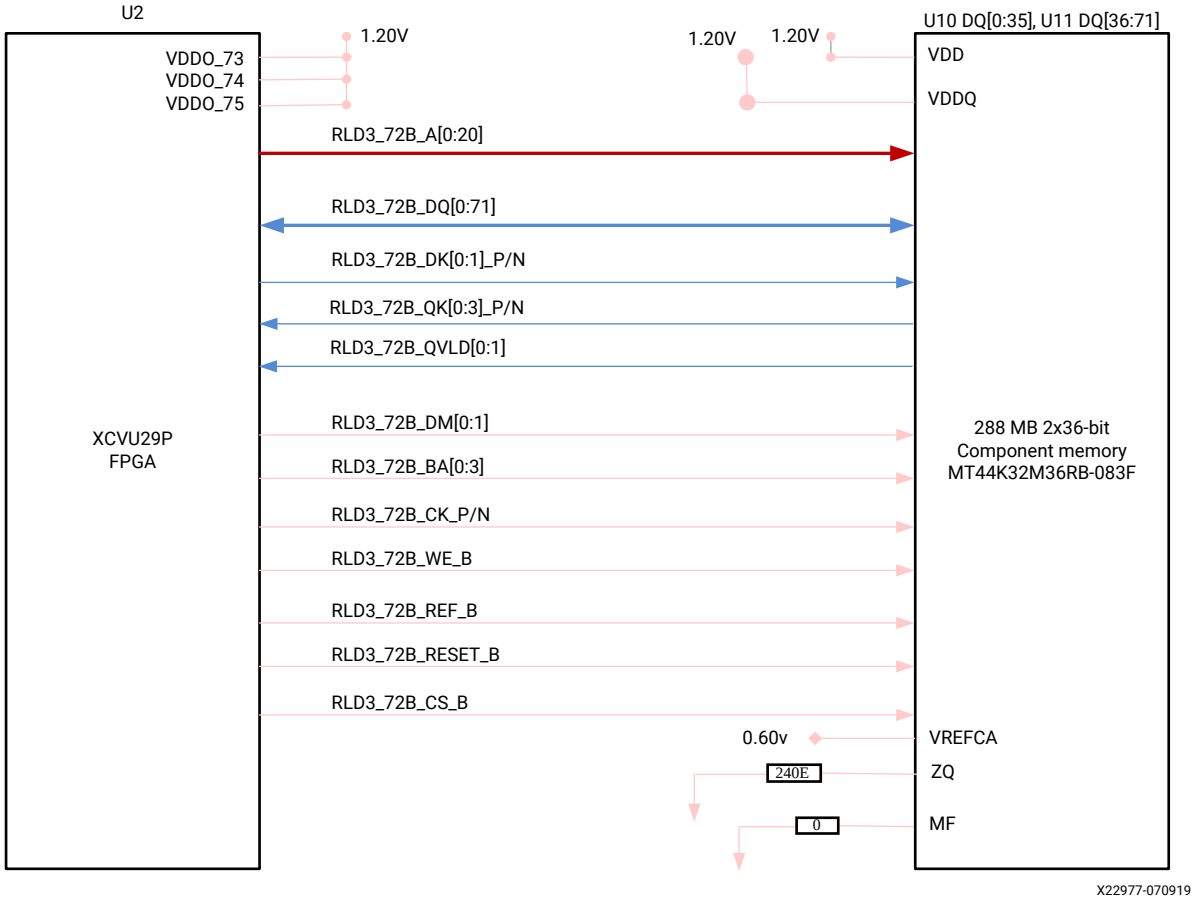
The 288 MB RLD3 72-bit wide component memory system is comprised of two 36-bit 1.125 Gb RLDRAM3 devices (U10, U11). This memory system is connected to the XCVU29P HP banks 73, 74, and 75.

- Manufacturer: Micron
- Part Number: MT44K32M36RB-083F
- Description:
  - 1.125 Gb (32 Mb x 36)
  - 1.2V 168-ball BGA
  - Supports up to RL3-2400

The VCU129 XCVU29P FPGA RLDRAM3 interface performance is documented in the *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* (DS923).

The RLD3 component memory interface diagram is shown in the figure below.

Figure 5: **RLD3 Memory Interface**



The RLD3 0.6V VTT termination voltage (net RLD3_VTERM_0V6) is sourced from TI TPS51200DR linear regulator U13. The RLD3 memory interface bank VREF pins are not connected, which, coupled with an XDC set_property INTERNAL_VREF constraint, invoke the INTERNAL VREF mode.

The detailed FPGA connections for the feature described in this section are documented in the VCU129 board XDC file, referenced in Appendix A: Xilinx Design Constraints.

The VCU129 RLD3 memory component interface adheres to the constraints guidelines documented in the RLD3 Design Guidelines section of *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150). The VCU129 RLD3 memory component interface is a 40Ω impedance implementation.

For more information on the internal VREF, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

For more details about the Micron RLD3 component memory, see the Micron MT44K32M36RB Data Sheet on the Micron website.

Quad SPI Flash Memory

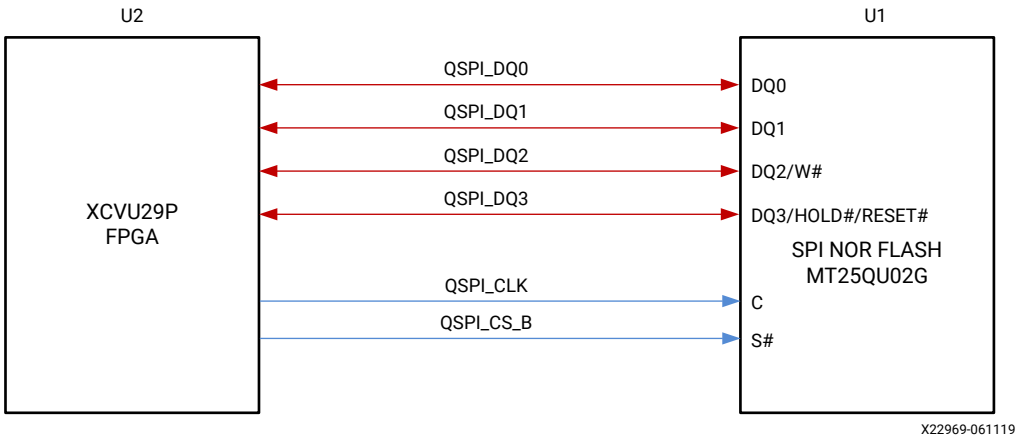
[Figure 2, callout 6]

VCU129 boards host a Micron MT25QU02GCBB8E12-0SIT 2 Gb (256 MB) serial NOR flash Quad SPI flash memory capable of holding the boot image for the XCVU29P FPGA. This interface supports the QSPI32 boot mode as defined in the *UltraScale Architecture Configuration User Guide* (UG570).

The Quad SPI flash memory U1 provides 2 Gb of non-volatile storage that can be used for configuration and data storage.

- Manufacturer: Micron
- Part number: MT25QU02GCBB8E12-0SIT
- Supply voltage: 1.8V
- Datapath width: 4 bits
- Data rate: various depending on single/dual/quad mode. The QSPI interface in the following figure.

Figure 6: **Quad SPI (2 Gb) Flash Memory Interface**



The detailed FPGA connections for the feature described in this section are documented in the VCU129 board XDC file, referenced in Appendix A: Xilinx Design Constraints.

The *UltraScale Architecture Configuration User Guide* (UG570) provides FPGA configuration details.

For Quad SPI component information, see the Micron MT25QU02GCBB8E12-0SIT data sheet at the Micron website.

USB JTAG Interface

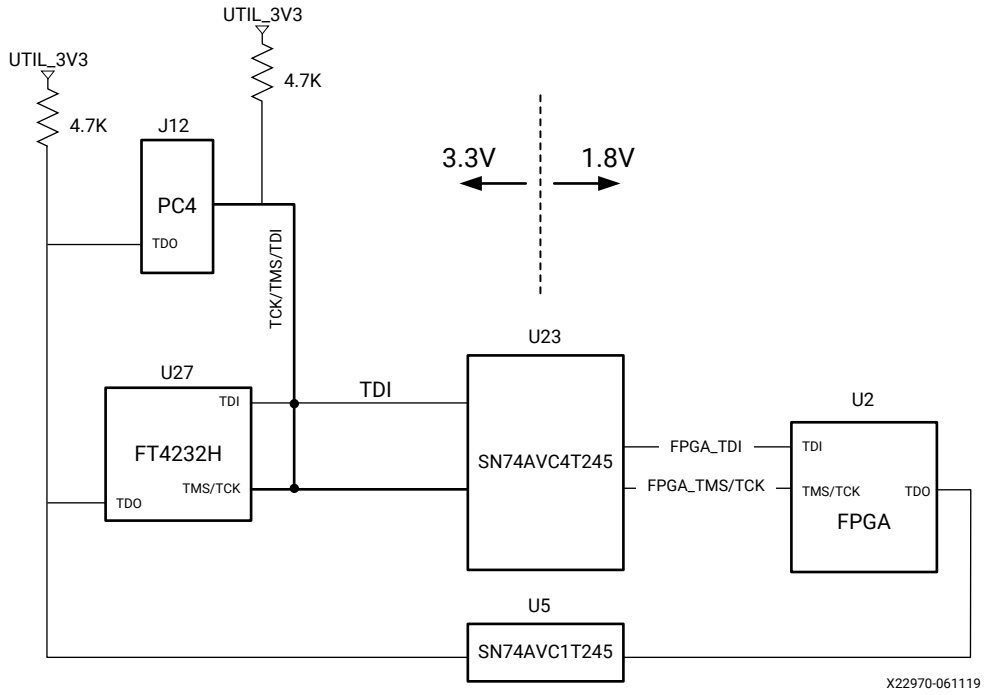
[Figure 2, callout 46]

JTAG configuration is provided through a dual-function FTDI FT4232HL USB-to-JTAG/UART bridge device (U27) where a host computer accesses the VCU129 board JTAG chain through a type-A (PC host side) to micro-AB (VCU129 board side J13) USB cable.

A 2 mm 2x7 JTAG keyed header (J12) is also provided in parallel for access by Xilinx® download cables, such as the Platform Cable USB II. JTAG initiated configuration takes priority over the configuration method selected through the FPGA mode pins M[2:0], wired to SW1 positions [2:4].

The JTAG chain of the VCU129 board is illustrated in the following figure.

Figure 7: **JTAG Chain Block Diagram**



The JTAG connectivity on the VCU129 board allows a host computer to download bitstreams to the FPGA using the Xilinx tools. In addition, the JTAG connector allows debug tools such as the Vivado serial I/O analyzer or a software debugger to access the FPGA. The Xilinx tools can also program the Quad SPI flash memory. For more information about the FT4232HL-REEL, see the data sheet at the FTDI website.

USB UART Interface

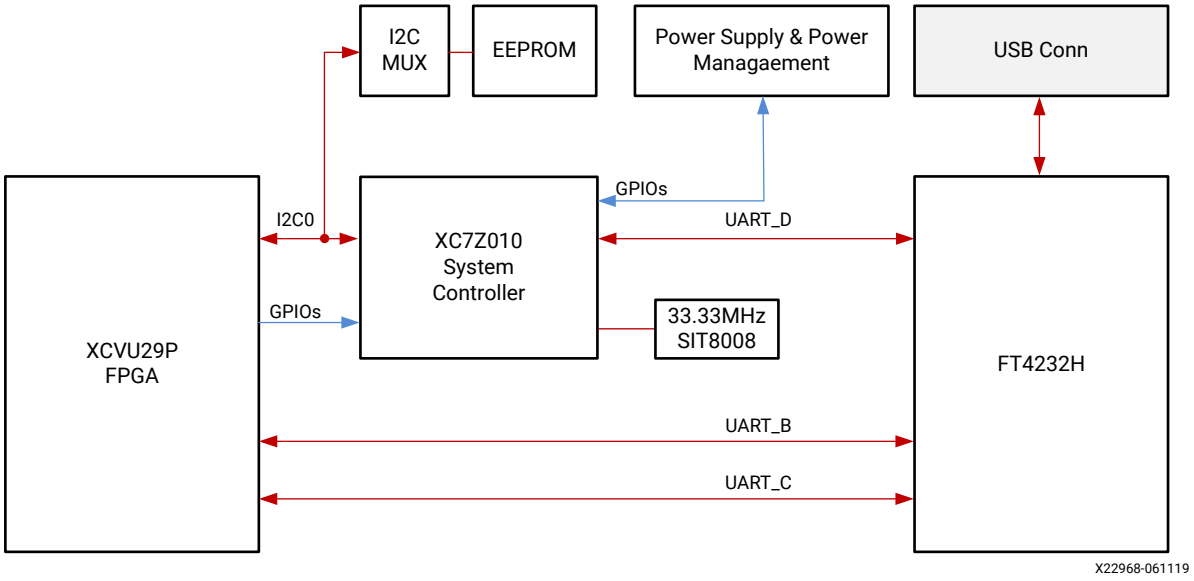
[Figure 2, callout 46]

The FT4232HL U27 multi-function USB-UART on the VCU129 board provides three level-shifted UART connections through the single micro-AB USB connector J2.

- Channel A (ADBUS) is configured in JTAG mode to support the JTAG chain.
- Channel B (BDBUS) implements 4-wire UART0 (U26 level-shifted) FPGA U2 bank 65 connections.
- Channel C (CDBUS) implements 4-wire UART1 (U28 level-shifted) FPGA U2 bank 65 connections.
- Channel D (DDBUS) implements 2-wire (U25 level-shifted) SYSCTLR U47 bank 501 connections.

The USB UART interface is shown in the following figure (level-shifters omitted for clarity).

Figure 8: **FTDI USB UART Circuit**



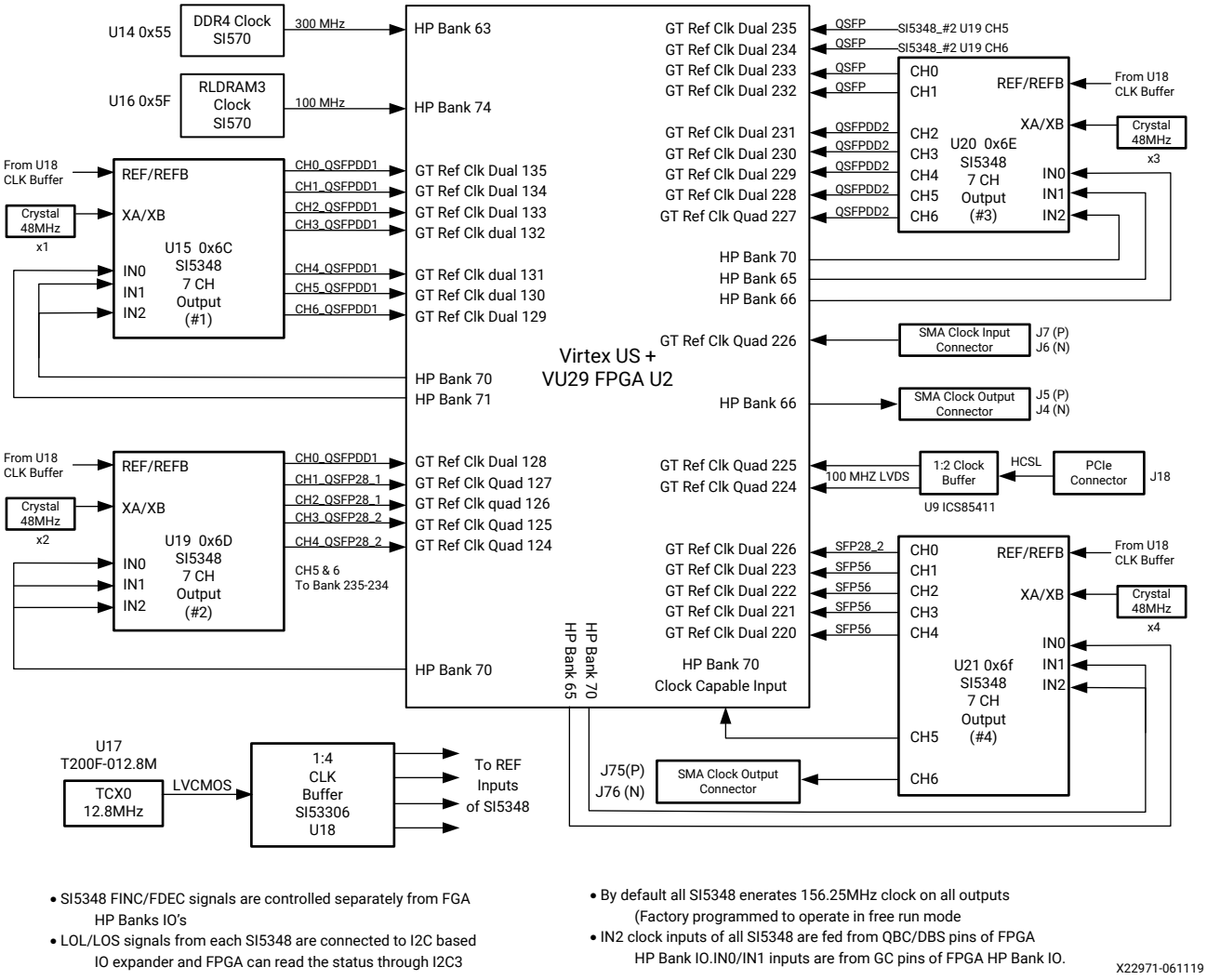
The detailed FPGA connections for the feature described in this section are documented in the VCU129 board XDC file, referenced in Appendix A: Xilinx Design Constraints.

Clock Generation

[Figure 2, callout 10–19]

The VCU129 evaluation board clocking diagram is shown in the following figure.

Figure 9: **VCU129 Clocking Diagram**



The VCU129 evaluation board fixed frequency clock sources are listed in the following table.

Table 6: **VCU129 Board Fixed Frequency Clock Sources**

Clock	Frequency	Standard / Bank
ICS85411 U9 (Schematic 0381873 Sheet 12)		
PCIE_CLK_1 ICS85411	100 MHz	LVDS - GTY224 Refclk input replicated from PCIe Connector via 1-to-2 clock buffer U9
PCIE_CLK_2 ICS85411	100 MHz	LVDS - GTY225 Refclk input replicated from PCIe Connector via 1-to-2 clock buffer U9

The VCU129 evaluation board variable frequency clock sources are listed in the following table.

Table 7: **VCU129 Board Variable Clock Sources**

Clock	I2C Address	Frequency	Standard / Bank
Si570 U14, U16 Clock Distribution 1 (Schematic 0381873 Sheet 27)			
CLK_300M_DDR4 SI570 (U14)	0x55	300 MHz	LVDS - HP Bank 63 GC input with external termination
CLK_100M_RLD3 SI570 (U16)	0x5F	100 MHz	LVDS - HP Bank 74 GC input with external termination
Si5348 U15 - Clock Distribution 1 (Schematic 0381873 Sheet 27)			
QSFPDD1_SI5348_1_CH0	0x6C	156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS - GTM135 REF CLOCK
QSFPDD1_SI5348_1_CH1		156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS - GTM134 REF CLOCK
QSFPDD1_SI5348_1_CH2		156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS - GTM133 REF CLOCK
QSFPDD1_SI5348_1_CH3		156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS - GTM132 REF CLOCK
QSFPDD1_SI5348_1_CH4		156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS - GTM131 REF CLOCK
QSFPDD1_SI5348_1_CH5		156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS - GTM130 REF CLOCK
QSFPDD1_SI5348_1_CH6		156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS - GTM129 REF CLOCK
SI5348 U19 - Clock Distribution 2 (Schematic 0381873 Sheet 28)			
QSFPDD1_SI5348_2_CH0	0x6D	156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS - GTM128 REF CLOCK
QSFP28_1_SI5348_2_CH1		156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS - GTY127 REF CLOCK
QSFP28_1_SI5348_2_CH2		156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS - GTY126 REF CLOCK
QSFP28_2_SI5348_2_CH3		156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS - GTY125 REF CLOCK
QSFP28_2_SI5348_2_CH4		156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS - GTY124 REF CLOCK
OSFP_SI5348_2_CH5		156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS - GTM235 REF CLOCK
OSFP_SI5348_2_CH6		156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS - GTM234 REF CLOCK
SI5348 U20 - Clock Distribution 3 (Schematic 0381873 Sheet 29)			

Table 7: **VCU129 Board Variable Clock Sources** *(cont'd)*

Clock	I2C Address	Frequency	Standard / Bank
OSFP_SI5348_3_CH0	0X6E	156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS - GTM233 REF CLOCK
OSFP_SI5348_3_CH1		156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS - GTM232 REF CLOCK
QSFPDD2_SI5348_3_CH2		156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS - GTM123 REF CLOCK
QSFPDD2_SI5348_3_CH3		156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS - GTM122 REF CLOCK
QSFPDD2_SI5348_3_CH4		156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS - GTM121 REF CLOCK
QSFPDD2_SI5348_3_CH5		156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS - GTM120 REF CLOCK
SFP28_1_SI5348_3_CH6		156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS – GTY227 REF CLOCK
SI5348 U21 - Clock Distribution 4 (Schematic 0381873 Sheet 30)			
SFP28_2_SI5348_4_CH0	0x6F	156.25 MHz (default), Programmable: 100 Hz to 1028 MHz	LVDS – GTY226 REF CLOCK
SFP56_SI5348_4_CH1		156.25 MHz (default), Programmable: 100 Hz to 1028MHz	LVDS – GTM223 REF CLOCK
SFP56_SI5348_4_CH2		156.25 MHz (default), Programmable: 100Hz to 1028MHz	LVDS – GTM222 REF CLOCK
SFP56_SI5348_4_CH3		156.25 MHz (default), Programmable: 100Hz to 1028MHz	LVDS – GTM221 REF CLOCK
SFP56_SI5348_4_CH4		156.25 MHz (default), Programmable: 100Hz to 1028MHz	LVDS – GTM220 REF CLOCK
CLK_OUT SI5428_4_CH5		HP Bank 70 GC input, Variable	LVDS – ac-coupled, no external termination
SMA_CLK_OUT SI5428_4_CH6		SMA J75 (P), J76 (N)	LVDS – ac-coupled, no external termination
XCVU29P U2 - SMA pair (Schematic 0381873 Sheet 12)			
SMA_REFCLK_INPUT	NA	SMA J7 (P), J6 (N)	GTY226 – ac-coupled, no external termination
XCVU29P U2 - SMA pair (Schematic 0381873 Sheet 5)			
SMA_CLK_OUTPUT	NA	SMA J5 (P), J4 (N)	Bank 66 GC IO (Vcco = VCC1V8) – ac-coupled, no external termination

DDR4 Interface Clock

[Figure 2, callout 10]

The VCU129 evaluation board has a Si570 I2C programmable frequency low-jitter 3.3V LVDS differential oscillator (U14) connected to FPGA U2 HP bank 63 GC pins AW35 (P) and AW36 (N), is AC coupled and has external parallel 100Ω termination.

- Silicon Labs SI570BAB000313DG
- I2C address `0x55`
- Default 300 MHz
- Frequency tolerance: 50 ppm
- 3.3V LVDS differential output

For more information about the Si570 see the data sheet at the Silicon Labs website.

RLD3 Interface Clock

[Figure 2, callout 11]

The VCU129 evaluation board has a Si570 I2C programmable frequency low-jitter 3.3V LVDS differential oscillator (U16) connected to FPGA U2 HP bank 74 GC pins L23 (P) and L22 (N), is AC coupled and has external parallel 100Ω termination.

Silicon Labs SI570BAC002038DG

- I2C address 0x5F
- Default 100 MHz
- Frequency tolerance: 50 ppm
- 3.3V LVDS differential output

QSFP Reference Clocks

[Figure 2, callout 13 –16]

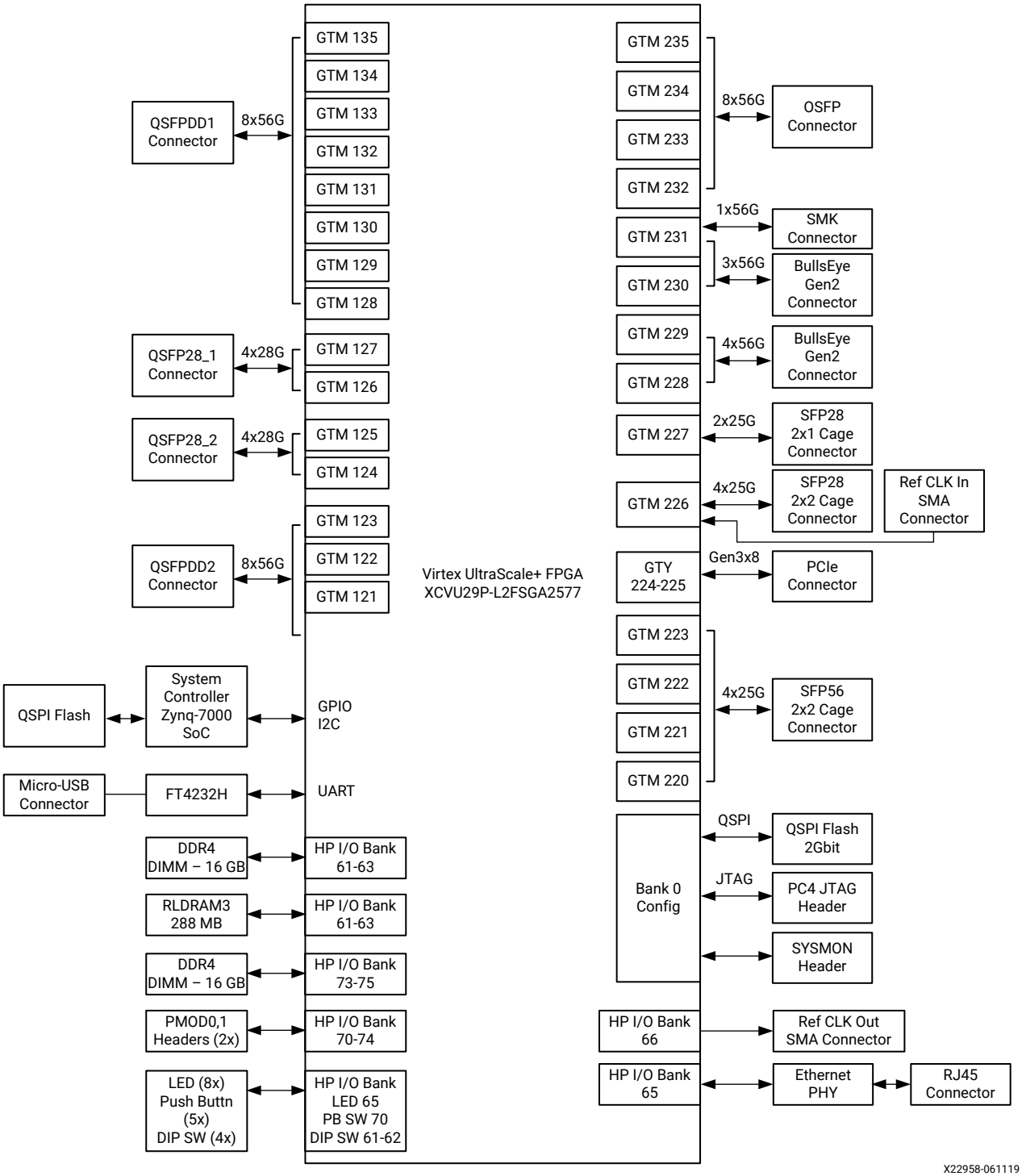
The VCU129 evaluation board implements four I2C programmable Si5348A Network Synchronizer Clock devices to support the various QSFP components.

- Silicon Labs SI5348A-D09879-GM
- I2C address 0x6C (U15), 0x6D (U19), 0x6E (U20), 0x6F (U21)
- Default 156.250 MHz
- Ultra-low jitter of 100 fs

- 1.8V a-c coupled LVDS differential output

The XVCU29P connectivity diagram is shown in the following figure.

Figure 10: **XVCU29P Connectivity Diagram**



QSFPDD1, QSFPDD2, OSFP, QSFP28_1, QSFP28_2, SFP28_1, SFP28_2, and SFP56 interface reference clocks are derived from SI5348 clock synthesizer whose channels can be individually programmed.

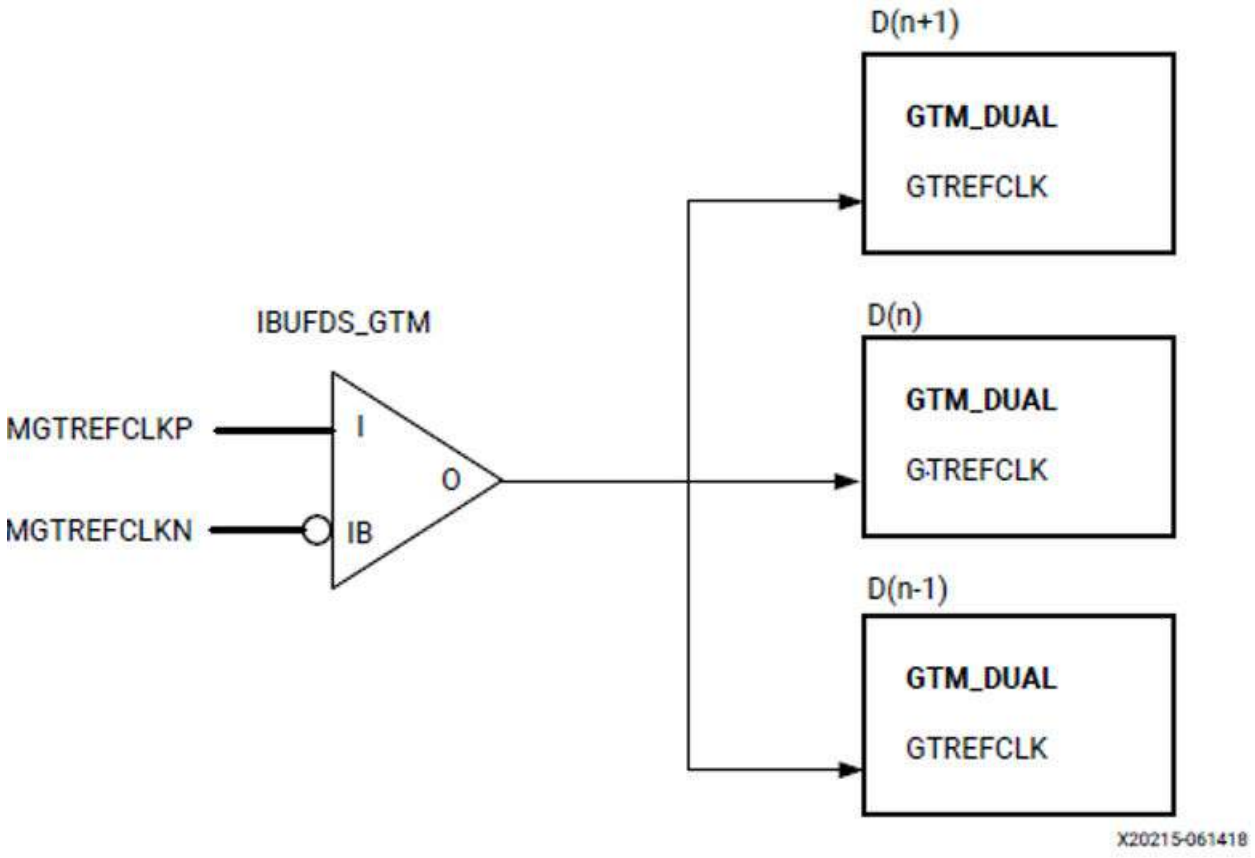
The QSFPDD1 high-speed transceiver mapping is done through SLR crossing.

See the following excerpts from the *Virtex UltraScale+ FPGAs GTM Transceivers User Guide* (UG581) on clock usage (with different SLR GT mapping).

From an architecture perspective, a dual transceiver contains a grouping of two GTM channels inside one GTM_DUAL primitive, one dedicated external reference clock pin pair, and dedicated reference clock routing. The reference clock for a GTM_DUAL primitive must also be instantiated. For dual transceivers operating at line rates lower than 16.3725 Gb/s (NRZ) and 32.7 Gb/s (PAM4), the reference clock for a dual transceiver can also be sourced from the Dual above via GTNORTHREFCLK or from the dual transceivers below via GTSOUTHREFCLK. For devices that support stacked silicon interconnect (SSI) technology, the reference clock sharing via the GTNORTHREFCLK and GTSOUTHREFCLK ports is limited within its own super logic region (SLR). Dual transceivers operating at line rates above 16.3725 Gb/s (NRZ) and 32.7 Gb/s (PAM4) should not source a reference clock from another dual transceivers.

The following figure shows a single external reference clock with multiple dual transceivers connected. The user design connects the IBUFDS_GTM output (O) to the GTREFCLK ports of the GTM_DUAL primitives. In this case, the Xilinx implementation tools make the necessary adjustments to the north/south routing as well as the pin swapping necessary to route the reference clock from one dual transceivers to another when required.

Figure 11: **Single External Reference Clock with Multiple Duals**



***Note*:** The IBUFDS_GTM diagram in the previous figure is a simplification. The output port ODIV2 is left floating, and the input port CEB is set to logic 0.

These rules must be observed when sharing a reference clock to ensure that jitter margins for high-speed designs are met:

- The number of Duals above the sourcing Dual must not exceed one.
- The number of Duals below the sourcing Dual must not exceed one.
- The total number of Duals sourced by an external clock pin pair (MGTREFCLKP/ MGTREFCLKN) must not exceed three Duals.

The maximum number of Duals that can be sourced by a single clock pin pair is three (six transceivers). Designs with more than three Duals require the use of multiple external clock pins to ensure that the rules for controlling jitter are followed. When multiple clock pins are used, an external buffer can be used to drive them from the same oscillator [end excerpt].

SMA Connector Clocks

[Figure 2, callout 18-19]

The VCU129 board implements two pairs of SMA connectors for reference clock input & output.

- SMA pair J7 (P) and J6 (N) are ac-coupled to GTY226
- SMA pair J5 (P) and J4 (N) are ac-coupled to FPGA U2 Bank 66 GC pins

The detailed FPGA connections for the feature described in this section are documented in the VCU129 board XDC file, referenced in Appendix A: Xilinx Design Constraints.

The Si570 and Si5348 device data sheets are available on the Silicon Labs website.

GTY and GTM Transceivers

GTY Transceivers

[Figure 2, callout 2]

The GTY transceivers in the XCVU29P are grouped into four channels or quads. The XCVU29P has four GTY Quads (GTYs 124, 125, 126, 127) on the right side of the device and four GTY Quads (GTYs 224,225, 226, 227) on the left side of the device.

The VCU129 board provides access to eight of the eight GTY Quads:

- Two Quads: GTY124/125 are wired to QSFP28_2, QSFP module connector (J15)
- Two Quads: GTY126/127 are wired to QSFP28_1, QSFP module connector (J14)
- Two Quads: GTY224/225 are wired to the PCIe 8-lane end-point connector (J18)
- Two Quads: GTY226 is wired to SFP28_2, 2x2 SFP module connector (J31)
- Two Quads: GTY227 is wired to SFP28_1, 2x1 SFP module connector (J32)
- **Right Side GTY Quads:** The four connected GTY quads on the right side of the XCVU29P FPGA include:
  - GTY 124
    - MGTREFCLK0 – QSFP28_B124_REFCLK_P/N
    - MGTREFCLK1 – NC
    - GTY0: QSFP2_TX/RX[4]_P/N
    - GTY1: NC
    - GTY2: QSFP2_TX/RX[3]_P/N
    - GTY3: NC
  - GTY 125
    - MGTREFCLK0 – QSFP28_B125_REFCLK_P/N

    - MGTREFCLK1 – NC
    - GTY0: QSFP2_TX/RX[1]_P/N
    - GTY1: NC
    - GTY2: QSFP2_TX/RX[2]_P/N
    - GTY3: NC
  - GTY 126
    - MGTREFCLK0 – QSFP28_B126_REFCLK_P/N
    - MGTREFCLK1 – NC
    - GTY0: QSFP1_TX/RX[4]_P/N
    - GTY1: NC
    - GTY2: QSFP1_TX/RX[3]_P/N
    - GTY3: NC
  - GTY 127
    - MGTREFCLK0 – QSFP28_B127_REFCLK_P/N
    - MGTREFCLK1 – NC
    - GTY0: QSFP1_TX/RX[1]_P/N
    - GTY1: NC
    - GTY2: QSFP1_TX/RX[2]_P/N
    - GTY3: NC
- **Left Side GTY Quads:** The four connected GTY quads on the left side of the XCVU29P FPGA include:
  - GTY 224
    - MGTREFCLK0 – PCIE_CLK1_P/N
    - MGTREFCLK1 – NC
    - GTY[0:3]: PCIE_EP_TX/RX[7:4]_P/N
  - GTY225
    - MGTREFCLK0 – PCIE_CLK2_P/N
    - MGTREFCLK1 – NC
    - GTY[0:3]: PCIE_EP_TX/RX[3:0]_P/N

- GTY 226
  - MGTREFCLK0 – SFP28_B226_REFCLK_P/N
  - MGTREFCLK1 – SMA_REFCLK_INPUT_P/N (J7(P), J6(N))
  - GTY0: SFP28_2_LT_TX/RX_P/N
  - GTY1: SFP28_2_LB_TX/RX_P/N
  - GTY2: SFP28_2_RT_TX/RX_P/N
  - GTY3: SFP28_2_RB_TX/RX_P/N
- GTY 227
  - MGTREFCLK0 – SFP28_B227_REFCLK_P/N
  - MGTREFCLK1 – NC
  - GTY0: SFP28_1_T_TX/RX_P/N
  - GTY1: SFP28_1_B_TX/RX_P/N
  - GTY2: NC
  - GTY3: NC

VCU129 GTY Interface Connections

[Figure 2, callout 20,21,25,45]

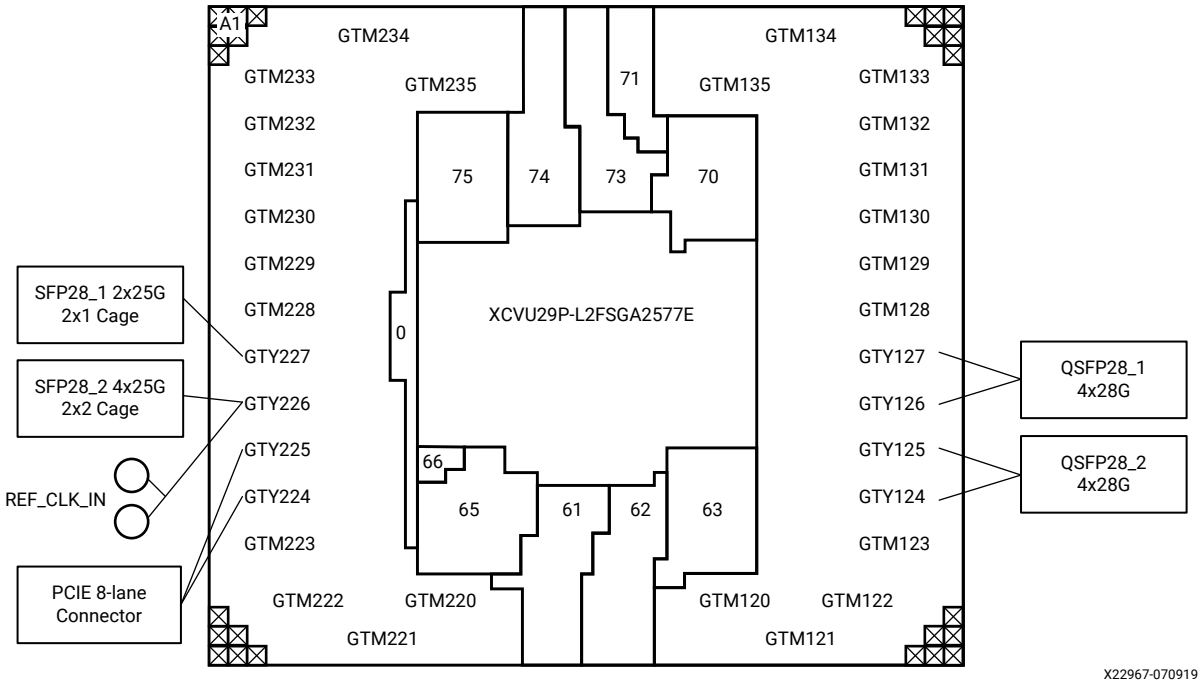
The VCU129 board hosts two QSFP28 small form-factor pluggable SFP connectors QSFP_1 J14 and QSFP_2 J15, which accept 28 Gb/s QSFP+ optical modules. Each QSFP28 connector is housed within a single 28 Gb/s QSFP+ cage assembly. The VCU129 board also supports six SFP28 connections in two multi-connector cage assemblies:

- GTY226 with four connections: SFP28_2 2x2 J31.
- GTY227 with two connections: SFP28_1 2x1 J32.

The GTY224 and GTY225 Quads support the 8-lane PCIe cable connector J18.

The following figure shows a block diagram of the eight GTY Quad connections.

Figure 12: **VCU129 GTY Connections**



The QSFP28 connector 3.3V to 1.8V level-shifted control nets are wired to FPGA U2 bank 65. Each of the SFP28 connectors TX_DISABL and MOD_ABS signals are wired to the TCA6416A dual 8-bit I2C (0x20) expansion port U92 (see the VCU129 board I2C Topology section for more details). The QSFP28 and SFP28 connector I2C interfaces are connected to bus I2C1 (see the VCU129 board I2C Bus Topology section for more details).

PCI Express Endpoint Connectivity

[Figure 2, callout 25]

The 8-lane PCI Express cable connector J18 supports up to Gen3 x8. J18 supports data transfers at the rate of 2.5 GT/s for Gen1 applications, 5.0 GT/s for Gen2 applications and 8.0 GT/s for Gen3 applications. The PCIe transmit and receive signal datapaths have a characteristic impedance of 85Ω ±10%. The PCIE_EP_REFCLK_P/N PCIe reference clock (routed as a 100Ω differential pair) received from J18 is routed to an ICS85411A 1-to-2 clock buffer U9. U9 buffer output Q0 PCIE_CLK1_P/N is routed to GTY224 (PCIE_EP_TX/RX[7:4]_P/N) and output Q1 PCIE_CLK2_P/N is routed to GTY 225 (PCIE_EP_TX/RX[3:0]_P/N).

The VCU129 is a PCIe endpoint that connects to a host system via a PCIe cable. The FPGA then appear as if it is sitting on the Host's PCIe bus and be enumerated as such. The cable assembly is expected to incorporate a null modem for the PCI Express transmit and receive pairs.

For additional information about UltraScale PCIe functionality, see *UltraScale Devices Gen3 Integrated Block for PCI Express LogiCORE IP Product Guide* (PG156). Additional information about the PCI Express standard is available at the PCI Express® standard website.

GTM Transceivers

[Figure 2, callout 3]

The GTM transceivers in the XCVU29P are grouped into two channels or duals. The XCVU29P has twelve GTM duals (GTMs 120-123 and 128-135) on the right side of the device and twelve GTM duals (GTMs 220-223 and 228-235) on the left side of the device.

The VCU129 board provides access to 24 of the 24 GTM duals:

- Two quads: GTM120-123 are wired to QSFPDD2, QSFPDD module connector (J71)
- Two quads: GTM128-135 are wired to QSFPDD1, QSFPDD module connector (J22)
- Two quads: GTM220-223 are wired to SFP56, 2x2 SFP56 module connector (J27)
- Two quads: GTM228-231 are wired to two Bulls Eye connectors (J29 and J30)
- Two quads: GTM232-235 are wired to OSFP module connector (J26)
- **Right Side GTM Duals:** The twelve connected GTM duals on the right side of the XCVU29P FPGA are documented here:
- GTM 120
  - MGTREFCLK – QSFPDD_B120_REFCLK_P/N
  - GTM[0:1]: QSFPDD2_TX/RX[8:7]_P/N
- GTM 121
  - MGTREFCLK – QSFPDD_B121_REFCLK_P/N
  - GTM[0:1]: QSFPDD2_TX/RX[6:5]_P/N
- GTM 122
  - MGTREFCLK – QSFPDD_B122_REFCLK_P/N
  - GTM[0:1]: QSFPDD2_TX/RX[4:3]_P/N
- GTM 128
  - MGTREFCLK – QSFPDD_B128_REFCLK_P/N
  - GTM[0]: NC
  - GTM[1]: QSFPDD1_TX/RX[1]_P/N

- GTM 129
  - MGTREFCLK – QSFPDD_B129_REFCLK_P/N
  - GTM[0]: NC
  - GTM[1]: QSFPDD1_TX/RX[2]_P/N
- GTM 130
  - MGTREFCLK – QSFPDD_B130_REFCLK_P/N
  - GTM[0]: NC
  - GTM[1]: QSFPDD1_TX/RX[3]_P/N
- GTM 131
  - MGTREFCLK – QSFPDD_B131_REFCLK_P/N
  - GTM[0]: NC
  - GTM[1]: QSFPDD1_TX/RX[4]_P/N
- GTM 132
  - MGTREFCLK – QSFPDD_B132_REFCLK_P/N
  - GTM[0]: NC
  - GTM[1]: QSFPDD1_TX/RX[5]_P/N
- GTM 133
  - MGTREFCLK – QSFPDD_B133_REFCLK_P/N
  - GTM[0]: NC
  - GTM[1]: QSFPDD1_TX/RX[6]_P/N
- GTM 134
  - MGTREFCLK – QSFPDD_B134_REFCLK_P/N
  - GTM[0]: NC
  - GTM[1]: QSFPDD1_TX/RX[7]_P/N
- GTM 135
  - MGTREFCLK – QSFPDD_B135_REFCLK_P/N
  - GTM[0]: NC
  - GTM[1]: QSFPDD1_TX/RX[8]_P/N

- **Left Side GTM Duals:** The twelve connected GTM duals on the left side of the XCVU29P FPGA are documented here:
- GTM 220
  - MGTREFCLK – SFP56_B220_REFCLK_P/N
  - GTM[0]: SFP56_LT_TX/RX_P/N
  - GTM[1]: NC
- GTM 221
  - MGTREFCLK – SFP56_B221_REFCLK_P/N
  - GTM[0]: SFP56_RT_TX/RX_P/N
  - GTM[1]: NC
- GTM 222
  - MGTREFCLK – SFP56_B222_REFCLK_P/N
  - GTM[0]: SFP56_LB_TX/RX_P/N
  - GTM[1]: NC
- GTM 223
  - MGTREFCLK – SFP56_B223_REFCLK_P/N
  - GTM[0]: SFP56_RB_TX/RX_P/N
  - GTM[1]: NC
- GTM 228
  - MGTREFCLK – BEYE_228_REFCLK_P/N
  - GTM[0:1]: BEYE_228_TX/RX[0:1]_P/N
- GTM 229
  - MGTREFCLK – BEYE_229_REFCLK_P/N
  - GTM[0:1]: BEYE_229_TX/RX[0:1]_P/N
- GTM 230
  - MGTREFCLK – BEYE_230_REFCLK_P/N
  - GTM[0:1]: BEYE_230_TX/RX[0:1]_P/N
- GTM 231
  - MGTREFCLK – BEYE_231_REFCLK_P/N
  - GTM[0]: BEYE_231_TX/RX[0]_P/N

    - GTM[1]: SMK_231_TX/RX[1]_P/N
- GTM 232
    - MGTREFCLK – B232_REFCLK_P/N
    - GTM[0:1]: QSFP_TX/RX[1:2]_P/N
- GTM 233
    - MGTREFCLK – B233_REFCLK_P/N
    - GTM[0:1]: QSFP_TX/RX[3:4]_P/N
- GTM 234
    - MGTREFCLK – B234_REFCLK_P/N
    - GTM[0:1]: QSFP_TX/RX[5:6]_P/N

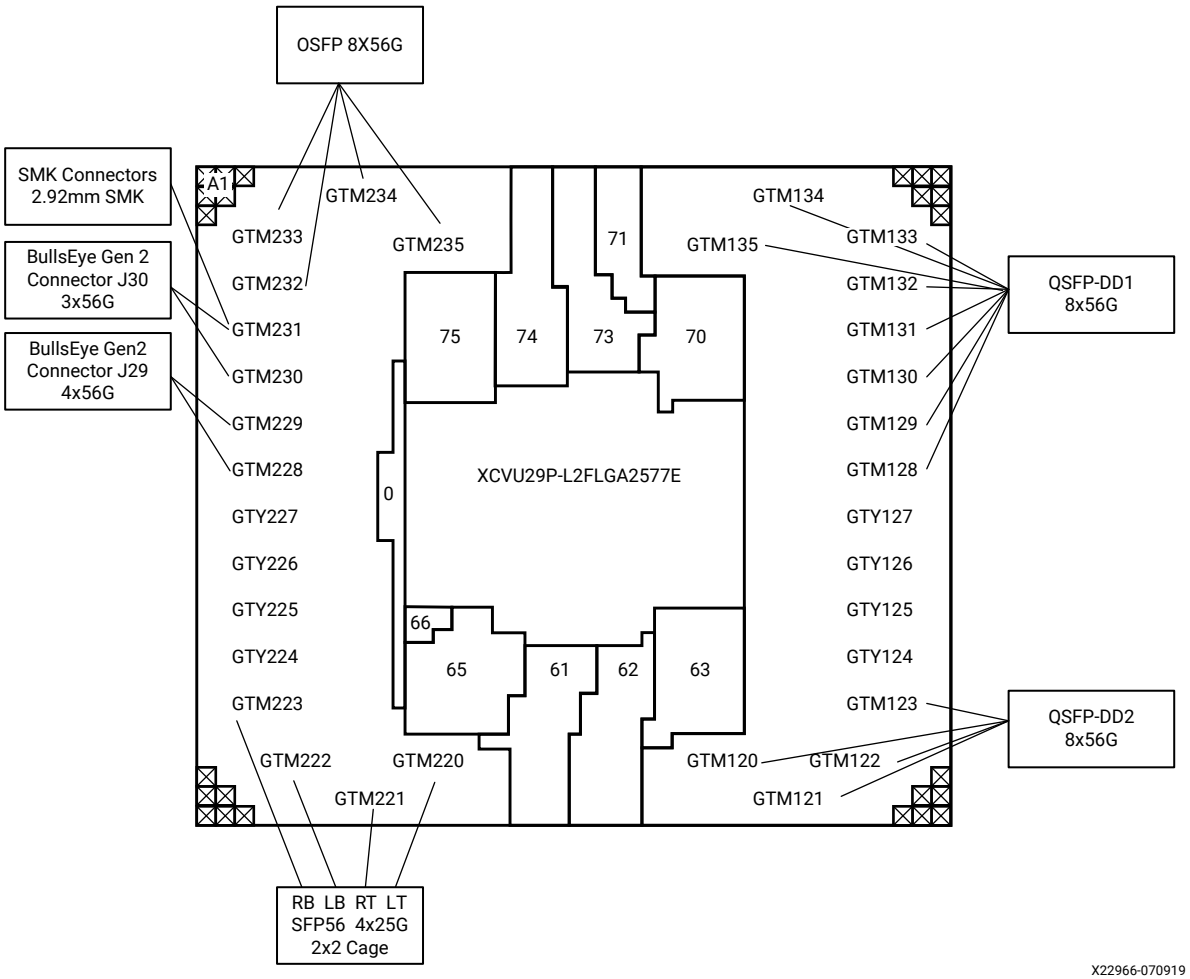
VCU129 GTM Interface Connections

[Figure 2, callout 22,23,24]

The VCU129 board hosts two pluggable small form-factor double density QSFP-DD connectors: QSFPDD1 J22 and QSFPDD2 J71, which accept 28 Gb/s QSFP+ optical modules. Each QSFP-DD connector is housed within a single cage assembly. The VCU129 board also supports a SFP56 2X2 multi-connector cage J27, an Octal Small Format Pluggable (OSFP) connector J26, two Bullseye connectors J29 and J30 and a set of four SubMiniature K-type (SMK) vertical 2.92 mm 50-ohm surface compression-mount connectors.

The following figure shows a block diagram of the 24 GTM dual connections.

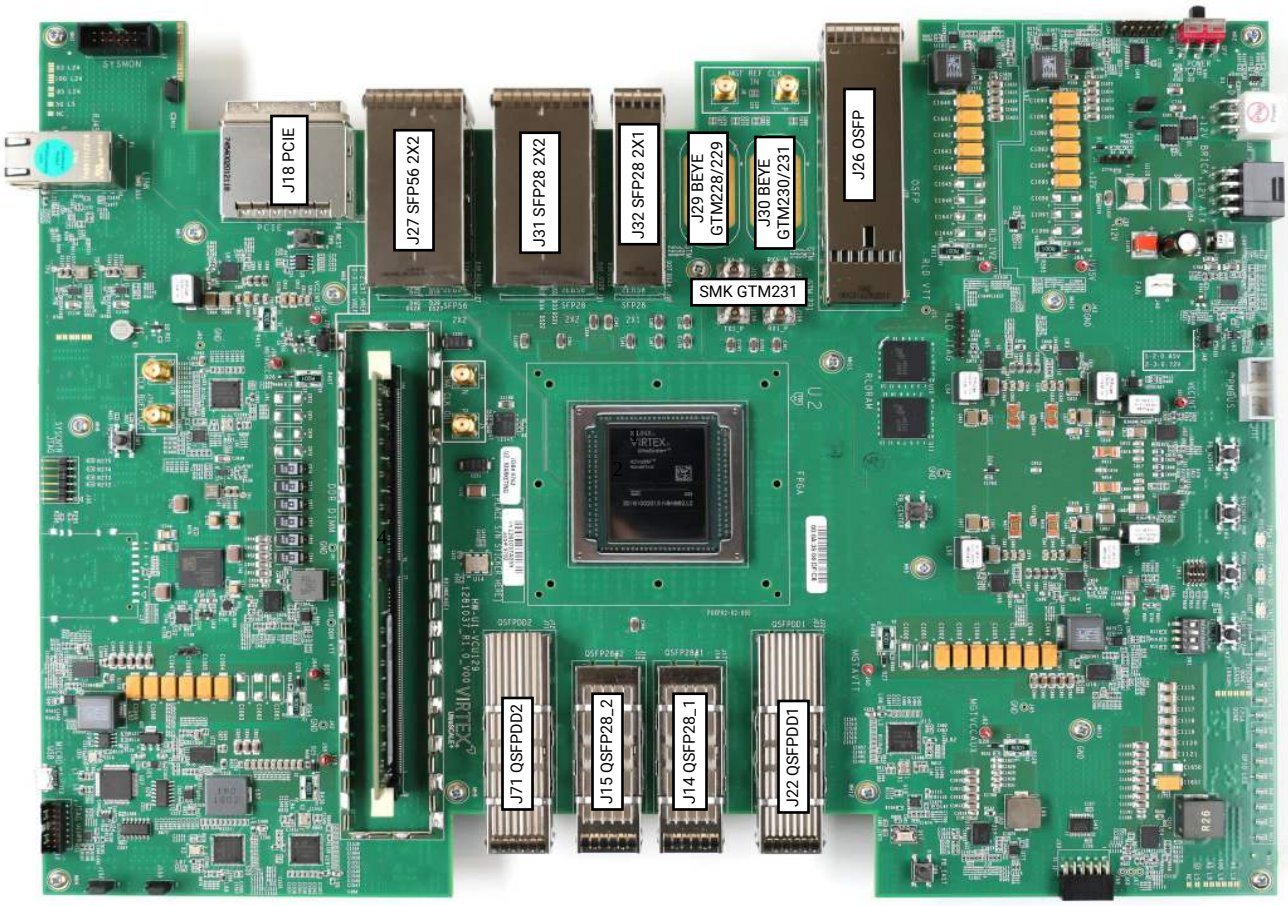
Figure 13: **VCU129 GTM Connections**



The QSFPDD1/2 and OSFP connectors 3.3V to 1.8V level-shifted control nets are wired to FPGA U2 bank 71. Each SFP28 connectors TX_DISABL and MOD_ABS signals are wired to TCA6416A dual 8-bit I2C (0x20) expansion port U92 (see the VCU129 board I2C Bus Topology section for more details). The QSFPDD, OSFP and SFP56 connector I2C interfaces are connected to bus I2C1 (see the VCU129 board I2C Topology section for more details).

The following figure shows the location of the connectors wired to the GTY and GTM transceivers.

Figure 14: **VCU129 GTY/GTM Connector Locations**



For additional information on GTM transceivers, see *Virtex UltraScale+ FPGAs GTM Transceivers User Guide* (UG581). Also see *UltraScale FPGAs Transceivers Wizard LogiCORE IP Product Guide* (PG182). For additional information about the quad small form factor pluggable (QSFP28) modules, see the SFF-8663 and SFF-8679 specifications for 28 Gb/s QSFP+ at the SNIA Technology Affiliates website. For additional information about the pluggable quad small form factor double density (QSFP-DD) module, see the QSFP-DD Multi-Source Agreement (MSA) Group website. The detailed FPGA connections for the feature described in this section are documented in the VCU129 board XDC file, referenced in Appendix A: Xilinx Design Constraints.

10/100/1000 Mb/s Tri-Speed Ethernet PHY

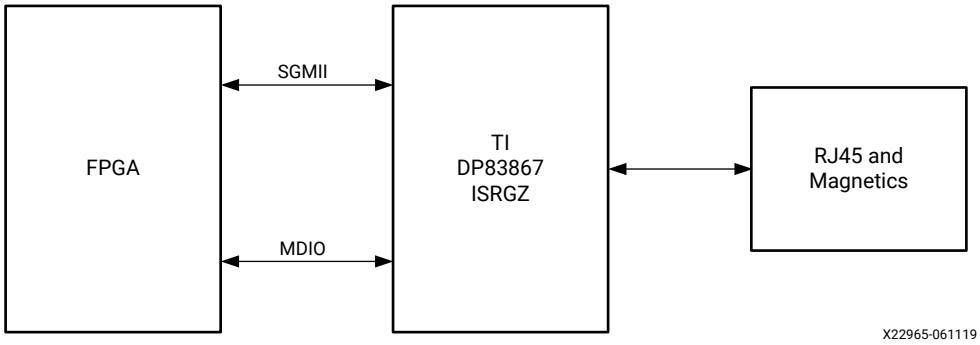
[Figure 2, callout 27]

The VCU129 evaluation board uses the TI PHY device DP83867ISRGZ (U40) for Ethernet communications at 10 Mb/s, 100 Mb/s, or 1000 Mb/s. The board supports SGMII mode only. The PHY connection to a user-provided Ethernet cable is through RJ-45 connector P1, a Wurth 7499111221A with built-in magnetics and status LEDs.

On power-up, or on reset, the PHY is configured to operate in SGMII mode with PHY address[4:0] = 00011.

The following figure shows the Ethernet block diagram.

Figure 15: **VCU129 Ethernet Block Diagram**



Ethernet PHY Status LEDs

[Figure 2, callout 27]

Two Ethernet PHY status LEDs are integrated into the metal frame of the P1 RJ-45 Connector, installed on the top edge and towards the back of the VCU129 board. The two PHY status LEDs are visible within the frame of the RJ45 Ethernet jack as shown in the figure below. As viewed from the front opening, the left green LED is the link activity indicator, the right green LED is the 1000BASE-T link mode indicator.

The following figure shows the Ethernet RJ-45 connector status indicator LEDs.

Figure 16: **VCU129 Ethernet PHY Status LEDs**

A separate discrete LED on top of the board (DS3, near P1 item 38 in Figure 2-1) indicates link established.

The detailed FPGA connections for the feature described in this section are documented in the VCU129 board XDC file, referenced in Appendix A: Xilinx Design Constraints. Details about the tri-mode Ethernet MAC core are provided in *Tri-Mode Ethernet MAC LogiCORE IP Product Guide* (PG051). The TI DP83867ISRGZ data sheet can be found on the TI website.

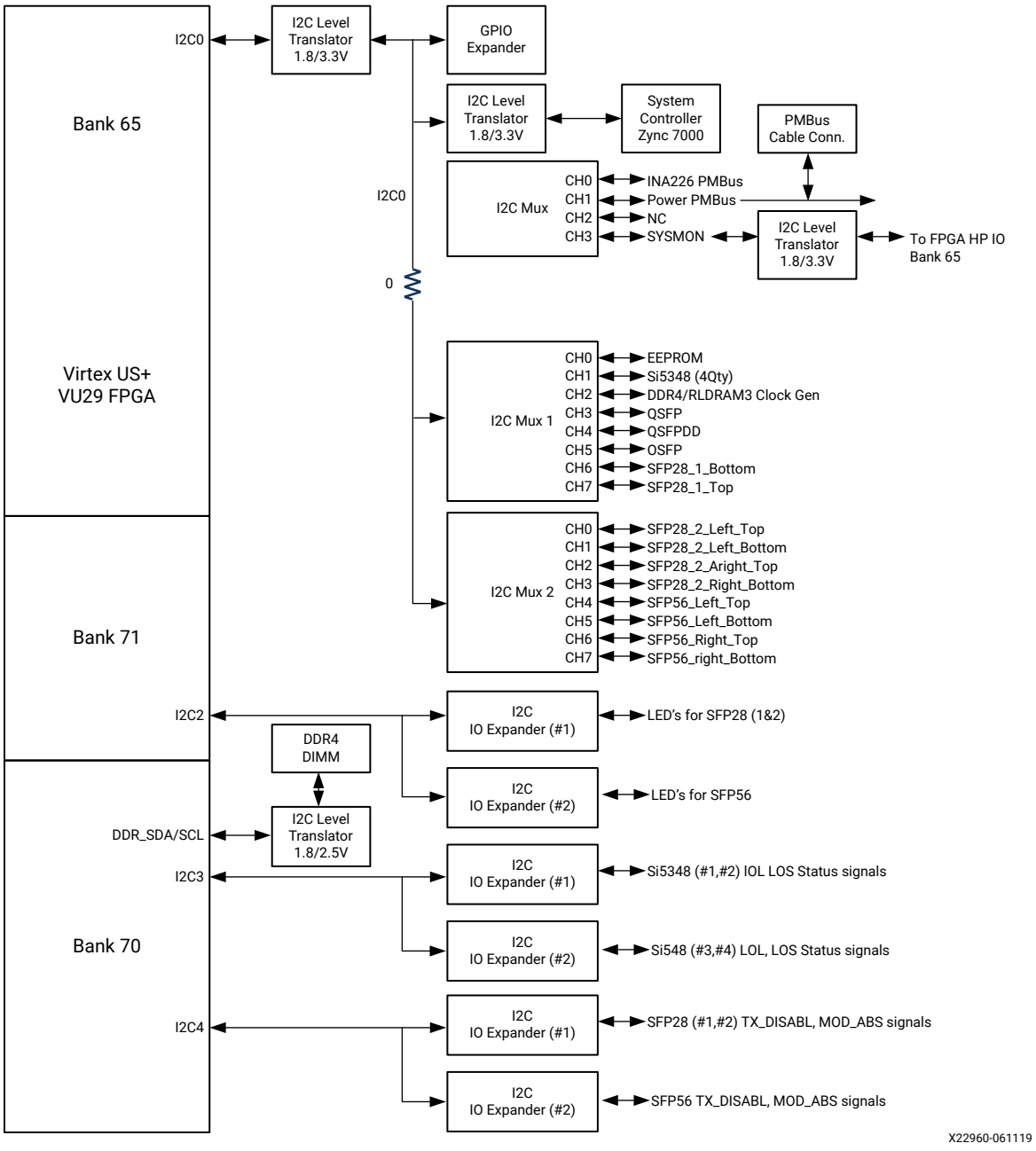
I2C Bus Topology

[Figure 2, callouts 29-32]

The VCU129 evaluation board I2C bus implements five I2C bus branches, DDR4_SDA/SCL, I2C0 and I2C2 - I2C4. System controller U47 bank 501 is also wired to I2C0 via level-shifters.

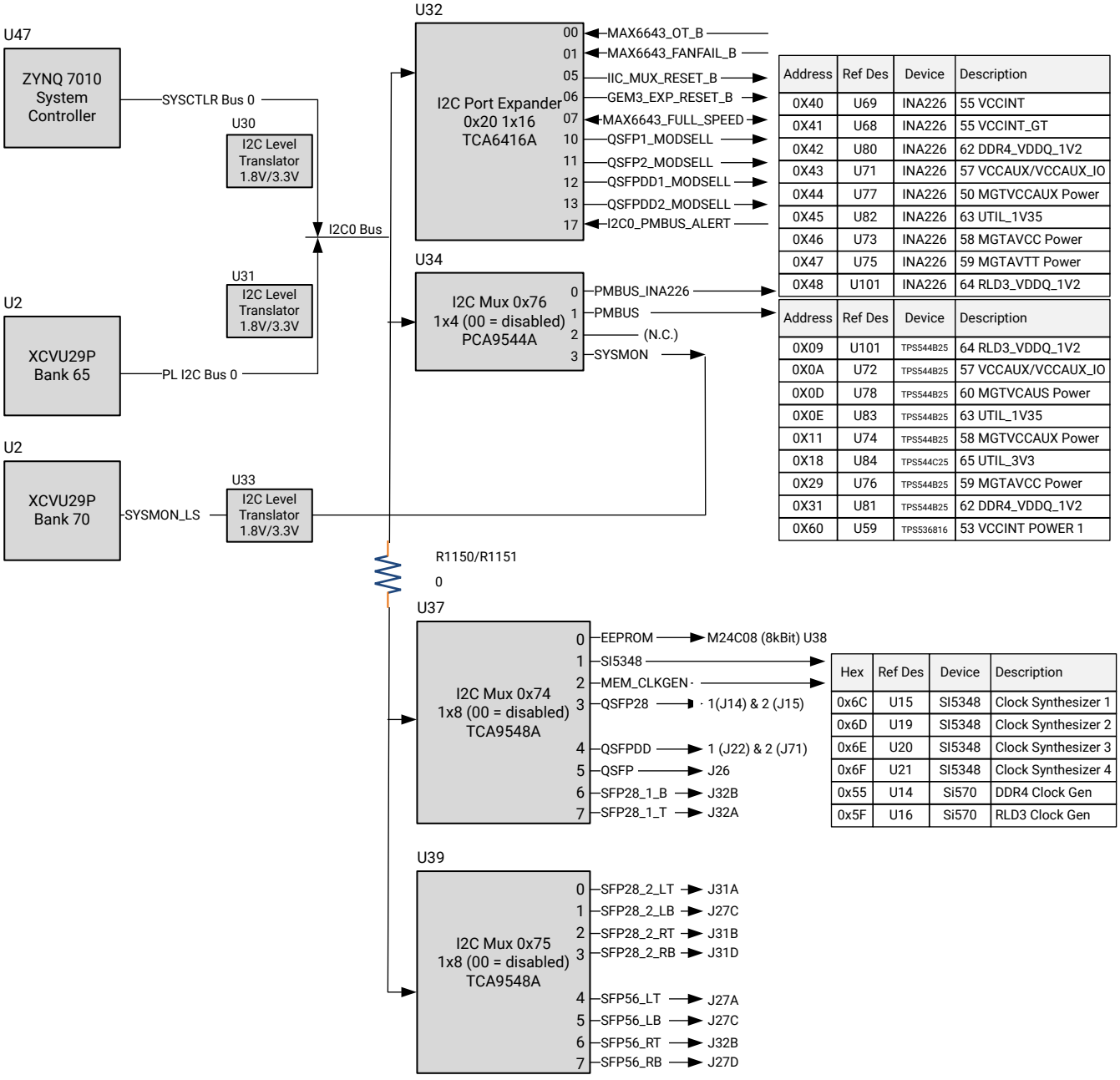
The VCU129 evaluation board I2C bus topology is shown in figure below.

Figure 17: **VCU129 I2C Bus Topology**



The VCU129 evaluation board I2C0 bus topology is shown in the figures below.

Figure 18: **VCU129 I2C0 Bus Topology**



Address	Ref Des	Device	Description
0X40	U69	INA226	55 VCCINT
0X41	U68	INA226	55 VCCINT_GT
0X42	U80	INA226	62 DDR4_VDDQ_1V2
0X43	U71	INA226	57 VCCAUX/VCCAUX_IO
0X44	U77	INA226	50 MGTVCCAUX Power
0X45	U82	INA226	63 UTIL_1V35
0X46	U73	INA226	58 MGTAVCC Power
0X47	U75	INA226	59 MGTAVTT Power
0X48	U101	INA226	64 RLD3_VDDQ_1V2

Address	Ref Des	Device	Description
0X09	U101	TPS544B25	64 RLD3_VDDQ_1V2
0X0A	U72	TPS544B25	57 VCCAUX/VCCAUX_IO
0X0D	U78	TPS544B25	60 MGTVCAUS Power
0X0E	U83	TPS544B25	63 UTIL_1V35
0X11	U74	TPS544B25	58 MGTVCCAUX Power
0X18	U84	TPS544C25	65 UTIL_3V3
0X29	U76	TPS544B25	59 MGTAVCC Power
0X31	U81	TPS544B25	62 DDR4_VDDQ_1V2
0X60	U59	TPS536816	53 VCCINT POWER 1

Hex	Ref Des	Device	Description
0x6C	U15	SI5348	Clock Synthesizer 1
0x6D	U19	SI5348	Clock Synthesizer 2
0x6E	U20	SI5348	Clock Synthesizer 3
0x6F	U21	SI5348	Clock Synthesizer 4
0x55	U14	Si570	DDR4 Clock Gen
0x5F	U16	Si570	RLD3 Clock Gen

X22959-061119

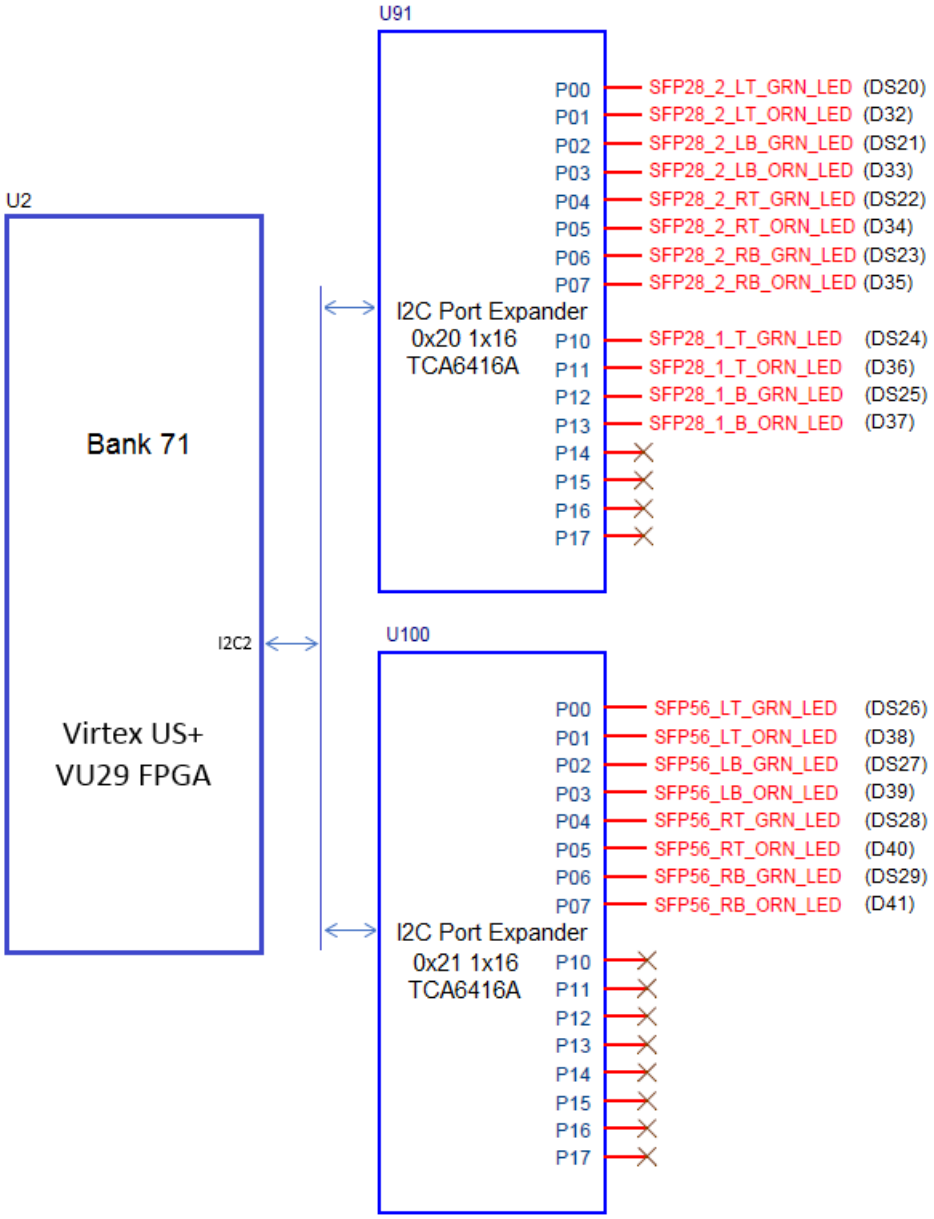
IMPORTANT! *TCA9548 U37 (Addr 0x74) and U39 (Addr 0x75) RESET_B pin 3 control signal IIC_MUX_RESET_B is connected to I2C0 bus TCA6416A U32 port expander (Addr 0x20) port P05 pin 9. The IIC_MUX_RESET_B signal must be driven hi-Z or High to enable I²C bus transactions with the target devices connected downstream of U37 and U39.*

User applications that communicate with any of the I2C bus downstream devices must first set up a path to the desired target device through the appropriate bus switch:

- I2C0 U34 4-port PCA9544A, address 0x76 (0b1110110)
- I2C0 U37 8-port TCA9548A, address 0x74 (0b1110100)
- I2C0 U39 8-port TCA9548A, address 0x75 (0b1110101)

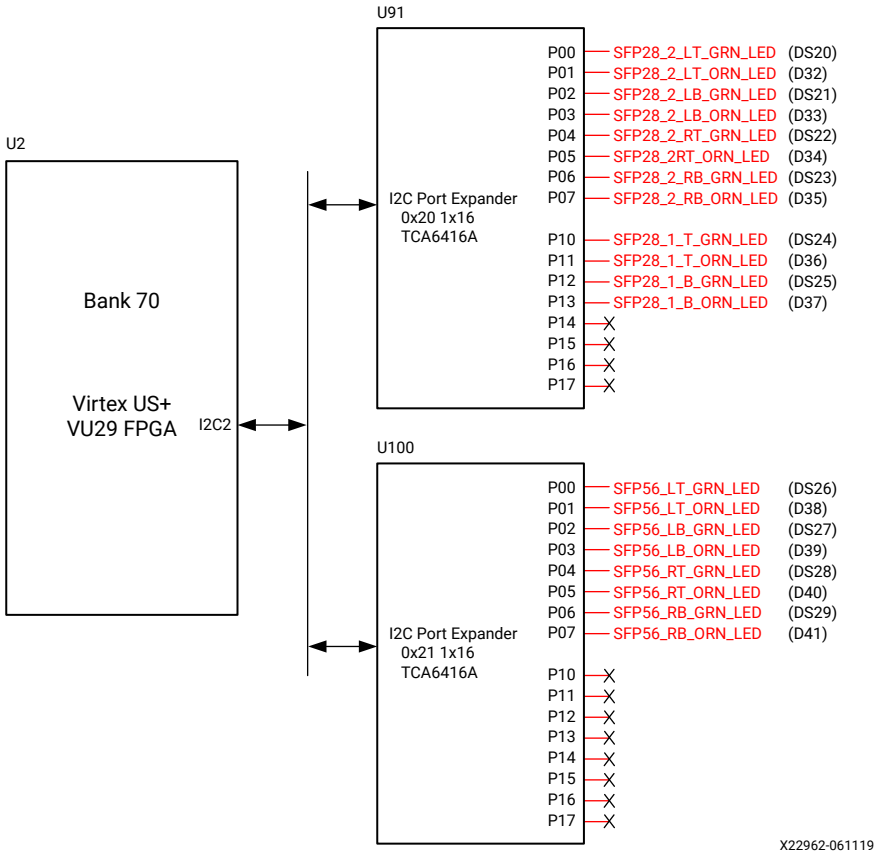
The VCU129 evaluation board I2C2 bus topology is shown in the figure below.

Figure 19: **VCU129 I2C2 Bus Topology**



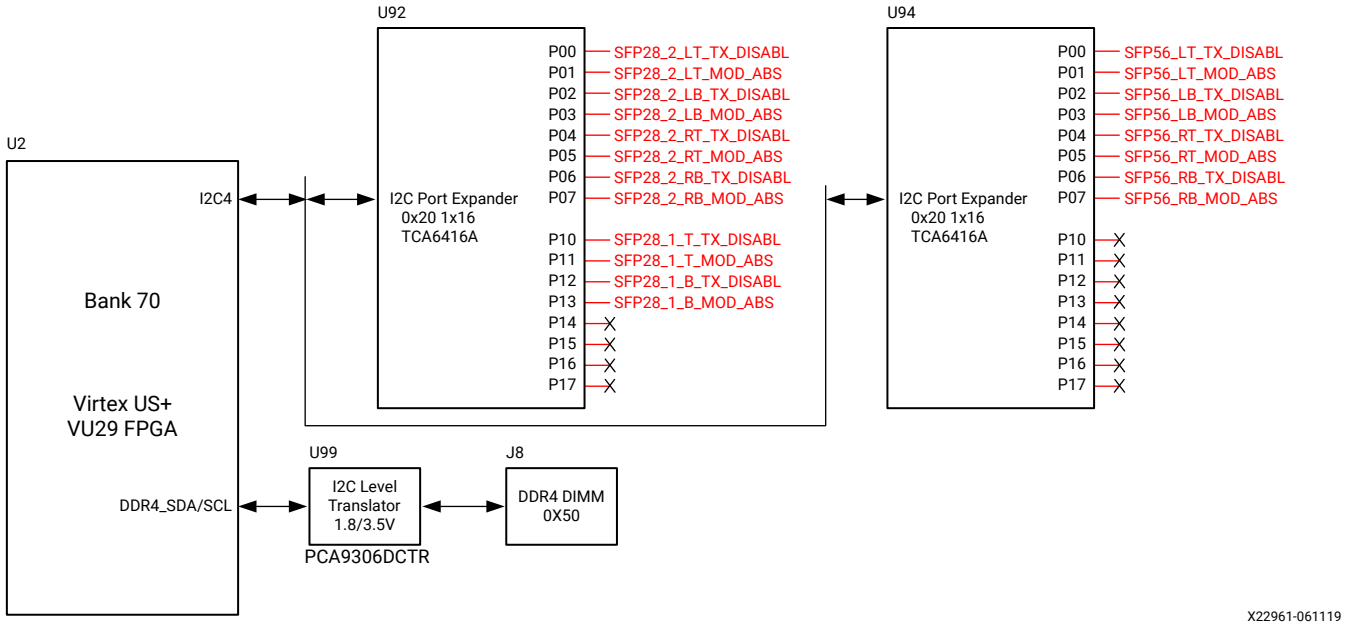
The VCU129 evaluation board I2C3 bus topology is shown in the figure below.

Figure 20: **VCU129 I2C3 Bus Topology**



The VCU129 evaluation board DDR4 I2C and I2C4 bus topologys are shown in the figure below.

Figure 21: **VCU129 DDR4 I2C and I2C4 Bus Topologies**



The table below lists the VCU129 I2C0 bus addresses.

Table 8: **VCU129 I2C0 Bus Addresses**

I2C Devices	I2C Switch Position	I2C Address		Device
		Binary Format	Hex Format	
I2C0 Bus (also connected to I2C1 Bus with 0-ohm resistors)				
TCA6416A 16-bit Port Expander	N/A	0b0100000	0x20	U32 TCA6416A
Function	Port	Direction		
MAX6643_OT_B	P00	IN	N/A	U56 MAX6643
MAX6643_FANFAIL_B	P01	IN	N/A	U56 MAX6643
N/A	P02 - P04 NC	N/A	N/A	N/A
I2C1 bus IIC_MUX_RESET	P05	OUT	N/A	U37,U39 TCA9548A
GEM3_EXP_RESET_B	P06	OUT	N/A	U40 DP83867ISRGZ
MAX6643_FULL_SPEED	P07	OUT	N/A	U56 MAX6643
QSFP1_MODSELL	P10	OUT	N/A	J14 QSFP28 #1
QSFP2_MODSELL	P11	OUT	N/A	J15 QSFP28 #2
QSFPDD1_MODSELL	P12	OUT	N/A	J22 QSFPDD #1
QSFPDD2_MODSELL	P13	OUT	N/A	J71 QSFPDD #2
N/A	P14 - P16 NC	N/A	N/A	N/A
I2C0_PMBUS_ALERT	P17	IN	N/A	J151 PMBUS HDR.
PCA9544A 4-Channel bus switch	N/A	0b1110110	0x76	U34 PCA9544A
PMBus INA226 power monitor (1)	0	0b1000000-0b1001000	0x40-0x48	INA226 U68,U69,U71,U73,U75, U77,U80,U82,U101

Table 8: **VCU129 I2C0 Bus Addresses** *(cont'd)*

I2C Devices	I2C Switch Position	I2C Address		Device
		Binary Format	Hex Format	
PMBus regulators (1)	1	0b0001001, 0b0001010, 0b0001101, 0b0001110, 0b0010001, 0b0011011, 0b0101001, 0b0110001, 0b1100000	0x09, 0x0A, 0x0D, 0x0E, 0x11, 0x1B, 0x29, 0x31, 0x60	Various TI Regulators U59,U72,U74,U76,U78, U81,U83,U84,U102
Not used	2	N/A	N/A	N/A
FPGA SYSMON	3	0b0110010	0x32	U2 BANK 65
I2C1 Bus connected to I2C0 Bus with 0-ohm resistors				
TCA9548 8-Channel bus switch	N/A	0b1110100	0x74	U37 TCA9548A
I2C EEPROM	0	0b1010100	0x54	U38 M24C08
SI5348_1 clock	1	0b1101100	0x6C	U15 SI5348B
SI5348_2 clock	1	0b1101101	0x6D	U19 SI5348B
SI5348_3 clock	1	0b1101110	0x6E	U20 SI5348B
SI5348_4 clock	1	0b1101111	0x55	U21 SI5348B
Si570 DDR4 clock	2	0b1010101	0x5F	U14 Si570
Si570 RLD3 clock	2	0b1011111	0x50	U16 Si570
QSFP1 module connector (1)	3	0b1010000	0x50	J14
QSFP2 module connector (1)	3	0b1010000	0x50	J15
QSFPDD1 module connector (1)	4	0b1010000	0x50	J22
QSFP2 module connector (1)	4	0b1010000	0x50	J71
OSFP module connector	5	0b1010000	0x50	J26
SFP28_1_B module connector (1)	6	0b1010000	0x50	J32B
SFP28_1_T module connector (1)	7	0b1010000	0x50	J32A
TCA9548 8-Channel bus switch	N/A	0b1110101	0x75	U39 TCA9548A
SFP28_2_LT module connector (1)	0	0b1010000	0x50	J31A
SFP28_2_LB module connector (1)	1	0b1010000	0x50	J31C
SFP28_2_RT module connector (1)	2	0b1010000	0x50	J31B
SFP28_2_RB module connector (1)	3	0b1010000	0x50	J31D
SFP56_LT module connector (1)	4	0b1010000	0x50	J27A
SFP56_LB module connector (1)	5	0b1010000	0x50	J27C
SFP56_RT module connector (1)	6	0b1010000	0x50	J27B
SFP56_RB module connector (1)	7	0b1010000	0x50	J27D

Notes:

1. Each connector has a unique MODSELL signal (pin 8), driven Low to enable its I2C interface.

The following table lists the VCU129 I2C2 bus addresses.

Table 9: **VCU129 I2C2 Bus Addresses**

I2C Devices	I2C Switch Position	I2C Address		Device
		Binary Format	Hex Format	
TCA6416A 16-bit Port Expander	N/A	0b0100000	0x20	U91 TCA6416A
Function	Port	Direction		
SFP28_2_LT	P00	IN	N/A	DS20 (GRN)
SFP28_2_LT	P01	IN	N/A	D32 (ORN)
SFP28_2_LB	P02	IN	N/A	DS21 (GRN)
SFP28_2_LB	P03	IN	N/A	D33 (ORN)
SFP28_2_RT	P04	IN	N/A	DS22 (GRN)
SFP28_2_RT	P05	IN	N/A	D34 (ORN)
SFP28_2_RB	P06	IN	N/A	DS23 (GRN)
SFP28_2_RB	P07	IN	N/A	D35 (ORN)
SFP28_1_T	P10	IN	N/A	DS24 (GRN)
SFP28_1_T	P11	IN	N/A	D36 (ORN)
SFP28_1_B	P12	IN	N/A	DS25 (GRN)
SFP28_1_B	P13	IN	N/A	D37 (ORN)
N/A	P14 - P17 NC	N/A	N/A	N/A
TCA6416A 16-bit Port Expander	N/A	0b0100001	0x21	U100 TCA6416A
Function	Port	Direction		
SFP56_LT	P00	IN	N/A	DS26 (GRN)
SFP56_LT	P01	IN	N/A	D38 (ORN)
SFP56_LB	P02	IN	N/A	DS27 (GRN)
SFP56_LB	P03	IN	N/A	D39 (ORN)
SFP56_RT	P04	IN	N/A	DS28 (GRN)
SFP56_RT	P05	IN	N/A	D40 (ORN)
SFP28_2_RB	P06	IN	N/A	DS29 (GRN)
SFP28_2_RB	P07	IN	N/A	D41 (ORN)
N/A	P10 - P17 NC	N/A	N/A	N/A

The following table lists the VCU129 I2C3 bus addresses.

Table 10: **VCU129 I2C3 Bus Addresses**

I2C Devices	I2C Switch Position	I2C Address		Device
		Binary Format	Hex Format	
TCA6416A 16-bit Port Expander	N/A	0b0100000	0x20	U93 TCA6416A
Function	Port	Direction		
SI5348_1_LOL_PLL_C	P00	IN	N/A	U15 Si5348A

Table 10: **VCU129 I2C3 Bus Addresses** *(cont'd)*

I2C Devices	I2C Switch Position	I2C Address		Device
		Binary Format	Hex Format	
SI5348_1_LOL_PLL_D	P01	IN	N/A	U15 Si5348A
SI5348_1_LOL_PLL_A	P02	IN	N/A	U15 Si5348A
SI5348_1_LOS_IN0	P03	IN	N/A	U15 Si5348A
SI5348_1_LOS_IN1	P04	IN	N/A	U15 Si5348A
SI5348_1_LOS_IN2	P05	IN	N/A	U15 Si5348A
SI5348_2_LOL_PLL_C	P06	IN	N/A	U19 Si5348A
SI5348_2_LOL_PLL_D	P07	IN	N/A	U19 Si5348A
SI5348_2_LOL_PLL_A	P10	IN	N/A	U19 Si5348A
SI5348_2_LOS_IN0	P11	IN	N/A	U19 Si5348A
SI5348_2_LOS_IN1	P12	IN	N/A	U19 Si5348A
SI5348_2_LOS_IN2	P13	IN	N/A	U19 Si5348A
SI5348_3_LOL_PLL_C	P14	IN	N/A	U20 Si5348A
SI5348_3_LOL_PLL_D	P15	IN	N/A	U20 Si5348A
SI5348_3_LOL_PLL_A	P16	IN	N/A	U20 Si5348A
SI5348_3_LOS_IN0	P17	IN	N/A	U20 Si5348A
TCA6416A 16-bit Port Expander	N/A	0b0100001	0x20	U104 TCA6416A
Function	Port	Direction		
SI5348_3_LOS_IN1	P00	IN	N/A	U20 Si5348A
SI5348_3_LOS_IN2	P01	IN	N/A	U20 Si5348A
SI5348_4_LOL_PLL_C	P02	IN	N/A	U21 Si5348A
SI5348_4_LOL_PLL_D	P03	IN	N/A	U21 Si5348A
SI5348_4_LOL_PLL_A	P04	IN	N/A	U21 Si5348A
SI5348_4_LOS_IN0	P05	IN	N/A	U21 Si5348A
SI5348_4_LOS_IN1	P06	IN	N/A	U21 Si5348A
SI5348_4_LOS_IN2	P07	IN	N/A	U21 Si5348A
N/A	P10 - P17 NC	N/A	N/A	N/A

The following table lists the VCU129 I2C4 bus addresses.

Table 11: **VCU129 I2C4 Bus Addresses**

I2C Devices	I2C Switch Position	I2C Address		Device
		Binary Format	Hex Format	
TCA6416A 16-bit Port Expander	N/A	0b0100000	0x20	U92 TCA6416A
Function	Port	Direction	N/A	
SFP28_2_LT_TX_DISABL	P00	OUT	N/A	J31A
SFP28_2_LT_MOD_ABS	P01	IN	N/A	J31A

Table 11: **VCU129 I2C4 Bus Addresses** *(cont'd)*

I2C Devices	I2C Switch Position	I2C Address		Device
		Binary Format	Hex Format	
SFP28_2_LB_TX_DISABL	P02	OUT	N/A	J31C
SFP28_2_LB_MOD_ABS	P03	IN	N/A	J31C
SFP28_2_RT_TX_DISABL	P04	OUT	N/A	J31B
SFP28_2_RT_MOD_ABS	P05	IN	N/A	J31B
SFP28_2_RB_TX_DISABL	P06	OUT	N/A	J31D
SFP28_2_RB_MOD_ABS	P07	IN	N/A	J31D
SFP28_1_T_TX_DISABL	P10	OUT	N/A	J32A
SFP28_1_T_MOD_ABS	P11	IN	N/A	J32A
SFP28_1_B_TX_DISABL	P12	OUT	N/A	J32B
SFP28_1_B_MOD_ABS	P13	IN	N/A	J32B
N/A	P14 - P17 NC	N/A	N/A	N/A
TCA6416A 16-bit Port Expander	N/A	0b0100001	0x21	U94 TCA6416A
Function	Port	Direction		
SFP56_LT_TX_DISABL	P00	OUT	N/A	J27A
SFP56_LT_MOD_ABS	P01	IN	N/A	J27A
SFP56_LB_TX_DISABL	P02	OUT	N/A	J27C
SFP56_LB_MOD_ABS	P03	IN	N/A	J27C
SFP56_RT_TX_DISABL	P04	OUT	N/A	J27B
SFP56_RT_MOD_ABS	P05	IN	N/A	J27B
SFP56_RB_TX_DISABL	P06	OUT	N/A	J27D
SFP56_RB_MOD_ABS	P07	IN	N/A	J27D
N/A	P10 - P17 NC	N/A	N/A	N/A

Information about the PCA9544A, TCA9548A and TCA6416A is available on the TI Semiconductor website.

Status and User LEDs

The following table defines VCU129 board status and user LEDs.

Table 12: **VCU129 Board Status and User LEDs**

Ref Des	Color	Description
DS1	RED/GRN	FPGA INIT
DS2	GRN	FPGA DONE
DS3	GRN	ENET_LED1
DS4	GRN	GPIO_LED_7

Table 12: **VCU129 Board Status and User LEDs** *(cont'd)*

Ref Des	Color	Description
DS5	GRN	GPIO_LED_6
DS6	GRN	GPIO_LED_5
DS7	GRN	GPIO_LED_4
DS8	GRN	GPIO_LED_3
DS9	GRN	GPIO_LED_2
DS10	GRN	GPIO_LED_1
DS11	GRN	GPIO_LED_0
DS12	GRN	SYSCTLR_DONE
DS13	GRN	SYSCTLR_STAT_LED
DS14	RED	SYSCTLR_ERR_LED
DS15	RED/GRN	SYSCTLR_INIT_B
DS16	GRN	12V PWR ON
DS17	RED/GRN	OR'D PWR GOOD
DS18	GRN	VCCINT 0.72V
DS19	GRN	VCCINT 0.85V
DS20	GRN	SFP28_2_LT
DS21	GRN	SFP28_2_LB
DS22	GRN	SFP28_2_RT
DS23	GRN	SFP28_2_RB
DS24	GRN	SFP28_1_T
DS25	GRN	SFP28_1_B
DS26	GRN	SFP56_LT
DS27	GRN	SFP56_LB
DS28	GRN	SFP56_RT
DS29	GRN	SFP56_RB
D32	ORN	SFP28_2_LT
D33	ORN	SFP28_2_LB
D34	ORN	SFP28_2_RT
D35	ORN	SFP28_2_RB
D36	ORN	SFP28_1_T
D37	ORN	SFP28_1_B
D38	ORN	SFP56_LT
D39	ORN	SFP56_LB
D40	ORN	SFP56_RT
D41	ORN	SFP56_RB

User GPIO

[Figure 2, callouts 33-34]

The VCU129 board provides these user and general purpose I/O capabilities:

- Eight user LEDs (callout 28)
  - GPIO_LED[7-0]: DS4-DS11
- Five user pushbutton switches (callout 28)
  - GPIO_SW_N, W, E, S, C: SW6, SW9, SW8, SW7, SW10
- CPU_RESET/GPIO pushbutton switch (callout 29)
  - CPU_RESET: SW3

The detailed FPGA connections for the feature described in this section are documented in the VCU129 board XDC file, referenced in Appendix A: Xilinx Design Constraints.

Switches

[Figure 2, callouts 36, 35]

The VCU129 evaluation board includes a power on/off slide switch and a configuration pushbutton switch:

- Power on/off slide switch SW5 (callout 33)
- FPGA Program_B SW2, active-Low (callout 30)

Power On/Off Slide Switch SW5

[Figure 2, callout 36]

The VCU129 board power switch is SW5. Sliding the switch actuator from the off to on position applies 12VDC power from either the 2x3 6-pin Mini-Fit power input connector J39 (power from an external 120VAC-to-12VDC power adapter) or the 2x4 8-pin ATX power supply PCIe-type connector JP1. Power to the VCU129 is intended to be mutually exclusive and only one of the two power connectors J39 or JP1 should be used to provide board power. Green LED DS16 illuminates when the VCU129 board power switch is on. See VCU129 Board Power System for details on the on-board power system.

Program_B Pushbutton Switch SW2

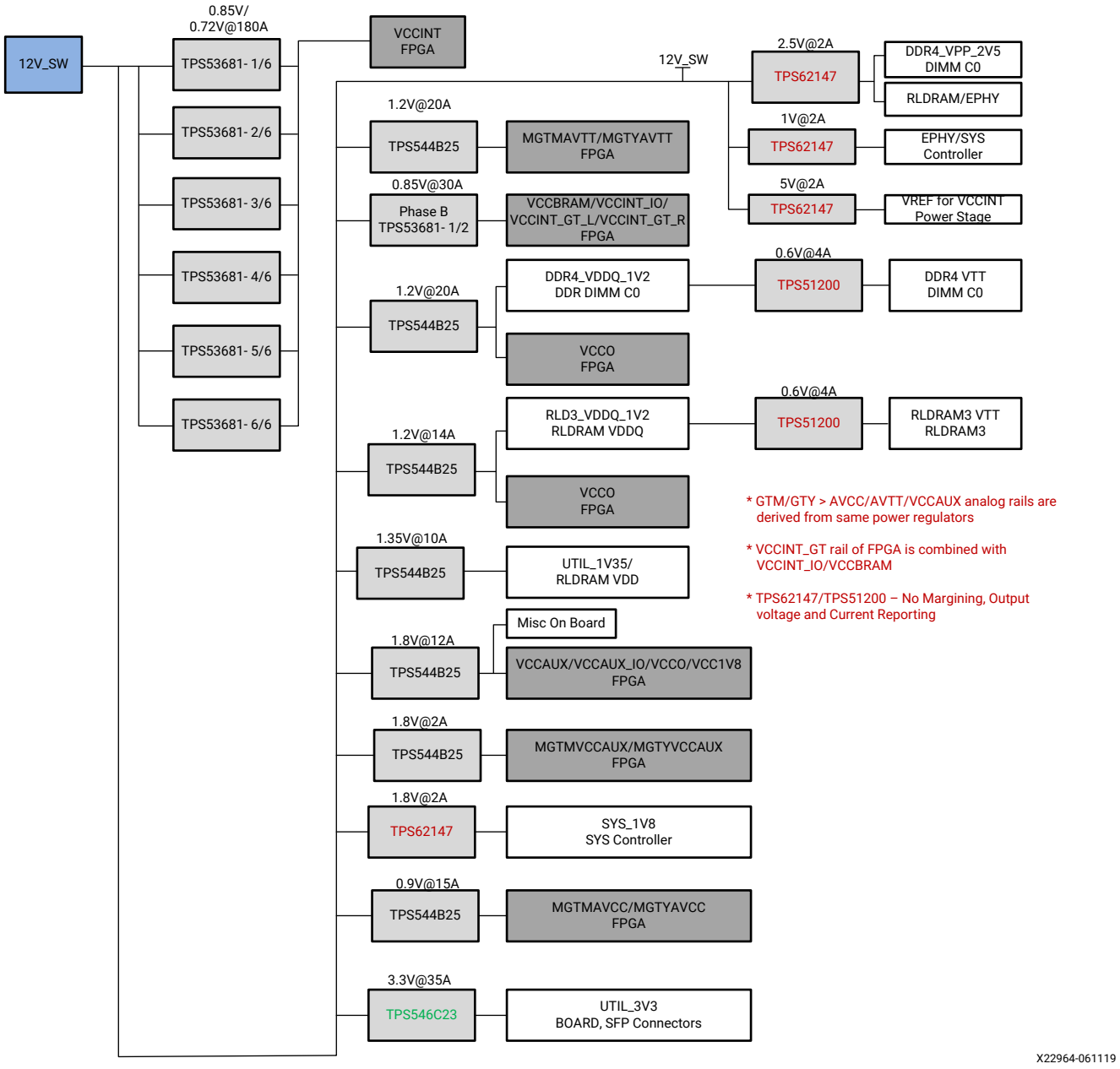
[Figure 2, callout 35]

Switch SW2 grounds the XCVU29P FPGA U2 PROGRAM_B pin when pressed. This action clears the FPGA configuration. The FPGA_PROG_B signal is connected to XCVU29P FPGA U2 pin AK14. See *UltraScale Architecture Configuration User Guide* (UG570) for further configuration details.

VCU129 Board Power System

The VCU129 hosts an Texas Instruments (TI) power system. The following figure shows the VCU129 power system block diagram.

Figure 22: **VCU129 Power System Block Diagram**



The VCU129 evaluation board uses programmable power regulators from TI to supply the core and auxiliary voltages listed in the table below.

Table 13: **VCU129 Power Regulator and INA336 I2C Address Map**

PMBus Regulators and INA226 I2C Address Map								
Schematic Page	**Rail Name**	**Regulator Type**	**U#**	**Vout (V)**	**Iout Range (A)**	**PMBus Address**	**INA226 U#**	**INA_PMBus Address**
PMBus Regulators								
51-53	VCCINT (APWM1-6)	TPS53681RSBT	U59	0.72/0.85	180	0X60	U69	0x40
53	VCCINT_GT (BPWM1) (also VCCBRAM, VCCINT_IO)	TPS53681RSBT	U59	0.85	30	0X60	U68	0x41
55	VCC1V8 (also VCCO, VCCAUX, VCCAUX_IO)	TPS544B25	U72	1.80	12	0x0A	U71	0x43
56	MGTMAVCC	TPS544B25	U74	0.90	15	0x11	U73	0x46
57	MGTMAVTT	TPS544B25	U76	1.20	20	0x29	U75	0x47
58	MGTMVCCAUX	TPS544B25	U78	1.80	2	0x0D	U77	0x44
60	DDR4_VDDQ_1V2 (also VCCO)	TPS544B25	U76	1.20	20	0x31	U80	0x42
61	UTIL_1V35	TPS544B25	U83	1.35	10	0x0E	U82	0x45
62	RLD3_VDDQ_1V2 (also VCCO)	TPS544B25	U102	1.20	14	0x09	U101	0x48
63	UTIL_3V3	TPS546C23	U84	3.30	35	0x1B	NA	NA
Non-PMBus Regulators								
59	SYS_1V8	TPS62147	U79	1.80	2	NA	NA	NA
64	SYS_1V0	TPS62147	U85	1.00	2	NA	NA	NA
64	SYS_5V0	TPS62147	U98	5.00	2	NA	NA	NA
64	DDR4_VPP_2V5	TPS62147	U86	2.50	2	NA	NA	NA
26	DDR4_C0_VTT	TPS51200	U12	0.60	3	NA	NA	NA
26	RLD3_VTERM_0V6	TPS51200	U13	0.60	3	NA	NA	NA

Documentation describing the programming of the TI power controllers is available at the TI website. The PCB layout and power system design meet the recommended criteria described in the *UltraScale Architecture PCB Design User Guide* (UG583).

Monitoring Voltage and Current

Voltage and current monitoring and control for selected power rails is available through either the VCU129 system controller or the Texas Instruments' Fusion Digital Power™ graphical user interface (GUI).

The VCU129 system controller is a simple and convenient way to monitor the voltage and current values for the power rails listed in Onboard Power System Devices table in VCU129 Board Power System. The TI PMBus programmable power controllers listed in Onboard Power System Devices table in VCU129 Board Power System can also be accessed through the 2x5 10-male pin keyed header J151. Using this connector requires the TI USB Interface Adapter PMBus pod (TI part number USB-TO-GPIO). This adapter cable can be ordered from the TI website. TI provides the Fusion Digital Power Designer software package on its Fusion Digital Power website.

Cooling Fan

The XCVU29P FPGA U2 cooling fan 3-pin connector is J46. The VCU129 fan control circuit uses Maxim MAX6643 fan controller U56 to autonomously monitor the FPGA die temperature pins DXP and DXN. The fan circuit is set up to increase fan speed as the FPGA temperature increases.

***Note*:** At initial power on, it is normal for the fan controller to energize at full speed for a few seconds.

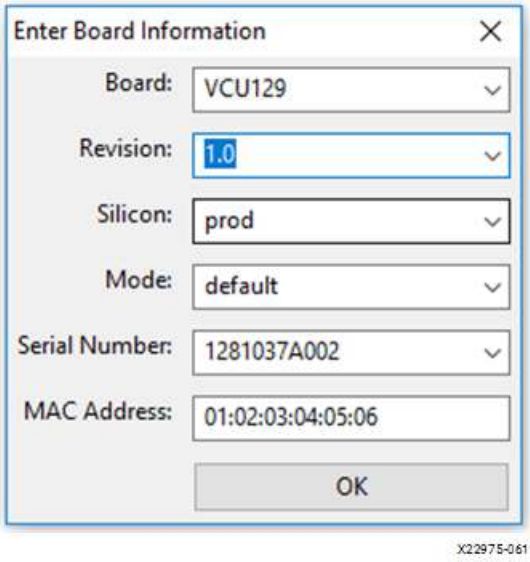
System Controller

[Figure 2, callout 7-9]

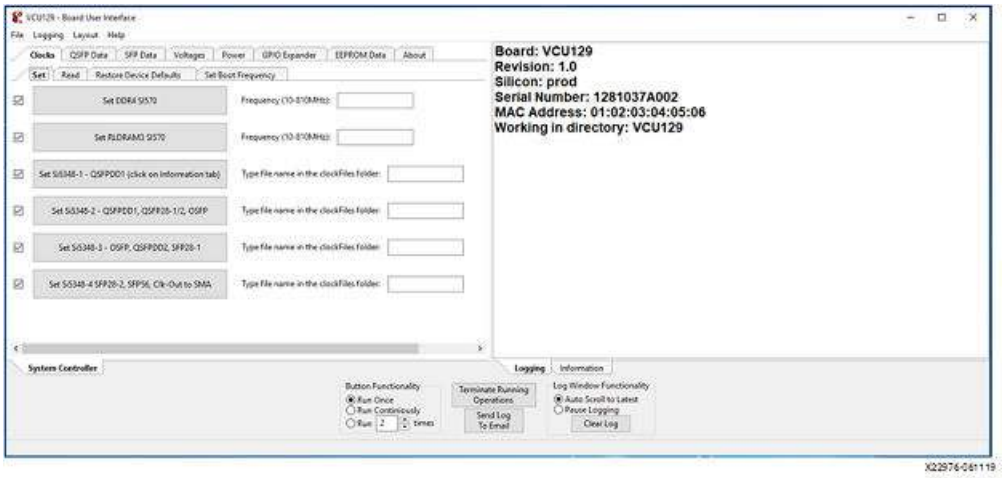
The VCU129 board includes an onboard Zynq-7000 SoC U47 as the system controller. Download the VCU129 - Board User Interface application from the VCU129 website. The Board User Interface can be used to query and control select programmable features such as clocks and power system regulators. The VCU129 evaluation kit website documentation also includes a VCU129 System Controller Tutorial (XTP564) and VCU129 Software Install and Board Setup Tutorial (XTP565).

A summary of the VCU129 Board User Interface installation steps is:

1. Ensure the Silicon Labs VCP USB-UART drivers are installed on the host PC. See *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033).
2. Download the VCU129 Board User Interface host PC application.
3. Connect the micro-B USB cable between the VCU129 board USB-UART connector (J2) and the host PC.
4. Power-cycle the VCU129 board.
5. Launch VCU129 Board User Interface (double-click on application icon).
6. Fill out the Enter Board Information dialog with your board specifics, for instance the figure below:



7. Click the **OK** button, and the initial VCU129 Board User Interface logging screen is presented, for instance the figure below:



See the VCU129 Software Install and Board Setup Tutorial (XTP565) and VCU129 System Controller Tutorial (XTP564) (which includes instructions for changing Si5348 clocks) for more information on installing and using the System Controller utility.

Configuration Options

[Figure 2, callout 40]

The VCU129 board supports two of the UltraScale+™ FPGA configuration modes:

- Master SPI using the onboard 2 Gbit Quad SPI flash memory
- JTAG using:
  - USB JTAG configuration port J13 (FTDI FT4232H bridge U27)

- Xilinx® Platform Cable 2 mm, keyed flat cable header (J12)

Each configuration interface corresponds to one or more configuration modes and bus widths as listed in the table below. The mode switches M2, M1, and M0 are on 4-pole DIP SW1 positions 2, 3, and 4, respectively. The FPGA default mode setting M[2:0] = 001, selecting the master SPI configuration mode.

Configuration Mode	SW16 DIP Switch Settings (M[2:0])	Bus Width	CCLK Direction
Master SPI	001	x1, x2, x4	Output
JTAG	101	x1	Not applicable

The mode pins settings on DIP SW1 determine if the Quad SPI flash is used for configuring the FPGA. DIP switch SW1 also includes a system controller enable switch in position 1. See *UltraScale Architecture Configuration User Guide* (UG570) for further details on configuration modes.

XILINX

Appendix A

Xilinx Design Constraints

Overview

The Xilinx® design constraints (XDC) file template for the VCU129 board provides for designs targeting the VCU129 evaluation board. Net names in the constraints list correlate with net names on the latest VCU129 evaluation board schematic. Users must identify the appropriate pins and replace the net names with net names in the user RTL. See the *Vivado Design Suite User Guide: Using Constraints* (UG903) for more information.

IMPORTANT! *See the VCU129 board website documentation tab (Board Files check box) for the XDC file.*

Appendix B

Regulatory and Compliance Information

This product is designed and tested to conform to the European Union directives and standards described in this section.

For Technical Support, open a Support Service Request.

CE Information

CE Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

CE Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

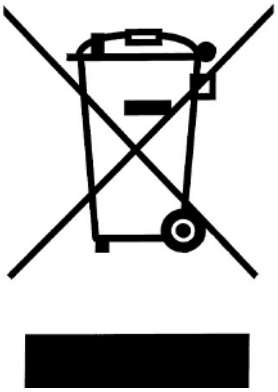
This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

CE Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Compliance Markings



In August of 2005, the European Union (EU) implemented the EU Waste Electrical and Electronic Equipment (WEEE) Directive 2002/96/EC and later the WEEE Recast Directive 2012/19/EU. These directives require Producers of electronic and electrical equipment (EEE) to manage and finance the collection, reuse, recycling and to appropriately treat WEEE that the Producer places on the EU market after August 13, 2005. The goal of this directive is to minimize the volume of electrical and electronic waste disposal and to encourage re-use and recycling at the end of life.

Xilinx has met its national obligations to the EU WEEE Directive by registering in those countries to which Xilinx is an importer. Xilinx has also elected to join WEEE Compliance Schemes in some countries to help manage customer returns at end-of-life.

If you have purchased Xilinx-branded electrical or electronic products in the EU and are intending to discard these products at the end of their useful life, please do not dispose of them with your other household or municipal waste. Xilinx has labeled its branded electronic products with the WEEE Symbol to alert our customers that products bearing this label should not be disposed of in a landfill or with municipal or household waste in the EU.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

Appendix C

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

The most up to date information related to the VCU129 board and its documentation is available on the following websites.

- https://www.xilinx.com/products/boards-and-kits/vcu129-pp.html
- VCU129 Evaluation Kit – Master Answer Record (AR 72069)

These documents provide supplemental material useful with this guide:

1. *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* (DS923)
2. *UltraScale Architecture Configuration User Guide* (UG570)
3. *UltraScale Architecture SelectIO Resources User Guide* (UG571)
4. *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150)
5. *UltraScale Architecture Clocking Resources User Guide* (UG572)
6. *UltraScale Architecture GTY Transceivers User Guide* (UG578)
7. *Virtex UltraScale+ FPGAs GTM Transceivers User Guide* (UG581)
8. *UltraScale FPGAs Transceivers Wizard LogiCORE IP Product Guide* (PG182)
9. *UltraScale Devices Gen3 Integrated Block for PCI Express LogiCORE IP Product Guide* (PG156)
10. *Tri-Mode Ethernet MAC LogiCORE IP Product Guide* (PG051)
11. *AXI UART Lite LogiCORE IP Product Guide* (PG142)
12. *Vivado Design Suite User Guide: Using Constraints* (UG903)
13. *UltraScale Architecture PCB Design User Guide* (UG583)
14. *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033)
15. VCU129 System Controller Tutorial (XTP564)
16. VCU129 Software Install and Board Setup Tutorial (XTP565)
17. VCU129 Restoring Flash Tutorial (XTP563)

    For additional documents associated with Xilinx devices, design tools, intellectual property, boards, and kits see the Xilinx documentation website.

    The following websites provide supplemental material useful with this guide:

18. Xilinx, Inc: www.xilinx.com (XCVU29P-L2FSGA2577E)
19. Micron Technology: www.micron.com

    (MTA18ASF2G72PZ-2G3B1, MT44K32M36RB-083F, MT25QU02GCBB8E12-0SIT)

20. Silicon Labs: www.silabs.com (Si570, Si5348)

21. Future Technology Devices International Ltd.: http://www.ftdichip.com (FT232HL)
22. SNIA Technology Affiliates: https://www.snia.org (SFF-8663, SFF-8679)
23. QSFP-DD Multi-Source Agreement (MSA) Group: http://www.qsfp-dd.com (QSFP-DD)
24. PCI Express® standard: www.pcisig.com/specifications
25. Texas Instruments: www.ti.com (TCA9548A, PCA9544A, TCA6416A, DP83867ISRGZ)

Please Read: Important Legal Notices

OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.

Copyright