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SDP-B Controller Board

INTRODUCTION

This user guide describes the EVAL-SDP-CB1Z system demonstration platform—Blackfin® (SDP-B) controller board from Analog Devices, Inc. The SDP-B controller board is part of the Analog Devices system demonstration platform (SDP). The SDP consists of a series of controller boards, interposer boards, and daughter boards.

SDP controller boards provide a means of communicating with the PC from the system under evaluation. Interposer boards route signals between two connectors. Daughter boards are a collection of product evaluation boards and Circuits from the Lab™ reference circuit boards. The SDP-B is used as part of the evaluation system for many Analog Devices components and reference circuits. The primary audience for this user guide is a system engineer who seeks to understand how to set up the SDP-B board and begin USB communications to the PC.

The SDP-B board is designed to be used in conjunction with various Analog Devices component evaluation boards and Circuits from the Lab reference circuits as part of a customer evaluation environment. The SDP-B provides USB connectivity through a USB 2.0 high speed connection to the computer allowing users to evaluate components on this platform from a PC application. The SDP-B is based on ADSP-BF527 Blackfin processor, with the Blackfin processor peripheral communication lines available to the component daughter board through two identical 120-pin small footprint connectors.

The SDP-B user guide provides instructions for installing the SDP-B hardware (EVAL-SDP-CB1Z board) and software onto your computer. The necessary installation files are provided with the evaluation daughter board package. The Getting Started section provides software and hardware installation procedures, PC system requirements, and basic board information. The Hardware Description section provides information on the EVAL-SDP-CB1Z components. The EVAL-SDP-CB1Z schematics are provided in the Schematics section.

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10/11—Rev. 0 to Rev. A

Change to Product Overview Section 3
Replaced Hardware Description Section 15
Replaced Schematics Section 13

6/11—Revision 0: Initial Version

PRODUCT OVERVIEW

The SDP-B board features

- Analog Devices ADSP-BF527 Blackfin processor
- Core performance up to 600 MHz
- 208-ball CSP-BGA package
- 24 MHz CLKIN oscillator
- 5 Mb of internal RAM memory
- 32 Mb flash memory
  - Numonyx M29W320EB or
  - Numonyx M25P32
- SDRAM memory
  - Micron MT48LC16M16A2P-6A - 16 Mb x 16 bits (256 Mb/32 MB)
- 3 × 120-pin small foot print connectors
  - Hirose FX8-120P-SV1(91), 120-pin header
- Blackfin processor peripherals exposed
  - SPI
  - SPORT
  - TWI/I^2C
  - GPIO
  - PPI
  - Asynchronous parallel
  - Timers

For more information, go to http://www.analog.com/sdp.

TECHNICAL OR CUSTOMER SUPPORT

You can reach Analog Devices customer support in the following ways:

- Visit the SDP website at http://www.analog.com/sdp
- Email processor questions to
  - processor.support@analog.com (worldwide support)
  - processor.europe@analog.com (Europe support)
  - processor.china@analog.com (China support)
- Phone questions to 1-800-ANALOGD
- Contact your Analog Devices local sales office or authorized distributor.
- Send questions by mail to
  Analog Devices, Inc.
  Three Technology Way
  P.O. Box 9106
  Norwood, MA 02062-9106
  USA

PRODUCT INFORMATION

Product information can be obtained from the Analog Devices website.

Analog Devices Web Site

The Analog Devices website, www.analog.com, provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

Note that MyAnalog.com is a free feature of the Analog Devices website that allows customization of a web page to display only the latest information about products of interest to you. You can choose to receive weekly email notifications containing updates to the web pages that meet your interests, including documentation errata against all documents. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

Visit MyAnalog.com to sign up. If you are a registered user, just log on. Your user name is your email address.

REGULATORY COMPLIANCE

The EVAL-SDP-CB1Z is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer end product or as a portion of a consumer end product. The board is an open system design, which does not include a shielded enclosure and therefore may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices. Store unused boards in the protective shipping package.

The EVAL-SDP-CB1Z board has been certified to comply with the essential requirements of the European EMC directive 89/36/EC amended by 93/68/EEC and therefore carries the CE mark.

GETTING STARTED

This section provides specific information to assist you with using the SDP-B board as part of your evaluation system.

The following topics are covered:

- Package contents
- PC configuration
- USB installation
- Powering up/powering down the SDP

PACKAGE CONTENTS

Your EVAL-SDP-CB1Z board package contains the following:

- EVAL-SDP-CB1Z board
- 1 m USB Standard-A to Mini-B cable

Contact the vendor where you purchased your SDP-B board or contact Analog Devices if anything is missing.

PC CONFIGURATION

For correct operation of the SDP board, your computer must have the following minimum configuration:

- Windows XP Service Pack 2 or Windows Vista®
- USB 2.0 port

When removing the SDP-B board from the package, handle the board carefully to avoid the discharge of static electricity, which can damage some components.

USB INSTALLATION

Perform the following tasks to safely install the SDP-B board onto the computer. There are two stages in the software application installation procedure. The first stage installs the application software. The second stage installs the .NET Framework 3.5 and the necessary drivers.

Installing the Software

1. Run the application install provided. The first stage installs the applications GUI and the necessary support files onto the computer
2. Immediately following the application install, the .NET Framework 3.5 and the driver package for the SDP board is installed. If the .NET Framework 3.5 is already preinstalled on the computer in question, this stage is skipped and Step 2 will consist of a driver package installation only

Connecting the SDP-B Board to the PC

Attach the SDP-B board to a USB 2.0 port on the computer via the Standard-A to Mini-B cable provided.

Verifying Driver Installation

Before using the SDP-B board, verify the driver software has installed properly.

Open the Windows Device Manager and verify the SDP board appears under **ADI Development Tools** as shown in Figure 1.

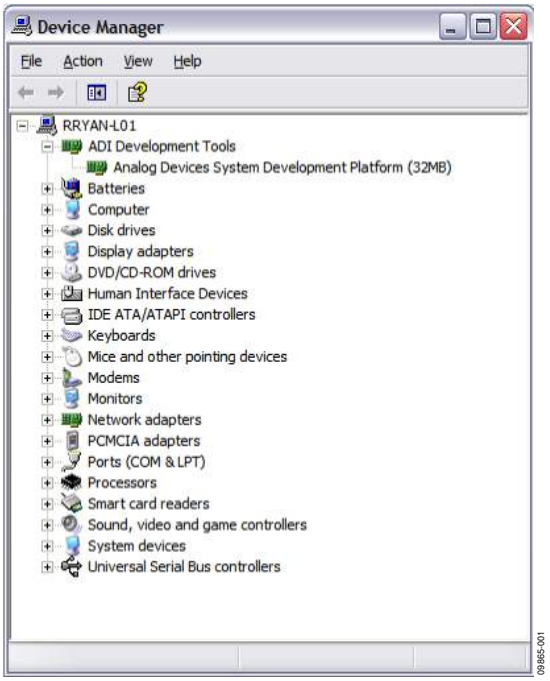

Figure 1. Device Manager

POWERING UP/POWERING DOWN THE SDP

The following sections describe how to safely power up and power down the SDP-B.

Powering Up the SDP-B Board

1. Connect the SDP-B board to the daughter evaluation board through the 120-pin mating connectors.
2. Power the daughter board.
3. Connect the USB port on the computer to the SDP-B board.

Powering Down the SDP-B Board

1. Power down the daughter evaluation board.
2. Disconnect the USB port on the computer from the SDP-B board.
3. Disconnect the SDP-B board from the daughter evaluation board.

HARDWARE DESCRIPTION

This section describes the hardware design of the EVAL-SDP-CB1Z board.

The following topics are covered:

- LEDs—This section describes the SDP on-board LEDs.
- Connector Details—This section details the pin assignments on the 120-pin connectors.
- Power—This section lists power requirements of the SDP and identifies connector power inputs and output pins.
- Daughter board design guidelines—This section provides guidelines on how to design daughter boards for use with the SDP.
- Mechanical specifications—This section provides dimensional information.

LEDS

There are two LEDs located on the SDP-B board (see Figure 2).

POWER LED

The green power LED indicates that the SDP-B board is powered. This is not an indication of USB connectivity between the SDP-B and the PC.

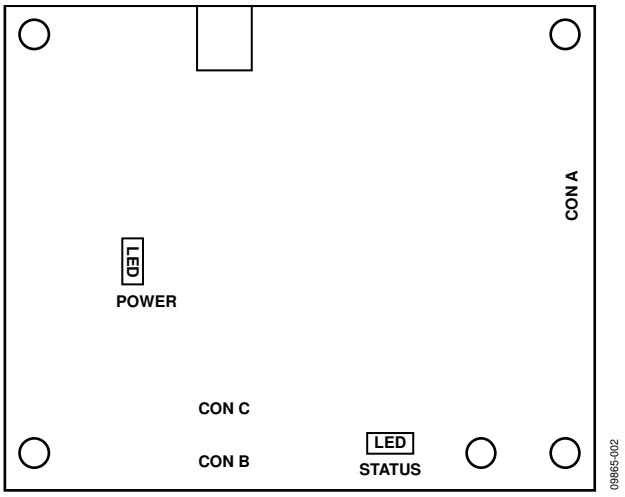

Figure 2. SDP-B Board LEDs

STATUS LED

The orange status LED is an LED used as a diagnostic tool for evaluation application developers. When there are two or more identical SDP controller board and daughter board combinations connected to the PC simultaneously, the status LED flashes during the connect routine to help the user identify which board they will communicate with.

CONNECTOR DETAILS

The SDP-B board contains three Hirose FX8-120P-SV1(91), 120-pin header connectors. Connector A and Connector B share identical pinouts and through these connectors, the peripheral communication interfaces of ADSP-BF527 Blackfin processor are exposed. The exposed peripherals are

- SPI
- SPORT
- I^2C/TWI
- GPIO
- Asynchronous parallel
- PPI
- UART
- Timers

In addition, included on the connector specification are input and output power pins, ground pins, and pins reserved for future use. For further details on the peripheral interfaces, including timing diagrams, see the *ADSP-BF52x Blackfin Processor Hardware Reference*.

Connector C exposes the entire Blackfin memory space, but is not used as part of the SDP platform.

Connector Pin Assignments

The connector pin assignments for Connector A and Connector B have been defined independently of the any internal pin sharing that occurs on the Blackfin processor. Table 1 lists the connector pins and identifies the functionality assigned to each connector pin for Connector A and Connector B on the SDP-B board.

Table 1. 120-Pin Connector Pin Assignments

Pin No.	Pin Name	Description
1	VIN	Power to SDP Board. Requires 200 mA at 5 V.
2	NC	No Connect. Leave this pin unconnected. Do not ground.
3	GND	Connect to ground plane of board.
4	GND	Connect to ground plane of board.
5	USB_VBUS	Connected directly to the USB +5 V supply.
6	GND	Connect to ground plane of board.
7	PAR_D23	Parallel Data Bus Bit 23. (No connect.)[1]
8	PAR_D21	Parallel Data Bus Bit 21. (No connect.)[1]
9	PAR_D19	Parallel Data Bus Bit 19. (No connect.)[1]
10	PAR_D17	Parallel Data Bus Bit 17. (No connect.)[1]
11	GND	Connect to ground plane of board.
12	PAR_D14	Parallel Data Bus Bit 14.
13	PAR_D13	Parallel Data Bus Bit 13.
14	PAR_D11	Parallel Data Bus Bit 11.
15	PAR_D9	Parallel Data Bus Bit 9.
16	PAR_D7	Parallel Data Bus Bit 7.
17	GND	Connect to ground plane of board.
18	PAR_D5	Parallel Data Bus Bit 5.
19	PAR_D3	Parallel Data Bus Bit 3.
20	PAR_D1	Parallel Data Bus Bit 1.
21	$\overline{\text{PAR\_RD}}$	Asynchronous Parallel Read Strobe.
22	$\overline{\text{PAR\_CS}}$	Asynchronous Parallel Chip Select.
23	GND	Connect to ground plane of board.
24	PAR_A3	Parallel Address Bus Bit 3.
25	PAR_A1	Parallel Address Bus Bit 1.
26	PAR_FS3	Synchronous (PPI) Parallel Frame Sync 3.
27	PAR_FS1	Synchronous (PPI) Parallel Frame Sync 1.
28	GND	Connect to ground plane of board.
29	SPORT_TDV0	SPI Data Line 3. (No connect.)[1]
30	SPORT_TDV1	SPI Data Line 2. (No connect.)[1]
31	SPORT_DR1	SPORT Data Receive 1. Secondary SPORT data into processor.
32	SPORT_DT1	SPORT Data Transmit 1. Secondary SPORT data from processor.
33	SPI_D2	SPORT Data Line. (No connect.)[1]
34	SPI_D3	SPORT Data Line. (No connect.)[1]
35	SERIAL_INT	Serial Interrupt. Used to trigger a nonperiodic serial event.
36	GND	Connect to ground plane of board.
37	$\overline{\text{SPI\_SEL\_B}}$	SPI Chip Select B. Use this to control a second device on the SPI bus.
38	$\overline{\text{SPI\_SEL\_C}}$	SPI Chip Select C. Use this for a third device on the SPI bus.
39	$\overline{\text{SPI\_SEL1/SPI\_SS}}$	SPI Chip Select 1.[2] Used to connect to SPI boot flash, if required. Also used as chip select when Blackfin processor is operating as SPI slave.
40	GND	Connect to ground plane of board.
41	SDA_1	I^2C Data 1.
42	SCL_1	I^2C Data 1.[2]
43	GPIO0	General-Purpose Input/Output.
44	GPIO2	General-Purpose Input/Output.
45	GPIO4	General-Purpose Input/Output.
46	GND	Connect to ground plane of board.
47	GPIO6	General-Purpose Input/Output.[2]
48	TMR_A	Timer A Flag Pin. Use as first timer, if required.
49	TMR_C	Timer C Flag Pin.[1] (No connect.)
50	NC	No Connect. Leave this pin unconnected. Do not ground.

Pin No.	Pin Name	Description
51	NC	No Connect. Leave this pin unconnected. Do not ground.
52	GND	Connect to ground plane of board.
53	NC	No Connect. Leave this pin unconnected. Do not ground.
54	NC	No Connect. Leave this pin unconnected. Do not ground.
55	NC	No Connect. Leave this pin unconnected. Do not ground.
56	EEPROM_A0	EEPROM A0. Connect to A0 address line of the EEPROM.
57	$\overline{\text{RESET\_OUT}}$	Active low reset signal from processor board.
58	GND	Connect to ground plane of board.
59	UART_RX	UART Receive Data.[2]
60	$\overline{\text{RESET\_IN}}$	Active low pin to reset controller board.
61	BMODE1	Boot Mode 1. Pull up with 10 kΩ resistor to set SDP to boot from SPI Flash. Enabled on Connector A only.
62	UART_TX	UART Transmit Data[2].
63	GND	Connect to ground plane of board.
64	$\overline{\text{SLEEP}}$	Active low sleep from processor board.
65	WAKE	External wake up to processor board.
66	NC	No Connect. Leave this pin unconnected. Do not ground.
67	NC	No Connect. Leave this pin unconnected. Do not ground.
68	NC	No Connect. Leave this pin unconnected. Do not ground.
69	GND	Connect to ground plane of board.
70	NC	No Connect. Leave this pin unconnected. Do not ground.
71	CLKOUT	CLKOUT from processor.
72	TMR_D	Timer D Flag Pin.[2]
73	TMR_B	Timer B Flag Pin. Use as second timer, if required.
74	GPIO7	General-Purpose Input/Output.
75	GND	Connect to ground plane of board.
76	GPIO5	General-Purpose Input/Output.
77	GPIO3	General-Purpose Input/Output.
78	GPIO1	General-Purpose Input/Output.
79	SCL_0	I^2C Clock 0. Daughter board EEPROM must be connected to this bus.
80	SDA_0	I^2C Data 0. Daughter board EEPROM must be connected to this bus.
81	GND	Connect to ground plane of board.
82	SPI_CLK	SPI Clock.
83	SPI_MISO	SPI Master In, Slave Out Data.
84	SPI_MOSI	SPI Master Out, Slave In Data.
85	$\overline{\text{SPI\_SEL\_A}}$	SPI Chip Select A. Use this to control the first device on the SPI bus.
86	GND	Connect to ground plane of board.
87	SPORT_TSCLK	SPORT Transmit Clock.
88	SPORT_DT0	SPORT Data Transmit 0. Primary SPORT data from processor.
89	SPORT_TFS	SPORT Transmit Frame Sync.
90	SPORT_RFS	SPORT Receive Frame Sync.
91	SPORT_DR0	SPORT Data Receive 0. Primary SPORT data into processor.
92	SPORT_RSCLK	SPORT Receive Clock.
93	GND	Connect to ground plane of board.
94	PAR_CLK	Clock for Synchronous Parallel Interface (PPI).
95	PAR_FS2	Synchronous (PPI) Parallel Frame Sync 2.
96	PAR_A0	Parallel Address Bus Bit 0.
97	PAR_A2	Parallel Address Bus Bit 2.
98	GND	Connect to ground plane of board.
99	PAR_INT	Parallel Interrupt. Used to trigger a nonperiodic parallel event.
100	$\overline{\text{PAR\_WR}}$	Asynchronous Parallel Write Strobe.
101	PAR_D0	Parallel Data Bus Bit 0.
102	PAR_D2	Parallel Data Bus Bit 2.
103	PAR_D4	Parallel Data Bus Bit 4.

Pin No.	Pin Name	Description
104	GND	Connect to ground plane of board.
105	PAR_D6	Parallel Data Bus Bit 6.
106	PAR_D8	Parallel Data Bus Bit 8.
107	PAR_D10	Parallel Data Bus Bit 10.
108	PAR_D12	Parallel Data Bus Bit 12.
109	GND	Connect to ground plane of board.
110	PAR_D15	Parallel Data Bus Bit 15.
111	PAR_D16	Parallel Data Bus Bit 16.1 (No connect.)[1]
112	PAR_D18	Parallel Data Bus Bit 18.1 (No connect.)[1]
113	PAR_D20	Parallel Data Bus Bit 20.1 (No connect.)[1]
114	PAR_D22	Parallel Data Bus Bit 22. (No connect.)[1]
115	GND	Connect to ground plane of board.
116	VIO (+3.3 V)	+3.3 V Output. 20 mA maximum current available to power IO voltage on daughter board.
117	GND	Connect to ground plane of board.
118	GND	Connect to ground plane of board.
119	NC	No Connect. Leave this pin unconnected. Do not ground.
120	NC	No Connect. Leave this pin unconnected. Do not ground.

[1] Functionality not implemented on the SDP board.
[2] Shared across both connectors.

Each interface provided by the SDP-B is available on unique pins of the SDP-B 120-pin connector. The connector pin numbering scheme is outlined in Figure 3.

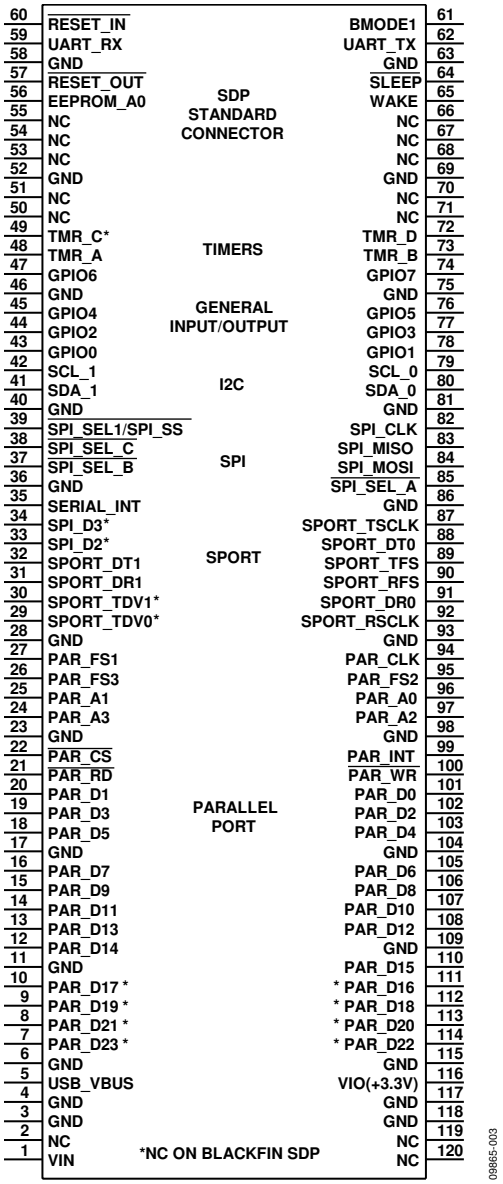

Figure 3. 120-Pin Connector Outline

Pin Sharing

Two types of pin sharing occur on the SDP-B board and must be considered when using two or more of the connector's peripheral interfaces between a daughter board and the SDP board. The first type is pin sharing that occurs internally in the Blackfin processor. The second type is pin sharing that occurs when a single Blackfin processor output pin is shared across both Connector A and Connector B.

Internal Blackfin processor pin sharing can restrict the simultaneous availability of peripheral interfaces on a single connector or across both connectors. The Blackfin processor's internal design has multiple signals physically sharing each single output pin. As mentioned previously, the pins on the 120-pin connector were defined independently of this pin sharing. This has the effect of limiting the peripherals, which can be used simultaneously on the SDP. A system designer must consult the ADSP-BF52x Blackfin Processor Hardware Reference for the ADSP-BF527 processor to ensure the selected peripherals are available simultaneously and their signals do not share Blackfin processor output pins. An example of this sharing is that the SPORT and PPI peripherals physically share the same Blackfin processor pins. Therefore, these two interfaces cannot be utilized in a single application. Pin sharing also occurs from certain Blackfin processor output pins to both Connector A and Connector B. The following signals are connected from a single Blackfin processor output pin to both Connector A and Connector B:

- I^2C Bus 1, Pin 41 and Pin 42
- SCL 0 on I^2C Bus 0, Pin 79
- GPIO 6 and GPIO 7, Pin 47 and Pin 67
- Timer D, Pin 72
- UART, Pin 59 and Pin 62

POWER

The SDP-B board requires that any daughter board connected to the SDP-B board provides the SDP-B board with 5 V at 200 mA. This supply should be made available on Pin 1 (VIN) of the 120-pin connector. This supply is required to power the Blackfin processor, the memory, and the other components on the SDP-B board. The SDP board also provides 3.3 V at 20 mA on Pin 116 (VIO_3.3) to connected daughter boards as the VIO voltage for the daughter board. Pin 5 (USB_VBUS) is connected to the +5 V line of the USB connector, providing 5 V ±10% as an output of the SDP board.

DAUGHTER BOARD DESIGN GUIDELINES

The daughter board design guidelines specify the layout, connector position, keep out areas, and dimensions of potential daughter boards. This guidance is to ensure that a daughter board can connect off either Connector A or Connector B of the SDP-B board. Following these guidelines ensures that both connectors on the SDP can have any one of the catalogue of daughter boards physically attached to the connectors simultaneously.

Connector Location

The daughter board connector and securing screw holes are to be located in the top left hand corner. This arrangement can be seen for Daughter Board A in Figure 4. Note that Daughter Board B is the same as Daughter Board A rotated clockwise through 90°. The exact location of the connector from the board's edge is important in order to allow both boards connect at the same time. As seen in Figure 4, if either board exceeds these dimensions, it is not possible to connect the other. Every effort was made to extend the 5.9 mm dimension as large as possible in order to allow space for vias between the connector and the edge of the board. These are absolute maximum dimensions and should not be exceeded.

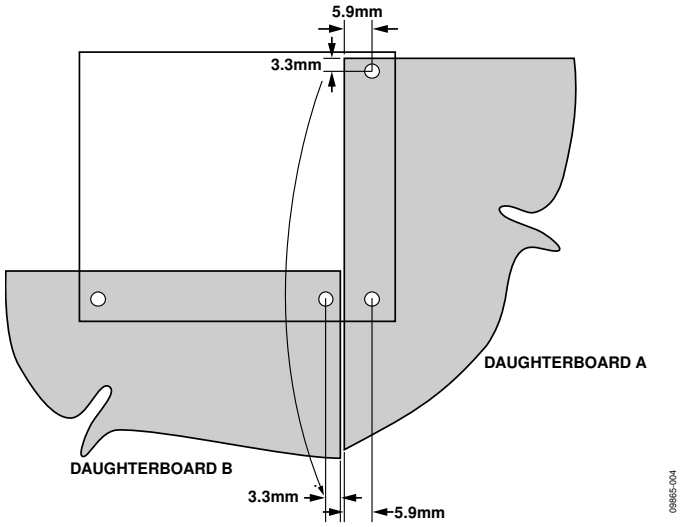

Figure 4. Maximum Board Dimensions for Connector Placement

The full specification drawing for the connector location on the daughter board can be seen in Figure 5.

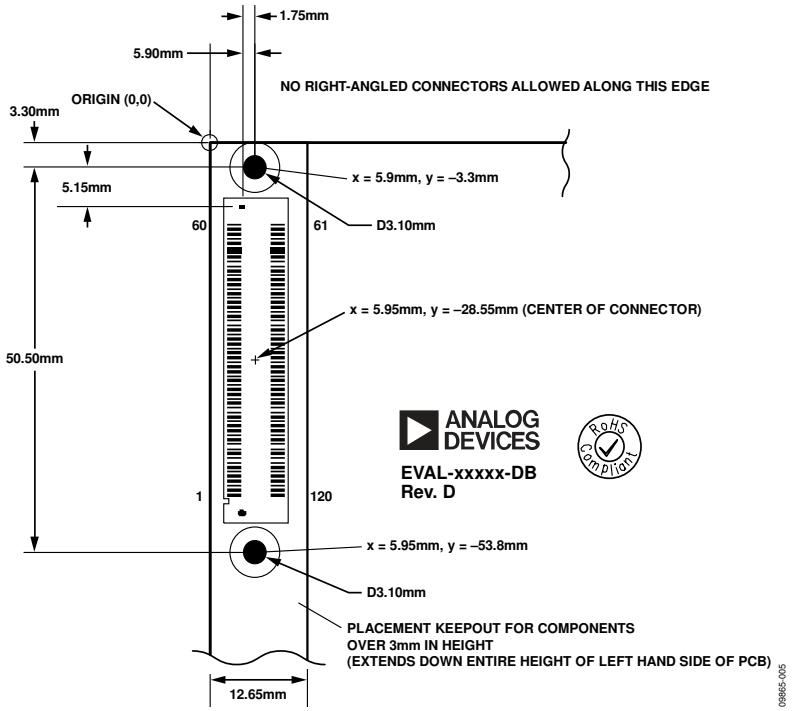

Figure 5. Connector Placement on Compatible Daughter Boards

The mating daughter board 120-pin connector is the Hirose FX8-120S-SV(21), 120-pin receptacle, FEC 132-4660, Digi-Key H1219-ND. Consult the connector's data sheet for full details on the connector. Note that Pin 1 to Pin 60 are placed on the left side of the connector and Pin 61 to Pin 120 are placed on the right side of the connector.

Keep Out Area

In order to allow the greatest flexibility for future controller boards, a keep out area is established for components higher that 3 mm. The keep out area is 12.65 mm wide and extends down the entire left side of the daughter board.

Restriction on Right Angle Connectors

Due to the close proximity of the edges of the A and B daughter boards (seen in Figure 4) right angle connectors are not allowed on the top and left edges of the daughter boards and (if required) should be placed on the right or bottom edges. The phrase "right angle connector" is used to describe any connector that requires the connection to protrude over the edge of the board (for example, right angle SMB or screw terminal)

MECHANICAL SPECIFICATIONS

The mechanical specifications of the SDP-B board are 2.75" × 2.25" (69.85 mm × 27.15 mm). The height of the 120-pin connectors from the bottom of the board is approximately 0.152" (3.86 mm). The tallest component on the top is approximately 0.125" (3.175 mm), and the tallest components on the bottoms are the connectors at approximately 0.152" (3.86 mm). Refer to Figure 6.

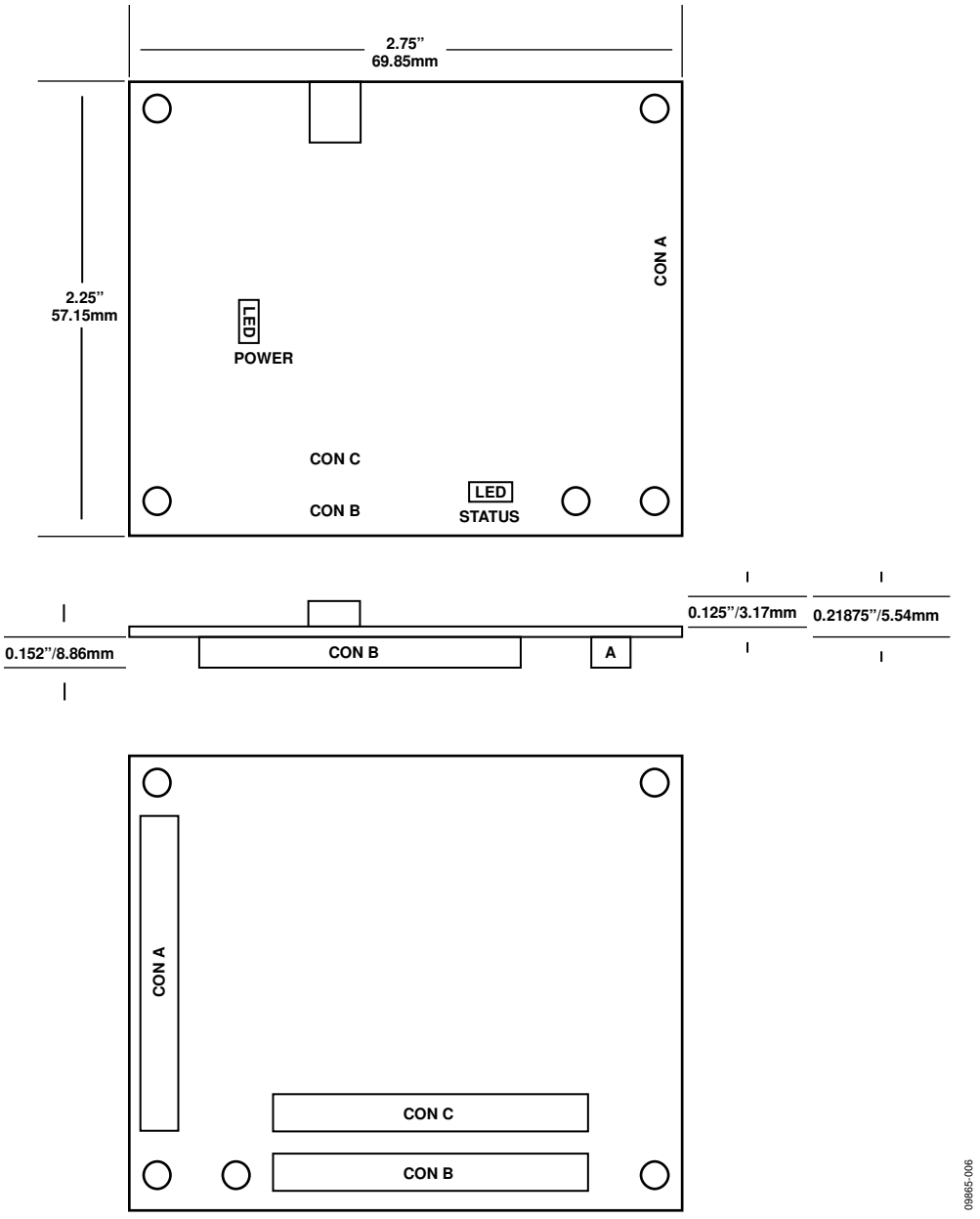

Figure 6. SDP-B Board Mechanical Specifications

SCHEMATICS

This section provides the schematic drawings for the EVAL-SDP-CB1Z board. The schematic pages include

- SDP-B—Power
- SDP-B—Memory
- SDP-B—Clocks_USB
- SDP-B—Blackfin_I/O
- SDP-B—Connector A
- SDP-B—Connector B
- SDP-B—Connector C

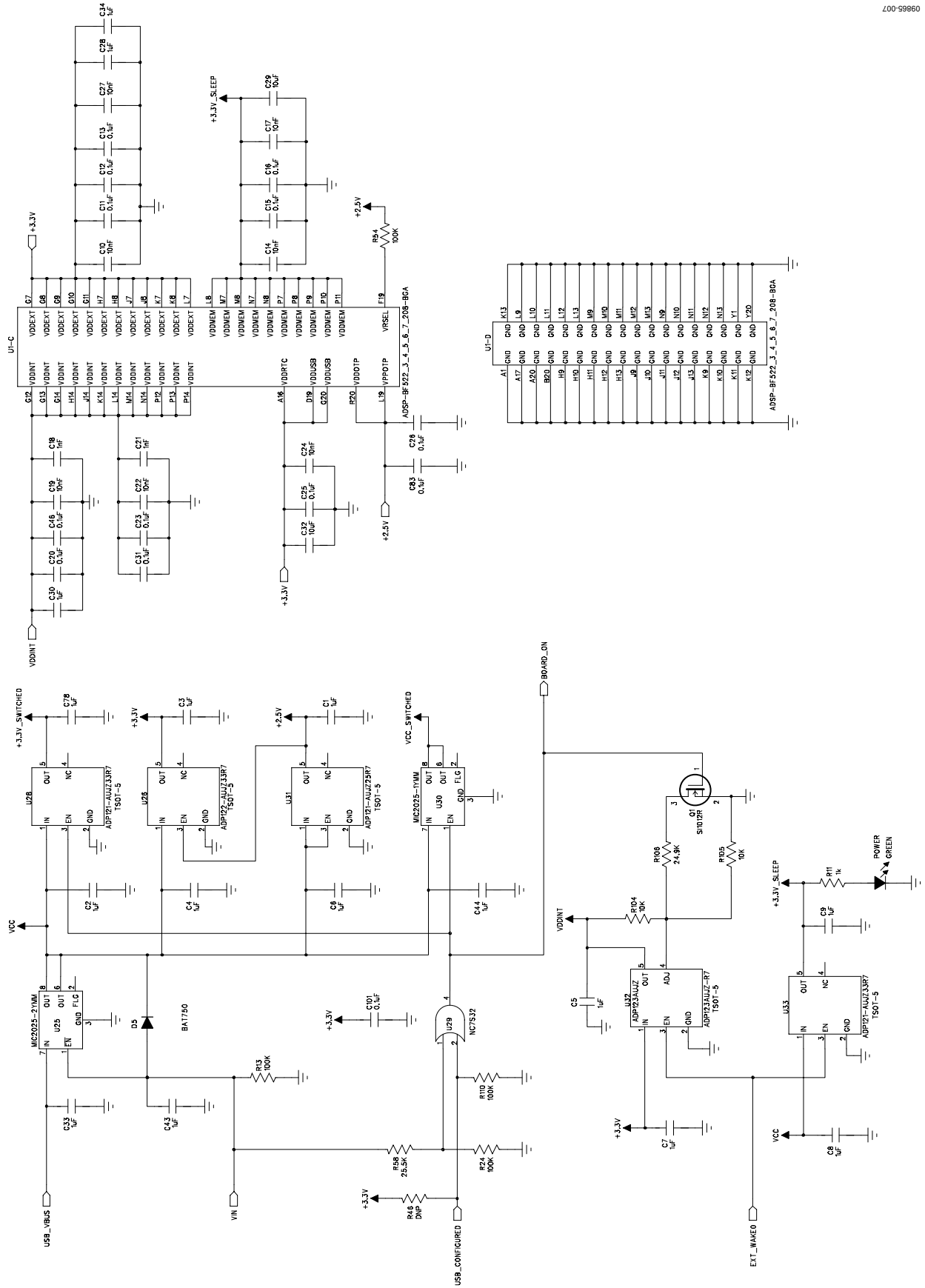

Figure 7. SDP-B —Power

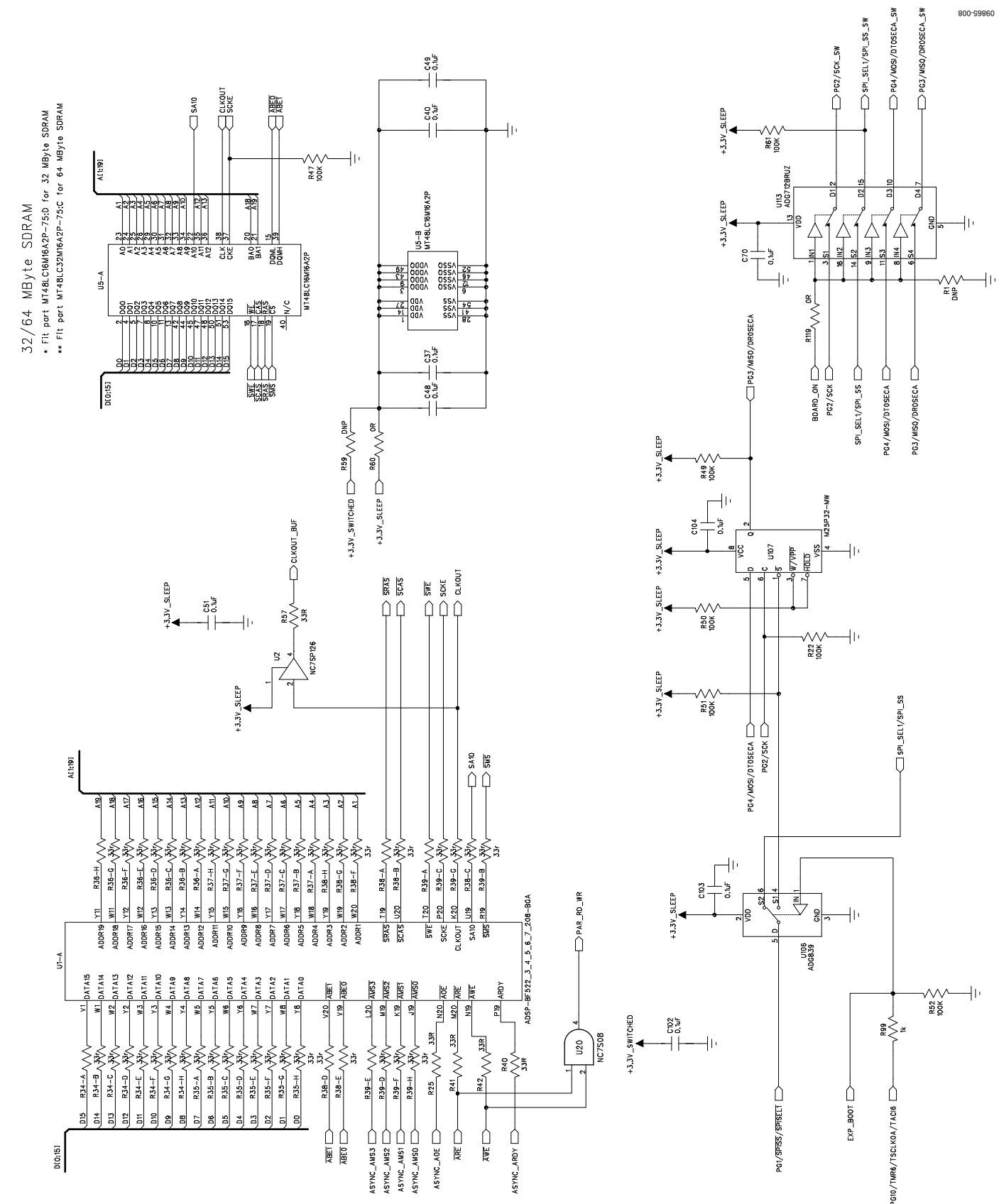

Figure 8. SDP-B —Memory

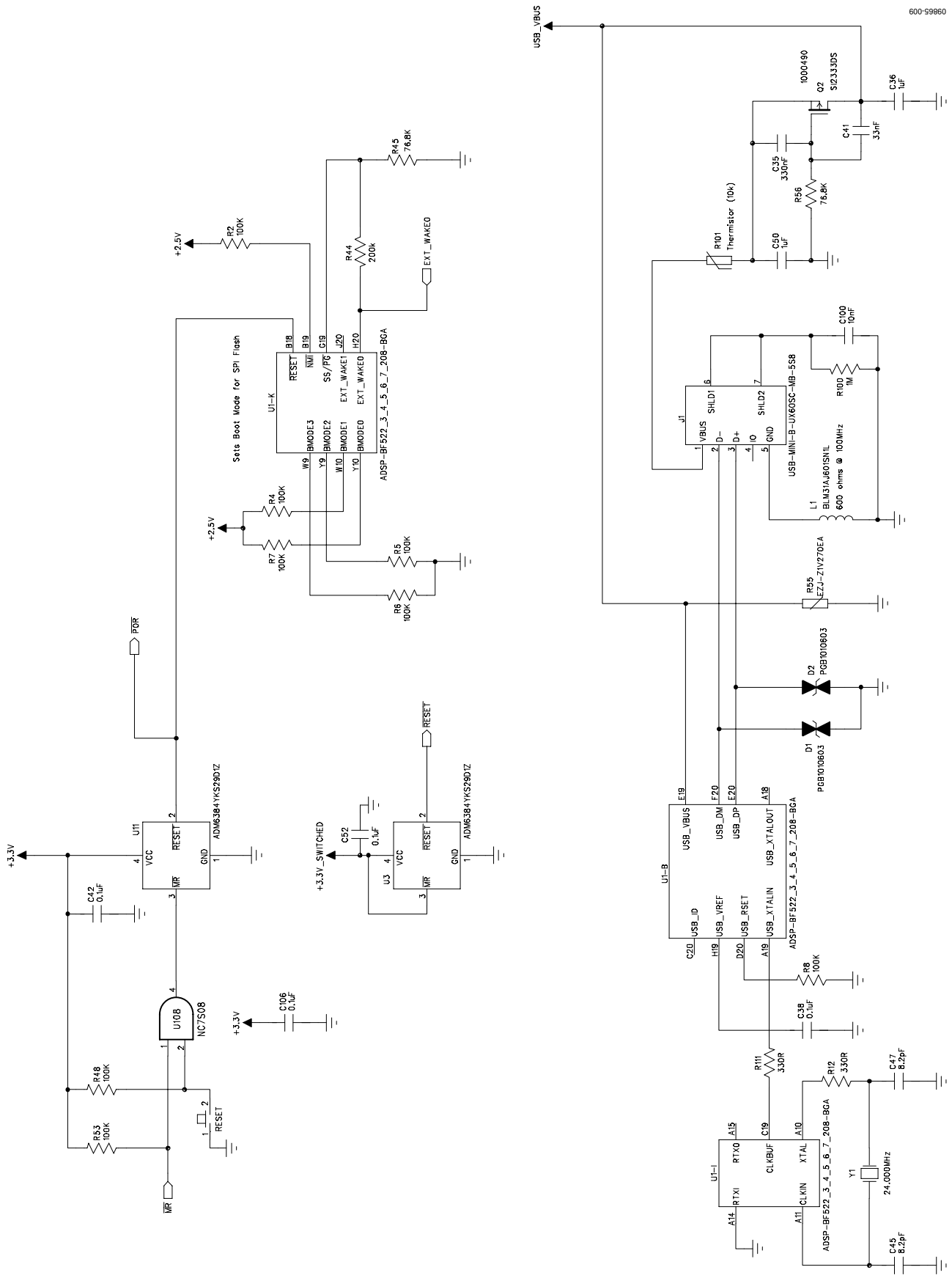

Figure 9. SDP-B —Clocks_USB

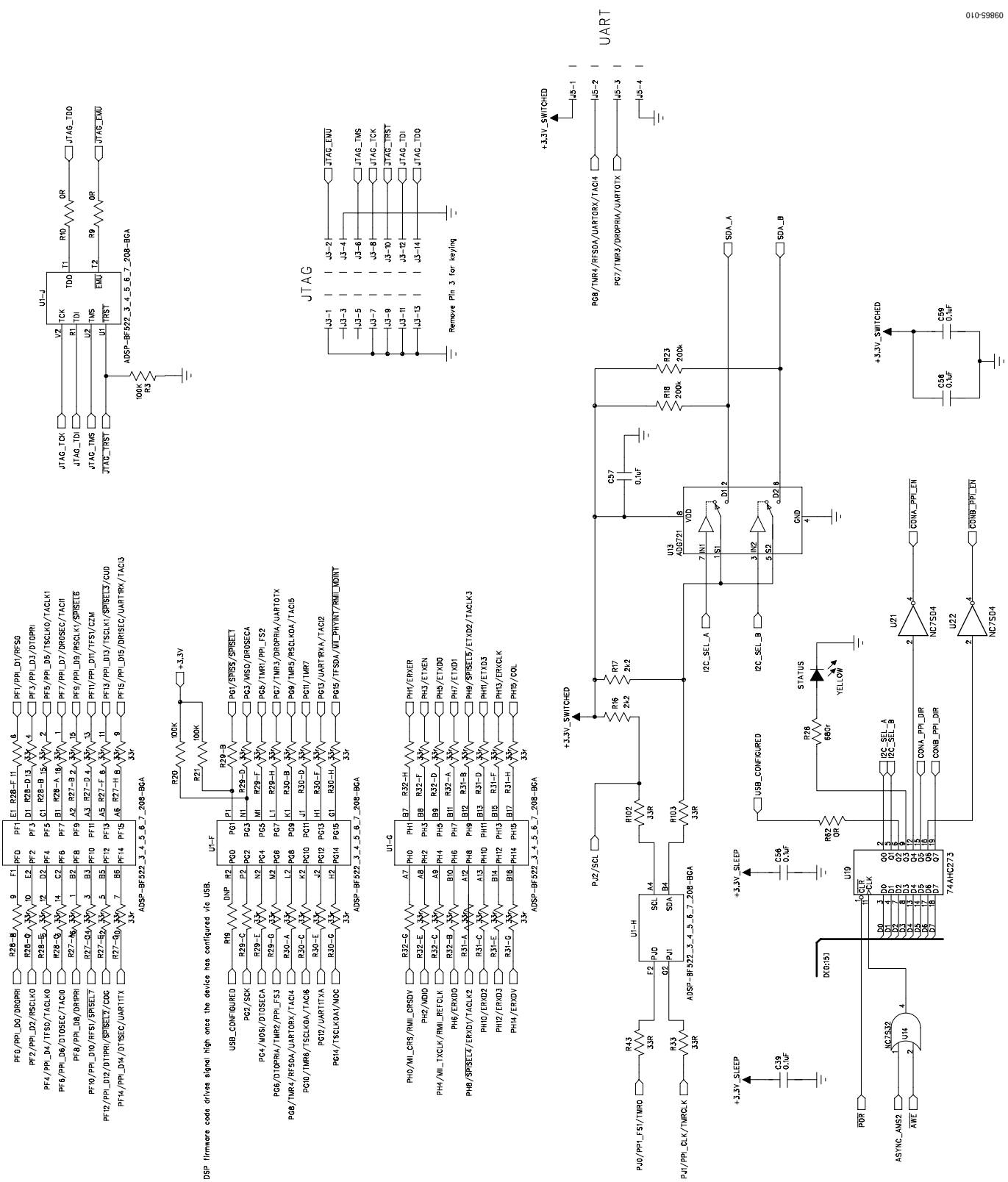

Figure 10. SDP-B —Blackfin_I/O

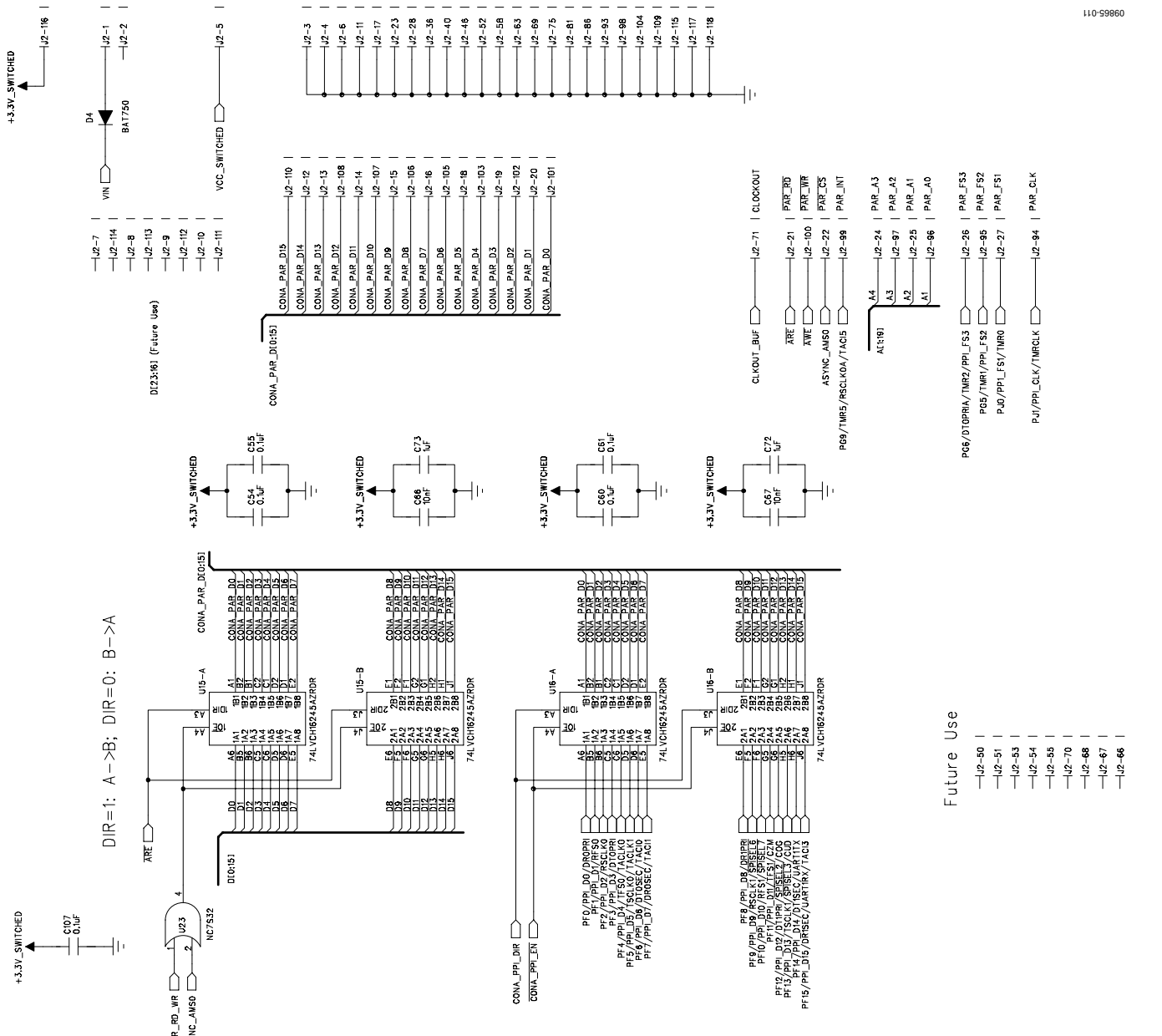

Figure 11. SDP-B —Connector A

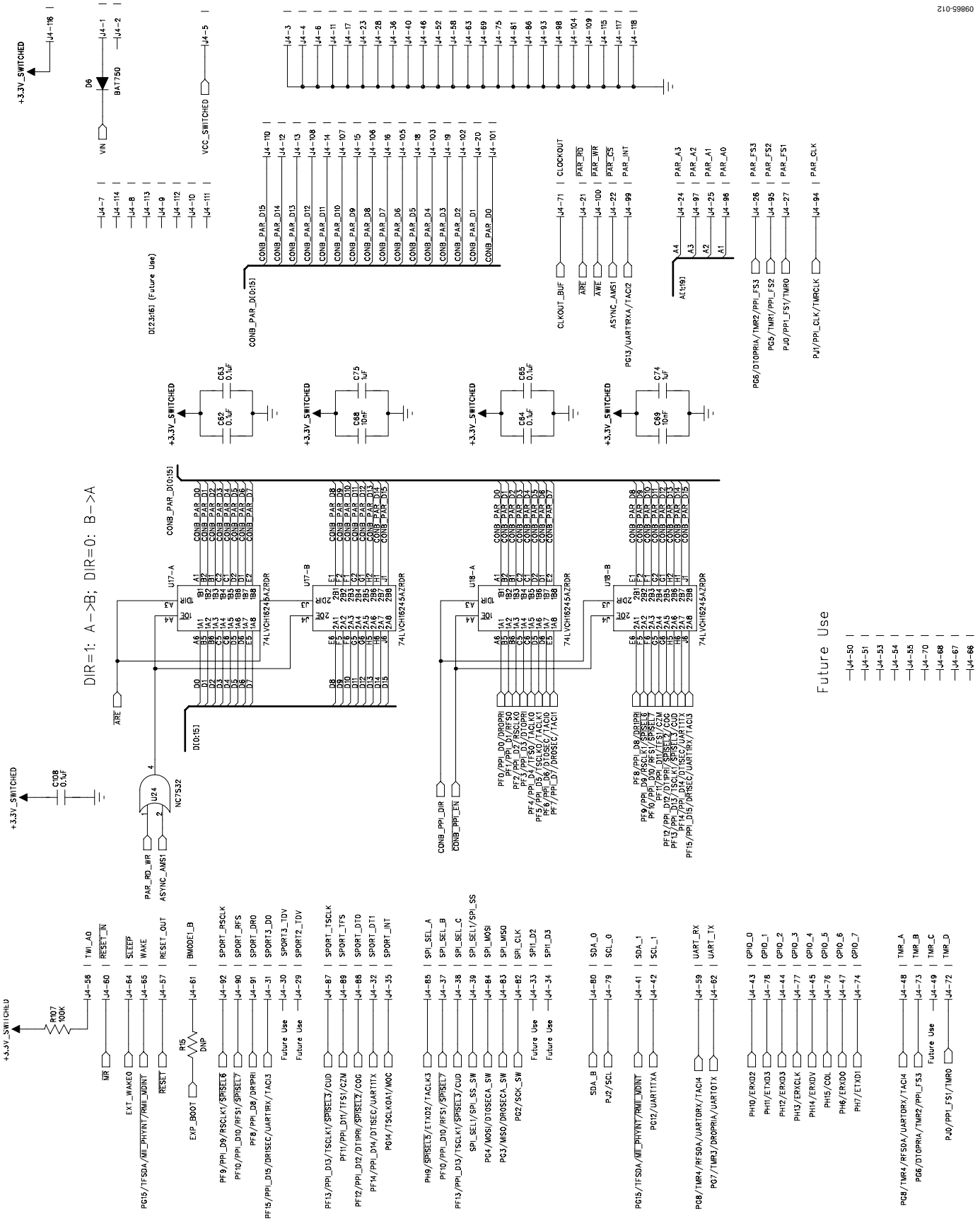

Figure 12. SDP-B —Connector B

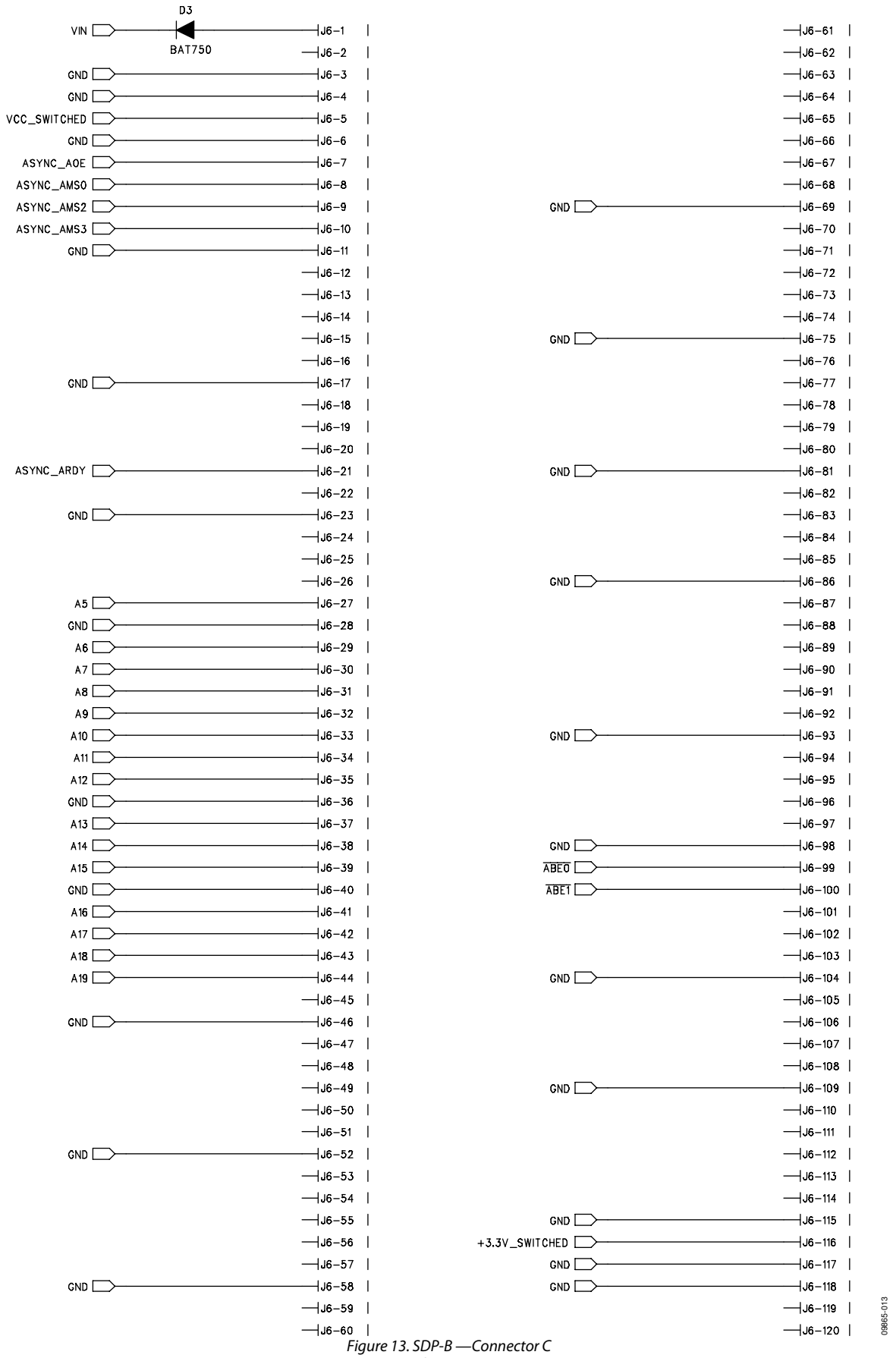

Figure 13. SDP-B —Connector C

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ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG09865-0-12/11(B)

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