

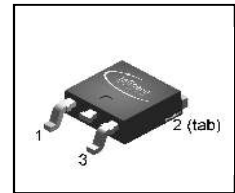
**OptiMOS™-T Power-Transistor**

**Features**

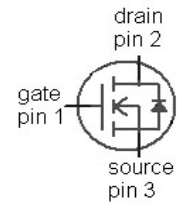
- N-channel - Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

**Product Summary**

$V_{DS}$	100	V
$R_{DS(on),max}$	11.5	mΩ
$I_D$	70	A

**PG-TO252-3-11**


Type	Package	Marking
IPD70N10S3L-12	PG-TO252-3-11	QN10L12


**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$T_C=25\text{ °C}, V_{GS}=10\text{V}$	70	A
		$T_C=100\text{ °C}, V_{GS}=10\text{V}^{1)}$	48	
Pulsed drain current <sup>1)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	280	
Avalanche energy, single pulse <sup>1)</sup>	$E_{AS}$	$I_D=35\text{A}$	410	mJ
Avalanche current, single pulse	$I_{AS}$		70	A
Gate source voltage <sup>2)</sup>	$V_{GS}$		±20	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	125	W
Operating and storage temperature	$T_j, T_{stg}$		-55 ... +175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
<b>Thermal characteristics<sup>1)</sup></b>						
Thermal resistance, junction - case	$R_{thJC}$		-	-	1.2	K/W
SMD version, device on PCB	$R_{thJA}$	minimal footprint	-	-	62	
		6 cm <sup>2</sup> cooling area <sup>3)</sup>	-	-	40	

**Electrical characteristics**, at  $T_j=25^\circ\text{C}$ , unless otherwise specified

#### Static characteristics

Drain-source breakdown voltage	$V_{(Br)DSS}$	$V_{GS}=0V, I_D=1mA$	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=83\mu A$	1.2	1.7	2.4	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=80V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	0.01	0.1	$\mu A$
		$V_{DS}=80V, V_{GS}=0V, T_j=125^\circ\text{C}^{1)}$	-	1	10	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=16V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=70A$	-	11.7	15.2	m $\Omega$
		$V_{GS}=10V, I_D=70A$	-	9.6	11.5	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics<sup>1)</sup>**

Input capacitance	$C_{iss}$	$V_{GS}=0V, V_{DS}=25V,$ $f=1MHz$	-	4270	5550	pF
Output capacitance	$C_{oss}$		-	950	1235	
Reverse transfer capacitance	$C_{rss}$		-	90	135	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20V, V_{GS}=10V,$ $I_D=70A, R_G=3.5\Omega$	-	12	-	ns
Rise time	$t_r$		-	6	-	
Turn-off delay time	$t_{d(off)}$		-	35	-	
Fall time	$t_f$		-	7	-	

**Gate Charge Characteristics<sup>1)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=80V, I_D=70A,$ $V_{GS}=0$ to 10V	-	16	21	nC
Gate to drain charge	$Q_{gd}$		-	11	17	
Gate charge total	$Q_g$		-	59	77	
Gate plateau voltage	$V_{plateau}$		-	3.7	-	V

**Reverse Diode**

Diode continuous forward current <sup>1)</sup>	$I_S$	$T_C=25^\circ C$	-	-	70	A
Diode pulse current <sup>1)</sup>	$I_{S,pulse}$		-	-	280	
Diode forward voltage	$V_{SD}$	$V_{GS}=0V, I_F=70A,$ $T_j=25^\circ C$	0.6	1	1.2	V
Reverse recovery time <sup>1)</sup>	$t_{rr}$	$V_R=50V, I_F=I_S,$ $di_F/dt=100A/\mu s$	-	80	-	ns
Reverse recovery charge <sup>1)</sup>	$Q_{rr}$		-	185	-	nC

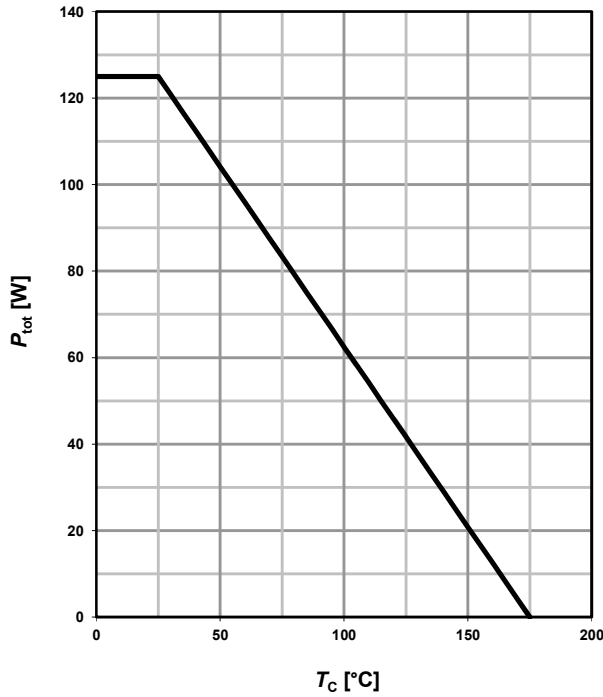
<sup>1)</sup> Defined by design. Not subject to production test.

<sup>2)</sup> -5V to -20V for max. 168 non-consecutive hours.

<sup>3)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

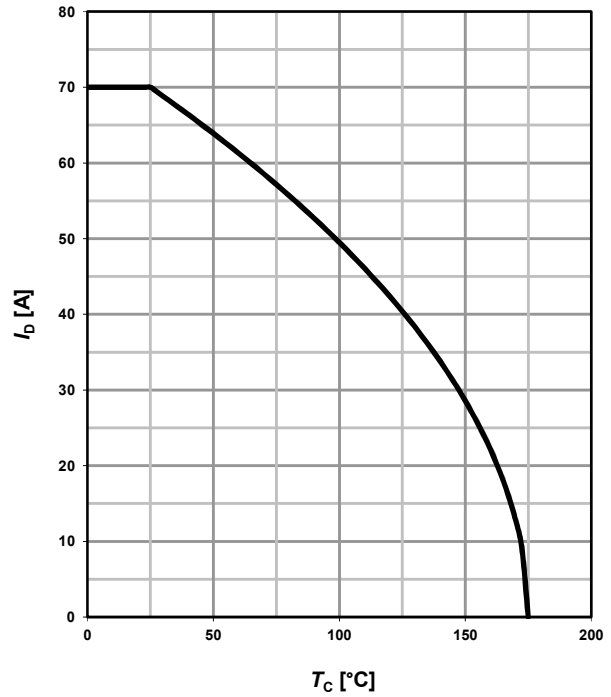
**1 Power dissipation**

$P_{tot} = f(T_C); V_{GS} \geq 6\text{ V}$



**2 Drain current**

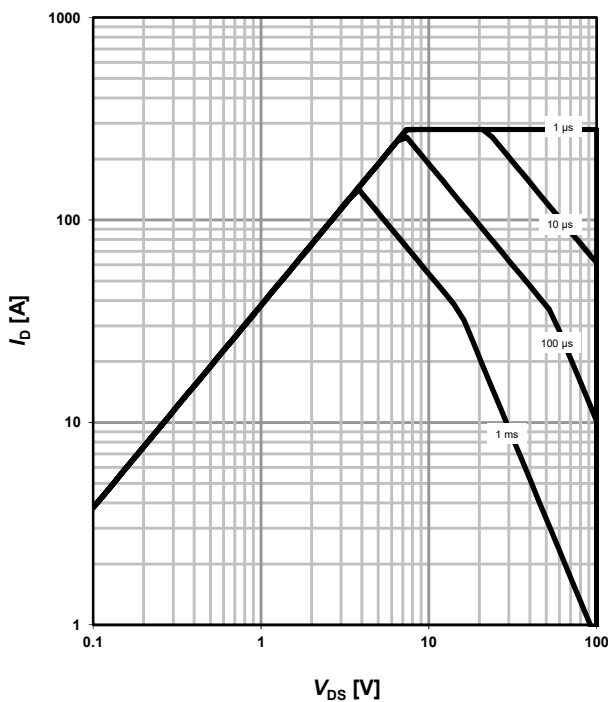
$I_D = f(T_C); V_{GS} \geq 6\text{ V}$



**3 Safe operating area**

$I_D = f(V_{DS}); T_C = 25\text{ °C}; D = 0$

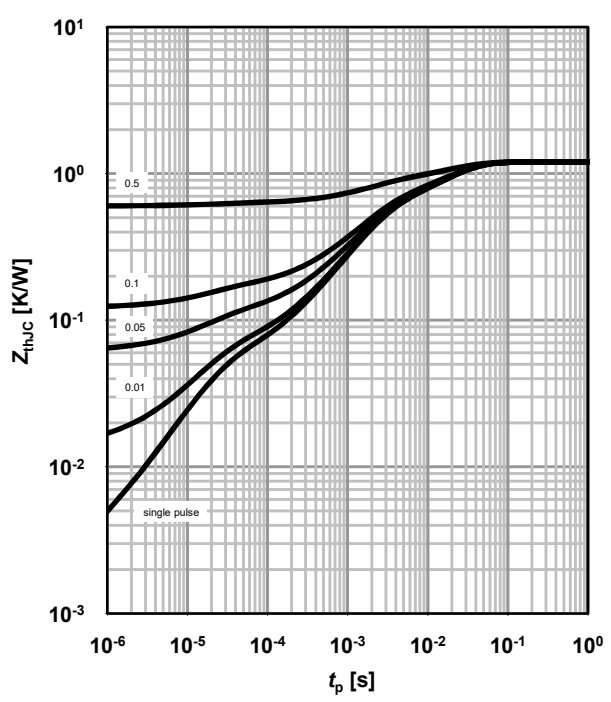
parameter:  $t_p$



**4 Max. transient thermal impedance**

$Z_{thJC} = f(t_p)$

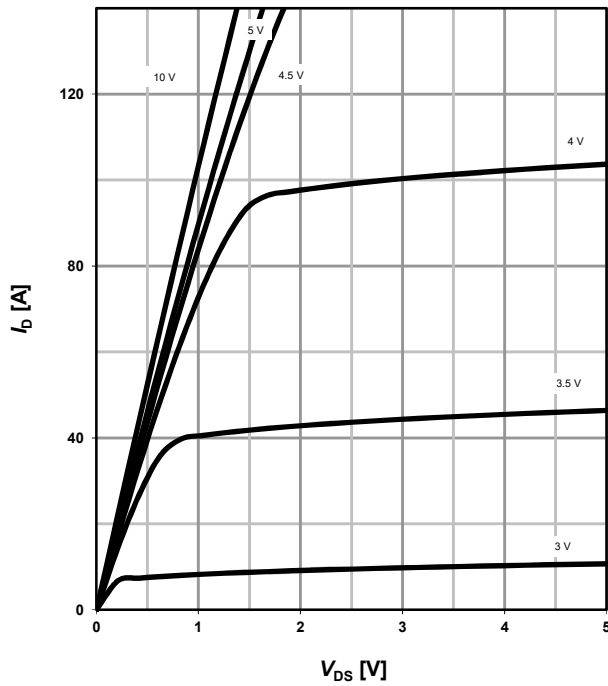
parameter:  $D = t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

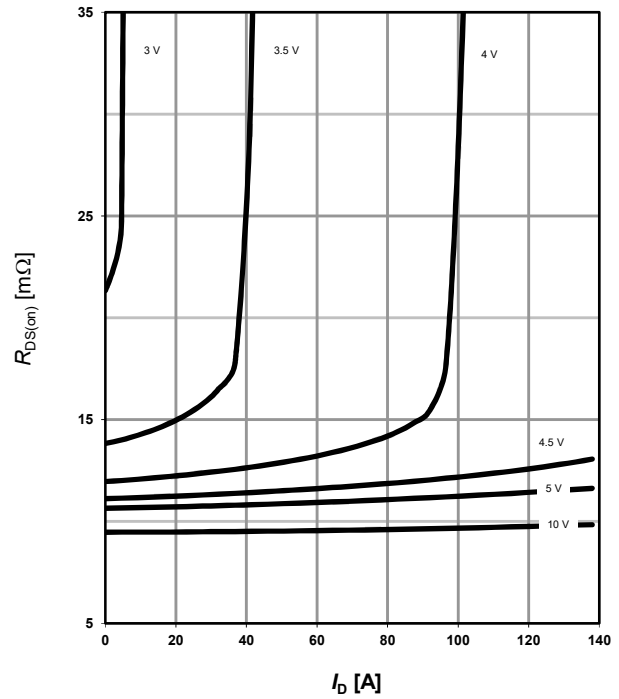
parameter:  $V_{GS}$



**6 Typ. drain-source on-state resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

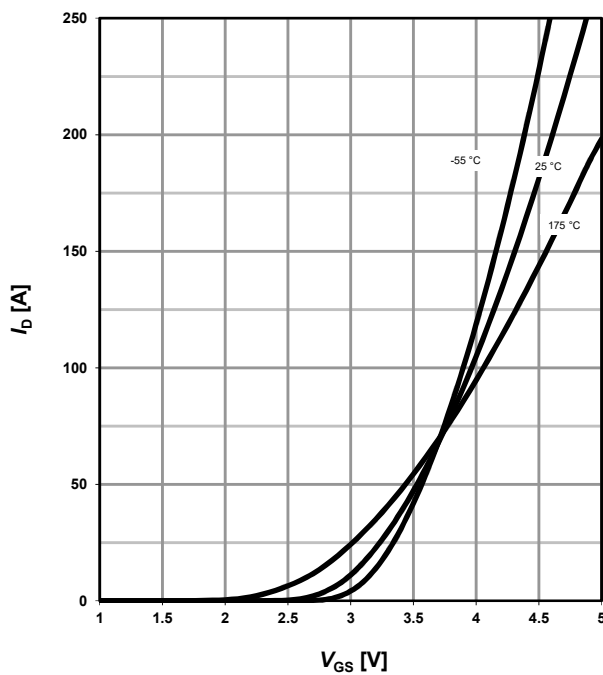
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

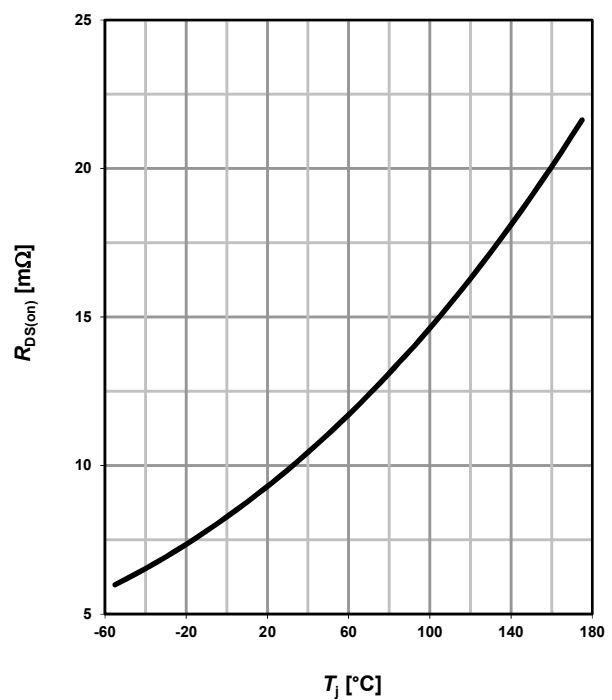
parameter:  $T_j$



**8 Typ. drain-source on-state resistance**

$R_{DS(on)} = f(T_j); I_D = 70\text{ A}; V_{GS} = 10\text{ V}$

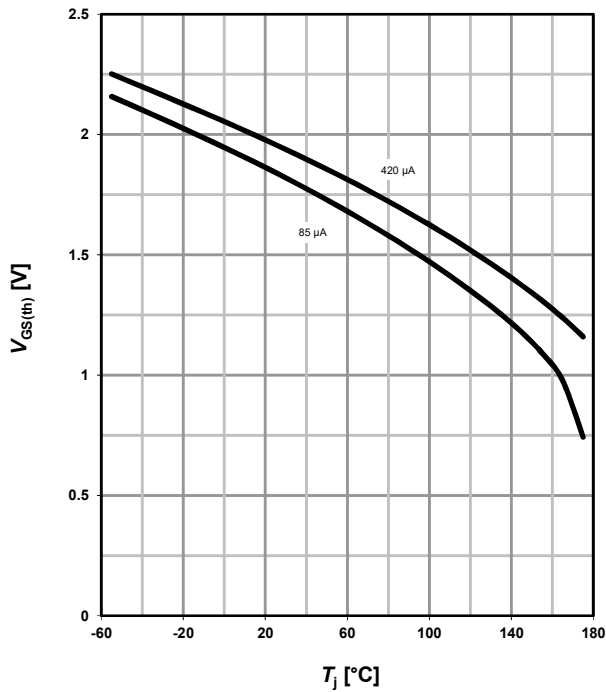
$\alpha = 0.56$



**9 Typ. gate threshold voltage**

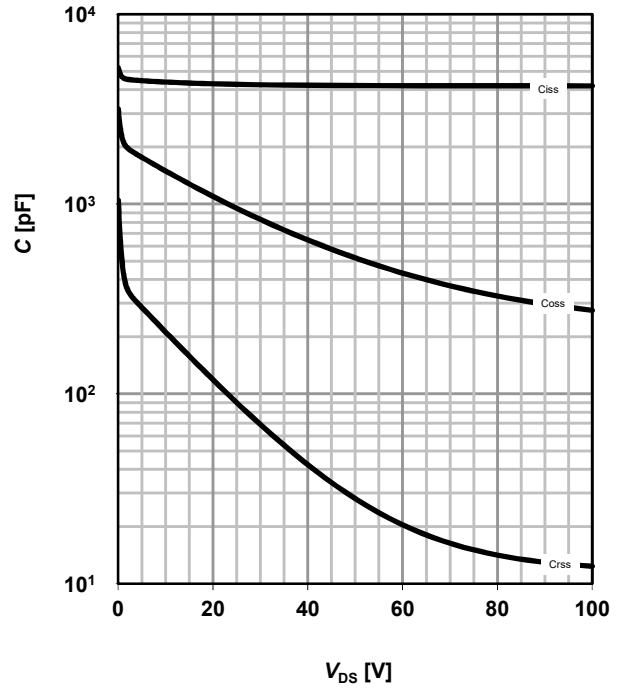
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter:  $I_D$



**10 Typ. capacitances**

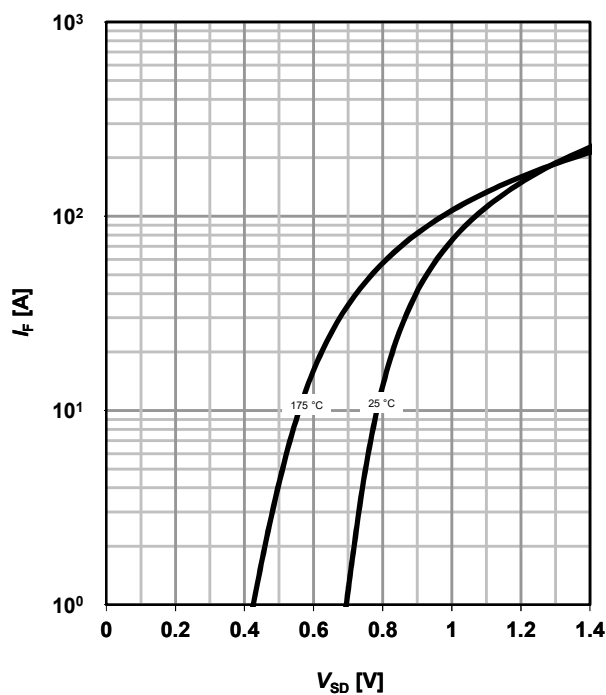
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



**11 Typical forward diode characteristics**

$I_F = f(V_{SD})$

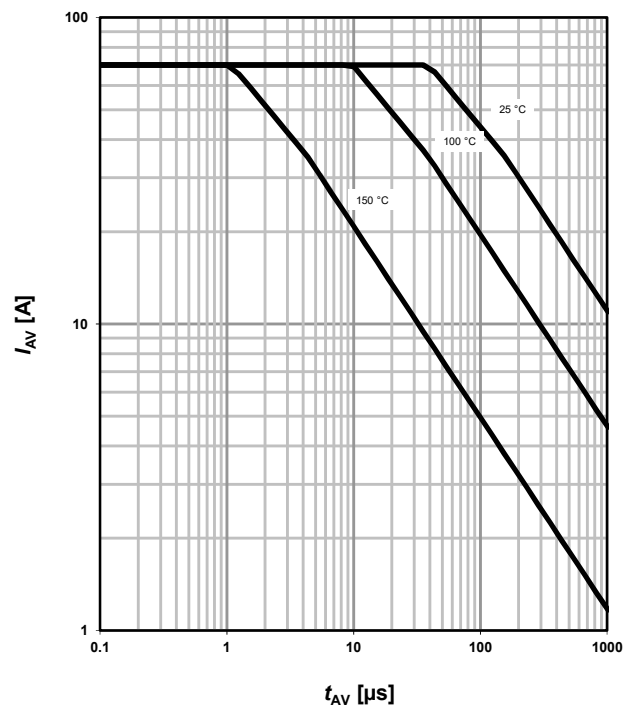
parameter:  $T_j$



**12 Typ. avalanche characteristics**

$I_{AS} = f(t_{AV})$

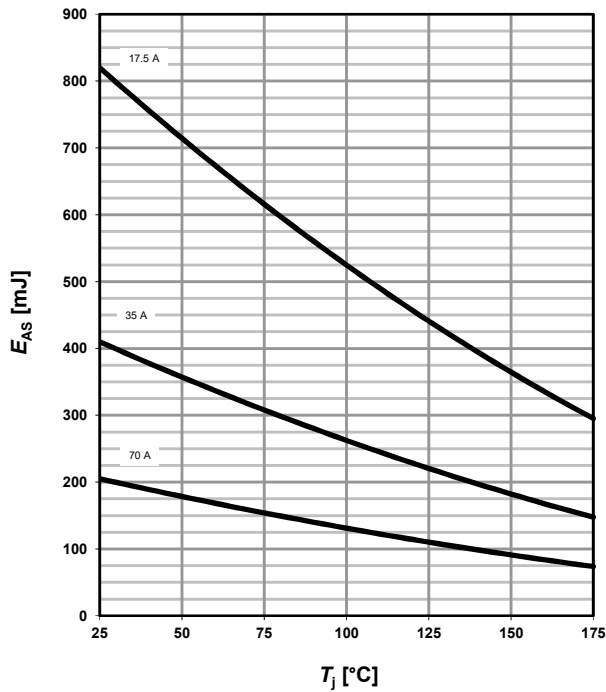
parameter:  $T_{j(start)}$



**13 Typical avalanche energy**

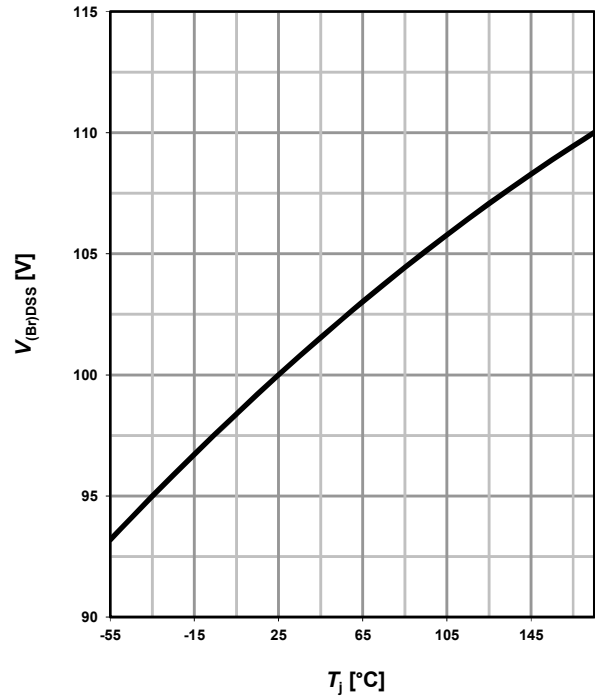
$$E_{AS} = f(T_j)$$

parameter:  $I_D$



**14 Typ. drain-source breakdown voltage**

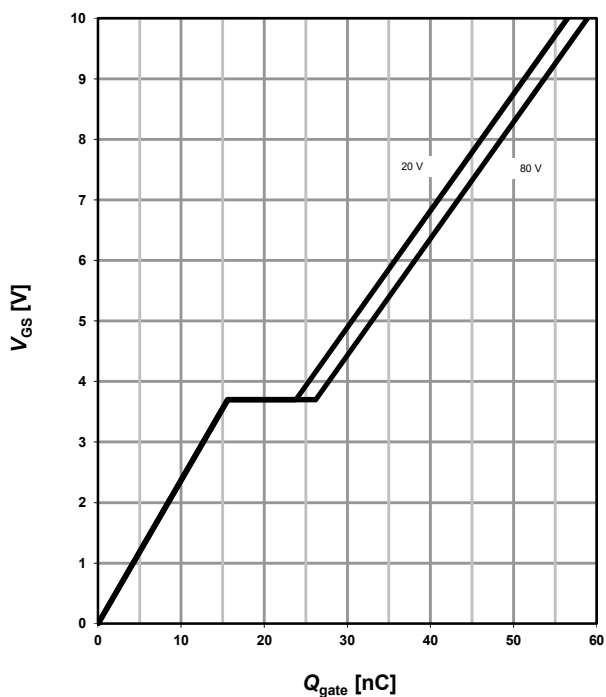
$$V_{(BR)DSS} = f(T_j); I_D = 1 \text{ mA}$$



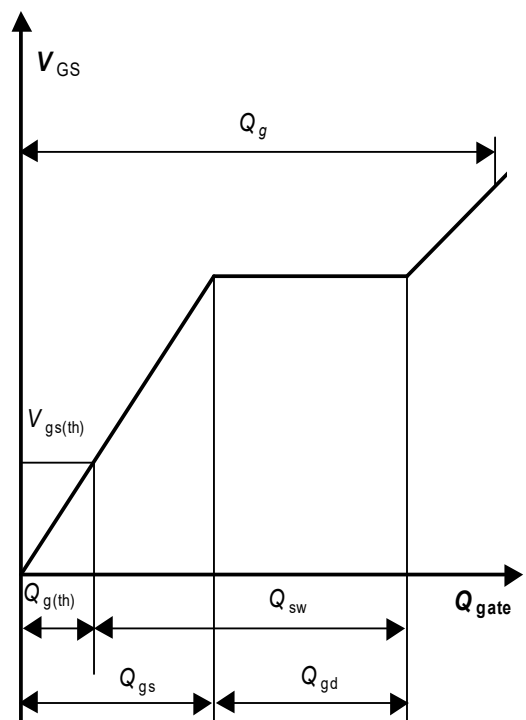
**15 Typ. gate charge**

$$V_{GS} = f(Q_{gate}); I_D = 70 \text{ A pulsed}$$

parameter:  $V_{DD}$



**16 Gate charge waveforms**



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## Revision History

Version	Date	Changes
Rev 1.1	2008-04-08	Page 1: $V_{GS}$ changed from $\pm 16V$ to $\pm 20V$
Rev 1.1	2008-04-08	Page 3: Footnote <sup>2)</sup> added
Rev 1.2	2023-06-15	Diagram 8 Typ. drain-source on-state resistance: used $\alpha$ value clarified
Rev 1.2	2023-06-15	Ratings of Gate Source Voltage $V_{GS}$ refined in footnote <sup>2)</sup>
Rev 1.2	2023-06-15	Corrected diagram 3 safe operating area
Rev 1.2	2023-06-15	Corrected diagram 10 typical capacitances