

LITIX™ Basic+ Family Board V1.1

November 2018



1 Board description

2 Quick start

3 Schematic and layout

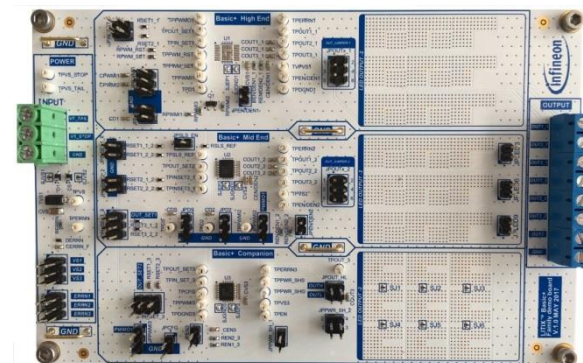
1 Board description

2 Quick start

3 Schematic and layout

Board description

- › Equipped with one TLD2141-3EP (High End), one TLD2331-3EP (Mid End) and one TLD1114-1EP (Companion) LITIX™ Basic+ devices
- › Compatible with all LITIX™ Basic+ High End and Mid End devices
- › Typical supply voltage range: 8V – 16V (5.5V – 40V), with possibility to power-ON and test each device separately
- › On-board LED load for each device, 3x3 LEDs per device
- › Possibility to connect to external load
- › 15cm x 10cm 2-layer PCB



Board connectors

- › POWER: Supply connector, VS and GND
 - VS_STOP: Board power supply and activation of the internal PWM engine for Basic+ High End device
 - VS_TAIL: Board power supply without activation of the internal PWM engine
 - GND

- › OUTPUT: External load
 - OUT1_1, OUT2_1, OUT3_1: For the Basic+ High End device (OUT1, OUT2, OUT3)
 - OUT1_2, OUT2_2, OUT3_1: For the Basic+ Mid End device (OUT1, OUT2, OUT3)
 - OUT3: For the Basic+ Companion
 - GND

Jumpers – Power Supply, Error Network

- › JPVS: Select which devices will be supplied (all devices share the same reverse polarity protection circuit)
 - VS1: Close to supply the Basic+ High End
 - VS2: Close to supply the Basic+ Mid End
 - VS3: Close to supply the Basic+ Companion

- › JPERRN: Select which devices will be connected to the error network (all devices share the same error network pull-up circuit)
 - ERRN1: Close to connect the Basic+ High End device to the error network
 - ERRN2: Close to connect the Basic+ Mid End device to the error network
 - ERRN3: Close to connect the Basic+ Companion device to the error network

Jumpers - Basic+ High End

- › JPIN_SET_1: Sets the output current of OUT
 - RSET1_1 (37.4 k Ω): sets output current to 10 mA (30 mA for TLD2142-1EP)
 - RSET2_1 (6.19 k Ω): sets output current to 59 mA (177 mA for TLD2142-1EP)

- › JPPWMI1: PWMI connection
 - CPWMI1 (120 nF): Set the PWM frequency to 220 Hz and duty cycle* 10%
 - CPWMI2 (68 nF): Set the PWM frequency to 400 Hz and duty cycle* 10%
 - GND: duty cycle is 100%

* Duty cycle set by the RPWM_SET and RPWM_RST resistors

Jumpers - Basic+ High End cont'd

- › JPD1: Diagnosis management
 - CD1: When a fault is detected, or ERRN is pulled-down externally, all the channels driven by the device are switched off after a delay time $t_{D(\text{set})}$. Delay time is set by CD1 capacitor
 - GND: Only the channel under fault condition will be deactivated

- › JPEN/DEN1: Close to connect EN/DEN to resistor divider to activate device and diagnosis

Jumpers – Basic+ Mid End

- › JPINSETx_2: Sets the output current of OUTx (1 or 2)
 - RSETx_1_2 (37.4 k Ω): sets output current to 10 mA (30 mA for TLD2132-1EP)
 - RSETx_2_2 (6.19 k Ω): sets output current to 59 mA (177 mA for TLD2132-1EP)

- › JPINSET3_2: Sets the output current of OUT3
 - OUT_SET1: Output current is controlled by the OUT_SET of the Basic+ High End device
 - RSET3_1_2 (37.4 k Ω): sets output current to 10 mA (30 mA for TLD2132-1EP)
 - RSET3_2_2 (6.19 k Ω): sets output current to 59 mA (177 mA for TLD2132-1EP)

- › JSLS_EN: When closed, the SLS diagnosis is deactivated. When open the voltage reference is set by the resistor RSLS_REF

Jumpers – Basic+ Mid End cont'd

- › JPEN/DEN2: Close to connect EN/DEN to resistor divider to activate device and diagnosis
- › JPD: Diagnosis management
 - GND: Only the channel under fault condition will be deactivated
 - CD2: When a fault is detected, or ERRN is pulled-down externally, all the channels driven by the device are switched off after a delay time $t_{D(set)}$. Delay time is set by CD2 capacitor
- › JPDS: SLS diagnosis
 - GND: Latched SLS detection
 - CDS: Automatic retry after $t_{SL(wait)}$. $t_{SL(wait)}$ time defined by CDS capacitor
- › JPWMI2: PWMI connection
 - PWMO1: Use of PWMO signal of Basic+ High End
 - GND: Outputs activated

Jumpers - Companion

- › JPIN_SET3: Sets the output current
 - OUT_SET2: Output current is driven by the OUT_SET
 - RSET1_3 (13.7 k Ω): Sets the output current to 80 mA
 - RSET2_3 (2.94 k Ω): Sets the output current to 373 mA

- › JPPWMI3: PWM connection
 - PWMO1: Use of PWMO signal of Basic+ High End
 - GND: Output activated

- › JPCFG: Close if higher current accuracy is needed to drive the target load (closed when OUTH is connected to the load)

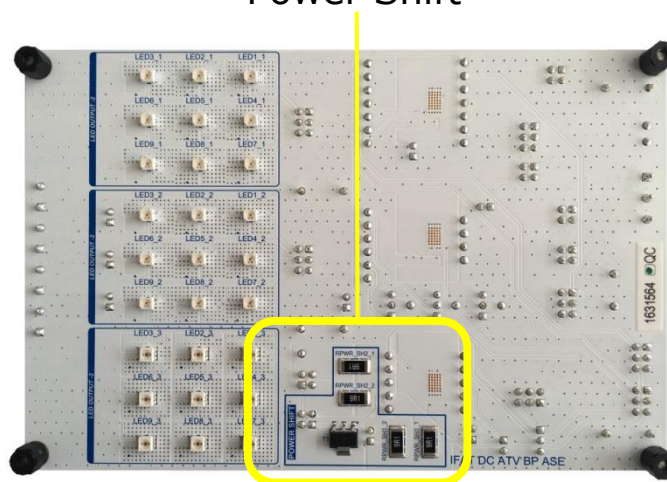
- › JPEN3: Close to connect EN/DEN to resistor divider to activate device and diagnosis

Jumpers – Companion cont'd

- › JPPWR_SH_1: Close to allow Power Shift control

- › JPPWR_SH_2: Change of R2
 - 1 - 2 or 3 - 4 closed: $R2 = 9.1 \Omega$, $IPSH_{max} = 350 \text{ mA}$
 - 1 - 2 and 3 - 4 closed: $R2 = 4.55 \Omega$, $IPSH_{max} = 700 \text{ mA}$

Power Shift



Jumpers – Load selection

- › OUT_JUMPER-1, 2: Bypass to connect the on-board load, LED OUTPUT-1, 2 to the outputs of Basic+ High End, Basic+ Mid End. Leave open to connect external load
 - 1-2 closed: Connect OUT1 of Basic+ High End, Basic+ Mid End
 - 3-4 closed: Connect OUT2 of Basic+ High End, Basic+ Mid End
 - 5-6 closed: Connect OUT3 of Basic+ High End, Basic+ Mid End

- › JPOUT_HL: Bypass to connect the on-board load, LED OUTPUT-3 to the output of Basic+ Companion. Leave open to connect to external load
 - OUTH: Connect OUTH of Basic+ Companion (JPCFG must be closed)
 - OUTL: Connect OUTL of Basic+ Companion (JPCFG must be open)

On-board Load

- › LED OUTPUT-1: 1 rows of 3 red LEDs (LS E6SF) for each channel (3x3) of Basic+ High End

- › LED OUTPUT-2: 1 rows of 3 red LEDs (LS E6SF) for each channel (3x3) of Basic+ Mid End
 - JPLED3, JPLED6, JPLED9: Bypass to simulate a SLS fault on the LED3, LED6 and LED9 respectively

- › LED OUTPUT-3: 3 rows of 3 LEDs (LR G6SP) for the output of Basic+ Companion. The middle row is currently in use
 - SJ1 – SJ6: Close to create an LED matrix for high current applications

1 Board description

2 Quick start

3 Schematic and layout

Quick Start

- › Connect battery to VS_TAIL or VS_STOP and GND (e.g. 8V – 16V)
- › Supply the device(s) under test (JPVS)
- › Connect the device(s) to the Error network (JPERRN)
- › Select the output current (JPINSET_x)
- › Enable the device(s) and diagnosis (JPEN/DENx)
- › Select the desired fault management (JPDx, JPDS)
- › Select load, close OUT_JUMPER-x jumpers to use the on-board LEDs or leave open and connect external load to the connector OUTPUT
- › Activate outputs using PWM input (JPPWMIx)

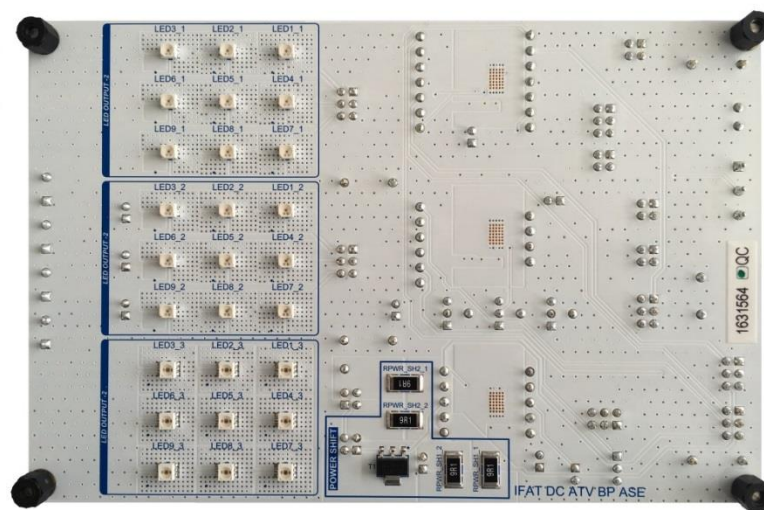
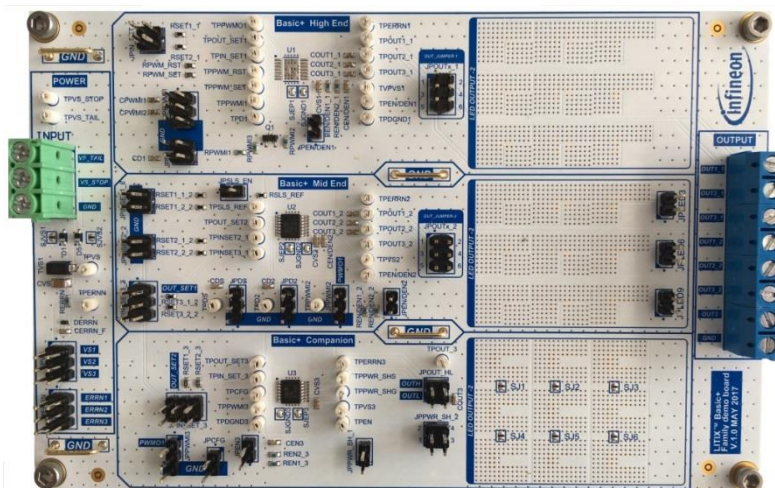
1 Board description

2 Quick start

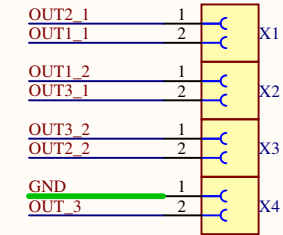
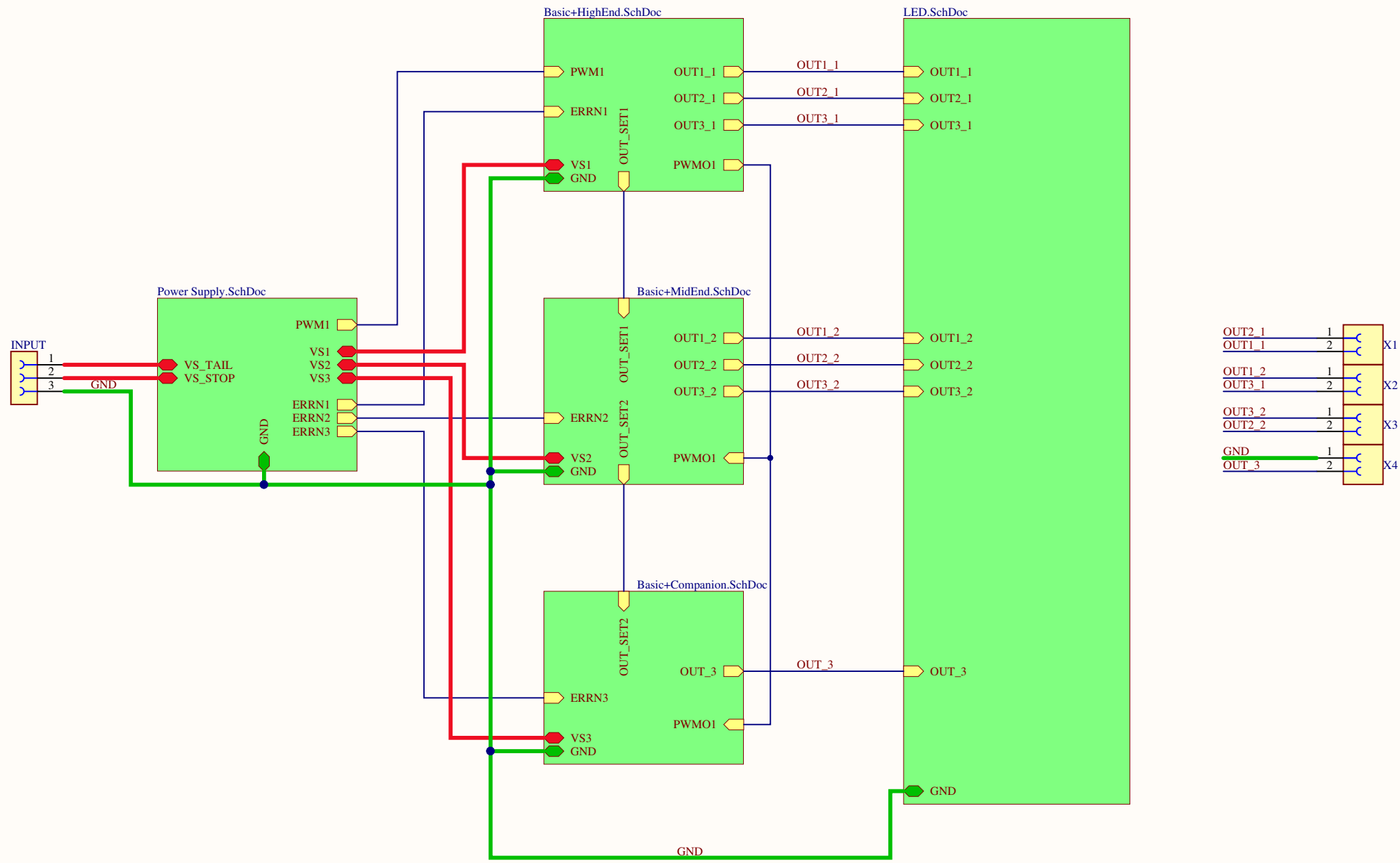
3 Schematic and layout

Schematic and board layout

- › The schematic and layout designs are shown on the following pages.
- › The visible content (names,...) can be activated or deactivated using the PDF reader layer settings.

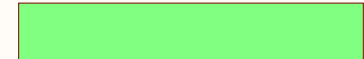



02_Top_Level.SchDoc



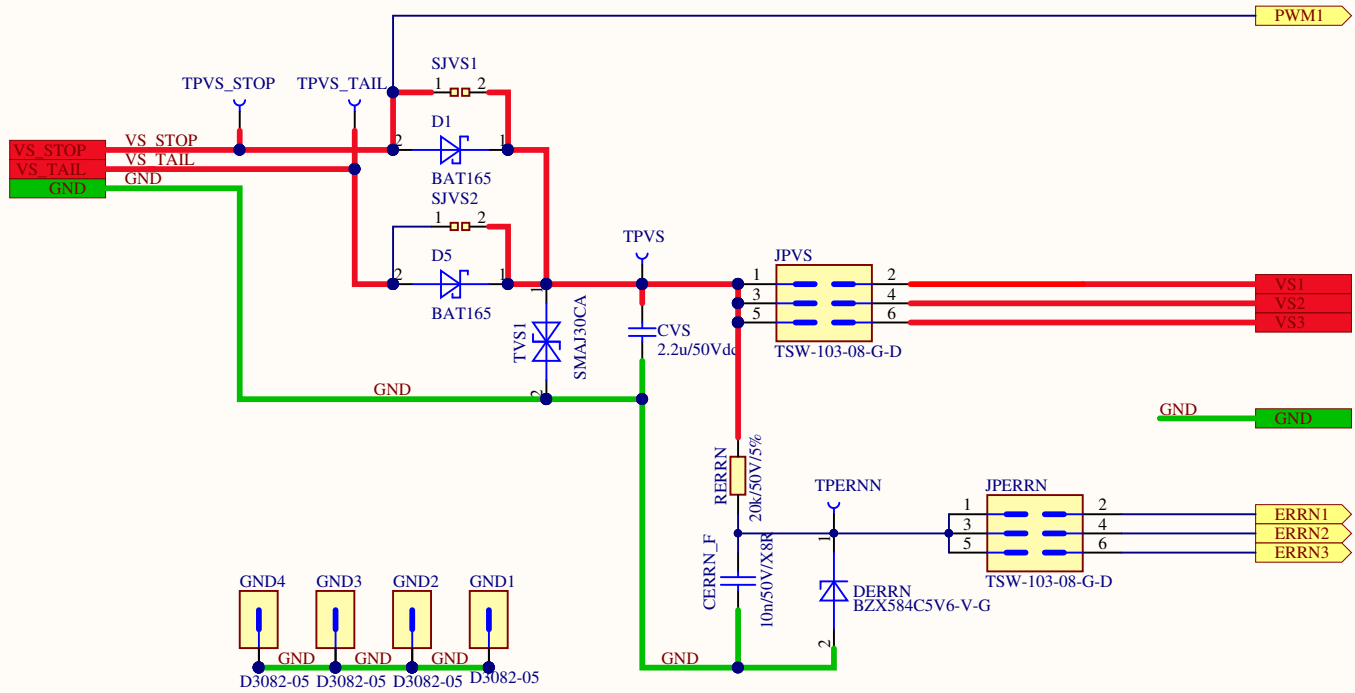
[Link to Miscellaneous Document](#)


Miscellaneous
Miscellaneous.SchDoc



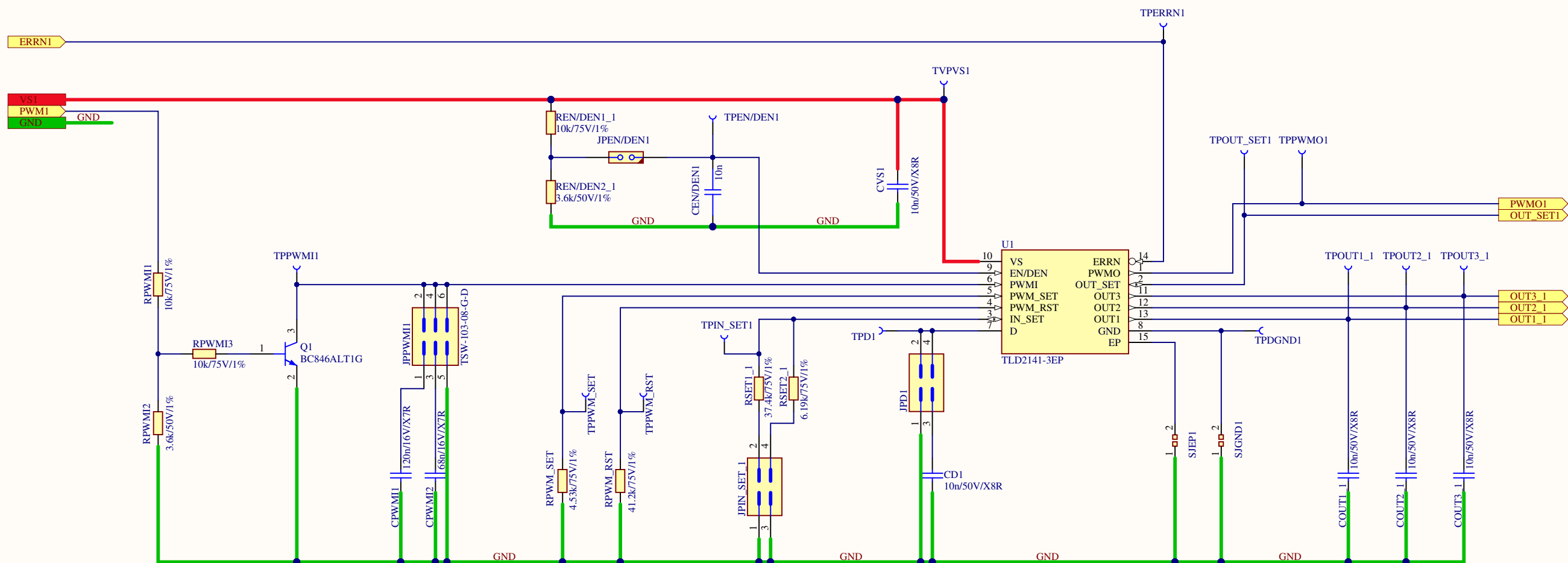
 Infineon Technologies Austria AG			
Title		LITIX™ Basic+ family board	
Variant		Default_Assembly	Approved <Appr.>
Size:	Document Name	Rel.	Rev.
A3	02_Top_Level.SchDoc	REL	V1.1.1
Author:			
Date: 19/2/2018		Time: 10:31:45 AM	
© Infineon Technologies AG 2015. All Rights Reserved.			Sheet 2 of 8


Power Supply.SchDoc

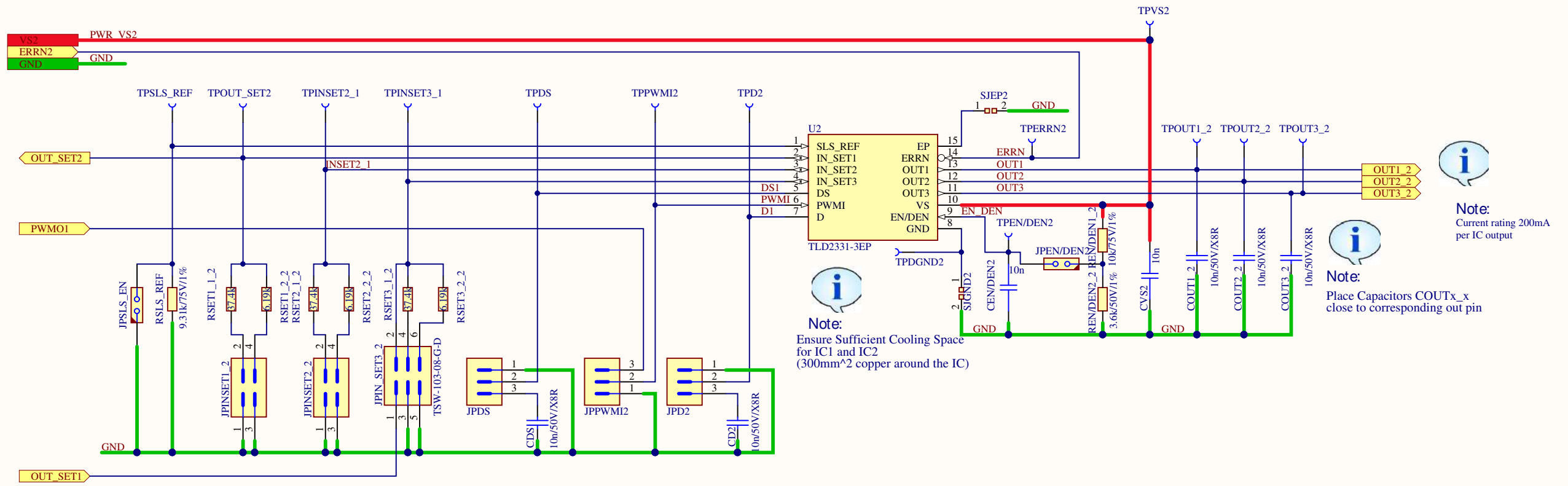


 Infineon Technologies Austria AG			
Title LITIX™ Basic+ family board			
Variant Default_Assembly			Approved <Appr.>
Size: A3	Document Name: Power Supply.SchDoc	Rel. REL	Rev. V1.1.1
Author:			
Date: 19/2/2018		Time: 10:31:45 AM	
© Infineon Technologies AG 2015. All Rights Reserved.			Sheet 3 of 8

Basic+HighEnd.SchDoc




 Infineon Technologies Austria AG			
Title: LITIX™ Basic+ family board			
Variant: Default_Assembly			Approved: <Appr.>
Size: A3	Document Name: Basic+HighEnd.SchDoc	Rel: REL	Rev: V1.1.1
Author:			
Date: 19/2/2018		Time: 10:31:46 AM	
© Infineon Technologies AG 2015. All Rights Reserved.			Sheet 4 of 8



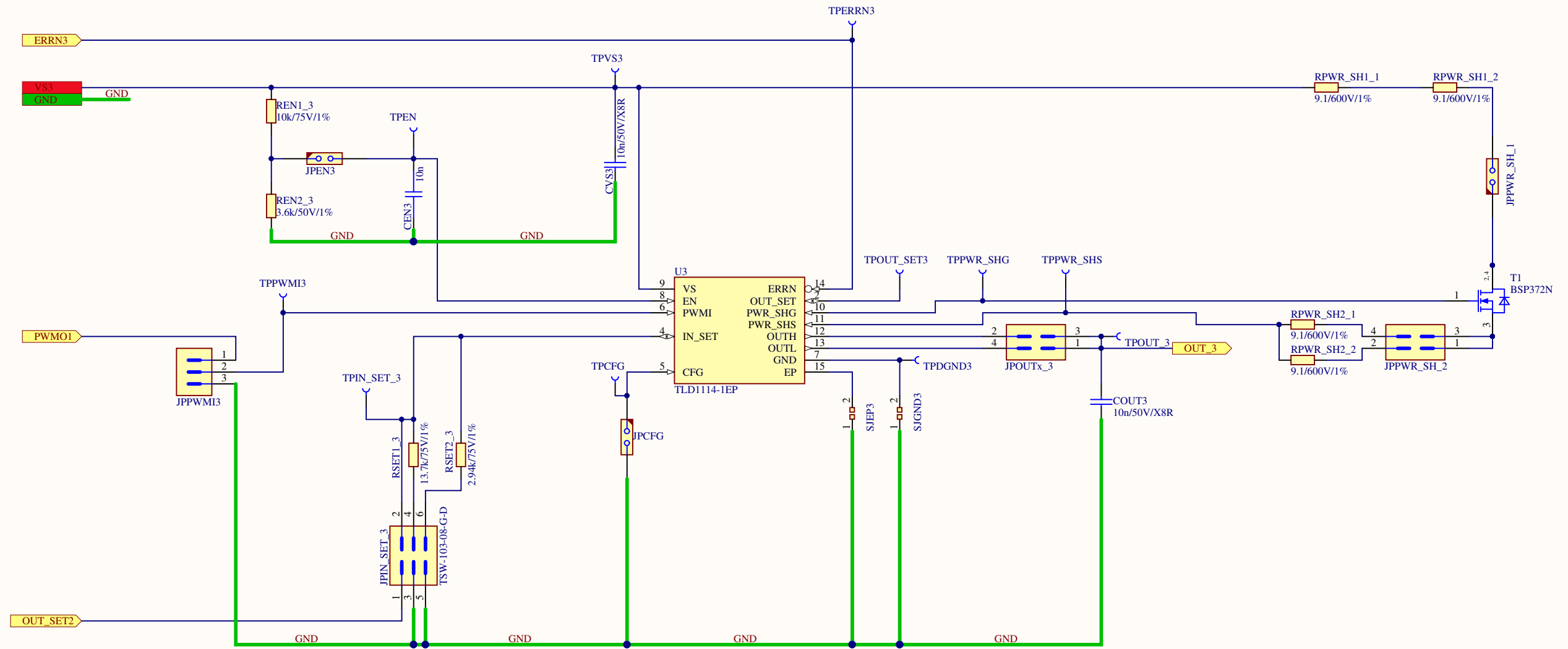
Note:
Ensure Sufficient Cooling Space for IC1 and IC2 (300mm² copper around the IC)


Note:
Current rating 200mA per IC output

Note:
Place Capacitors COUT_x_x close to corresponding out pin

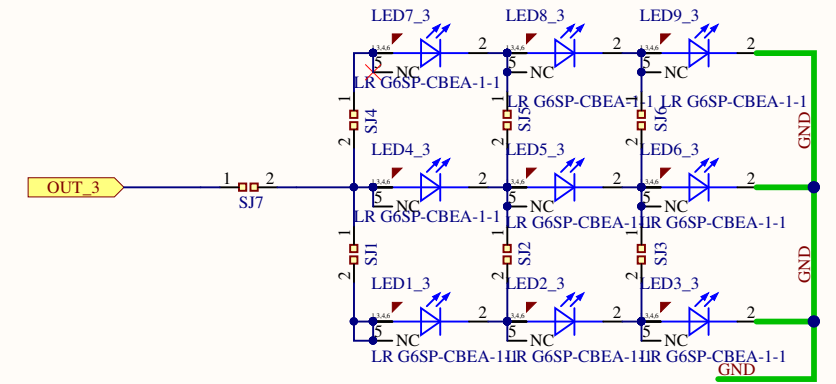
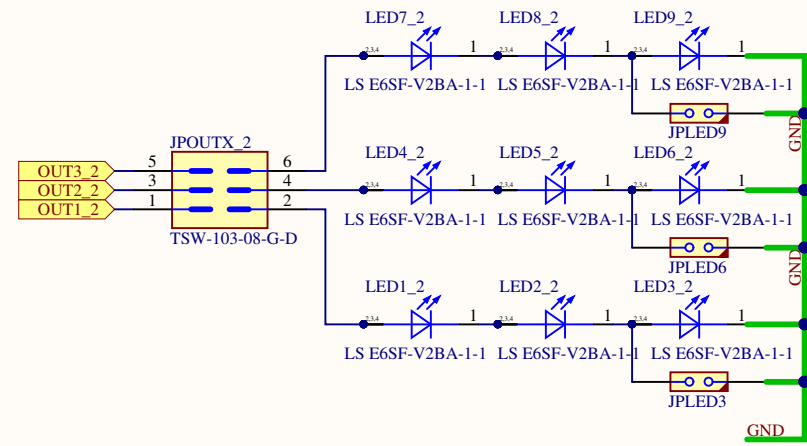
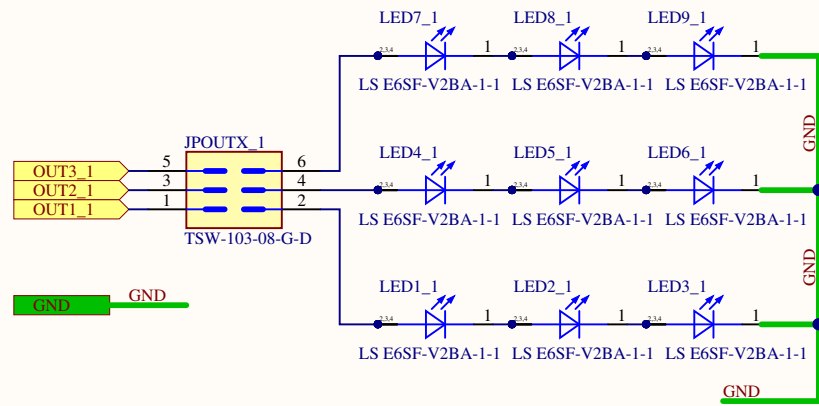
 Infineon Technologies Austria AG			
Title LITIX™ Basic+ family board			
Variant Default_Assembly			Approved <Appr.>
Size: A3	Document Name: Basic+MidEnd.SchDoc	Rel. REL	Rev. V1.1.1
Author:			
Date: 19/2/2018 Time: 10:31:46 AM			
© Infineon Technologies AG 2015. All Rights Reserved.			Sheet 5 of 8


Basic+Companion.SchDoc

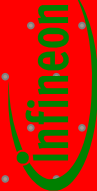


 Infineon Technologies Austria AG			
Title: LITIX™ Basic+ family board			
Variant: Default_Assembly			Approved: <Appr.>
Size: A3	Document Name: Basic+Companion.SchDoc	Rel: REL	Rev: V1.1.1
Author: _____			
Date: 19/2/2018 Time: 10:31:46 AM			
© Infineon Technologies AG 2015. All Rights Reserved.			Sheet 6 of 8

LED.SchDoc



 Infineon Technologies Austria AG			
Title LITIX™ Basic+ family board			
Variant Default_Assembly			Approved <Appr.>
Size: A3	Document Name: LED.SchDoc	Rel. REL	Rev. V1.1.1
Author:			
Date: 19/2/2018 Time: 10:31:47 AM			
© Infineon Technologies AG 2015. All Rights Reserved.			Sheet 7 of 8



GND

POWER

INPUT

VS_TAIL

VS_STOP

GND

VS1

VS2

VS3

ERRN1

ERRN2

ERRN3

GND

Basic+ High End

GND

Basic+ Mid End

GND

Basic+ Companion

GND

LED OUTx-1

LED OUTx-2

LED OUT-3

OUTPUT

OUT1_1

OUT2_1

OUT3_1

OUT1_2

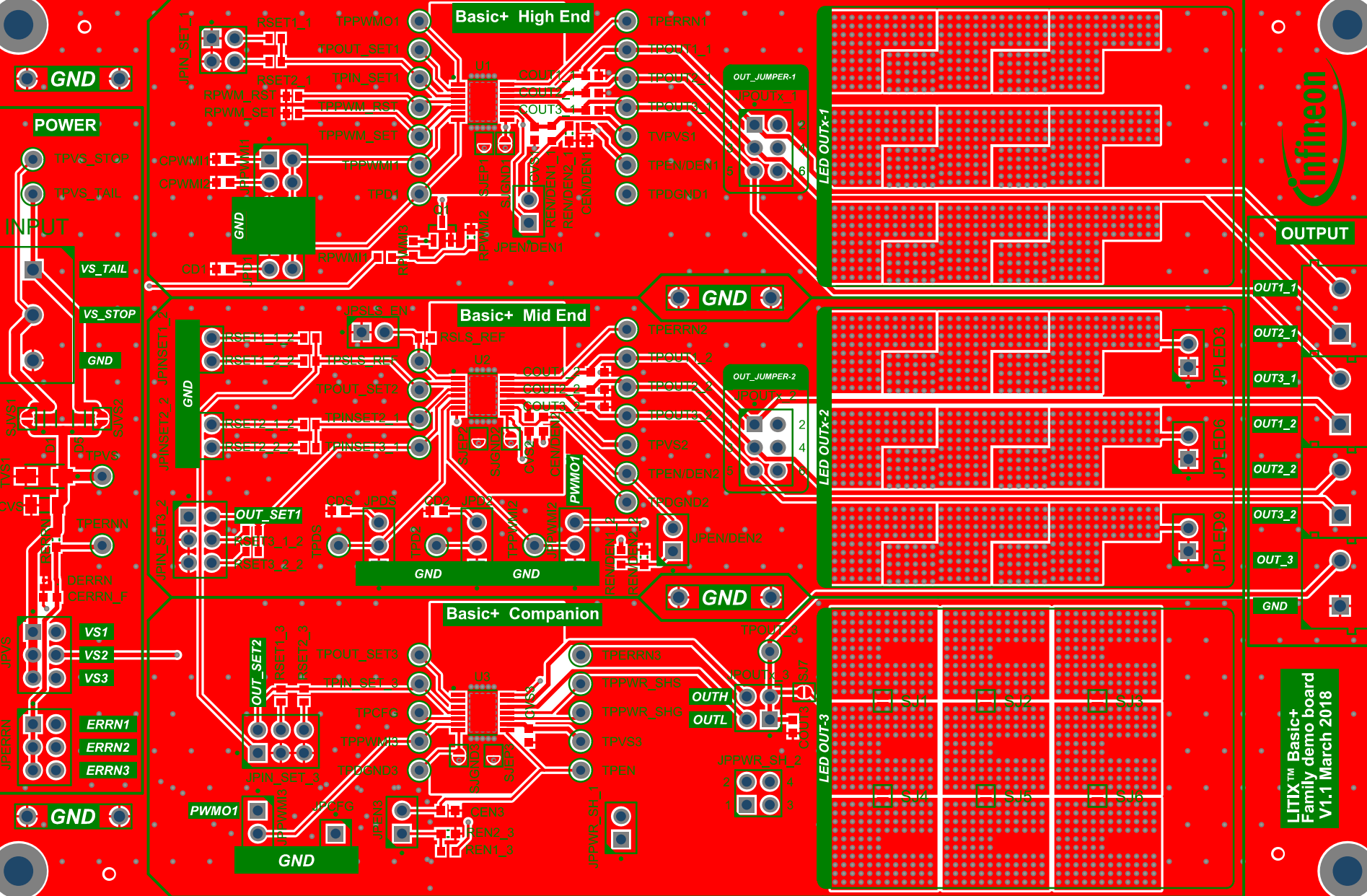
OUT2_2

OUT3_2

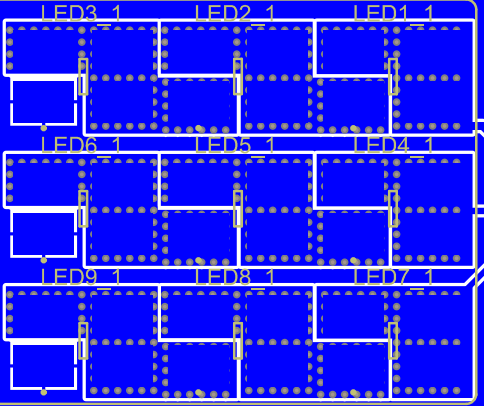
OUT_3

GND

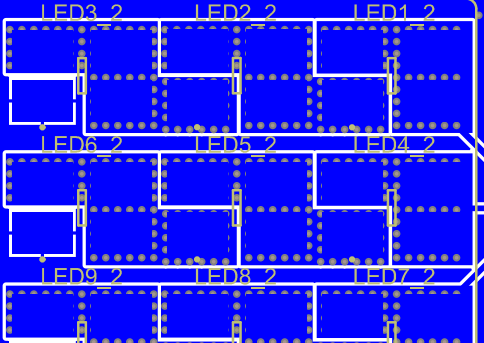
LITIX™ Basic+ Family demo board V1.1 March 2018



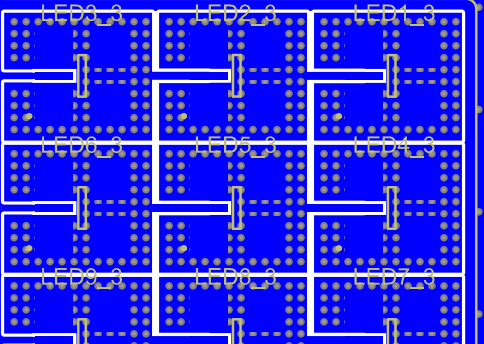
LED_OUTx-1



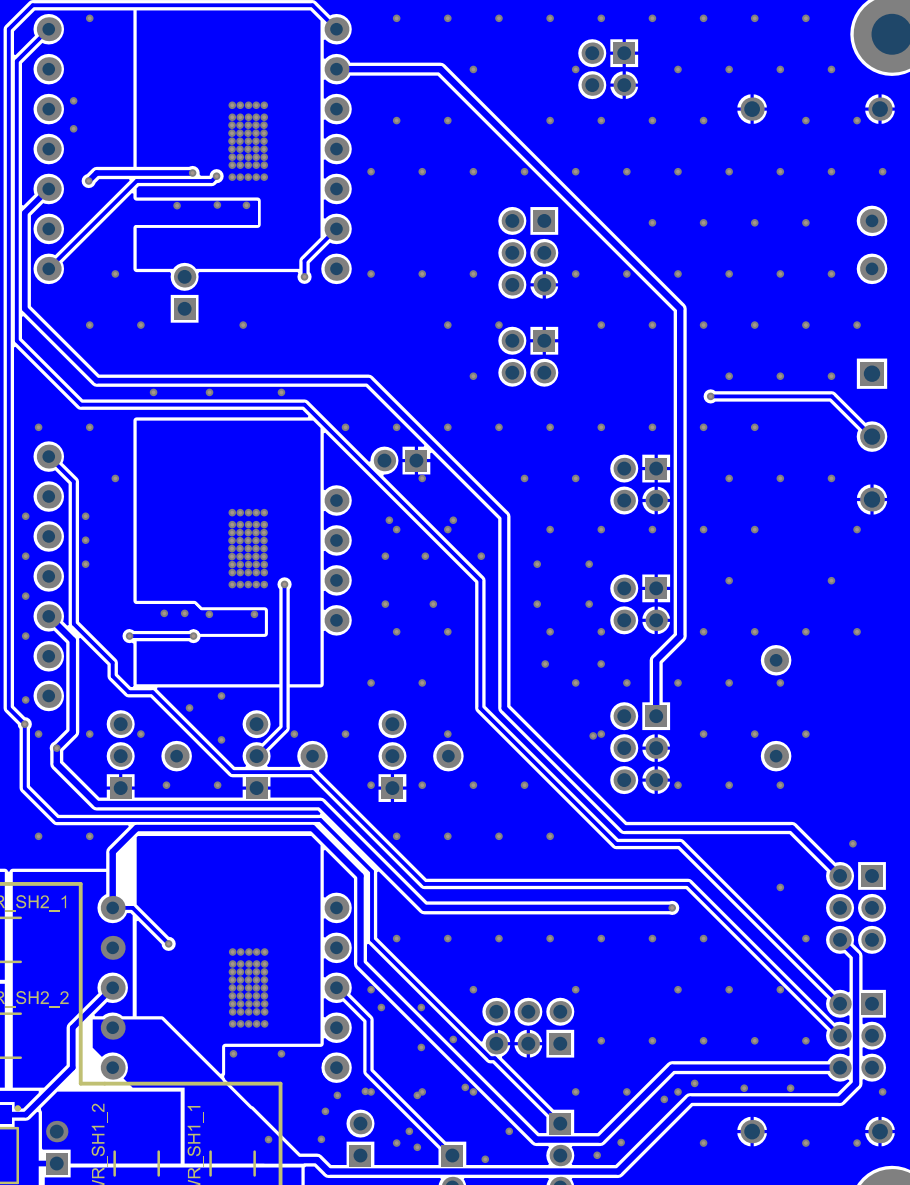
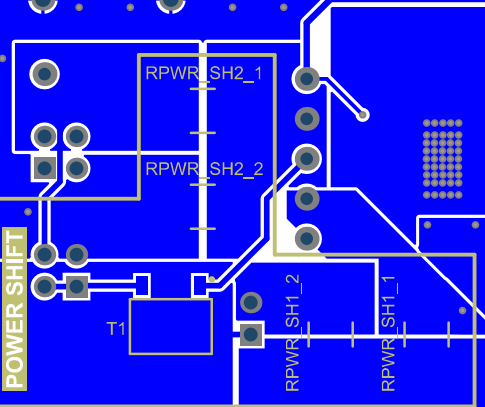
LED_OUTx-2



LED_OUT-3



POWER SHIFT



IFAT DC ATV BP ASE

Disclaimer

Edition 2018-03-28
Published by Infineon Technologies AG,
Am Campeon 1-8,
85579 Neubiberg, Germany
© Infineon Technologies AG 2018.
All Rights Reserved.

LEGAL DISCLAIMER:

THE INFORMATION GIVEN IN THIS DOCUMENT IS GIVEN AS A HINT FOR THE IMPLEMENTATION OF THE INFINEON TECHNOLOGIES COMPONENT ONLY AND SHALL NOT BE REGARDED AS ANY DESCRIPTION OR WARRANTY OF A CERTAIN FUNCTIONALITY, CONDITION OR QUALITY OF THE INFINEON TECHNOLOGIES COMPONENT. THE RECIPIENT OF THIS DOCUMENT MUST VERIFY ANY FUNCTION DESCRIBED HEREIN IN THE REAL APPLICATION. INFINEON TECHNOLOGIES HEREBY DISCLAIMS ANY AND ALL WARRANTIES AND LIABILITIES OF ANY KIND (INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS OF ANY THIRD PARTY) WITH RESPECT TO ANY AND ALL INFORMATION GIVEN IN THIS DOCUMENT.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office. Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.



Part of your life. Part of tomorrow.

