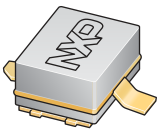


BLA1011-2

Avionics LDMOS transistor

Rev. 6 — 6 May 2013 **Product data sheet**

1. Product profile

1.1 General description

Silicon N-channel enhancement mode LDMOS transistor encapsulated in a 2-lead flangeless package (SOT538A) with a ceramic cap. The common source is connected to the mounting base.

Table 1. Typical performance

RF performance at Th = 25 °C in a common source test circuit.

Mode of operation	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)
Pulsed class-AB; t_p = 50 μs; δ = 2%	1030 to 1090	36	2	>16

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features and benefits

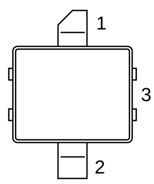
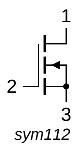
- High power gain
- Easy power control
- Excellent ruggedness
- Source on mounting base eliminates DC isolators, reducing common mode inductance.

1.3 Applications

- Avionics applications in the 1030 to 1090 MHz frequency range.

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source, connected to mounting base		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLA1011-2	-	ceramic surface mounted package; 2 leads	SOT538A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	75	V
V_{GS}	gate-source voltage		-	±15	V
I_D	drain current (DC)		-	2.2	A
P_{tot}	total power dissipation	$T_h \leq 25$ °C		10	W
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-mb)}$	thermal impedance from junction to mounting base	[1]	1	K/W
$R_{th(mb-h)}$	thermal resistance from mounting base to heatsink	[2]	6.5	K/W

[1] Thermal impedance is determined under RF operating conditions with pulsed bias and T_h = 25 °C.

[2] Typical value for mounting on PCB with 32 0.4 mm thermal vias with 20 μm tin plating and thermal compound between PCB and heatsink.

6. Characteristics

Table 6. Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 0.2 mA	75	-	-	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 20 mA	2	-	5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 26 V	-	-	0.1	mA
I_{DSX}	on-state drain current	$V_{GS} = V_{GSth}$ + 9 V; V_{DS} = 10 V	2.8	-	-	A
I_{GSS}	gate leakage current	V_{GS} = ±15 V; V_{DS} = 0	-	-	40	nA

Table 6. Characteristics *...continued*

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 0.75 A	-	0.5	-	S
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 0.75 A	-	1.2	-	Ω
C_{is}	input capacitance	V_{GS} = 0 V; V_{DS} = 26 V; f = 1 MHz	-	11	-	pF
C_{os}	output capacitance	V_{GS} = 0 V; V_{DS} = 26 V; f = 1 MHz	-	9	-	pF
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 26 V; f = 1 MHz	-	0.5	-	pF

7. Application information

Table 7. RF performance in a common source class-AB circuit

T_h = 25 °C; $R_{th\ mb-h}$ = 6.5 K/W unless otherwise specified.

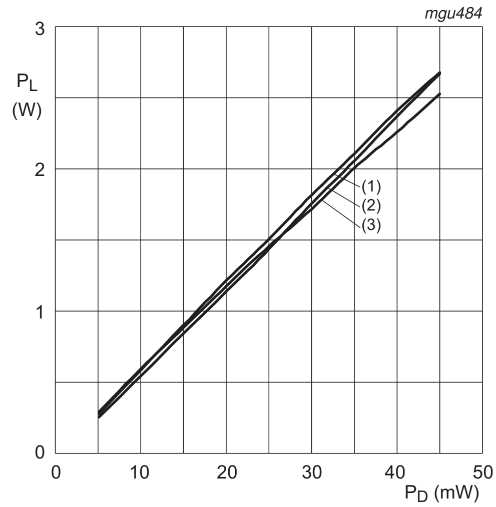
Mode of operation	f	V_{DS}	I_{DQ}	P_L	G_p	t_r	t_f	Pulse droop
	(MHz)	(V)	(mA)	(W)	(dB)	(ns)	(ns)	(dB)
Pulsed class-AB; t_p = 50 μs; δ = 2%	1030 to 1090	36	50	2	>16	<15	<15	<0.5

7.1 Ruggedness in class-AB operation

The BLA1011-2 is capable of withstanding a load mismatch corresponding to VSWR = 5 : 1 through all phases under the operating conditions.

Table 8. Typical impedance values

Frequency	Z_S	Z_L
(MHz)	(Ω)	(Ω)
1030	1.51 + j 11.76	6.9 + j 5
1060	1.51 + j 11.26	6.7 + j 5.9
1090	1.52 + j 10.77	5.1 + j 6.6



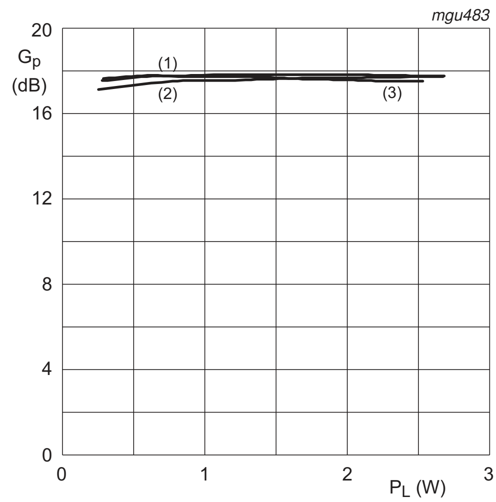
T_h = 25 °C; V_{DS} = 36 V; I_{DQ} = 50 mA; class-AB; t_p = 50 µs; δ = 2%.

(1) f = 1060 MHz.

(2) f = 1030 MHz.

(3) f = 1090 MHz.

Fig 1. Load power as a function of drive power; typical values.



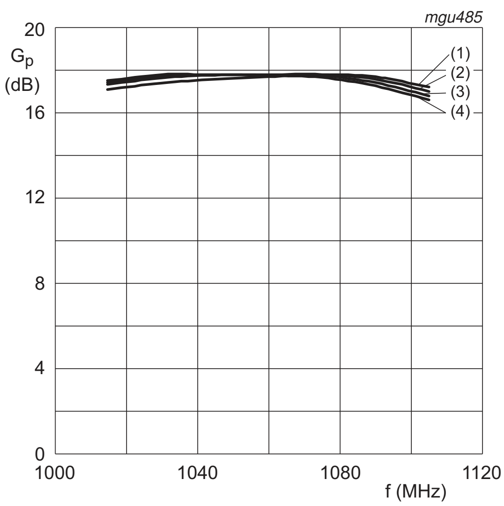
T_h = 25 °C; V_{DS} = 36 V; I_{DQ} = 50 mA; class-AB; t_p = 50 µs; δ = 2%.

(1) f = 1060 MHz.

(2) f = 1030 MHz.

(3) f = 1090 MHz.

Fig 2. Power gain as a function of load power; typical values.



T_h = 25 °C; V_{DS} = 36 V; I_{DQ} = 50 mA; class-AB; t_p = 50 µs; δ = 2%.

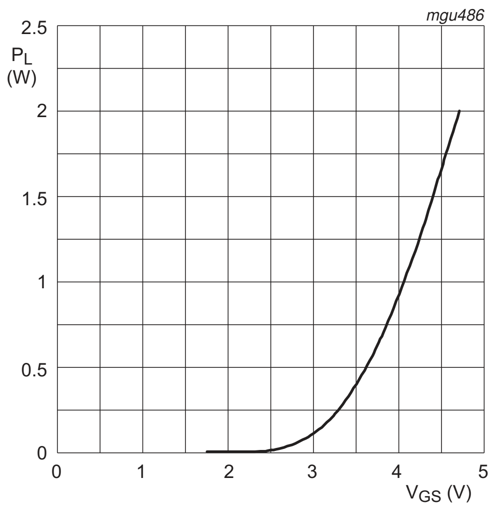
(1) P_L = 1 W.

(2) P_L = 2 W.

(3) P_L = 3 W.

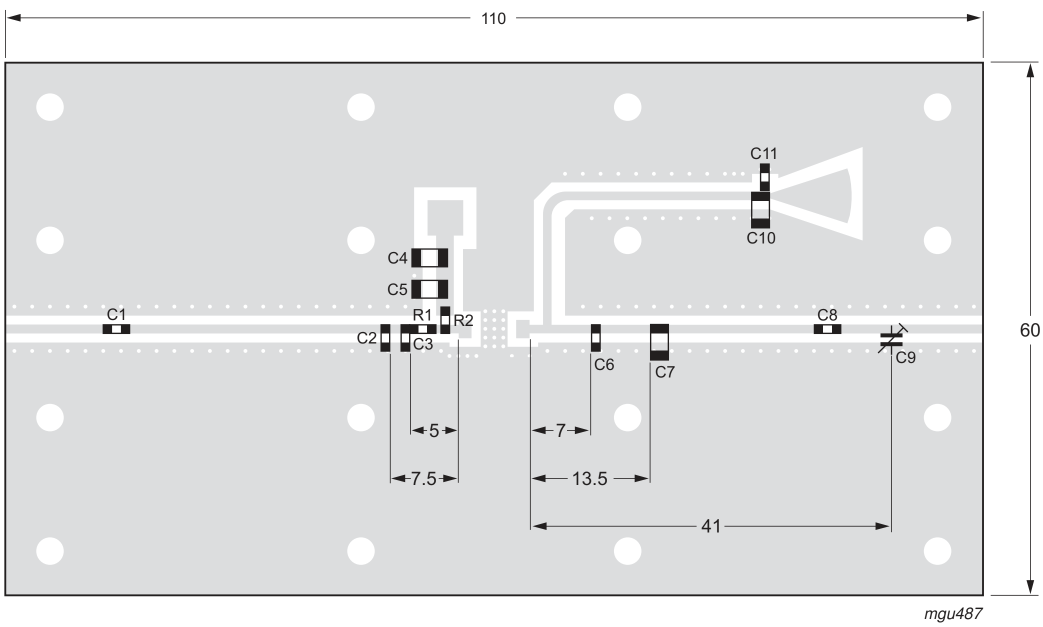
(4) P_L = 4 W.

Fig 3. Power gain as a function of frequency; typical values.



T_h = 25 °C; V_{DS} = 36 V; I_{DQ} = 50 mA; class-AB; f = 1090 MHz; t_p = 50 µs; δ = 2%.

Fig 4. Load power as a function of gate-source voltage; typical values.



Dimensions in mm.

The components are situated on one side of the Rogers 6006 printed-circuit board (thickness = 0.64 mm; ε_r = 6.2), the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through-metallization.

Fig 5. Printed-circuit board for class-AB test circuit.

8. Test information

Table 9. List of components for class-AB test circuit

(see Figure 5)

Component	Description		Value
C1, C8	multilayer ceramic chip capacitor	[1]	56 pF
C2	multilayer ceramic chip capacitor	[1]	7.5 pF
C3	multilayer ceramic chip capacitor	[1]	1.8 pF
C4, C10	multilayer ceramic chip capacitor	[2]	20 nF
C5	multilayer ceramic chip capacitor	[3]	33 pF
C6	multilayer ceramic chip capacitor	[1]	5.6 pF
C7	multilayer ceramic chip capacitor	[3]	6.2 pF
C9	tekelec trimmer; type 37283		0.4 to 2.5 pF
C11	multilayer ceramic chip capacitor	[1]	33 pF
R1	SMD resistor		2.2 Ω (2 in parallel)
R2	SMD resistor		22 Ω

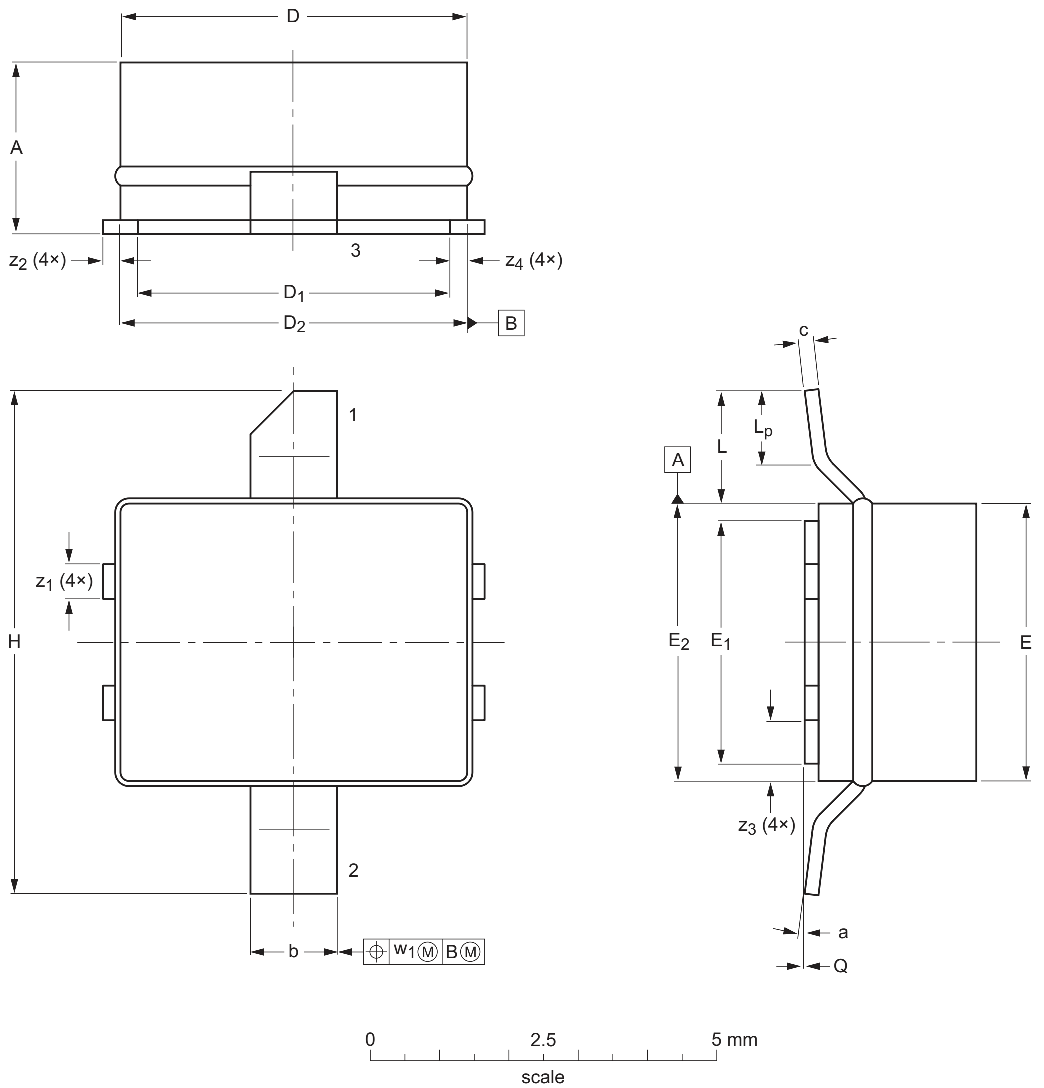
[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 200B or capacitor of same quality.

[3] American Technical Ceramics type 100B or capacitor of same quality.

9. Package outline

Ceramic surface-mounted package; 2 leads **SOT538A**



Dimensions (mm are the original dimensions)

Unit		A	b	c	D	D_1	D_2	E	E_1	E_2	H	L	L_p	Q	w_1	z_1	z_2	z_3	z_4	θ
mm	max	2.34	1.35	0.23	5.16	4.65	5.16	4.14	3.63	4.14	7.49	2.03	1.02	0.1		0.58	0.25	0.97	0.51	7°
	nom														0.25					
	min	2.13	1.19	0.18	5.00	4.50	5.00	3.99	3.48	3.99	7.24	1.27	0.51	0.0		0.43	0.18	0.81	0.00	0°

sot538a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT538A						~~06-03-16~~ 13-02-07

Fig 6. Package outline SOT538A

10. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLA1011-2 v.6	20130506	Product data sheet	-	BLA1011-2 v.5
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Package outline drawings have been updated to the latest version.			
BLA1011-2 v.5	20031119	Product specification	-	BLA1011-2 v.4

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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13. Contents

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