M100PFSEVP Hardware Manual

Release 1

Diana Korchmar

April 08, 2021

CONTENTS:

CHAPTER

ONE

ABOUT THIS MANUAL

1.1 Imprint

Adress:

ARIES Embedded GmbH

Schöngeisinger Str. 84

D-82256 Fürstenfedbruck

Germany

Phone:

+49 (0) 8141/36 367-0

Fax:

+49 (0) 8141/36 367-67

1.2 Disclaimer

ARIES Embedded does not guarantee that the information in this document is up-to-date, correct, complete or of good quality. Liability claims against ARIES Embedded, referring to material or non-material related damages caused, due to usage or non-usage of the information given in this document, or due to usage of erroneous or incomplete information, are exempted, as long as there is no proven intentional or negligent fault of ARIES Embedded. ARIES Embedded explicitly reserves the rights to change or add to the contents of this Preliminary User's Manual or parts of it without notification.

1.3 Copyright

1.4 Registered Trademarks

1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

1.6 Change Log

Revision	Date	Revised	Comment
1.0	08.04.2021	dk	Initial creation

CHAPTER

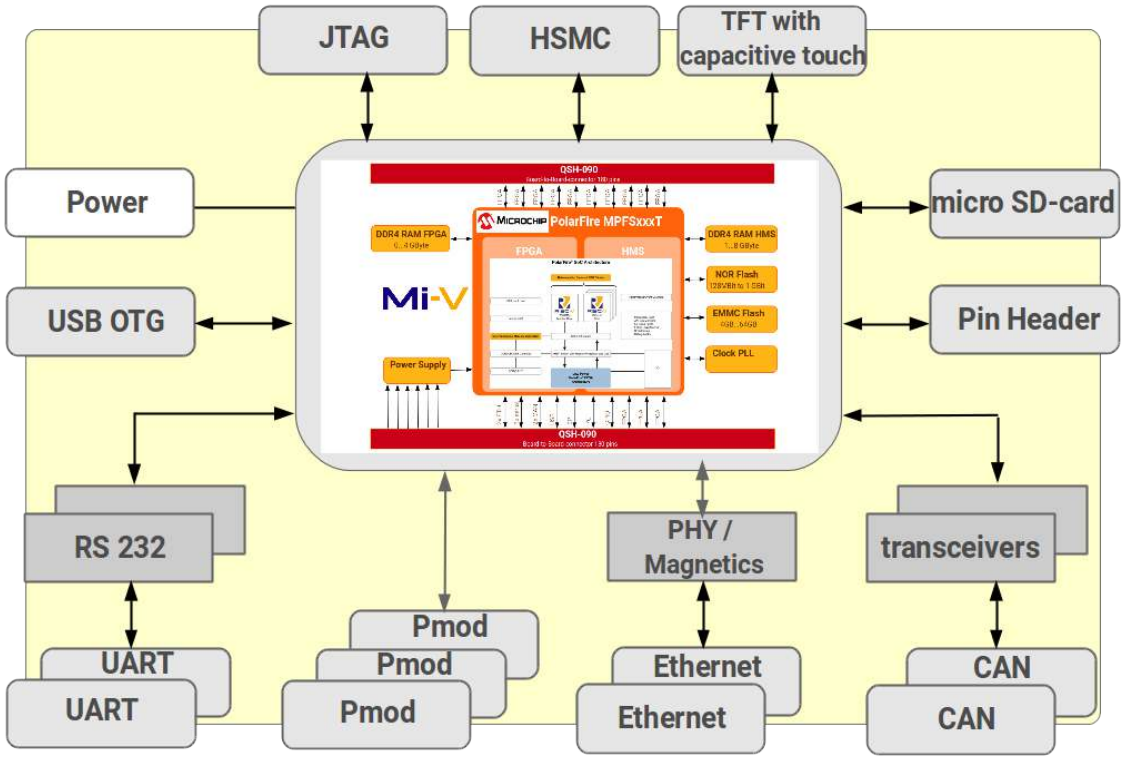
TWO

OVERVIEW

M100PFSEVP represents the flexible Evaluation Platform for working with the M100PFS SoM for PolarFire FPGAs.

The system helps developers to have a smooth start with the M100PFS SoMs, it can be used for designing IP, developing software as well as implementing prototypes.

2.1 Block Diagram

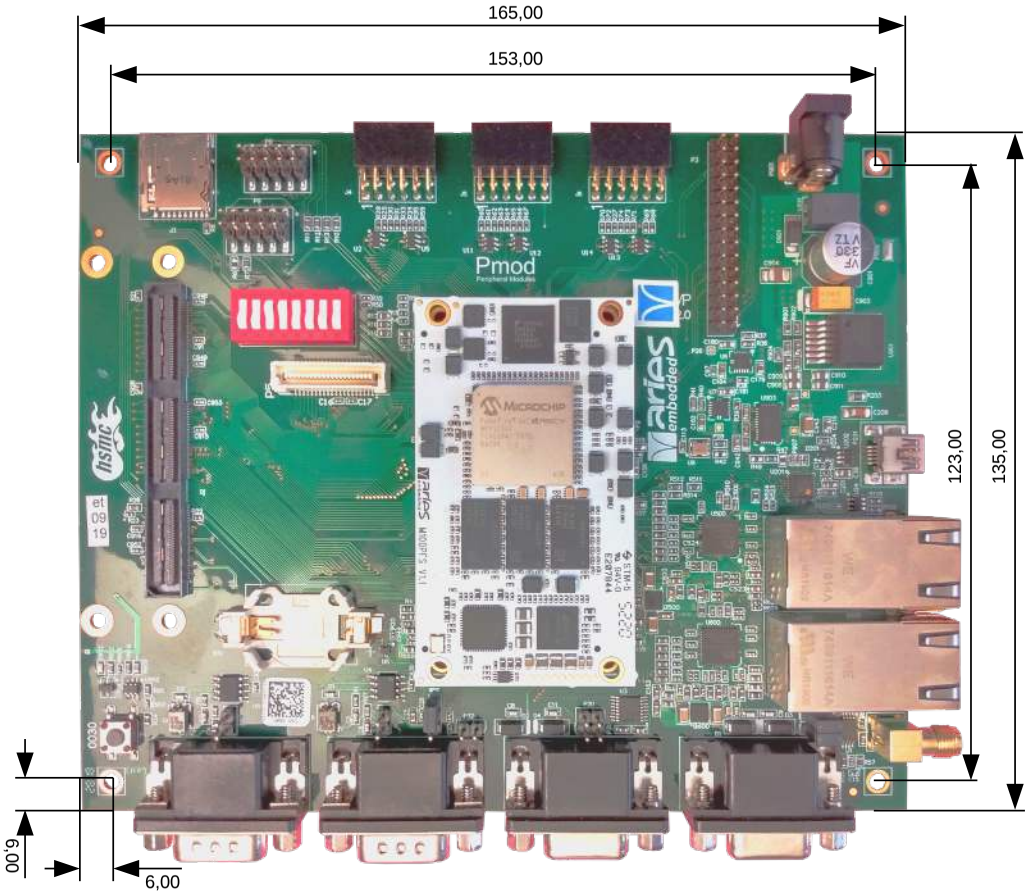


2.2 Feature Set

For supporting development projects and fast prototyping in the best possible way M100PFEVP supplies:

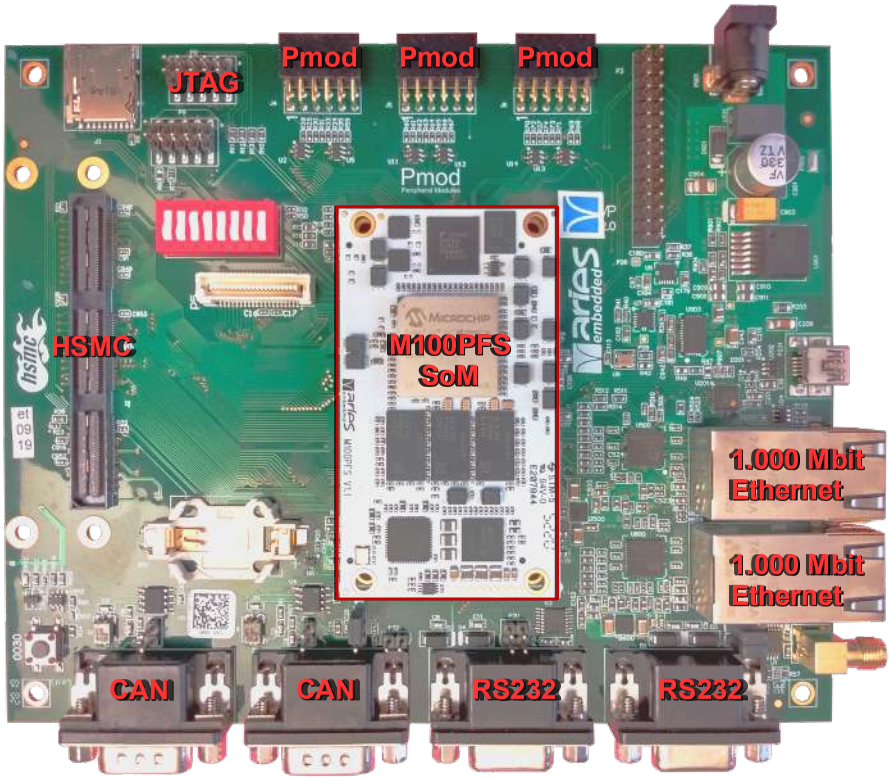
- 2x Gigabit Ethernet on a RJ45 connector
- USB on a mini-USB connector
- 2x UART on a DUSB-9 connector each
- 2x CAN on a DUSB-9 connector each
- TFT with Touch
- HSMC extension connector
- 3x PMOD extension connectors
- microSD-card slot
- JTAG pin header
- flexible supply voltage 7V to 36V DC

2.3 Dimensions



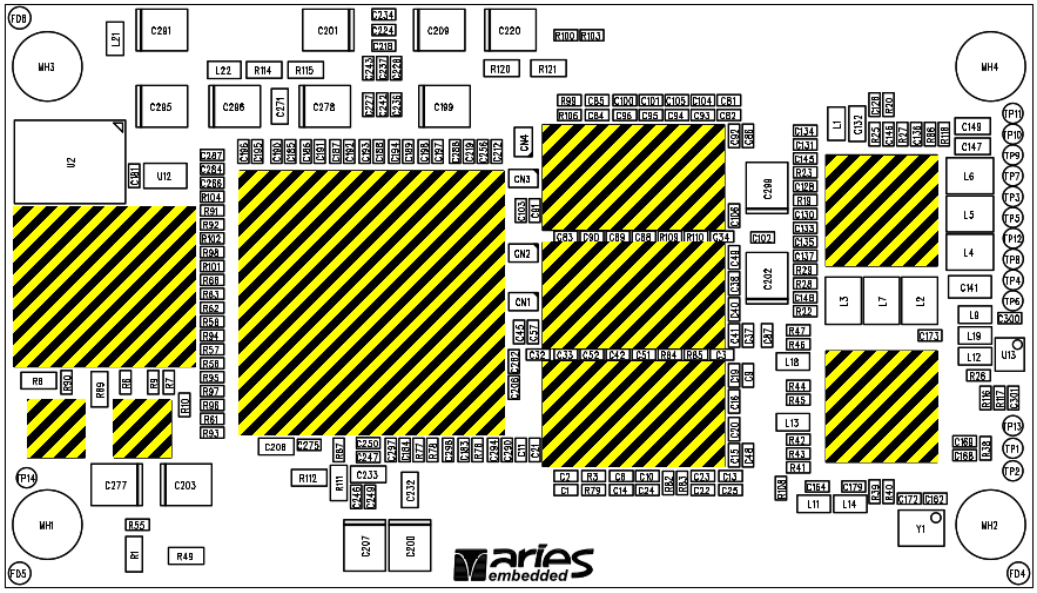
2.4 Parts Location

The available functional blocks can be found on the baseboard as follows:



2.5 Handling Recommendations

The populated Samtec connectors require certain mechanical force to insert the SoM into its mating baseboard connectors. To avoid mechanical damage to the components populated on M100PFS it is strongly recommended not to apply mechanical force on the Ball Grid Array (BGA) components. The BGA components are marked as shaded in the figure below:



CHAPTER

THREE

RESOURCES

3.1 Ethernet

M100PFSEVP offers two Ethernet Ports in RGMII mode to be controlled by the PolarFire FPGA. These ports can be accessed via the RJ45 connectors P500 and P600 supported by Microchip KSZ903 Ethernet physical-layer transceivers.

3.2 UART

Two UARTs are available on a RS232 signal level.

The interface jumpers can be set vertical or horizontal so that the interface complies with straight- or cross-type RS232 cables. The following table shows the signal for horizontal jumper setting, in case of vertical jumper settings RX and TX signals are swapped accordingly.

3.2.1 UART 1 (P21)

Pin	Function	FPGA Pin	Connector	Component MSS/FPGA
2	UART0_TX	E3	J2-C 132	MSS_IO36
3	UART0_RX	A3	J2-C 138	MSS_IO35
5	GND			

3.2.2 UART 2 (P22)

Pin	Function	FPGA Pin	Connector	Component MSS/FPGA
2	TXD2	E14	J1-B 75	GPIO9NB1
3	RXD2	B14	J1-B 77	GPIO3NB1
5	GND			

3.3 USB-OTG

M100PFSEVP supports an USB-OTG port. The Microchip USB3320 USB-OTG Phy drives the physical connection. The respective connector on M100PFSEVP can be found at position P201.

Function	FPGA	Connector	Component MSS
USB_DIR	F1	J2-81	MSS_IO15
USB_CLK	G2	J2-83	MSS_IO14
USB_D4	D1	J2-85	MSS_IO22
USB_D1	E1	J2-87	MSS_IO19
USB_STP	G4	J2-95	MSS_IO17
USB_D3	F5	J2-99	MSS_IO21
USB_D6	F6	J2-82	MSS_IO24
USB_D7	F3	J2-84	MSS_IO25
USB_D5	D2	J2-86	MSS_IO23
USB_NXT	G5	J2-88	MSS_IO16
USB_D2	G3	J2-98	MSS_IO20
USB_D0	F2	J2-100	MSS_IO18

3.4 CAN

Two CAN ports are available on M100PFSEVP. The signals on the DSUB connector can optionally be terminated by 120 Ohms. This is done by setting the jumpers at position P19 and P20.

Function	FPGA	Connector	Component MSS
CAN0_TX	B4	J2-129	MSS_IO31
CAN0_RX	B2	J2-137	MSS_IO32
CAN1_TX	D3	J2-135	MSS_IO28
CAN1_RX	B5	J2-130	MSS_IO29

3.4.1 CAN1 (P23)

Pin	Function
2	CAN-L
3	GND
7	CAN-H

3.4.2 CAN2 (P24)

Pin	Function
2	CAN-L
3	GND
7	CAN-H

3.5 JTAG (P8)

P8 provides the JTAG signals of the FPGA to the outer world. The JTAG connector complies with the standard pinout, the FlashPro5 can be directly connected. The following signals are available:

Pin	Function	FPGA Pin	Connector
1	TCK	E9	P1-6
3	TDO	E8	P1-4
5	TMS	F8	P1-10
7	–	–	–
9	TDI	G9	P1-8
2	GND	–	–
4	3.3V	–	–
6	–	–	–
8	–	–	–
10	GND	–	–

3.6 Pmod Module Connectors

Three 2x6 angled pin headers are available on the M100PFSEVP board which fit the requirements for Pmod modules. To support a wider range of possible modules, each connector has its own level shifter. A corresponding jumper allows the selection between 3.3V or 5V module voltage.

3.6.1 Pmod J4:

Pin	Function	Connector	Component FPGS	FPGA Pin
1	IOB4A16	P1-120	GPIO_D12	D12
2	IOB4A44	P1-133	GPIO_E13	E13
3	IOB4A52	P1-115	GPIO_H12	H12
4	HPS_GPIO37	P2-70	GPIO_B19	B19
5	GND	–	–	–
6	3.3V	–	–	
7	IOB4A17	P1-118	GPIO_E11	E11
8	IOB4A45	P1-131	GPIO_F13	F13
9	IOB4A53	P1-113	GPIO_G12	G12
10	HPS_GPIO44	P2-71	GPIO_B20	B20
11	GND	–	–	–
12	3.3V	–	–	–

3.6.2 Pmod J5:

Pin	Function	Connector	Component FPGS	FPGA Pin
1	HPS_GPIO48	P2-136	GPIO_C20	C20
2	IOB5A6	P1-162	GPIO_G13	G13
3	IOB8A3	P1-15	LPRB_B	C15
4	IOB8A2	P2-17	LPRB_A	C14
5	GND	–	–	–
6	3.3V	–	–	
7	HPS_GPIO63	P2-127	GPIO_C19	C19
8	HPS_GPIO64	P2-121	GPIO_A21	A21
9	HPS_GPIO65	P2-128	GPIO_B22	B22
10	HPS_GPIO66	P2-123	GPIO_A20	A20
11	GND	–	–	–
12	3.3V	–	–	–

3.6.3 Pmod J6:

Note: Pmod J6 is not supported by the current version of the M100PFS SoM.

Pin	Function	Connector	Component FPGS	FPGA Pin
1	HPS_GPIO26	P2-93	–	–
2	HPS_GPIO27	P2-80	–	–
3	HPS_GPIO21	P2-90	–	–
4	HPS_GPIO20	P2-97	–	–
5	GND	–	–	–
6	3.3V	–	–	
7	HPS_GPIO58	P2-125	–	–
8	HPS_GPIO59	P2-122	–	–
9	HPS_GPIO60	P2-133	–	–
10	HPS_GPIO19	P2-94	–	–
11	GND	–	–	–
12	3.3V	–	–	–

3.7 HSMC Connector (J2)

M100PFSEVP hosts a High Speed Mezzanine Card (HSMC) connector. Its pinout is shown in the following table.

Function	Connector	FPGA	Pin	Pin	FPGA	Connector	Function
–	–	–	1	2	–	–	–
–	–	–	3	4	–	–	–
GND	–	–	5	6	–	–	GND
–	–	–	7	8	–	–	–
–	–	–	9	10	–	–	–
GND	–	–	11	12	–	–	GND
GXB_TX_L5_P	P2-40	M7	13	14	K6	P2-34	GXB_RX_L5_P
GXB_TX_L5_N	P2-42	M8	15	16	K7	P2-36	GXB_RX_L5_N
GND	–	–	17	18	–	–	GND

Continued on next page

Table 3.1 – continued from previous page

Function	Connector	FPGA	Pin	Pin	FPGA	Connector	Function
GXB_TX_L4_P	P2-28	N6	19	20	L5	P2-22	GXB_RX_L4_P
GXB_TX_L4_N	P2-30	N7	21	22	L6	P2-24	GXB_RX_L4_N
GND	–	–	23	24	–	–	GND
GXB_TX_L3_P	P2-16	T22	25	26	R20	P2-10	GXB_RX_L3_P
GXB_TX_L3_N	P2-18	T21	27	28	R19	P2-12	GXB_RX_L3_N
GND	–	–	29	30	–	–	GND
GXB_TX_L2_P	P2-39	P22	31	32	M22	P2-33	GXB_RX_L2_P
GXB_TX_L2_N	P2-41	P21	33	34	M21	P2-35	GXB_RX_L2_N
GND	–	–	35	36	–	–	GND
GXB_TX_L1_P	P2-27	H22	37	38	K22	P2-21	GXB_RX_L1_P
GXB_TX_L1_N	P2-29	H21	39	40	K21	P2-23	GXB_RX_L1_N
GND	–	–	41	42	–	–	GND
GXB_TX_L0_P	P2-15	F22	43	44	G20	P2-9	GXB_RX_L0_P
GXB_TX_L0_N	P2-17	F21	45	46	G19	P2-11	GXB_RX_L0_N
GND	–	–	47	48	–	–	GND
HPS_GPIO51	P2-134	D20	49	50	D21	P2-131	HPS_GPIO52
TCK	P1-6	E9	51	52	F8	P1-10	TMS
GND	–	–	53	54	–	–	GND
HSMC_TDO	–	–	55	56	–	–	HSMC_TDI
CLK25_HSMC	–	–	57	58	–	–	–
GND	–	–	59	60	–	–	GND
IOB4A11	P1-132	–	61	62	–	P1-156	IOB4A0/CLK3p
IOB4A10	P1-134	–	63	64	–	P1-154	IOB4A1/CLK3n
3.3V	–	–	65	66	–	–	VIN
IOB4A28	P1-94	–	67	68	–	P1-152	IOB4A2
IOB4A29	P1-92	–	69	70	–	P1-150	IOB4A3
3.3V	–	–	71	72	–	–	VIN
IOB4A30	P1-90	–	73	74	–	P1-148	IOB4A4
IOB4A31	P1-88	–	75	76	–	P1-146	IOB4A5
3.3V	–	–	77	78	–	–	VIN
IOB4A32	P1-84	–	79	80	–	P1-144	IOB4A6
IOB4A33	P1-82	–	81	82	–	P1-142	IOB4A7
3.3V	–	–	83	84	–	–	VIN
IOB4A40	P1-143	–	85	86	–	P1-136	IOB4A9
IOB4A41	P1-141	–	87	88	–	P1-138	IOB4A8
3.3V	–	–	89	90	–	–	VIN
IOB4A42	P1-137	–	91	92	–	P1-128	IOB4A13
IOB4A43	P1-135	–	93	94	–	P1-130	IOB4A12
3.3V	–	–	95	96	–	–	VIN
IOB4A48	P1-125	–	97	98	–	P1-124	IOB4A15
IOB4A49	P1-123	–	99	100	–	P1-126	IOB4A14
3.3V	–	–	101	102	–	–	VIN
IOB4A50	P1-119	–	103	104	–	P1-116	IOB4A18
IOB4A51	P1-117	–	105	106	–	P1-114	IOB4A19
3.3V	–	–	107	108	–	–	VIN
IOB4A54	P1-111	–	109	110	–	P1-21	IOB8A0
IOB4A55	P1-109	–	111	112	–	P1-19	IOB8A1
3.3V	–	–	113	114	–	–	VIN
CLKEXT_P	P2-160	–	115	116	L20	P2-3	REFCLK0L_P

Continued on next page

Table 3.1 – continued from previous page

Function	Connector	FPGA	Pin	Pin	FPGA	Connector	Function
CLKEXT_N	P2-162	–	117	118	L19	P2-5	REFCLK0L_N
3.3V	–	–	119	120	–	–	VIN
IOB4A56	P1-107	–	121	122	–	P1-108	IOB4A22
IOB4A57	P1-105	–	123	124	–	P1-106	IOB4A23
3.3V	–	–	125	126	–	–	VIN
IOB4A58	P1-101	–	127	128	–	P1-102	IOB4A24
IOB4A59	P1-99	–	129	130	–	P1-100	IOB4A25
3.3V	–	–	131	132	–	–	VIN
IOB4A62	P1-93	–	133	134	–	P1-98	IOB4A26
IOB4A63	P1-91	–	135	136	–	P1-96	IOB4A27
3.3V	–	–	137	138	–	–	VIN
IOB4A64	P1-89	–	139	140	–	P1-155	IOB4A34
IOB4A65	P1-87	–	141	142	–	P1-153	IOB4A35
3.3V	–	–	143	144	–	–	VIN
IOB4A66	P1-83	–	145	146	–	P1-151	IOB4A36
IOB4A67	P1-81	–	147	148	–	P1-149	IOB4A37
3.3V	–	–	149	150	–	–	VIN
IOB3B24	P1-59	–	151	152	–	P1-147	IOB4A38
IOB3B25	P1-57	–	153	154	–	P1-145	IOB4A39
3.3V	–	–	155	156	–	–	VIN
IOB3B19	P1-71	–	157	158	–	P1-129	IOB4A46
IOB3B18	P1-73	–	159	160	–	P1-127	IOB4A47
3.3V	–	–	161	162	–	–	VIN
IOB3B20	P1-69	–	163	164	–	P1-97	IOB4A60
IOB3B21	P1-67	–	165	166	–	P1-95	IOB4A61
3.3V	–	–	167	168	–	–	VIN
IOB3B22	P1-65	–	169	170	–	P1-24	IOB5B0/CLK4p
IOB3B23	P1-63	–	171	172	–	P1-22	IOB5B1/CLK4n
3.3V	–	–	173	174	–	–	VIN
IOB5B2/CLKOUTp	P1-20	–	175	176	–	P1-16	IOB5B4/CLK5p
IOB5B3/CLKOUTn	P1-18	–	177	178	–	P1-14	IOB5B5/CLK5n
3.3V	–	–	179	180	A2	P2-156	HPS_GPI0
GND	–	–	181	182	–	–	GND
GND	–	–	183	184	–	–	GND
GND	–	–	185	186	–	–	GND
GND	–	–	187	188	–	–	GND
GND	–	–	189	190	–	–	GND
GND	–	–	191	192	–	–	GND

3.8 Samtec Connector

The M100PFS SoM connects to the M100PFSEVP Baseboard using two Samtec QSH-090-01-F-D-A connectors.

3.8.1 Connector P1

Function	FPGA	Pin	Pin	FPGA	Function
3.3V	–	1	2	G8	GND
3.3V	–	3	4	E8	JTAG_TDO
3.3V	–	5	6	E9	JTAG_TCK
3.3V	–	7	8	G9	JTAG_TDI
3.3V	–	9	10	F8	JTAG_TMS
3.3V	–	11	12	–	2.5V / 3.3V
2.5V / 3.3V (*)	–	13	14	–	HSMC 178
PMod J5 3	C15	15	16	–	HSMC 176
PMod J5 4	C14	17	18	–	HSMC 177 (*)
HSMC 112 (*)	–	19	20	–	HSMC 175 (*)
HSMC 110 (*)	–	21	22	–	HSMC 172 (*)
2.5V / 3.3V (*)	–	23	24	–	HSMC 170 (*)
3.3V	–	25	26	–	2.5V / 3.3V (*)
SD_DATA2	K4	27	28	C12	LCD_CLK
SD_DATA3	J7	29	30	B12	LCD_R0
SD_CMD	K5	31	32	D16	LCD_R1
SD_CLK	J1	33	34	E16	LCD_R2
SD_DATA0	H1	35	36	F16	LCD_R3
SD_DATA1	J4	37	38	F17	LCD_R4
SD_DETECT	K3	39	40	D17	LCD_R5
LCD_T_RESET	A12	41	42	C16	LCD_R6
3.3V (*)	–	43	44	–	3.3V (*)
LCD_B4	C9	45	46	A17	LCD_R7
LCD_B5	C10	47	48	A16	LCD_G0
LCD_B6	A11	49	50	D19	LCD_G1
LCD_B7	A10	51	52	E19	LCD_G2
LCD_DIM	D11	53	54	C17	LCD_G3
LCD_DISP	C11	55	56	B17	LCD_G4
HSMC 153 (*)	–	57	58	D6	LCD_G5
HSMC 151 (*)	–	59	60	D7	LCD_G6
3.3V (*)	–	61	62	–	3.3V (*)
HSMC 171 (*)	–	63	64	B9	LCD_G7
HSMC 169 (*)	–	65	66	B10	LCD_B0
HSMC 165 (*)	–	67	68	B18	LCD_B1
HSMC 163 (*)	–	69	70	A18	LCD_B2
HSMC 157 (*)	–	71	72	F10	LCD_B3
HSMC 159 (*)	–	73	74	E10	LCD_HSYNC
TXD2	E16	75	76	F11	LCD_VSYNC
RXD2	B14	77	78	F12	LCD_DE
3.3V (*)	–	79	80	–	3.3V (*)
HSMC 147 (*)	–	81	82	–	HSMC 81 (*)
HSMC 145 (*)	–	83	84	–	HSMC 79 (*)

Continued on next page

Table 3.2 – continued from previous page

Function	FPGA	Pin	Pin	FPGA	Function
3.3V (*)	–	85	86	–	3.3V (*)
HSMC 141 (*)	–	87	88	–	HSMC 75 (*)
HSMC 139 (*)	–	89	90	–	HSMC 73 (*)
HSMC 135 (*)	–	91	92	–	HSMC 69 (*)
HSMC 133 (*)	–	93	94	–	HSMC 67 (*)
HSMC 166 (*)	–	95	96	–	HSMC 136 (*)
HSMC 164 (*)	–	97	98	–	HSMC 134 (*)
HSMC 129 (*)	–	99	100	–	HSMC 130 (*)
HSMC 127 (*)	–	101	102	–	HSMC 128 (*)
3.3V (*)	–	103	104	–	3.3V (*)
HSMC 123 (*)	–	105	106	–	HSMC 124 (*)
HSMC 121 (*)	–	107	108	–	HSMC 122 (*)
HSMC 111 (*)	–	109	110	C6	ETH1_RXC
HSMC 109 (*)	–	111	112	A12	P3 26
Pmod J4 9	T5	113	114	–	HSMC 106 (*)
Pmod J4 3	R3	115	116	–	HSMC 104 (*)
HSMC 105 (*)	–	117	118	E11	Pmod J4 7
HSMC 103 (*)	–	119	120	D12	Pmod J4 1
3.3V (*)	–	121	122	–	3.3V (*)
HSMC 99 (*)	–	123	124	–	HSMC 98 (*)
HSMC 97 (*)	–	125	126	–	HSMC 100 (*)
HSMC 160 (*)	–	127	128	–	HSMC 92 (*)
HSMC 158 (*)	–	129	130	–	HSMC 94 (*)
Pmod J4 8	F13	131	132	–	HSMC 61 (*)
Pmod J4 2	E13	133	134	–	HSMC 63 (*)
HSMC 93 (*)	–	135	136	–	HSMC 86 (*)
HSMC 91 (*)	–	137	138	–	HSMC 88 (*)
3.3V (*)	–	139	140	–	3.3V (*)
HSMC 87 (*)	–	141	142	–	HSMC 82 (*)
HSMC 85 (*)	–	143	144	–	HSMC 80 (*)
HSMC 154 (*)	–	145	146	–	HSMC 76 (*)
HSMC 152 (*)	–	147	148	–	HSMC 74 (*)
HSMC 148 (*)	–	149	150	–	HSMC 70 (*)
HSMC 146 (*)	–	151	152	–	HSMC 68 (*)
HSMC 142 (*)	–	153	154	–	HSMC 64 (*)
HSMC 140 (*)	–	155	156	–	HSMC 62 (*)
2.5V / 3.3V (*)	–	157	158	–	2.5V / 3.3V (*)
ETH1_GTXCLK	D18	159	160	F2	P3 28
ETH1_MDC	B5	161	162	T6	Pmod J5 2
ETH1_TXD1	D9	163	164	E18	ETH1_MDIO
ETH1_RX_DV	C4	165	166	G15	ETH1_TXD3
P3 10	B4	167	168	B7	ETH1_RXD2
ETH1_RXD0	A5	169	170	A6	ETH1_RXD1
ETH1_TXD2	B8	171	172	C5	ETH1_TX_EN
ETH1_RXD3	A7	173	174	D8	ETH1_TXD0
2.5V / 3.3V (*)	–	175	176	–	2.5V / 3.3V (*)
3.3V	–	177	178	–	3.3V
3.3V	–	179	180	–	3.3V
Ground Plate	–	181	182	–	Ground Plate

Continued on next page

Table 3.2 – continued from previous page

Function	FPGA	Pin	Pin	FPGA	Function
Ground Plate	–	183	184	–	Ground Plate
Ground Plate	–	185	186	–	Ground Plate
Ground Plate	–	187	188	–	Ground Plate
Ground Plate	–	189	190	–	Ground Plate
Ground Plate	–	191	192	–	Ground Plate

Note: Functions marked with (*) are not connected on the M100PFS SoM side.

3.8.2 Connector P2

Function	FPGA	Pin	Pin	FPGA	Function
GND	–	1	2	–	GND
HSMC 116	L20	3	4	J20	REFCLK1_P
HSMC 118	L19	5	6	J19	REFCLK1_N
GND	–	7	8	–	GND
HSMC 44	G20	9	10	R20	HSMC 26
HSMC 46	G19	11	12	R19	HSMC 28
GND	–	13	14	–	GND
HSMC 43	F22	15	16	T22	HSMC 25
HSMC 45	F21	17	18	T21	HSMC 27
GND	–	19	20	–	GND
HSMC 38	K22	21	22	L5	HSMC 20
HSMC 40	K21	23	24	L6	HSMC 22
GND	–	25	26	–	GND
HSMC 37	H22	27	28	N6	HSMC 19
HSMC 39	H21	29	30	N7	HSMC 21
GND	–	31	32	–	GND
HSMC 32	M22	33	34	K6	HSMC 14
HSMC 34	M21	35	36	K7	HSMC 16
GND	–	37	38	–	GND
HSMC 31	P22	39	40	M7	HSMC 13
HSMC 33	P21	41	42	M8	HSMC 15
GND	–	43	44	–	GND
–	AA20	45	46	L20	–
–	AA19	47	48	L19	–
GND	–	49	50	–	GND
–	AB22	51	52	K22	–
–	AB21	53	54	K21	–
GND	–	55	56	–	GND
–	–	57	58	–	–
–	–	59	60	–	–
3.3V	–	61	62	–	3.3V
–	–	63	64	–	–
–	–	65	66	–	–

Continued on next page

Table 3.3 – continued from previous page

Function	FPGA	Pin	Pin	FPGA	Function
–	–	67	68	–	–
–	–	69	70	B19	Pmod J4 4
Pmod J4 10	B20	71	72	–	–
–	–	73	74	–	–
3.3V	–	75	76	–	3.3V
1.8V (*)	–	77	78	–	2.5V (*)
P3 5 (*)	–	79	80	–	Pmod J6 2 (*)
USB_DIR	F1	81	82	F6	USB_D6
USB_CLK	G2	83	84	F3	USB_D7
USB_D4	D1	85	86	D2	USB_D5
USB_D1	E1	87	88	G5	USB_NXT
P3 3 (*)	–	89	90	–	Pmod J6 3 (*)
P32 BMode (*)	–	91	92	–	P3 7 (*)
Pmod J6 1 (*)	–	93	94	–	Pmod J6 10 (*)
USB_STP	G4	95	96	–	P3 2 (*)
Pmod J6 4 (*)	–	97	98	G3	USB_D2
USB_D3	F5	99	100	F2	USB_D0
1.8V (*)	–	101	102	–	2.5V (*)
3.3V	–	103	104	–	3.3V
ETH0_TXD3	G15	105	106	G14	ETH0_TXD0
ETH0_TXD1	F15	107	108	H15	ETH0_TXD2
ETH0_RXD3	D13	109	110	D22	ETH0_RXD0
ETH0_RXD2	D14	111	112	B15	ETH0_MDC
ETH0_GTXCLK	G17	113	114	A15	ETH0_TX_EN
ETH0_MDIO	H17	115	116	C22	ETH0_RXD1
ETH0_RX_DV	B13	117	118	E15	ETH0_RXC
3.3V	–	119	120	–	3.3V
Pmod J5 8	A21	121	122	–	Pmod J6 8 (*)
Pmod J5 10	A20	123	124	B21	LCD_T_INT
Pmod J6 (*)	–	125	126	B1	I2C0_SDA
Pmod J5 7	C19	127	128	B22	Pmod J5 9
CAN0_TX	E4	129	130	E5	CAN1_RX
HSMC 50	D21	131	132	E3	UART0_TX
Pmod J6 9 (*)	–	133	134	D20	HSMC 49
CAN1_TX	D3	135	136	C20	Pmod J5 1
CAN0_RX	B2	137	138	A3	UART0_RX
I2C0_SCL	C1	139	140	–	3.3V
3.3V	–	141	142	–	3.3V
P3 23 (*)	–	143	144	–	P3 9 (*)
P3 25 (*)	–	145	146	–	P3 13 (*)
P3 17 (*)	–	147	148	–	ETH1_INT (*)
P3 11 (*)	–	149	150	–	P3 15 (*)
–	–	151	152	–	P3 27 (*)
P3 19	D4	153	154	B3	ETH0_INT
P3 21	E5	155	156	A2	HSMC 180
3.3V	–	157	158	–	3.3V
RST_N	–	159	160	–	OCLK_P
VBAT	–	161	162	–	OCLK_N
3.3V	–	163	164	–	2.5V (*)

Continued on next page

Table 3.3 – continued from previous page

Function	FPGA	Pin	Pin	FPGA	Function
IDT_SDAT	–	165	166	–	CLKEXT_P (*)
IDT_SCLK	–	167	168	–	CLKEXT_N (*)
IDT_SEL0	–	169	170	–	2.5V (*)
IDT_SEL1	–	171	172	A13	CLKEXTF
IDT_SEL2	–	173	174	–	CLK25_3
3.3V	–	175	176	–	3.3V
3.3V	–	177	178	–	3.3V
3.3V	–	179	180	–	3.3V
Ground Plate	–	181	182	–	Ground Plate
Ground Plate	–	183	184	–	Ground Plate
Ground Plate	–	185	186	–	Ground Plate
Ground Plate	–	187	188	–	Ground Plate
Ground Plate	–	188	190	–	Ground Plate
Ground Plate	–	191	192	–	Ground Plate

Note: Functions marked with (*) are not connected on the M100PFS SoM side.

CHAPTER

FOUR

APPENDIX

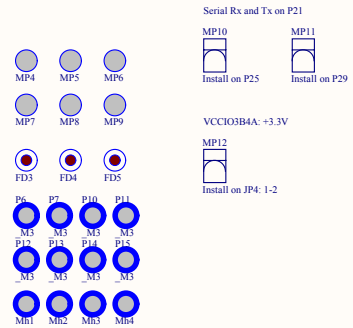
4.1 Schematics

MCV Evaluation Platform (EVP)

Table of Content

Revision History

Revision	Date	Changes
1.0	2016-09-20	Initial release, based on MCVEVK V3.1
1.1	2017-04-11	BOM corrections (R42, R47, R49, mechanical parts)
2.0	2018-05-24	Display connector, second 1G Eth, Pmod (3.3V only)



Serial Rx and Tx on P21

MP10 Install on P25

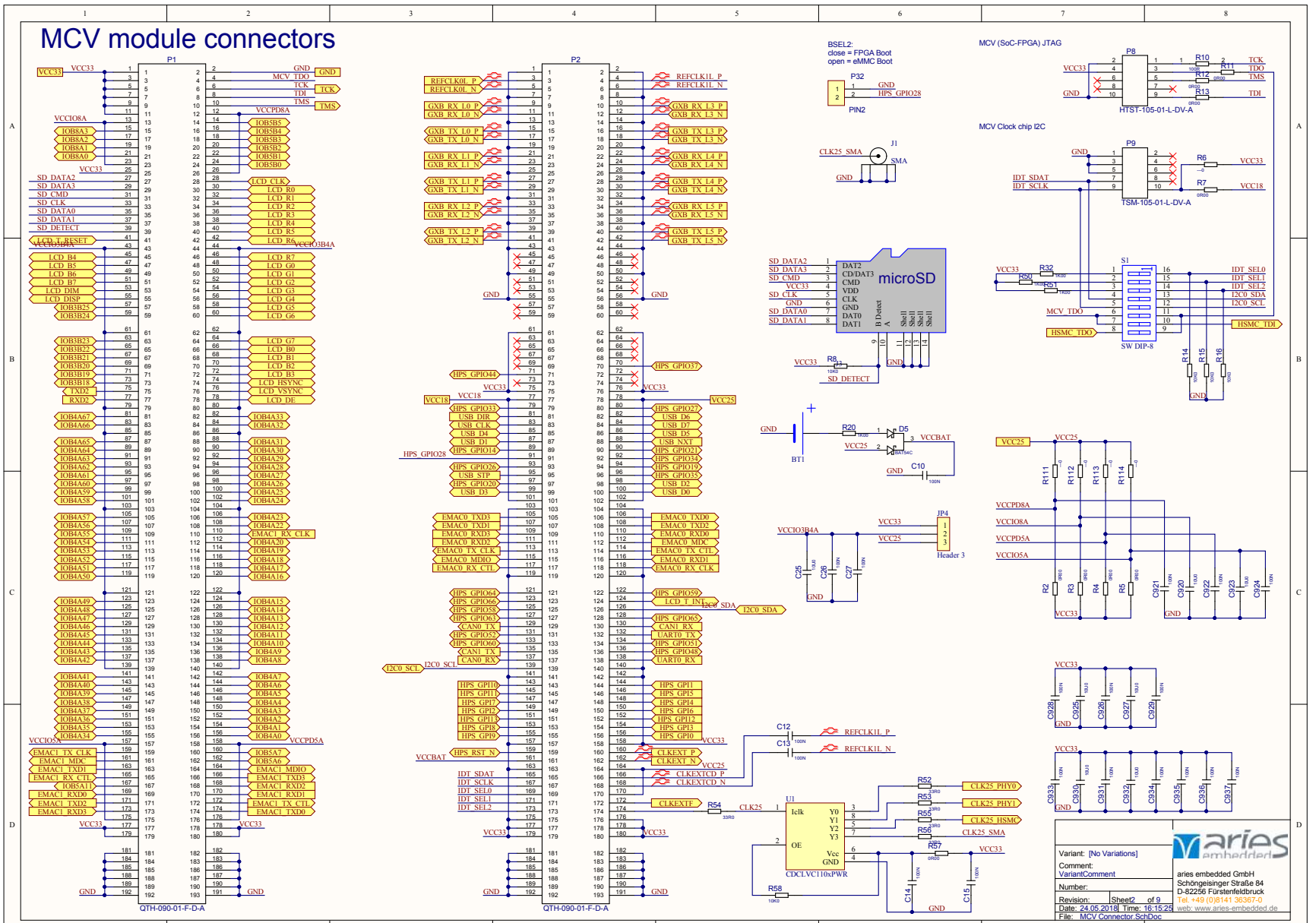
MP11 Install on P29

VCCIO3B4A: +3.3V

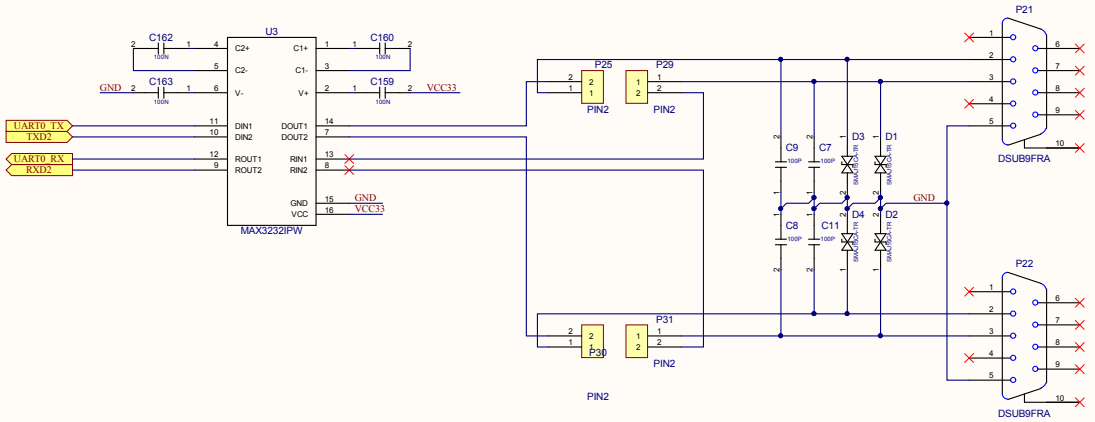
MP12 Install on JP4: 1-2

Variant: [No Variations]
Comment: VariantComment
Number:
Revision: Sheet1 of 9
Date: 24.05.2018 Time: 16:15:25
File: First_Sheet.SCHDOC

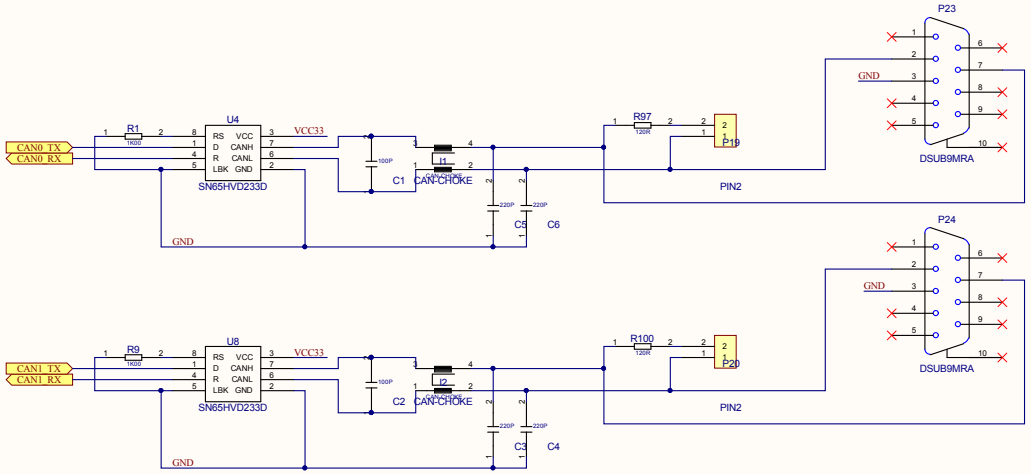
aries embedded GmbH
Schöngeisinger Straße 84
D-82256 Fürstenfeldbruck
Tel. +49 (0)8141 36367-0
web: www.aries-embedded.de


MCV module connectors
P1
P2
QTH-090-01-F-D-A
BSEL2:
close = FPGA Boot
open = eMMC Boot
P32
PIN2
MCV (SoC-FPGA) JTAG
P8
HTST-105-01-L-DV-A
MCV Clock chip I2C
P9
TSM-105-01-L-DV-A
J1
SMA
microSD
SW DIP-8
BT1
JP4
Header 3
U1
CDCLVC110xPWR
aries embedded GmbH
Schöngeisinger Straße 84
D-82256 Fürstenfeldbruck
Tel. +49 (0)8141 36367-0
web: www.aries-embedded.de
Variant: [No Variations]
Comment:
VariantComment
Number:
Revision:
Sheet2 of 9
Date: 24.05.2018 Time: 16:15:25
File: MCV Connector.SchDoc

UART (RS-232)

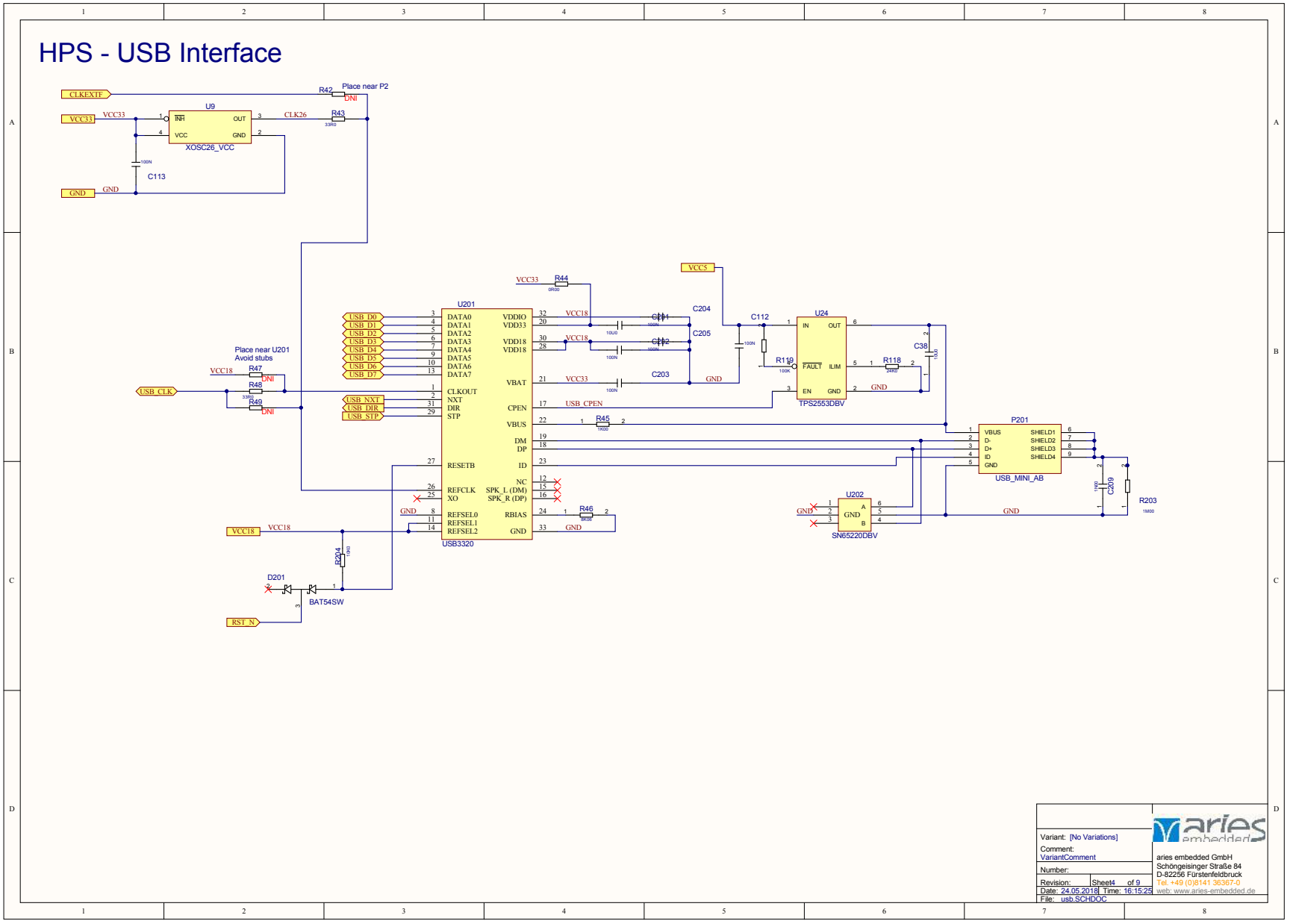


CAN-bus

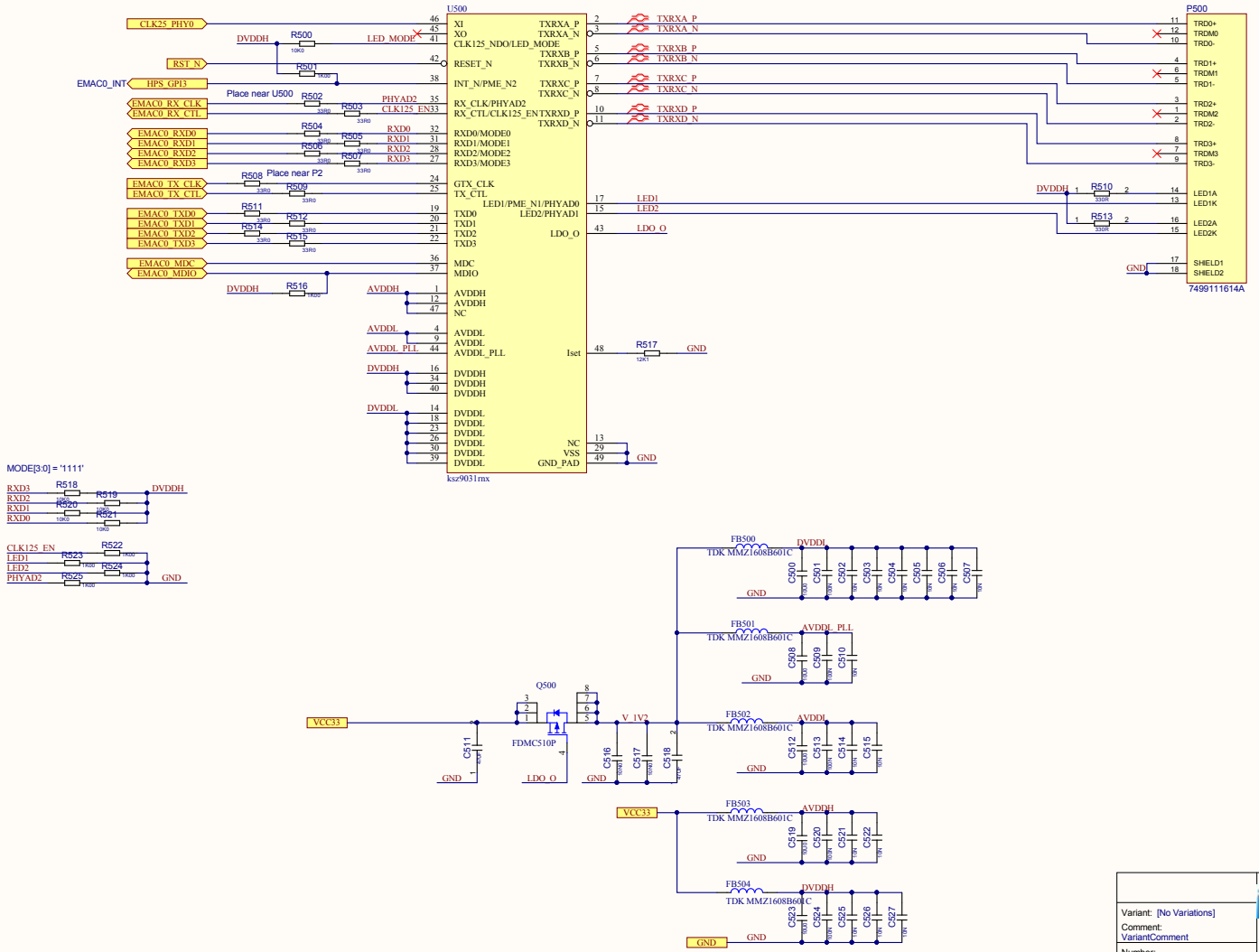


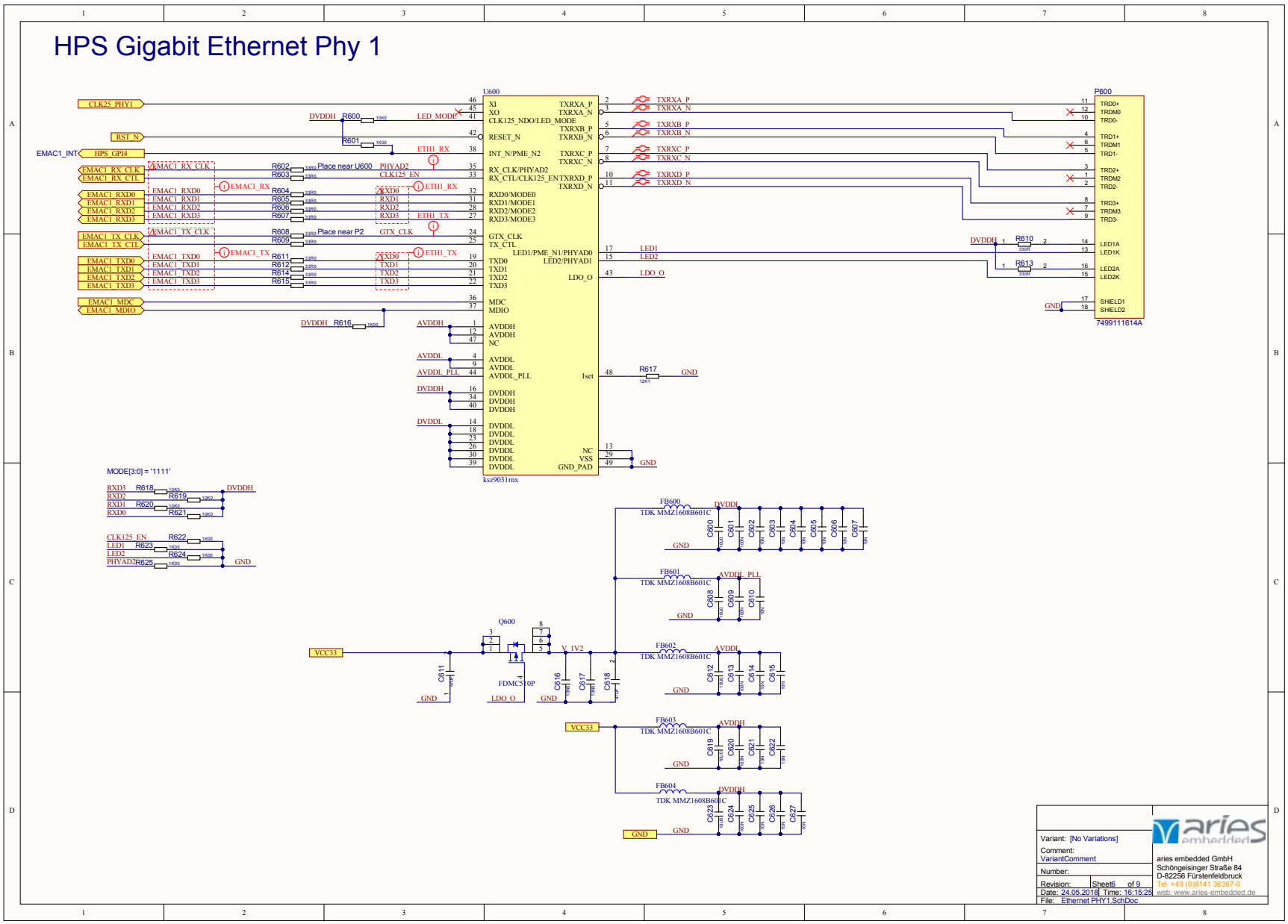
Variant: [No Variations]
Comment: VariantComment
Number:
Revision: Sheet3 of 9
Date: 24.05.2018 Time: 16:15:25
File: UART.SCHDOC

aries embedded GmbH
Schöngeisinger Straße 84
D-82256 Fürstenfeldbruck
Tel. +49 (0)8141 36367-0
web: www.aries-embedded.de

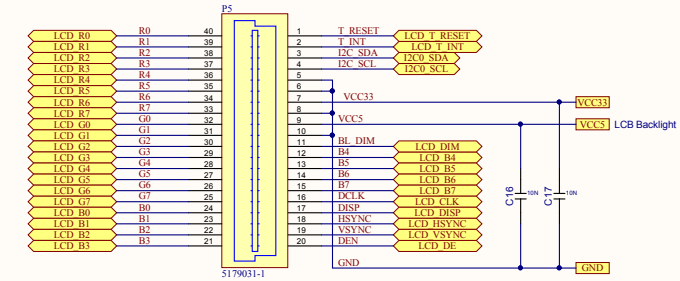

HPS - USB Interface
CLKEXTF
VCC33
GND
U9
XOSC26_VCC
CLK26
R42
Place near P2
DNI
R43
33R0
C113
100N
Place near U201
Avoid stubs
R47
R48
R49
USB_CLK
USB_NXT
USB_DIR
USB_STP
USB_D0
USB_D1
USB_D2
USB_D3
USB_D4
USB_D5
USB_D6
USB_D7
U201
USB3320
DATA0
DATA1
DATA2
DATA3
DATA4
DATA5
DATA6
DATA7
CLKOUT
NXT
DIR
STP
RESETB
REFCLK
XO
REFSEL0
REFSEL1
REFSEL2
VDDIO
VDD33
VDD18
VBAT
CPEN
VBUS
DM
DP
ID
NC
SPK_L (DM)
SPK_R (DP)
RBIAS
R44
R45
R46
VCC18
VCC5
C201
C202
C203
C204
C205
C112
U24
TPS2553DBV
IN
OUT
FAULT
ILIM
EN
R119
R118
C38
USB_CPEN
P201
USB_MINI_AB
VBUS
D-
D+
ID
SHIELD1
SHIELD2
SHIELD3
SHIELD4
C209
R203
U202
SN65220DBV
D201
BAT54SW
R204
RST_N
Variant: [No Variations]
Comment:
VariantComment
Number:
Revision:
Sheet4 of 9
Date: 24.05.2018 Time: 16:15:25
File: usb.SCHDOC
aries embedded GmbH
Schöngeisinger Straße 84
D-82256 Fürstenfeldbruck
Tel. +49 (0)8141 36367-0
web: www.aries-embedded.de

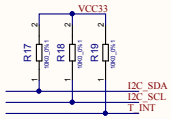
HPS Gigabit Ethernet Phy 0




HPS Gigabit Ethernet Phy 1
U600
ksz9031rnx
P600
7499111614A
CLK25_PHY1
RST_N
EMAC1_INT
HPS_GPI4
EMAC1_RX_CLK
EMAC1_RX_CTL
EMAC1_RXD0
EMAC1_RXD1
EMAC1_RXD2
EMAC1_RXD3
EMAC1_TX_CLK
EMAC1_TX_CTL
EMAC1_TXD0
EMAC1_TXD1
EMAC1_TXD2
EMAC1_TXD3
EMAC1_MDC
EMAC1_MDIO
LED_MODE
ETH1_RX
ETH1_TX
GTX_CLK
PHYAD2
CLK125_EN
LED1
LED2
LDO_O
Iset
TXRXA_P
TXRXA_N
TXRXB_P
TXRXB_N
TXRXC_P
TXRXC_N
TXRXD_P
TXRXD_N
MODE[3:0] = '1111'
Q600
FDMC510P
FB600
FB601
FB602
FB603
FB604
TDK MMZ1608B601C
VCC33
V_1V2
AVDDH
AVDDL
AVDDL_PLL
DVDDH
DVDDL
GND
Variant: [No Variations]
Comment: VariantComment
Number:
Revision:
Sheet6 of 9
Date: 24.05.2018 Time: 16:15:25
File: Ethernet PHY1.SchDoc
aries embedded GmbH
Schöngeisinger Straße 84
D-82256 Fürstenfeldbruck
Tel. +49 (0)8141 36367-0
web: www.aries-embedded.de

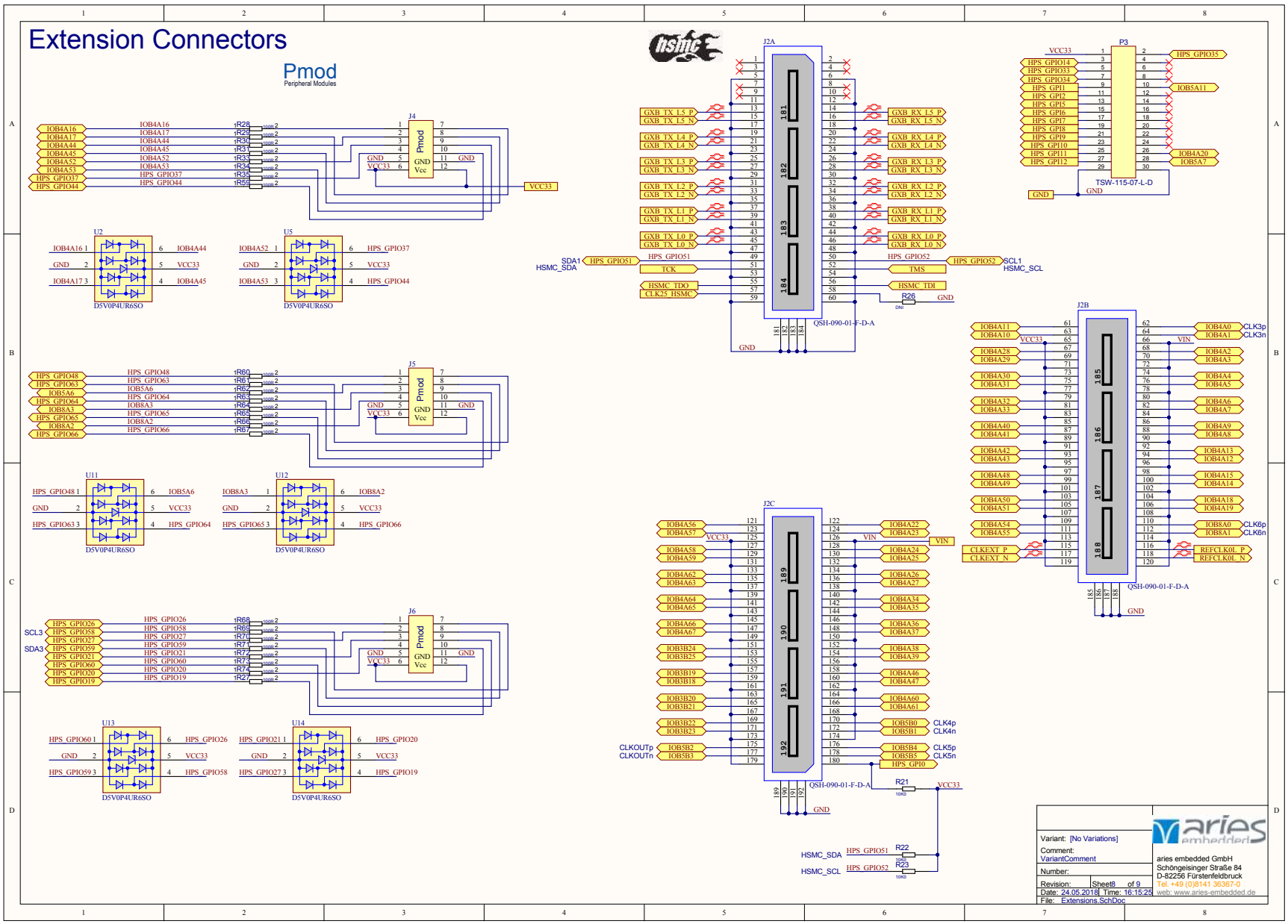
TFT Interface and Touch Controller

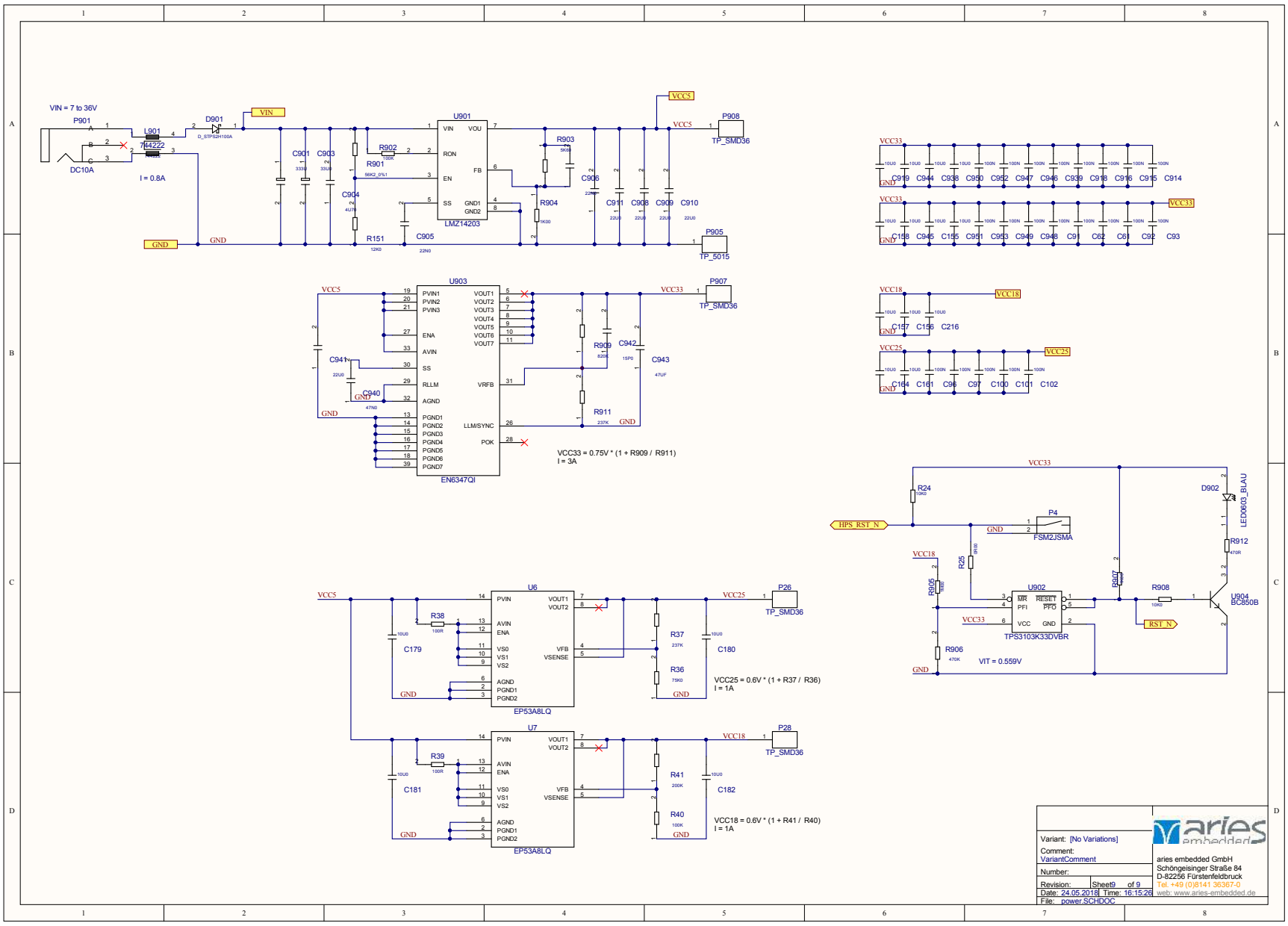




Variant: [No Variations]
Comment: VariantComment
Number:
Revision:
Sheet7 of 9
Date: 24.05.2018 Time: 16:15:25
File: LCD.SchDoc

aries embedded GmbH
Schöngeisinger Straße 84
D-82256 Fürstenfeldbruck
Tel. +49 (0)8141 36367-0
web: www.aries-embedded.de


Extension Connectors
Pmod
Peripheral Modules
J4
J5
J6
U2
U5
U11
U12
U13
U14
D5V0P4UR6SO
J2A
J2B
J2C
QSH-090-01-F-D-A
P3
TSW-115-07-L-D
R21
R22
R23
HSMC_SDA
HSMC_SCL
Variant: [No Variations]
Comment:
VariantComment
Number:
Revision:
Sheet8 of 9
Date: 24.05.2018 Time: 16:15:25
File: Extensions.SchDoc
aries embedded GmbH
Schöngeisinger Straße 84
D-82256 Fürstenfeldbruck
Tel. +49 (0)8141 36367-0
web: www.aries-embedded.de


VIN = 7 to 36V
P901
DC10A
I = 0.8A
L901
74422
D901
D_STPS2H100A
VIN
GND
C901
C903
C904
R901
R902
R151
C905
U901
VIN
VOU
RON
FB
EN
SS
GND1
GND2
LMZ14203
R903
R904
C906
C911
C908
C909
C910
VCC5
P908
TP_SMD36
P905
TP_5015
VCC33
C919
C944
C938
C950
C952
C947
C946
C939
C918
C916
C915
C914
C158
C945
C155
C951
C953
C949
C948
C91
C62
C61
C92
C93
U903
PVIN1
PVIN2
PVIN3
ENA
AVIN
SS
RLLM
AGND
PGND1
PGND2
PGND3
PGND4
PGND5
PGND6
PGND7
VOUT1
VOUT2
VOUT3
VOUT4
VOUT5
VOUT6
VOUT7
VRFB
LLM/SYNC
POK
EN6347QI
C941
C940
R909
C942
C943
R911
P907
VCC18
C157
C156
C216
VCC25
C164
C161
C96
C97
C100
C101
C102
VCC33 = 0.75V * (1 + R909 / R911)
I = 3A
HPS_RST_N
P4
FSM2JSMA
R24
D902
LED0603_BLAU
R912
R25
R905
R907
R908
U902
MR
RESET
PFI
PFO
VCC
GND
TPS3103K33DVBR
U904
BC850B
RST_N
R906
VIT = 0.559V
U6
EP53A8LQ
R38
C179
R37
C180
R36
P26
VCC25 = 0.6V * (1 + R37 / R36)
I = 1A
U7
EP53A8LQ
R39
C181
R41
C182
R40
P28
VCC18 = 0.6V * (1 + R41 / R40)
I = 1A
Variant: [No Variations]
Comment:
VariantComment
Number:
Revision:
Sheet9 of 9
Date: 24.05.2018 Time: 16:15:26
File: power.SCHDOC
aries embedded GmbH
Schöngeisinger Straße 84
D-82256 Fürstenfeldbruck
Tel. +49 (0)8141 36367-0
web: www.aries-embedded.de

4.2 Layout Diagram