MP2612

2A,24V Input, 600kHz 2-3 Cells Switching Li-Ion Battery Charger

The Future of Analog IC Technology

DESCRIPTION

The MP2612 is a monolithic switching charger for 2-3 cells series Li-Ion cells battery with a built-in internal power MOSFET. It achieves up to 2A charge current with current mode control for fast loop response and easy compensation. The charge current can be programmed by sensing the current through an accurate sense resistor.

MP2612 regulates the charge current and charge voltage using two control loops to realize high accuracy CC charge and CV charge.

Fault condition protection includes cycle- by-cycle current limiting and thermal shutdown. Other safety features include battery temperature monitoring, charge status indication and programmable timer to finish the charging cycle.

The MP2612 requires a minimum number of readily available standard external components.

The MP2612 is available in 16-pin 4mm x 4mm QFN package.

FEATURES

- Charges 2-3 Cells Series Li-Ion Battery Packs
- Wide Operating Input Range
- Up to 2 A Programmable Charging Current
- ±0.75% V_{BATT} Accuracy
- 0.2Ω Internal Power MOSFET Switch
- Up to 90% Efficiency
- Fixed 600kHz Frequency
- Preconditioning for Fully Depleted Batteries
- Charging Operation Indicator
- Input Supply and Battery Fault Indicator
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Battery Temperature Monitor and Protection

APPLICATIONS

- Distributed Power Systems
- Chargers for 2-Cell or 3-Cell Li-Ion Batteries
- Pre-Regulator for Linear Regulators
- Smart Phones
- Net-book

TYPICAL APPLICATION

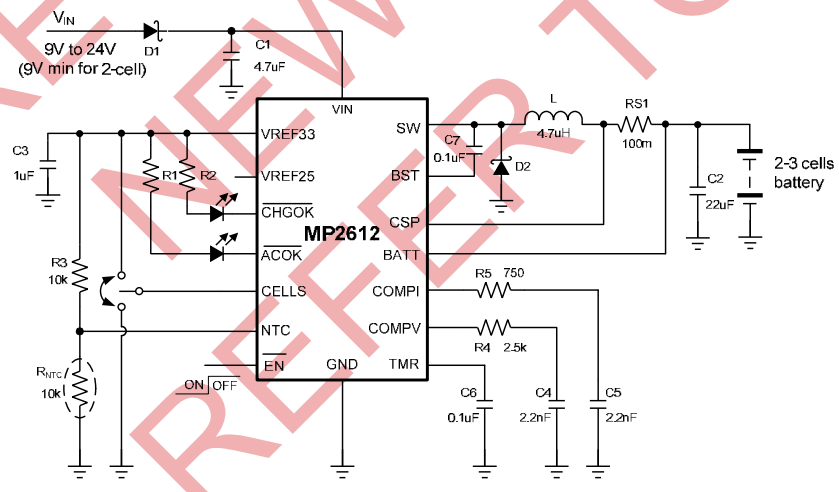


Figure 1—Standalone Switching Charger

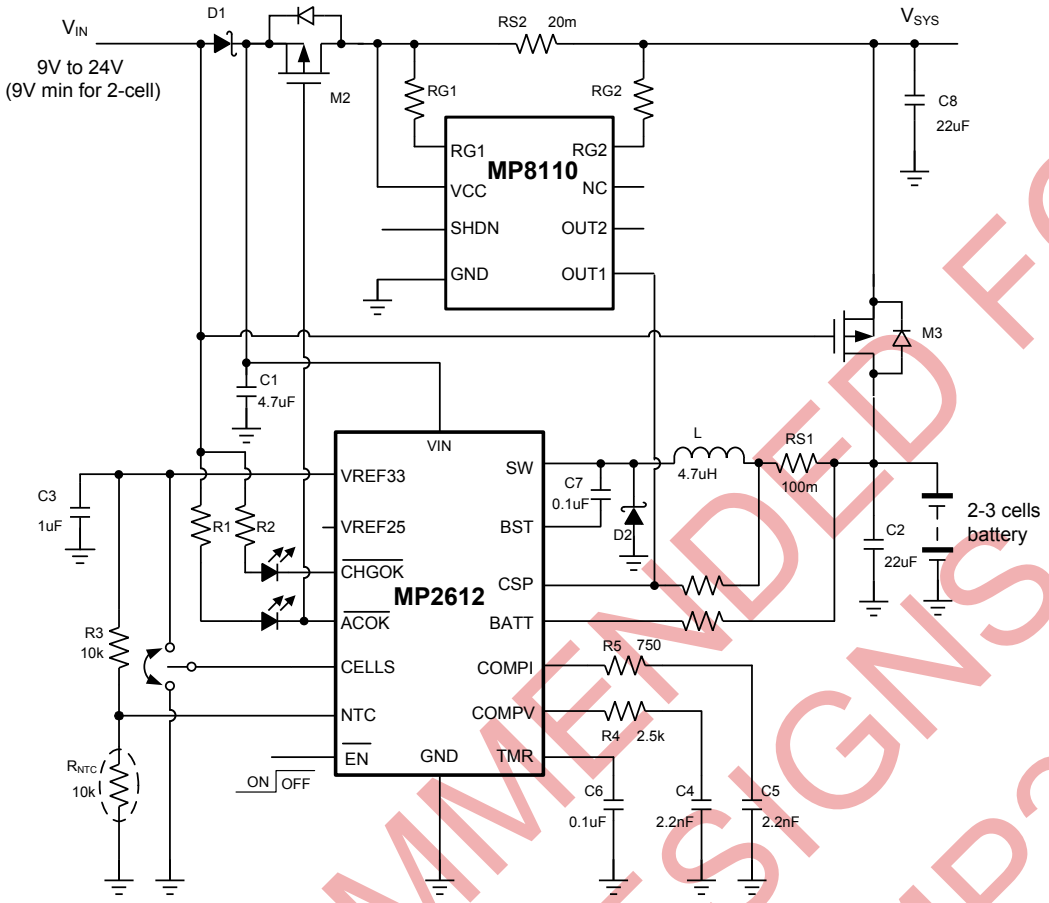


Figure 2—Switching Charger with Power Path Management (1)

Notes:

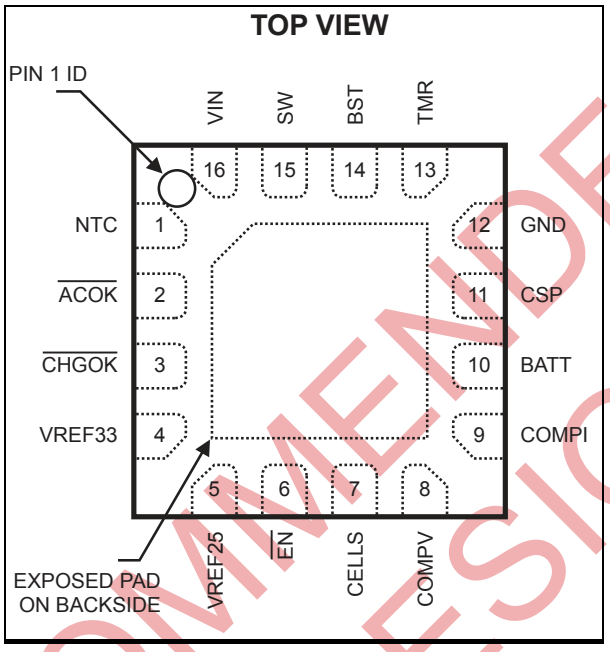
1) $\overline{\text{ACOK}}$ should be pulled up to VIN in the power path management application.

ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP2612ER	4mm x 4mm QFN16	2612ER	-20°C to +85°C

*For Tape & Reel, add suffix –Z (eg. MP2612ER–Z);
For RoHS compliant packaging, add suffix –LF (eg. MP MP2612ER–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (2)

Supply Voltage V_{IN} 26V
V_{SW} ..... -0.3V to V_{IN} + 0.3V
V_{BST} ..... V_{SW} + 6V
V_{CSP}, V_{BATT}, ... -0.3V to +18V
$V_{\overline{ACOK}}$, $V_{\overline{CHGOK}}$, ... -0.3V to +26V
All Other Pins ..... -0.3V to +6V
Continuous Power Dissipation (T_A=+25°C) (3) 2.7W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN} ..... 9V to 24V
Maximum Junction Temp. (T_J) ..... +125°°C

Thermal Resistance (5)

	θ_{JA}	θ_{JC}	
4x4 QFN16	46	10	°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7 4-layer board.

ELECTRICAL CHARACTERISTICS (6)

V_{IN} = 19V, T_A = +25°C, CELLS=0V, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Terminal Battery Voltage	V_{BATT}	CELLS=0V	8.337	8.4	8.463	V
		CELLS= VREF33	12.505	12.6	12.695	
CSP，BATT Current	I_{CSP},I_{BATT}	Charging disabled		1		μA
Switch On Resistance	$R_{DS(ON)}$			0.2		Ω
Switch Leakage		$\overline{EN}$= 4V, V_{SW} = 0V		0	10	μA
Peak Current Limit	CC(6)			4.1		A
	Trickle			2		A
CC current	I_{CC}	RS1=100mΩ	1.8	2.0	2.2	A
Trickle charge current	$I_{TRICKLE}$			10%		I_{CC}
Trickle charge voltage threshold				2.8		V/cell
Trickle charge hysteresis				350		mV
Termination current threshold	I_{BF}		5%	10%	15%	I_{CC}
Oscillator Frequency	f_{SW}	CELLS=0V, V_{BATT} =4.5V		600		kHz
Fold-back Frequency		V_{BATT} =0V		190		kHz
Maximum Duty Cycle			90			%
Maximum current Sense Voltage (CSP to BATT)	V_{SENSE}		170	200	230	mV
Minimum On Time (6)	t_{ON}	CELLS=0V, V_{BATT} =5V		100		ns
Under Voltage Lockout Threshold Rising			3	3.2	3.4	V
Under Voltage Lockout Threshold Hysteresis				200		mV
Open-drain sink current		V_{DRAIN} =0.3V	5			mA
Dead-battery indication		Stay at trickle mode C_{TMR}=0.1μF		30		min
Termination delay		Time after I_{BF} reached, C_{TMR}=0.1μF		1		min
Recharge threshold at V_{BATT}	V_{RECHG}			4.0		V/cell
Recharge Hysteresis				100		mV
NTC Low Temp Rising Threshold		R_{NTC}=NCP18XH103(0°C)		73		%VREF33
NTC High Temp Falling Threshold		R_{NTC}=NCP18XH103(50°C)		30		%VREF33
VIN min head-room (reverse blocking)		VIN-VBATT		180		mV
$\overline{EN}$ Input Low Voltage					0.4	V
$\overline{EN}$ Input High Voltage			1.8			V
$\overline{EN}$ Input Current		$\overline{EN}$=4V		4		μA
		$\overline{EN}$=0V		0.2		

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 19V, T_A = +25°C, CELLS=0V, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)		$\overline{EN}$ =4V		0.16		mA
		$\overline{EN}$ =4V, Consider VREF33 pin output current, R_3=10k,R_{NTC}=10k		0.32		mA
Supply Current (Quiescent)		$\overline{EN}$ =0V, CELLS=0V			2.0	mA
Thermal Shutdown (6)				150		°C
VREF25 output voltage				2.5		V
VREF33 output voltage				3.3		V
VREF33 load regulation		I_{LOAD} =0 to 10mA		30		mV

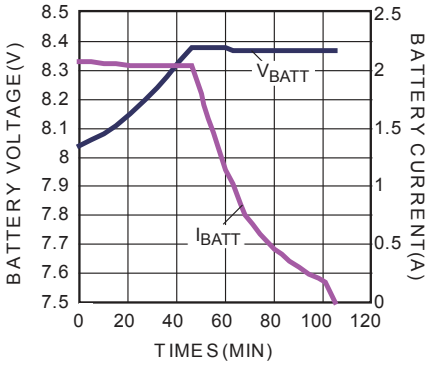
Notes:

6) Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

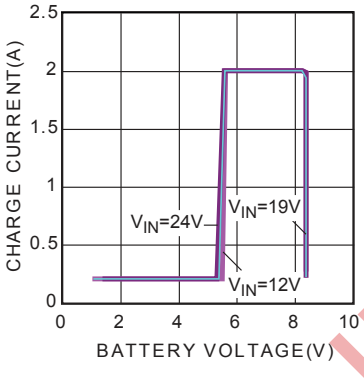
V_{IN}=19V, C1=4.7µF, C2=22µF, L=4.7µH, RS1=100mΩ, Real Battery Load, T_A=25ºC, unless otherwise noted.

2 Cells Battery Charge Curve

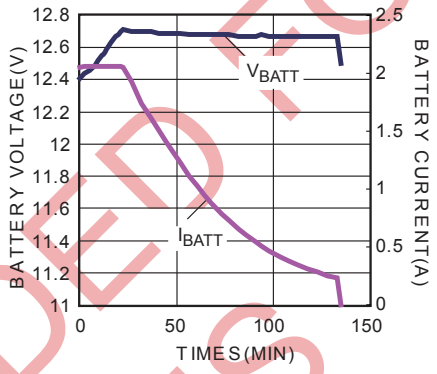


2 Cells Charge Current vs. Battery Voltage

CV Load

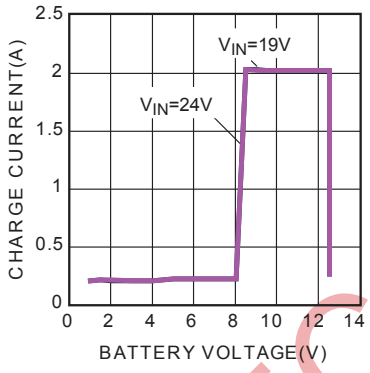


3 Cells Battery Charge Curve

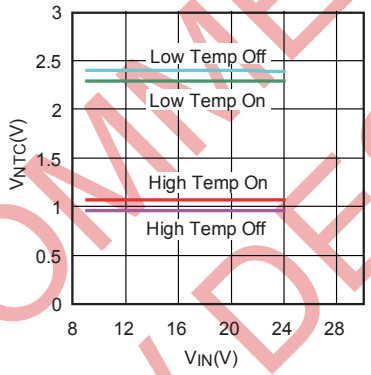


3 Cells Charge Current vs. Battery Voltage

CV Load

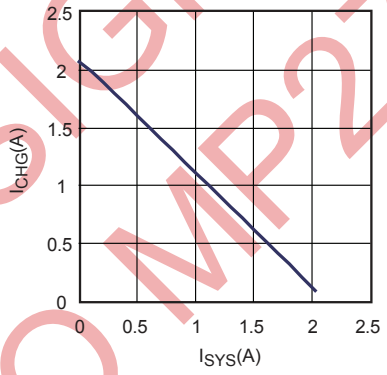


NTC Control Window



Current Sharing

Power Path Management,
RS1=110mΩ, RS2=20 mΩ

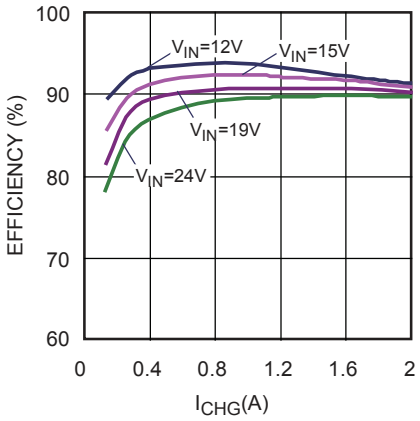


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=19V, C1=4.7µF, C2=22µF, L=4.7µH, RS1=100mΩ, Real Battery Load, T_A=25ºC, unless otherwise noted.

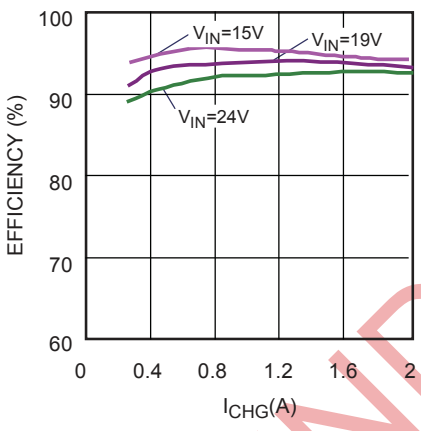
Efficiency vs. I_{CHG}

2 Cells, V_{BATT}=8.4V



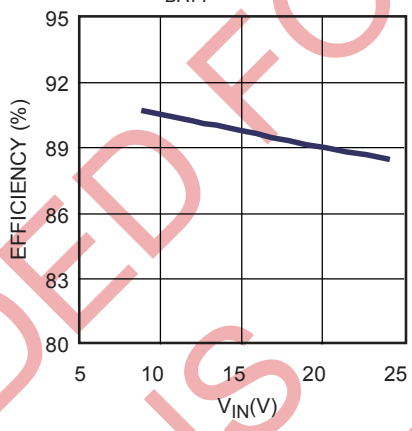
Efficiency vs. I_{CHG}

3 Cells, V_{BATT}=12.6V



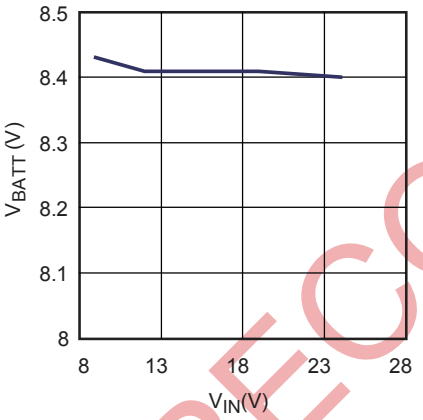
Efficiency vs. V_{IN}

2 Cells, V_{BATT}=7.4V



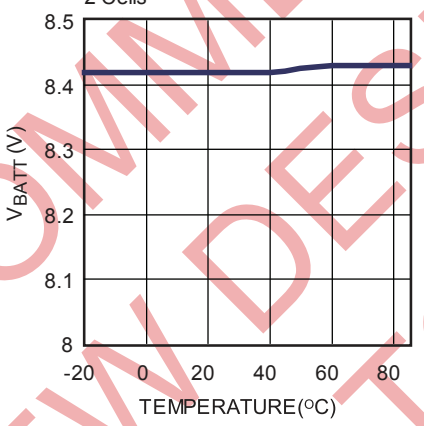
BATT Float Voltage vs. V_{IN}

2 Cells



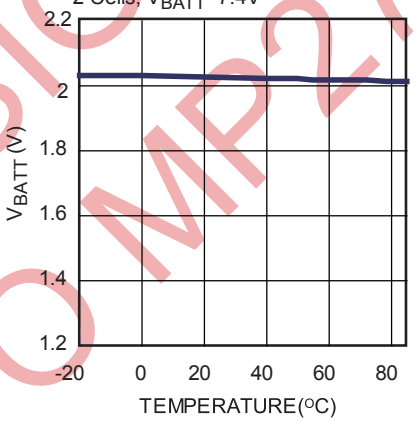
BATT Float Voltage vs. Temperature

2 Cells



Charge Current vs. Temperature

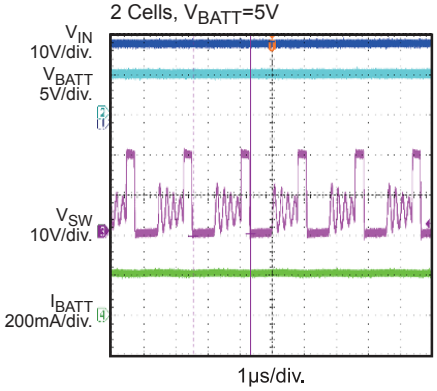
2 Cells, V_{BATT}=7.4V



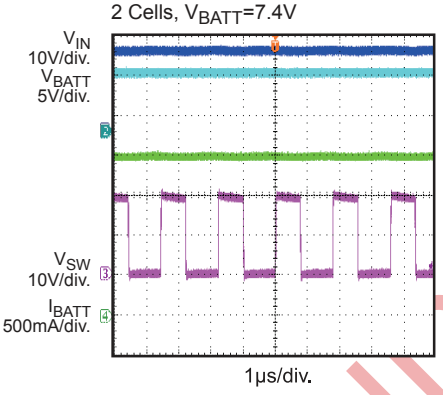
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=19V, C1=4.7µF, C2=22µF, L=4.7µH, RS1=100mΩ, Real Battery Load, T_A=25ºC, unless otherwise noted.

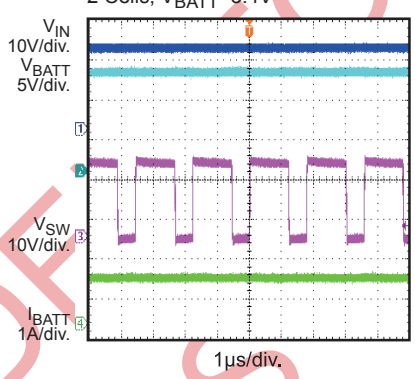
Steady State Waveform
Trickle Charge
2 Cells, V_{BATT}=5V



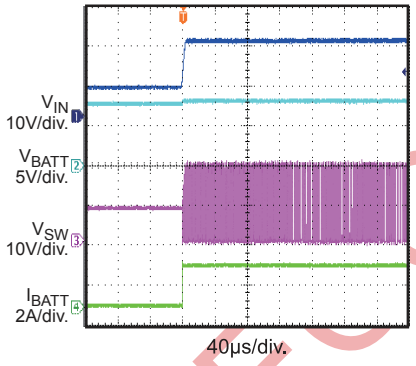
Steady State Waveform
CC Charge
2 Cells, V_{BATT}=7.4V



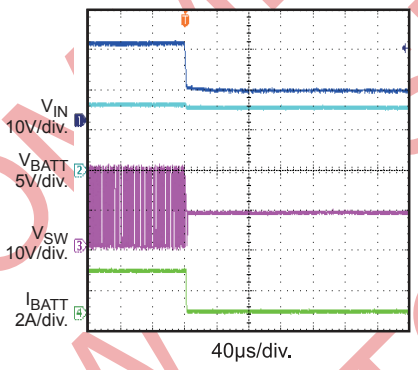
Steady State Waveform
CV Charge
2 Cells, V_{BATT}=8.4V



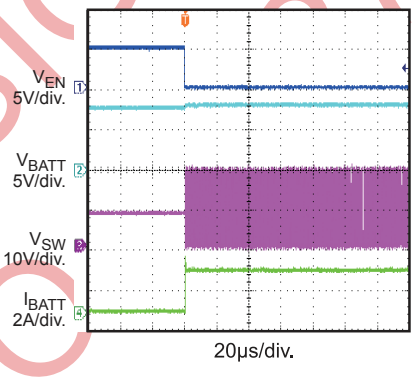
Power On Waveform
2 Cells, I_{CHG}=2A,V_{BATT}=8V



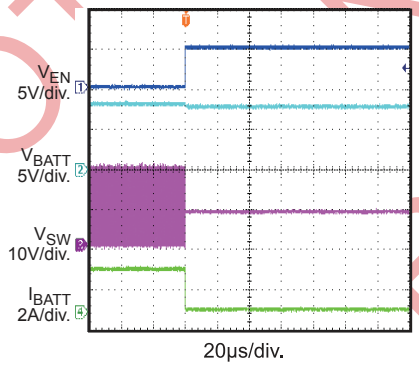
Power Off Waveform
2 Cells, I_{CHG}=2A,V_{BATT}=8V



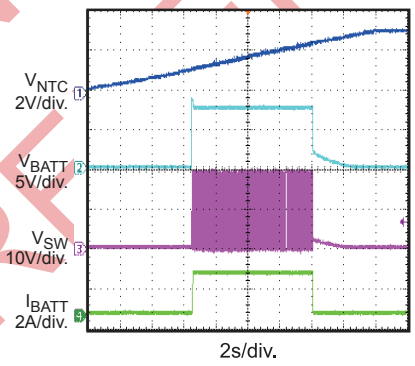
EN On Waveform
2 Cells, I_{CHG}=2A,V_{BATT}=8V



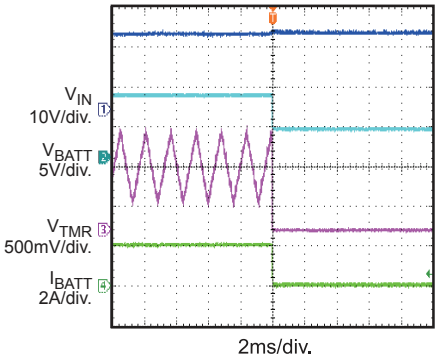
EN Off Waveform
2 Cells, I_{CHG}=2A,V_{BATT}=8V



NTC Control
V_{BATT}=7.4V



Timer Out
2 Cells, V_{BATT}=7.4V, C_{TMR}=1nF

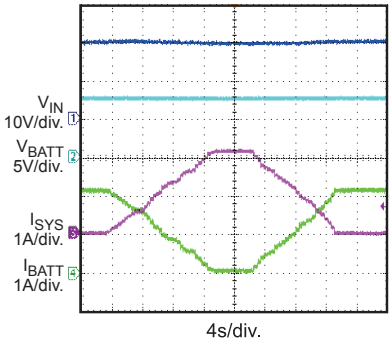


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=19V, C1=4.7µF, C2=22µF, L=4.7µH, RS1=110mΩ, RS2=20mΩ, Real Battery Load, T_A=25ºC, unless otherwise noted.

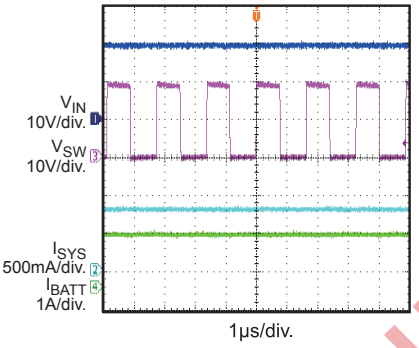
Power Path Management Current Sharing

2 Cells, I_{CHG}=2A, V_{BATT}=7.4V



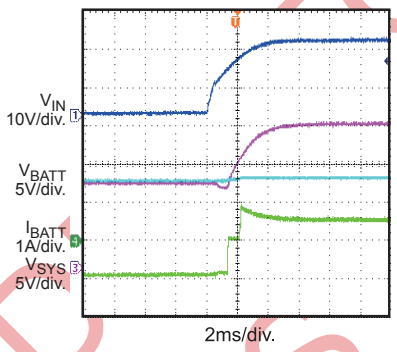
Power Path Management Steady State

2 Cells, I_{CHG}=2A, V_{BATT}=8V, I_{SYS}=0.8A



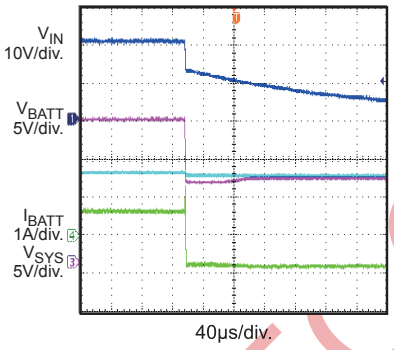
Power Path Management Power On

3 Cells, I_{CHG}=2A,V_{BATT}=12V, 10Ω SYS Load



Power Path Management Power Off

3 Cells, I_{CHG}=2A,V_{BATT}=12V, 10Ω SYS Load



PIN FUNCTIONS

Pin #	Name	Description
1	NTC	Thermistor Input. Connect a resistor from this pin to the pin VREF33 and the Thermistor from this pin to ground.
2	$\overline{\text{ACOK}}$	Valid Input Supply Indicator. A logic LOW on this pin indicates the presence of a valid input supply.
3	$\overline{\text{CHGOK}}$	Charging Completion Indicator. A logic LOW indicates charging operation. The pin will become an open drain once the charging is complete.
4	VREF33	Internal linear regulator 3.3V reference output. Bypass to GND with a 1μF ceramic capacitor.
5	VREF25	Internal linear 2.5V reference circuit. PLEASE KEEP THIS PIN FLOATING.
6	$\overline{\text{EN}}$	On/Off Control Input.
7	CELLS	Command Input for the number of Li-Ion Cells. Connect this pin to VREF33 for 3-cell operation or ground the pin for 2-cell operation. DO NOT LEAVE THIS PIN FLOAT.
8	COMPV	V-LOOP Compensation. Decouple this pin with a capacitor and a resistor.
9	COMPI	I-LOOP Compensation. Decouple this pin with a capacitor and a resistor.
10	BATT	Positive Battery Terminal.
11	CSP	Battery Current Sense Positive Input. Connect a resistor R_{SEN} between CSP and BATT. The full charge current is: $I_{CHG}(A)=\frac{200mV}{RS1(m\Omega)}$.
12	GND	Ground. This pin is the voltage reference for the regulated output voltage. For this reason care must be taken in its layout. This node should be placed outside of the switching diode (D2) to the input ground path to prevent switching current spikes from inducing voltage noise into the part.
13	TMR	Set time constant. 0.1uA current charges and discharges the external cap.
14	BST	Bootstrap. This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between SW and BS pins to form a floating supply across the power switch driver.
15	SW	Switch Output.
16	IN	Supply Voltage. The MP2612 operates from a 9V to 24V unregulated input to charge 2~3 cell li-ion battery. Capacitor is needed to prevent large voltage spikes from appearing at the input.

BLOCK DIAGRAM

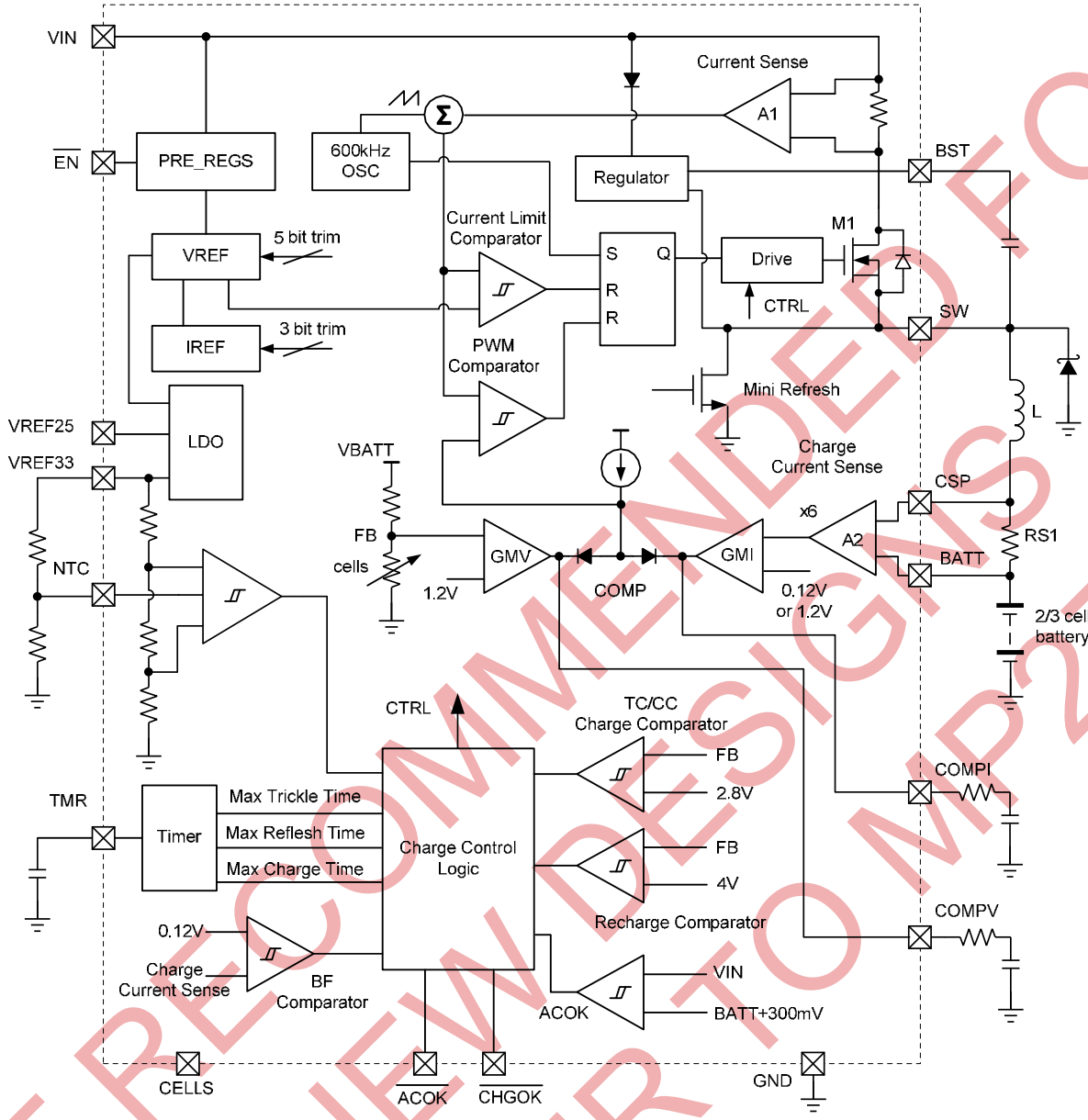


Figure 3—Function Block Diagram

OPERATION

The MP2612 is a peak current mode controlled switching charger for use with Li-Ion batteries.

Figure 3 shows the block diagram. At the beginning of a cycle, M1 is off. The COMP voltage is higher than the current sense result from amplifier A1's output and the PWM comparator's output is low. The rising edge of the 600 kHz CLK signal sets the RS Flip-Flop. Its output turns on M1 thus connecting the SW pin and inductor to the input supply.

The increasing inductor current is sensed and amplified by the Current Sense Amplifier A1. Ramp compensation is summed to the output of A1 and compared to COMP by the PWM comparator.

When the sum of A1's output and the Slope Compensation signal exceeds the COMP voltage, the RS Flip-Flop is reset and M1 is turned off. The external switching diode D2 then conducts the inductor current.

If the sum of A1's output and the Slope Compensation signal does not exceed the COMP voltage, then the falling edge of the CLK resets the Flip-Flop.

The MP2612 have two internal linear regulators power internal circuit, VREF33 and VREF25. The output of 3.3V reference voltage can also power external circuitry as long as the maximum current (50mA) is not exceeded. A 1μF bypass capacitor is required from VREF33 to GND to ensure stability. The output of 2.5V reference voltage can not carry any load.

In typical application, VREF25 should be float and no capacitor is required. It can only connect to a capacitor which is smaller than 100pF.

Charge Cycle (Mode change: Trickle→ CC→ CV)

The battery current is sensed via RS1 (Figure 3) and amplified by A2. The charge will start in "trickle charging mode" (10% of the R_{SEN} programmed current I_{CC}) until the battery voltage reaches 2.8V/cell. If the charge stays in the "trickle charging mode" till "timer out" condition is triggered, the charge is terminated. Otherwise, the output of A2 is then regulated to the level set by RS1. The charger is operating at "constant current charging mode." The duty cycle of the switcher is determined by the COMPI voltage that is regulated by the amplifier GMI.

When the battery voltage reaches the "constant voltage mode" threshold, the amplifier GMV will regulate the COMP pin, and then the duty cycle. The charger will then operate in "constant voltage mode."

Automatic Recharge

A programmable time delay after the battery charging current drops below the termination threshold, the charger will cease charging and the $\overline{CHGOK}$ pin becomes an open drain. If for some reason, the battery voltage is lowered to 4.0V/Cell, recharge will automatically kick in.

$$\text{Termination Delay} = 1\text{min} \times \frac{C_{TMR}}{0.1\text{uF}}$$

Charger Status Indication

MP2612 has two open-drain status outputs: $\overline{CHGOK}$ and $\overline{ACOK}$. The $\overline{ACOK}$ pin pulls low when an input voltage is greater than battery voltage 300mV and over the under voltage lockout threshold. $\overline{CHGOK}$ is used to indicate the status of the charge cycle. Table 1 describes the status of the charge cycle based on the $\overline{CHGOK}$ and $\overline{ACOK}$ outputs.

Table 1—Charging Status Indication

$\overline{ACOK}$	$\overline{CHGOK}$	Charger status
low	low	In charging
low	high	End of charge,
high	high	Vin<UVLO, timer out, thermal shutdown $\overline{EN}$ disable

Timer Operation

MP2612 uses internal timer to terminate the charge if the timer times out. The timer duration is programmed by an external capacitor at the TMR pin.

The trickle mode charge time is:

$$T_{TICKLE\_TMR} = 30mins \times \frac{C_{TMR}}{0.1uF}$$

The total charge time is:

$$T_{TOTAL\_TMR} = 3hours \times \frac{C_{TMR}}{0.1uF}$$

Negative Thermal Coefficient (NTC) Thermistor

The MP2612 has a built-in NTC resistance window comparator, which allows MP2612 to sense the battery temperature via the thermistor packed internally in the battery pack to ensure a safe operating environment of the battery. A resistor with appropriate value should be connected from VREF33 to NTC pin and the thermistor is connected from NTC pin to GND. The voltage on NTC pin is determined by the resistor divider whose divide ratio depends on the battery temperature. When the voltage of pin NTC falls out of NTC window range, MP2612 will stop the charging. The charger will restart if the temperature goes back into NTC window range.

Power Path Management

Using MP8110 together with MP2612 can implement a switching charger circuit with power path management function, which realizes the current sharing of the charger and system load (Figure 2). In another word, MP8110 senses the system current and feeds back to MP2612 and MP2612 reduces charge current according to the increase of the system current.

However, after the charge current decrease to 0, the system current can only be limited by the adapter.

The system current is satisfied first and always. It chooses the adapter as its power source when the adapter plugs in, and the battery is the backup power source when the adapter is removed.

Figure 4 to 8 shows the charge profile, operation waveform and flow chart, respectively.

CHARGE PROFILE AND POWER PATH MANAGEMENT FUNCTION

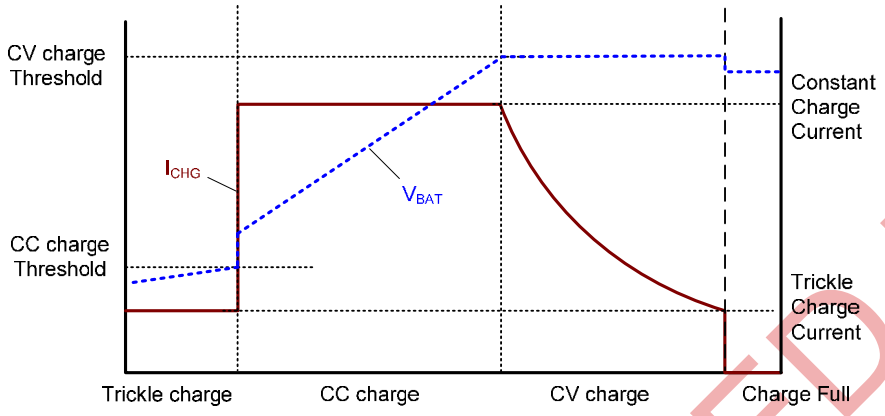


Figure 4—Li-Ion Battery Charge Profile

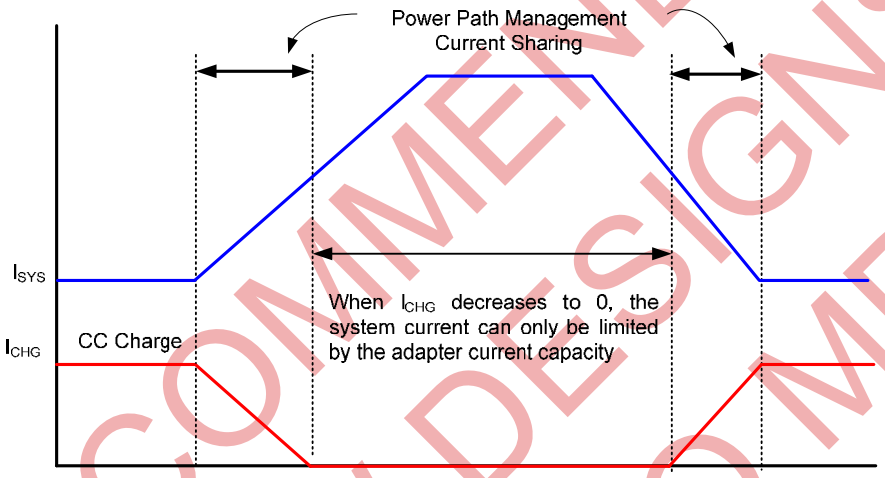


Figure 5 — Power Path Management Function- Current Sharing

OPERATION FLOW CHART

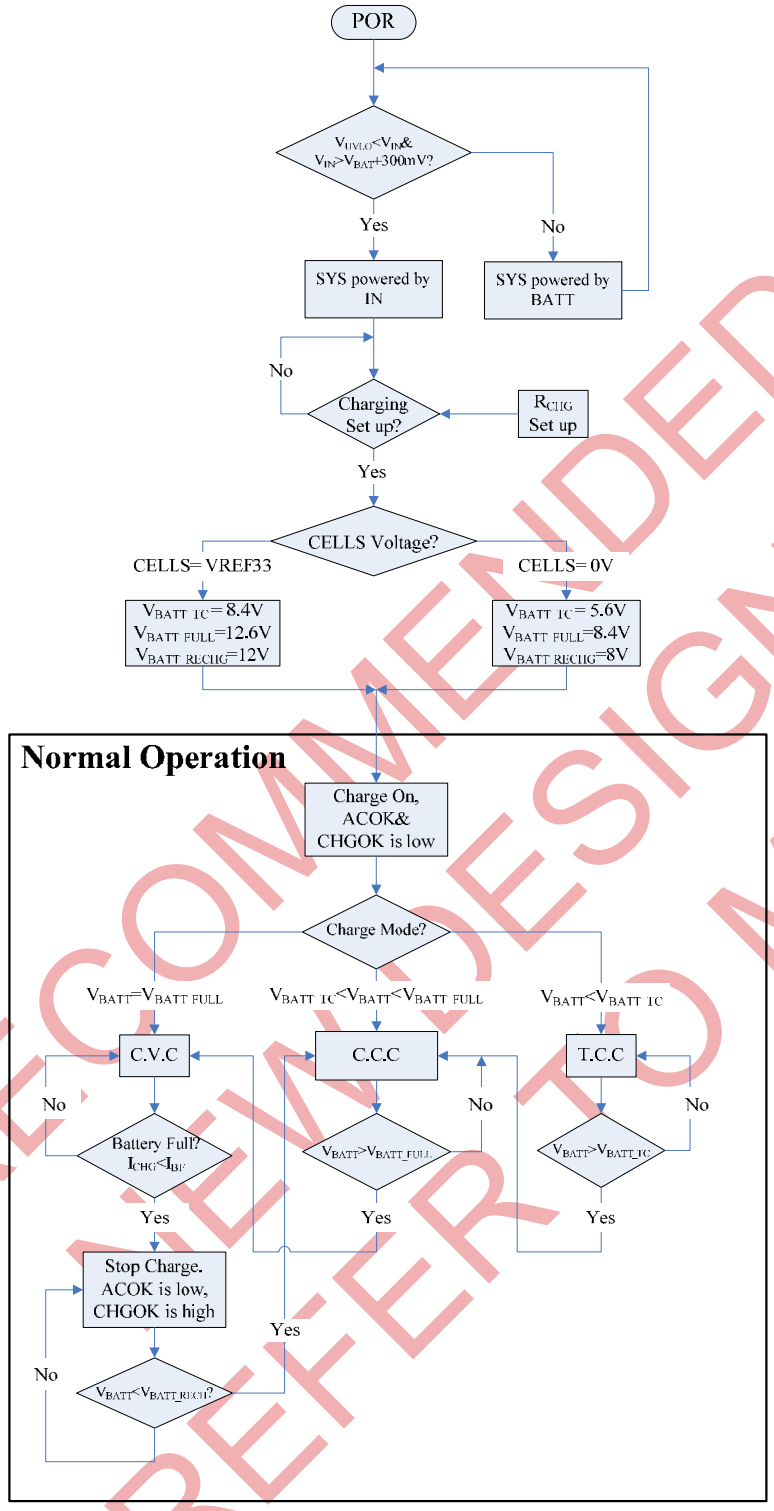


Figure 6— Normal Charging Operation Flow Chart

OPERATION FLOW CHART (*continued*)

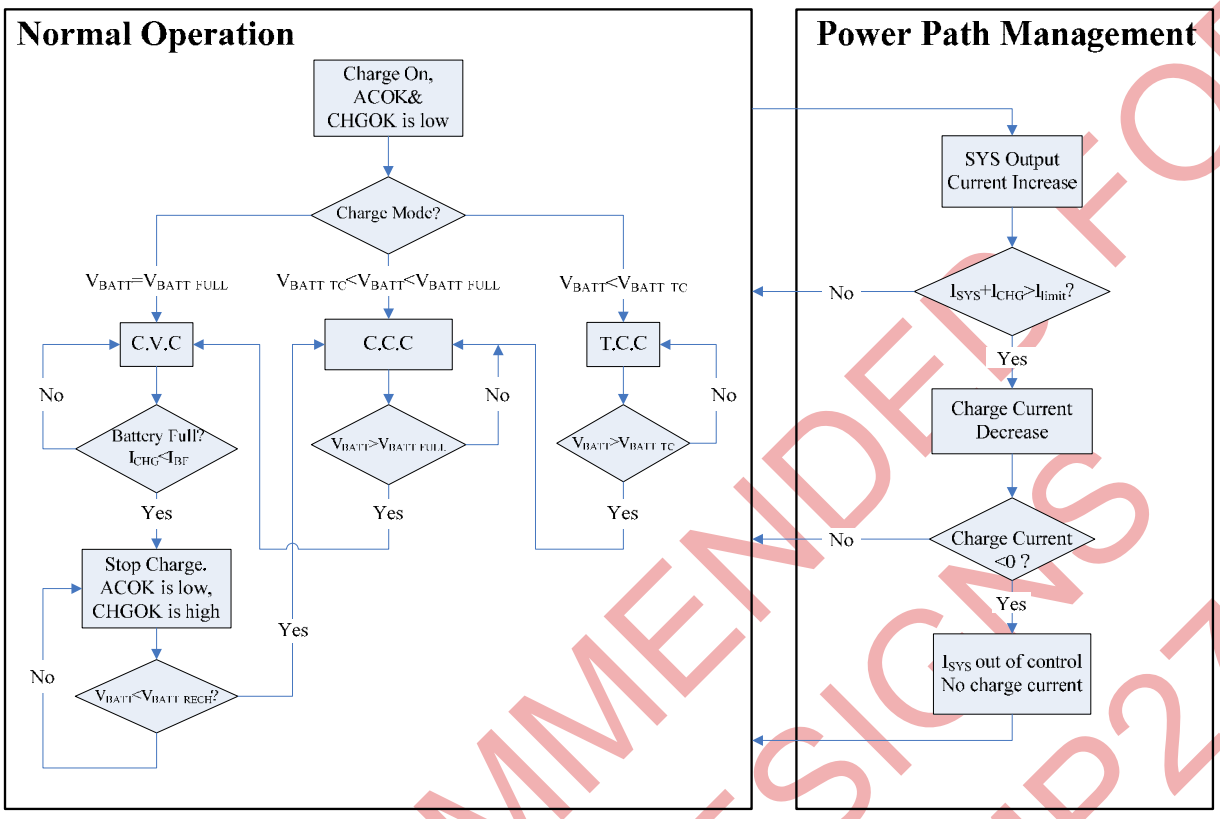


Figure 7— Power Path Management Operation Flow Chart

OPERATION FLOW CHART *(continued)*

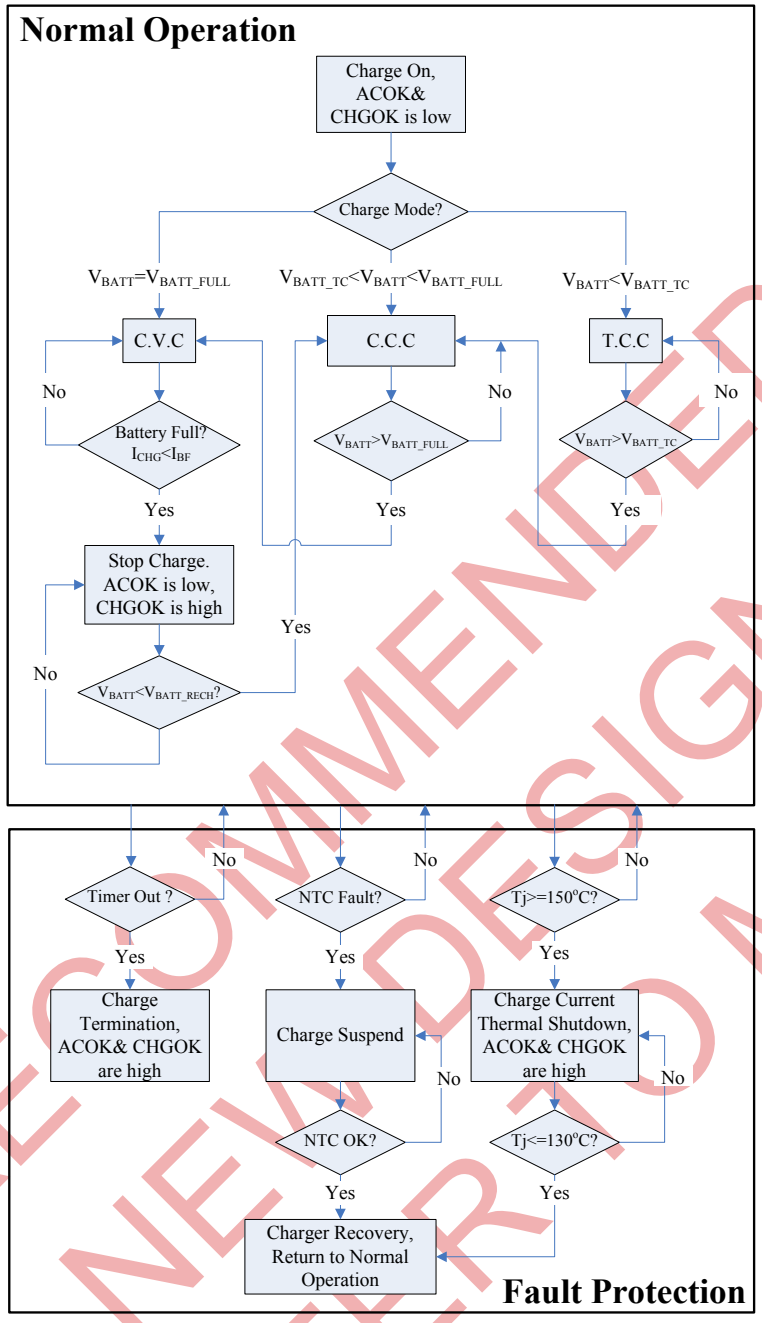


Figure 8— Fault Protection Flow Chart

APPLICATION INFORMATION

Setting the Charge Current

1. Standalone Switching Charger

The charge current of MP2612 is set by the sense resistor RS1 (Figure1). The charge current programmable formula is as following:

$$I_{CHG}(A)=\frac{200mV}{RS1(m\Omega)} \quad (1)$$

2. Switching Charger with Power Path Management

When MP2612 is applied together with MP8110, the charge current setting should be calibrated (Figure2).

Figure 8 shows MP8110 sensing the system current and feeding back to the MP2612.

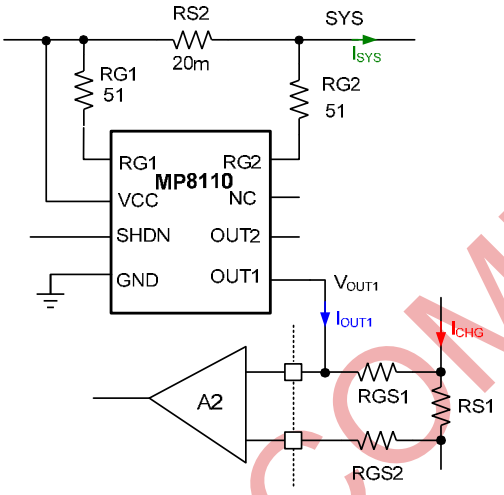


Figure 8— System Current Sensing Circuit

The gain of MP8110 is set as:

$$Gain=\frac{RGS1}{RG1} \quad (2)$$

The voltage of OUT1 pin, V_{OUT1} can be calculated from:

$$V_{OUT1}=I_{SYS}\times RS2\times Gain=\frac{I_{SYS}\times RS2\times RGS1}{RG1} \quad (3)$$

When the system current increased ΔI_{SYS}, to satisfy the charge current decreased ΔI_{SYS} accordingly, the relationship should be:

$$\Delta I_{BAT}=\frac{\Delta V_{OUT1}}{RS1}=\frac{\Delta I_{SYS}\times RS2\times RGS1}{RS1\times RG1} \quad (4)$$

Because $\Delta I_{SYS}=\Delta I_{BATT}$, we can get:

$$\frac{RS1}{RS2}=\frac{RGS1}{RG1} \quad (5)$$

$R_{GS1/2}$ causes charge current sense error as it changes the sense gain of A2, which can be calculated from:

$$G_{A2}=\frac{12.3(k\Omega)}{2(k\Omega)+RGS(k\Omega)} \quad (6)$$

The charge current is set as:

$$I_{CHG}(A)=\frac{1230}{G_{A2}\times RS1(m\Omega)} \quad (7)$$

Then the influence of R_{GS1} to the charge current is:

$$I_{CHG}(A)=\frac{2000+RGS(\Omega)}{10\times RS1(m\Omega)} \quad (8)$$

To decrease the power loss of the sensing circuit, choose RS2 as small as possible, 20m is recommended. Too small R_{G1} results in too big current sense error of MP8110, 50Ω is at least.

Substitute these two values into equation (5), then the calibrated charge current set formula in power path application is got from equation (8):

$$I_{CHG}(A)=\frac{2000+2.5\times RS1(m\Omega)}{10\times RS1(m\Omega)} \quad (9)$$

Following table is the calculated RS1 and R_{GS1} value for setting different charge current.

Table2—I_{CHG} Set in Power Path Application

I_{CHG}(A)	R_{GS}(Ω)	RS1(mΩ)
2	280	110
1.5	402	160
1	665	260
0.8	909	360
0.5	2k	800

If choose different RS2 and R_{G1}, re-calculated from equation (5) and equation (8), then get the different equation (9) and the table.

Also, any relationship between ΔI_{SYS} and ΔI_{BATT} can be realized by re-calculate equation (4),(5) and (8).

Selecting the Inductor

A 1μH to 10μH inductor is recommended for most applications. The inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (10)$$

Where ΔI_L is the inductor ripple current. V_{OUT} is the 2/3 cell battery voltage.

Choose inductor current to be approximately 30% if the maximum charge current, 2A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{CHG} + \frac{\Delta I_L}{2} \quad (11)$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

For optimized efficiency, the inductor DC resistance is recommended to be less than 200mΩ.

NTC Function

As Figure 9 shows, the low temperature threshold and high temperature threshold are preset internally via a resistive divider, which are 73%·VREF33 and 30%·VREF33. For a given NTC thermistor, we can select appropriate R3 and R6 to set the NTC window.

In detail, for the thermistor (NCP18XH103) noted in above electrical characteristic,

At 0ºC, R_{NTC_Cold} = 27.445k;

At 50ºC, R_{NTC_Hot} = 4.1601k.

Assume that the NTC window is between 0ºC and 50ºC, the following equations could be derived:

$$\frac{R6//R_{NTC\_Cold}}{R3 + R6//R_{NTC\_Cold}} = \frac{V_{TH\_Low}}{VREF33} = 73\% \quad (12)$$

$$\frac{R6//R_{NTC\_Hot}}{R3 + R6//R_{NTC\_Hot}} = \frac{V_{TH\_High}}{VREF33} = 30\% \quad (13)$$

According to equation (12) and equation (13), we can find that R3 = 9.63k and R6 = 505k.

To be simple in project, making R3=10k and R6 no connect will approximately meet the specification.

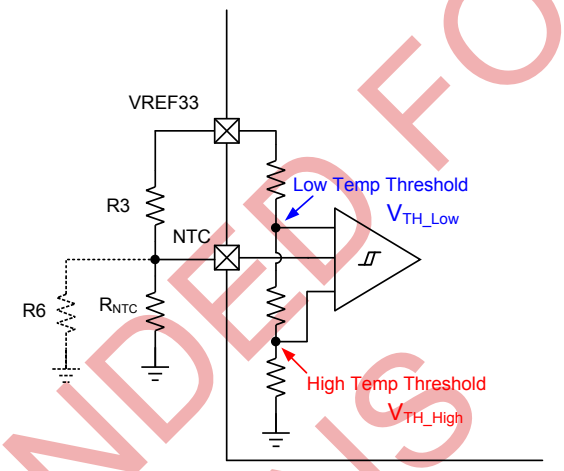


Figure 9— NTC function block

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input and also the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high frequency switching current passing to the input. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 4.7μF capacitor is sufficient.

Selecting the Output Capacitor

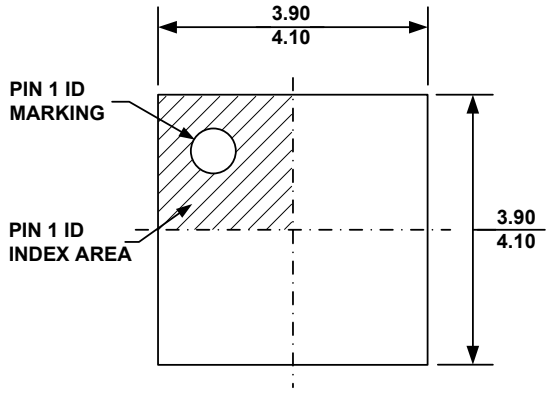
The output capacitor keeps output voltage ripple small and ensures regulation loop stability. The output capacitor impedance should be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended.

PC Board Layout

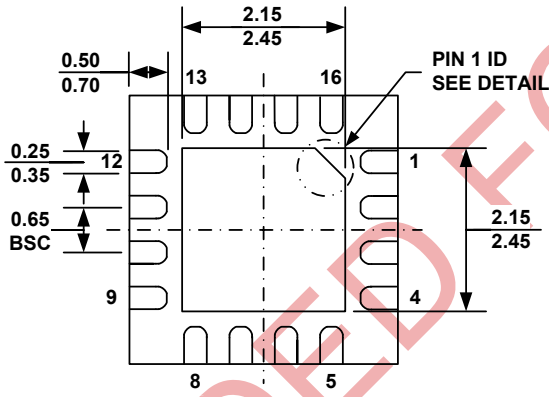
The high frequency and high current paths (GND, IN and SW) should be placed to the device with short, direct and wide traces. The input capacitor needs to be as close as possible to the IN and GND pins. The external feedback resistors should be placed next to the FB pin. Keep the switching node SW short and away from the feedback network.

PACKAGE INFORMATION

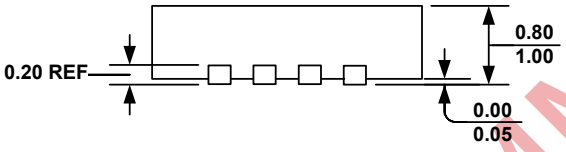
QFN16 (4mm x 4mm)



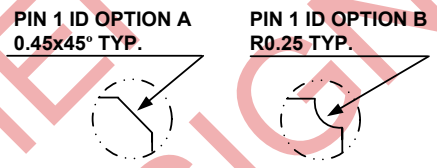
TOP VIEW



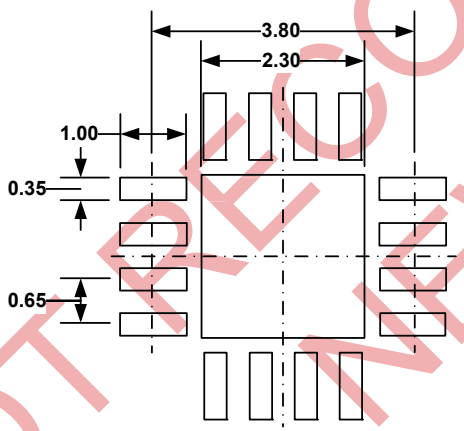
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-220, VARIATION VGGC.
5) DRAWING IS NOT TO SCALE.