19-2617; Rev 1; 12/02

MAXIM

Differential 5:1 or 4:1 ECL/PECL Multiplexers with Single/Dual Output Buffers

General Description

The MAX9386/MAX9387/MAX9388 are fully differential, high-speed, low-jitter ECL/PECL multiplexers (muxes) with output buffer(s). The devices are designed for clock-and-data distribution applications, and feature extremely low propagation delays (318ps, typ) and output-to-output skews (3.9ps, typ). The MAX9386 is a 5:1 mux with a single output buffer. The MAX9387 is a 5:1 mux with dual output buffers, and is intended for use in redundant systems. The MAX9388 is a 4:1 mux with a single output buffer, and is pin compatible with the MC100EP57.

Three single-ended select inputs, SEL0, SEL1, and SEL2, control the mux function on the MAX9386/MAX9387. The MAX9388 has two select inputs, SEL0 and SEL1. The mux select inputs are compatible with ECL/PECL logic, and are internally referenced to the on-chip output V_{BB}, nominally V_{CC} - 1.425V. The select inputs accept signals between V_{CC} and V_{EE}. Internal pulldowns to V_{EE} ensure a low-default condition if the select inputs are left open.

The differential inputs D_, $\overline{D}$_ can be configured to accept a single-ended signal when the unused complementary input is connected to the on-chip reference output V_{BB}. All the differential inputs have internal bias and clamping circuits that ensure low-default output states when the inputs are left open.

The MAX9386/MAX9387/MAX9388 operate with a wide supply range $|V_{CC} - V_{EE}|$ of 2.375V to 5.5V. The MAX9386/MAX9388 are offered in 20-pin TSSOP and QSOP packages. The MAX9387 is offered in 24-pin TSSOP and QSOP packages.

Applications

High-Speed Telecom and Datacom Applications

Central Office Backplane Clock Distribution

DSLAM/DLC

Features

- **318ps (typ) Propagation Delay**
- **>2.7GHz Toggle Frequency**
- **0.3ps(RMS) Random Jitter**
- **<14ps (max) at +25°C Output-to-Output Skew (MAX9387)**
- **-2.375V to -5.5V Supplies for Differential LVECL/ECL**
- **+2.375V to +5.5V Supplies for Differential LVPECL/PECL**
- **Outputs Low for Open Inputs**
- **Dual Output Buffers (MAX9387)**
- **Pin Compatible with MC100EP57 (MAX9388EUP)**
- **>2kV ESD Protection (Human Body Model)**

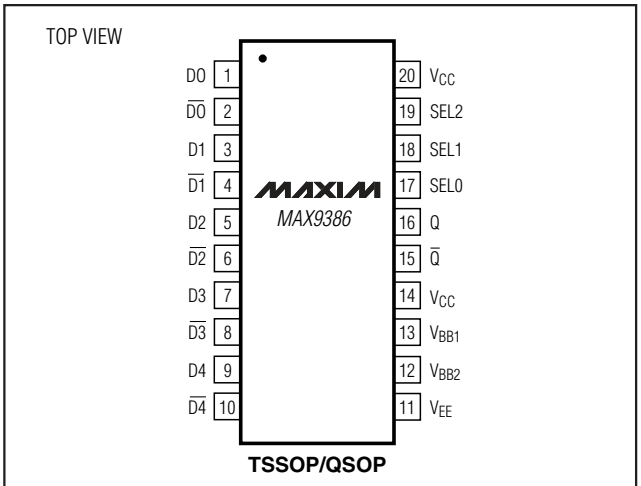
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	SELECTION
MAX9386EUP	-40°C to +85°C	20 TSSOP	5:1 mux with 1 output buffer
MAX9386EEP*	-40°C to +85°C	20 QSOP	5:1 mux with 1 output buffer

Ordering Information continued at end of data sheet.

**Future product—contact factory for availability.*

Pin Configurations



Pin Configurations continued at end of data sheet.

Differential 5:1 or 4:1 ECL/PECL Multiplexers with Single/Dual Output Buffers

ABSOLUTE MAXIMUM RATINGS

V_{CC} - V_{EE} ..... -0.3V to +6.0V
Inputs (D_, $\overline{D}$_, SEL_) to V_{EE} ..... -0.3V to (V_{CC} + 0.3V)
D_ to $\overline{D}$_ ..... ±3.0V
Continuous Output Current 50mA
Surge Output Current 100mA
V_{BB}_ Sink/Source Current ..... ±600µA
Continuous Power Dissipation (T_A = +70°C)
20-Lead TSSOP (derate 11.0mW/°C above +70°C) 880mW
θ_{JA} in Still Air ..... +91°C/W
θ_{JC} ..... +20°C/W
24-Lead TSSOP (derate 12.2mW/°C above +70°C) 976mW
θ_{JA} in Still Air ..... +82°C/W
θ_{JC} ..... +15°C/W
20-Lead QSOP (derate 9.1mW/°C above +70°C) 727mW
θ_{JA} in Still Air ..... +110°C/W
θ_{JC} ..... +34°C/W
24-Lead QSOP (derate 9.5mW/°C above +70°C) 762mW
θ_{JA} in Still Air ..... +105°C/W
θ_{JC} ..... +34°C/W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
ESD Protection
Human Body Model ($\overline{D}$_, D_, Q_, $\overline{Q}$_, SEL_, V_{BB}_) ..... ≥2kV
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = 2.375V to 5.5V, outputs loaded with 50Ω ±1% to V_{CC} - 2V. Typical values are at V_{CC} - V_{EE} = 3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, unless otherwise noted.) (Notes 1–4)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT (D_, $\overline{D}$_, SEL_)												
Single-Ended Input High Voltage	V_{IH}	V_{BB} connected to the unused input (Figure 1)	V_{CC} - 1.225		V_{CC} - 0.880	V_{CC} - 1.225		V_{CC} - 0.880	V_{CC} - 1.225		V_{CC} - 0.880	V
Single-Ended Input Low Voltage	V_{IL}	V_{BB} connected to the unused input (Figure 1)	V_{CC} - 1.945		V_{CC} - 1.625	V_{CC} - 1.945		V_{CC} - 1.625	V_{CC} - 1.945		V_{CC} - 1.625	V
Differential Input High Voltage	V_{IHD}	Figure 1	V_{EE} + 1.2		V_{CC}	V_{EE} + 1.2		V_{CC}	V_{EE} + 1.2		V_{CC}	V
Differential Input Low Voltage	V_{ILD}	Figure 1	V_{EE}		V_{CC} - 0.095	V_{EE}		V_{CC} - 0.095	V_{EE}		V_{CC} - 0.095	V
Differential Input Voltage	V_{IHD} - V_{ILD}	Figure 1, V_{CC} - V_{EE} < 3.0V	0.095		V_{CC} - V_{EE}	0.095		V_{CC} - V_{EE}	0.095		V_{CC} - V_{EE}	V
		Figure 1, V_{CC} - V_{EE} ≥ 3.0V	0.095		3.000	0.095		3.000	0.095		3.000	
Input Current	I_{IN}	V_{IH}, V_{IL}, V_{IHD}, V_{ILD}	-100		+100	-100		+100	-100		+100	µA

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} - V_{EE} = 2.375V to 5.5V, outputs loaded with 50Ω ±1% to V_{CC} - 2V. Typical values are at V_{CC} - V_{EE} = 3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, unless otherwise noted.) (Notes 1–4)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT (Q_, $\overline{Q}$_)												
Single-Ended Output High Voltage	V_{OH}	Figure 2	V_{CC} - 1.145		V_{CC} - 0.895	V_{CC} - 1.145		V_{CC} - 0.895	V_{CC} - 1.145		V_{CC} - 0.895	V
Single-Ended Output Low Voltage	V_{OL}	Figure 2	V_{CC} - 1.945		V_{CC} - 1.695	V_{CC} - 1.945		V_{CC} - 1.695	V_{CC} - 1.945		V_{CC} - 1.695	V
Differential Output Voltage	V_{OH} - V_{OL}	Figure 2	650	830		650	840		650	840		mV
REFERENCE OUTPUT (V_{BB}_)												
Reference Voltage Output	V_{BB1}, V_{BB2}	I_{BB1} + I_{BB2} = ±0.5mA (Note 5)	V_{CC} - 1.525	V_{CC} - 1.425	V_{CC} - 1.325	V_{CC} - 1.525	V_{CC} - 1.425	V_{CC} - 1.325	V_{CC} - 1.525	V_{CC} - 1.425	V_{CC} - 1.325	V
POWER SUPPLY												
Supply Current (Note 6)	I_{EE}	MAX9386		34	50		36	50		38	50	mA
		MAX9387		40	60		42	60		45	60	
		MAX9388		31	47		33	47		35	47	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = 2.375V to 5.5V, outputs loaded with 50Ω ±1% to V_{CC} - 2V, V_{IHD} - V_{ILD} = 0.15V to 1V, f_{IN} ≤ 2.5GHz input duty cycle = 50%, input transition time = 125ps (20% to 80%). Typical values are at V_{CC} - V_{EE} = 3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, f_{IN} = 622MHz, input duty cycle = 50%, input transition time = 125ps (20% to 80%), unless otherwise noted.) (Note 7)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Differential Input-to-Output Delay	t_{PLHD}, t_{PHLD}	Figure 2	222	309	377	238	318	395	254	333	431	ps
SEL_-to-Output Delay	t_{PLH2}, t_{PHL2}	Figure 4, input transition time = 500ps (20% to 80%) (Note 8)			1.64			1.4			1.6	ns
Output-to-Output Skew	t_{SKOO}	MAX9387 only, Figure 5 (Note 9)		3.9	26		3.9	14		8.0	26	ps
Input-to-Output Skew	t_{SKIO}	Figure 6 (Note 10)		7.3	53		7.7	50		8.3	50	ps
Part-to-Part Skew	t_{SKPP}	(Note 11)			111			130			133	ps

Differential 5:1 or 4:1 ECL/PECL Multiplexers with Single/Dual Output Buffers

AC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} - V_{EE} = 2.375V to 5.5V, outputs loaded with 50Ω ±1% to V_{CC} - 2V, V_{IHD} - V_{ILD} = 0.15V to 1V, f_{IN} ≤ 2.5GHz input duty cycle = 50%, input transition time = 125ps (20% to 80%). Typical values are at V_{CC} - V_{EE} = 3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, f_{IN} = 622MHz, input duty cycle = 50%, input transition time = 125ps (20% to 80%), unless otherwise noted.) (Note 7)

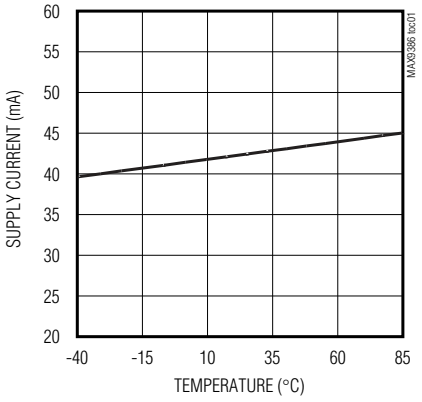
PARAMETER	SYMBOL	CONDITIONS		-40°C			+25°C			+85°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Added Random Jitter (Note 12)	t_{RJ}	Clock pattern	f_{IN} = 156MHz		0.3	1.15		0.3	1.15		0.3	1.15	ps(RMS)
			f_{IN} = 622MHz		0.3	1.15		0.3	1.15		0.3	1.15	
			f_{IN} = 2.5GHz		0.3	1.15		0.3	1.15		0.3	1.15	
Added Deterministic Jitter (Note 12)	T_{DJ}	PRBS 2^{23} - 1	f_{IN} = 156Mbps		33	95		33	95		33	95	ps_{P-P}
			f_{IN} = 622Mbps		21	61		21	61		21	61	
Switching Frequency	f_{MAX}	V_{OH} - V_{OL} ≥ 300mV, Figure 2		2.7			2.7			2.7			GHz
Select Toggle Frequency	f_{SEL}			100			100			100			MHz
Output Rise and Fall Time (20% to 80%)	t_R, t_F	Figure 2		67	105	138	74	117	155	81	128	165	ps

Note 1: Measurements are made with the device in thermal equilibrium.
Note 2: Current into an I/O pin is defined as positive. Current out of an I/O pin is defined as negative.
Note 3: DC parameters production tested at T_A = +25°C and guaranteed by design over the full operating temperature range.
Note 4: Single-ended data input operation using $V_{BB\_}$ is limited to (V_{CC} - V_{EE}) ≥ 3.0V.
Note 5: Use $V_{BB\_}$ only for inputs that are on the same device as the $V_{BB\_}$ reference.
Note 6: All pins open except V_{CC} and V_{EE}.
Note 7: Guaranteed by design and characterization. Limits are set at ±6 sigma.
Note 8: Measured from the 50% point of the input signal with the 50% point equal to V_{BB}, to the 50% point of the output signal.
Note 9: Measured between outputs of the same part at the signal crossing points for a same-edge transition.
Note 10: Measured between input-to-output paths of the same part at the signal crossing points for a same-edge transition of the differential input signal.
Note 11: Measured between outputs of different parts at the signal crossing points under identical conditions for a same-edge transition.
Note 12: Device jitter added to the differential input signal.

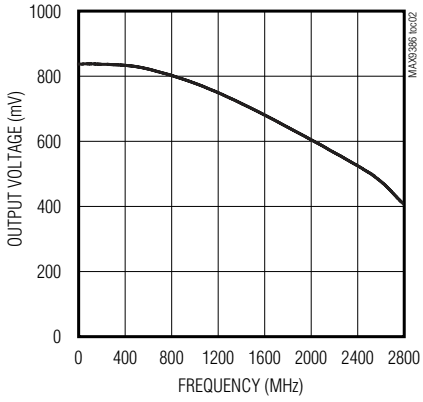
Typical Operating Characteristics

(V_{CC} - V_{EE} = 3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, outputs loaded with 50Ω ±1% to V_{CC} - 2V, f_{IN} = 1.5GHz, input duty cycle = 50%, input transition time = 125ps (20% to 80%), unless otherwise noted.)

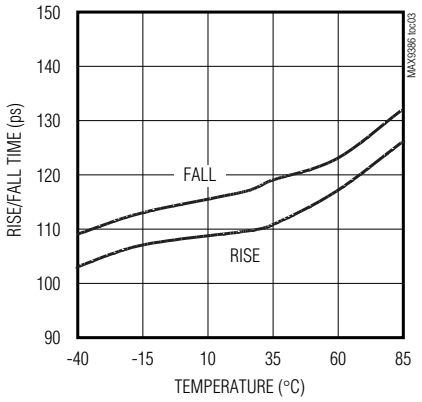
SUPPLY CURRENT (I_{EE}) vs. TEMPERATURE



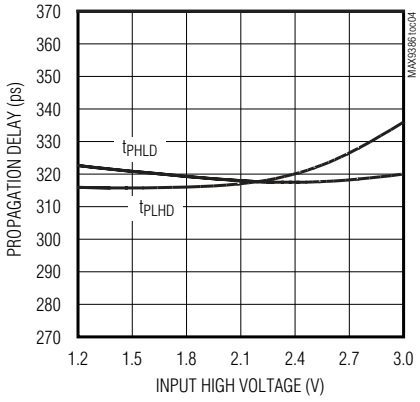
OUTPUT AMPLITUDE (V_{OH} - V_{OL}) vs. FREQUENCY



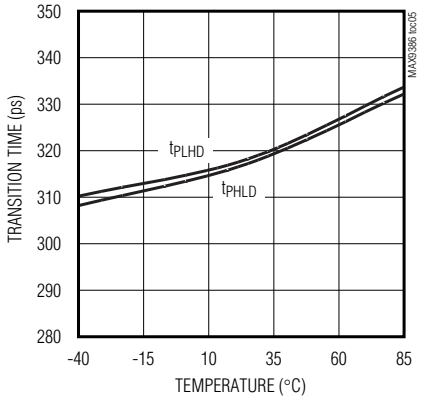
OUTPUT RISE/FALL vs. TEMPERATURE



DIFFERENTIAL PROPAGATION DELAY vs. INPUT HIGH VOLTAGE



DIFFERENTIAL PROPAGATION DELAY vs. TEMPERATURE



Differential 5:1 or 4:1 ECL/PECL Multiplexers with Single/Dual Output Buffers

MAX9386/MAX9388 Pin Description

PIN		NAME	FUNCTION
MAX9386	MAX9388		
1	2	D0	Noninverting Differential Input 0. Internal 250kΩ to V_{CC} and 150kΩ to V_{EE}.
2	3	$\overline{D0}$	Inverting Differential Input 0. Internal 150kΩ to V_{CC} and 150kΩ to V_{EE}.
3	4	D1	Noninverting Differential Input 1. Internal 250kΩ to V_{CC} and 150kΩ to V_{EE}.
4	5	$\overline{D1}$	Inverting Differential Input 1. Internal 150kΩ to V_{CC} and 150kΩ to V_{EE}.
5	6	D2	Noninverting Differential Input 2. Internal 250kΩ to V_{CC} and 150kΩ to V_{EE}.
6	7	$\overline{D2}$	Inverting Differential Input 2. Internal 150kΩ to V_{CC} and 150kΩ to V_{EE}.
7	8	D3	Noninverting Differential Input 3. Internal 250kΩ to V_{CC} and 150kΩ to V_{EE}.
8	9	$\overline{D3}$	Inverting Differential Input 3. Internal 150kΩ to V_{CC} and 150kΩ to V_{EE}.
9	—	D4	Noninverting Differential Input 4. Internal 250kΩ to V_{CC} and 150kΩ to V_{EE}.
10	—	$\overline{D4}$	Inverting Differential Input 4. Internal 150kΩ to V_{CC} and 150kΩ to V_{EE}.
11	10, 11	V_{EE}	Negative Supply
12	12	V_{BB2}	Reference Output Voltage 2. Connect to the inverting or noninverting data input to provide a reference for single-ended operation. When used, bypass V_{BB2} to V_{CC} with a 0.01µF ceramic capacitor. Otherwise leave open.
13	13	V_{BB1}	Reference Output Voltage 1. Connect to the inverting or noninverting data input to provide a reference for single-ended operation. When used, bypass V_{BB1} to V_{CC} with a 0.01µF ceramic capacitor. Otherwise leave open.
14, 20	1, 14 17, 20	V_{CC}	Positive Supply. Bypass each V_{CC} to V_{EE} with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
15	15	$\overline{Q}$	Inverting Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
16	16	Q	Noninverting Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
17	18	SEL0	Select Logic Input 0. Internal 120kΩ pulldown to V_{EE}.
18	19	SEL1	Select Logic Input 1. Internal 120kΩ pulldown to V_{EE}.
19	—	SEL2	Select Logic Input 2. Internal 120kΩ pulldown to V_{EE}.

MAX9387 Pin Description

PIN	NAME	FUNCTION
MAX9387		
1, 18, 24	V_{CC}	Positive Supply. Bypass each V_{CC} to V_{EE} with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
2	D0	Noninverting Differential Input 0. Internal 250kΩ to V_{CC} and 150kΩ to V_{EE}.
3	$\overline{D0}$	Inverting Differential Input 0. Internal 150kΩ to V_{CC} and 150kΩ to V_{EE}.
4	D1	Noninverting Differential Input 1. Internal 250kΩ to V_{CC} and 150kΩ to V_{EE}.
5	$\overline{D1}$	Inverting Differential Input 1. Internal 150kΩ to V_{CC} and 150kΩ to V_{EE}.
6	D2	Noninverting Differential Input 2. Internal 250kΩ to V_{CC} and 150kΩ to V_{EE}.
7	$\overline{D2}$	Inverting Differential Input 2. Internal 150kΩ to V_{CC} and 150kΩ to V_{EE}.
8	D3	Noninverting Differential Input 3. Internal 250kΩ to V_{CC} and 150kΩ to V_{EE}.
9	$\overline{D3}$	Inverting Differential Input 3. Internal 150kΩ to V_{CC} and 150kΩ to V_{EE}.
10	D4	Noninverting Differential Input 4. Internal 250kΩ to V_{CC} and 150kΩ to V_{EE}.
11	$\overline{D4}$	Inverting Differential Input 4. Internal 150kΩ to V_{CC} and 150kΩ to V_{EE}.
12, 13	V_{EE}	Negative Supply
14	V_{BB2}	Reference Output Voltage 2. Connect to the inverting or noninverting data input to provide a reference for single-ended operation. When used, bypass V_{BB2} to V_{CC} with a 0.01µF ceramic capacitor. Otherwise leave open.
15	V_{BB1}	Reference Output Voltage 1. Connect to the inverting or noninverting data input to provide a reference for single-ended operation. When used, bypass V_{BB1} to V_{CC} with a 0.01µF ceramic capacitor. Otherwise leave open.
16	$\overline{Q1}$	Inverting Output 1. Typically terminate with 50Ω resistor to V_{CC} - 2V.
17	Q1	Noninverting Output 1. Typically terminate with 50Ω resistor to V_{CC} - 2V.
19	$\overline{Q0}$	Inverting Output 0. Typically terminate with 50Ω resistor to V_{CC} - 2V.
20	Q0	Noninverting Output 0. Typically terminate with 50Ω resistor to V_{CC} - 2V.
21	SEL0	Select Logic Input 0. Internal 120kΩ pulldown to V_{EE}.
22	SEL1	Select Logic Input 1. Internal 120kΩ pulldown to V_{EE}.
23	SEL2	Select Logic Input 2. Internal 120kΩ pulldown to V_{EE}.

Differential 5:1 or 4:1 ECL/PECL Multiplexers with Single/Dual Output Buffers

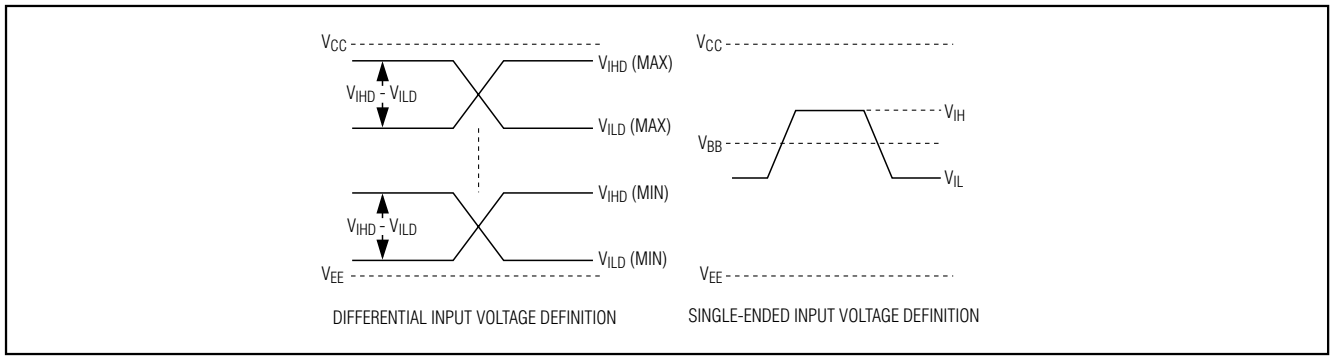


Figure 1. Input Definitions

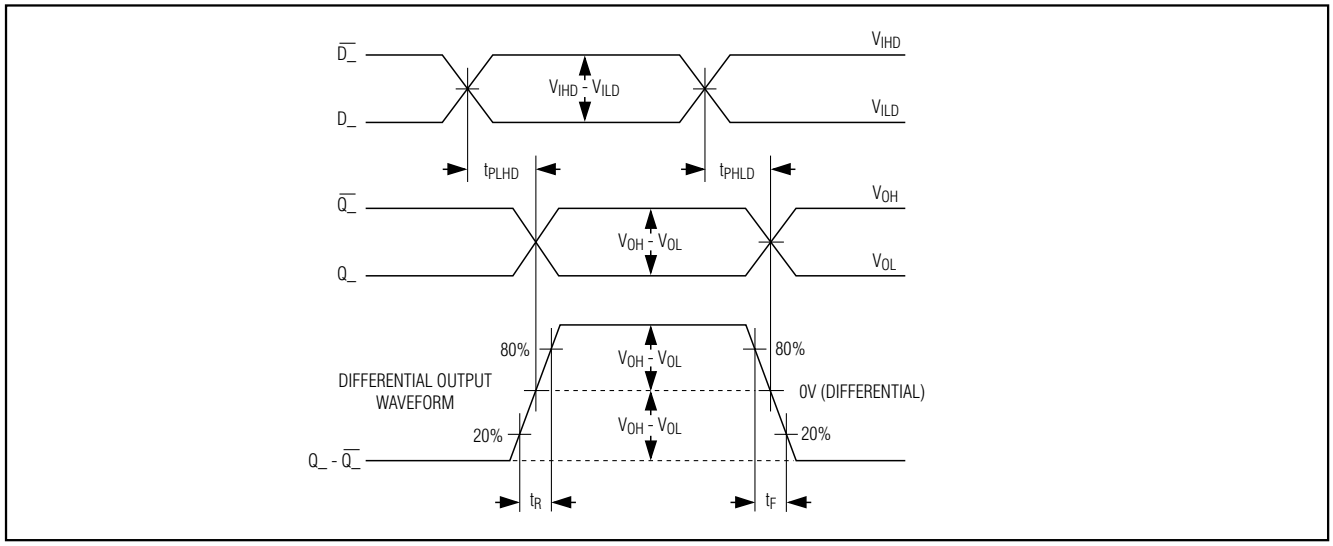


Figure 2. Differential Input-to-Output Propagation Delay Timing Diagram

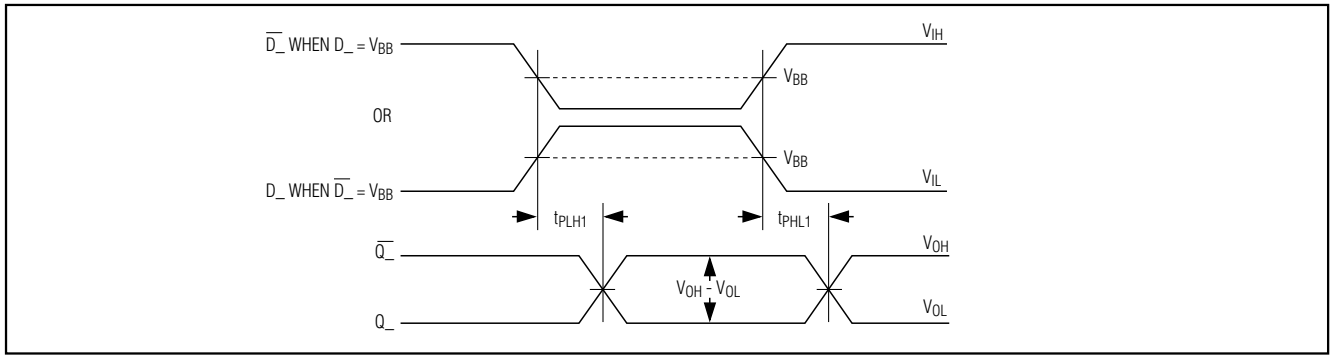


Figure 3. Single-Ended Input-to-Output Propagation Delay Timing Diagram

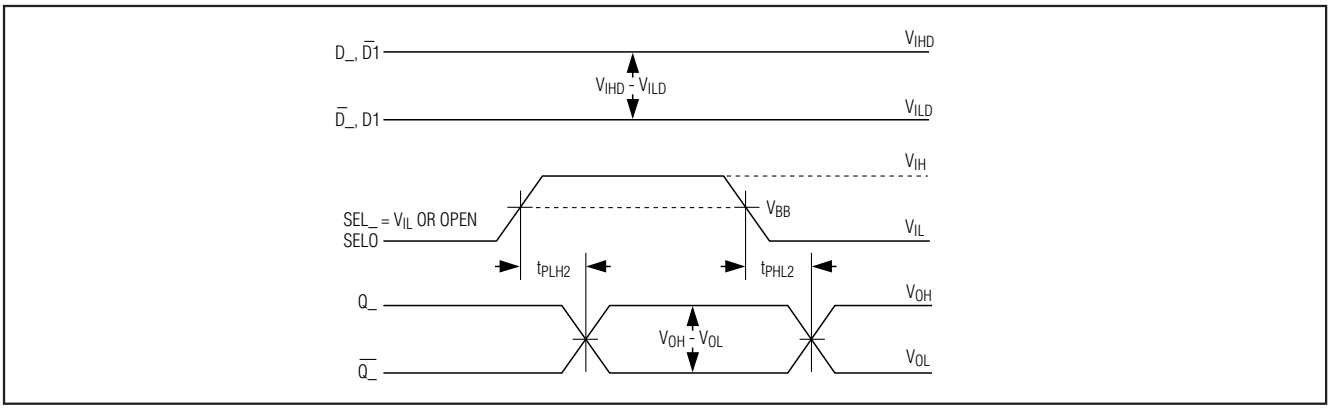


Figure 4. Select Input (SEL0)-to-Output (Q_, Q_) Delay Timing Diagram

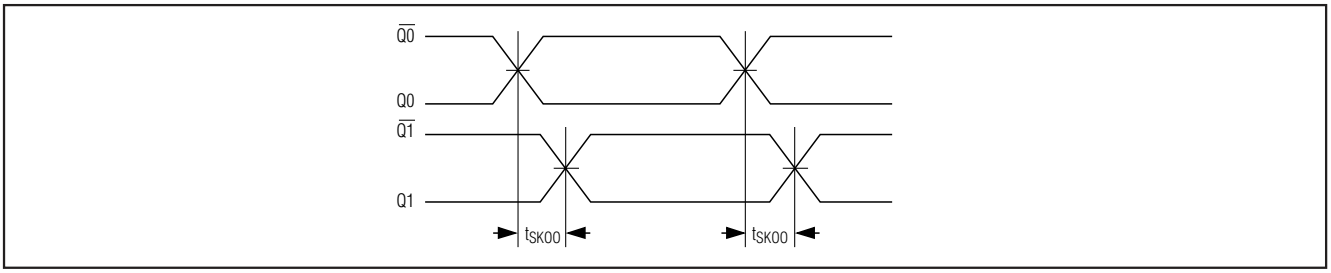


Figure 5. Output-to-Output Skew (t_{SKOO}) Definition (MAX9387 Only)

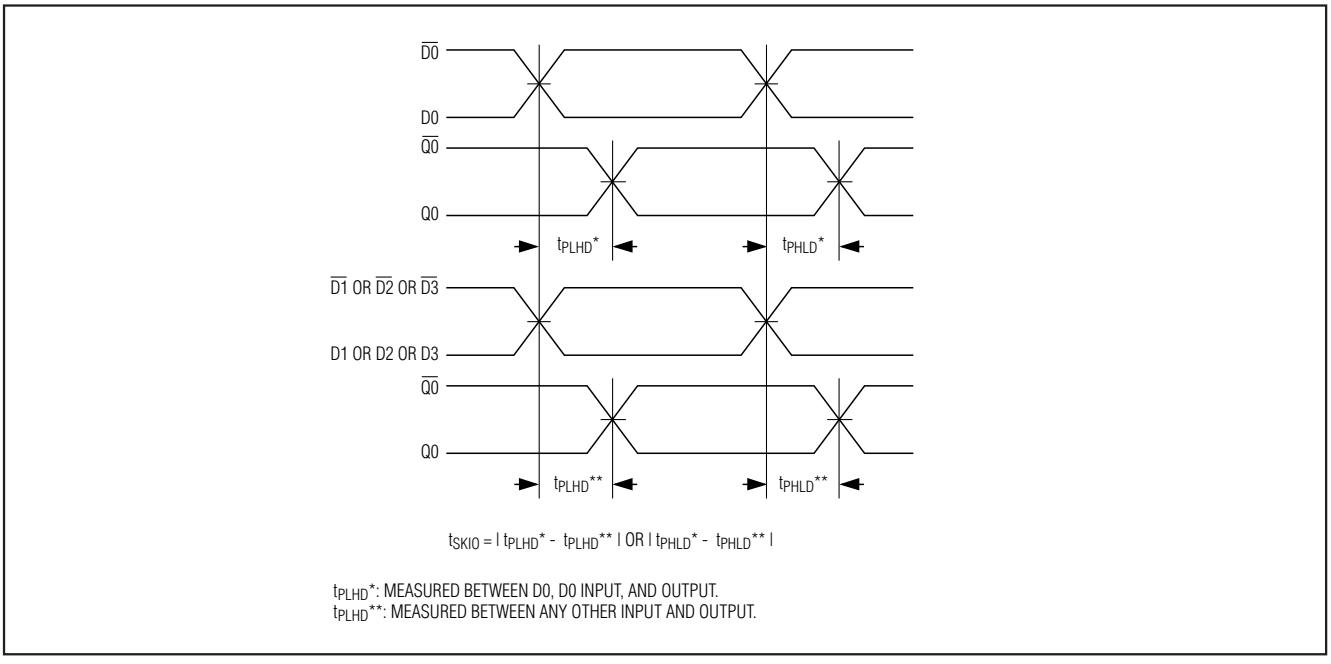


Figure 6. Input-to-Output Skew (t_{SKIO}) Definition

Differential 5:1 or 4:1 ECL/PECL Multiplexers with Single/Dual Output Buffers

Detailed Description

The MAX9386/MAX9387/MAX9388 are fully differential, high-speed, and low-jitter ECL/PECL muxes with output buffer(s). The devices are designed for clock-and-data distribution applications, and feature extremely low propagation delays (318ps, typ) and output-to-output skews (3.9ps, typ). The MAX9386 is a 5:1 mux with a single output buffer. The MAX9387 is a 5:1 mux with dual output buffers, and is intended for use in redundant systems. The MAX9388 is a 4:1 mux with a single output buffer, and is pin compatible with the MC100EP57.

Three single-ended select inputs, SEL0, SEL1, and SEL2, control the mux function on the MAX9386/MAX9387. The MAX9388 has two select inputs, SEL0 and SEL1 (see Tables 1 and 2). The mux select inputs are compatible with ECL/PECL logic, and are internally referenced to the on-chip output V_{BB}, nominally V_{CC} - 1.425V. The select inputs accept signals between V_{CC} and V_{EE}. Internal 120kΩ pulldowns to V_{EE} ensure a low default condition if the select inputs are left open, selecting the D0, $\overline{D0}$ input.

The differential inputs D, $\overline{D}$ can be configured to accept a single-ended signal when the unused complementary input is connected to the on-chip reference voltage V_{BB}. The reference output voltages, V_{BB1} and V_{BB2}, provide the reference voltage for single-ended operation for each mux. A single-ended input of at least $V_{BB\_}$ ±100mV or a differential input of at least 100mV switches the outputs to the V_{OH} and V_{OL} levels specified in the *DC Electrical Characteristics*. The maximum magnitude of the differential input from D to $\overline{D}$ is ±3.0V. This limit also applies to the difference between a single-ended input and any reference voltage input.

Specifications for the high and low voltages of a differential input (V_{IHD} and V_{ILD}) and the differential input voltage (V_{IHD} - V_{ILD}) apply simultaneously.

Single-Ended Operation

The recommended supply voltage for single-ended operation is 3.0V to 5.5V. The differential inputs (D, $\overline{D}$) can be configured to accept single-ended inputs when operating at supply voltages greater than 2.725V. In single-ended mode operation, the unused complementary input needs to be connected to the on-chip reference voltage, V_{BB}, as a reference. For example, the differential D, $\overline{D}$ input is converted to a noninverting, single-ended input by connecting V_{BB} to $\overline{D}$ and connecting the single-ended input to D. Similarly, an inverting input is obtained by connecting V_{BB} to D and connecting the single-ended input to $\overline{D}$. With a differential input configured as single ended (using V_{BB}), the single-ended input can be driven to V_{CC} or V_{EE} or with a single-ended LVPECL/LVECL signal.

In single-ended mode operation, a user must ensure that the supply voltage (V_{CC} - V_{EE}) is greater than 2.725V. This is because the input high minimum level must be at (V_{EE} + 1.2V) or higher for proper operation. The reference voltage, V_{BB}, must be at least (V_{EE} + 1.2V) for the same reason because it becomes the high-level input when a single-ended input swings below it. The minimum V_{BB} output for the MAX9386/MAX9387/MAX9388 is (V_{CC} - 1.38V). Substituting the minimum V_{BB} output for (V_{BB} = V_{EE} + 1.2V) results in a minimum supply (V_{CC} - V_{EE}) of 2.725V. Rounding up to standard supplies gives the recommended single-ended operating supply ranges (V_{CC} - V_{EE}) of 3.0V to 5.5V.

When using the V_{BB} reference output, bypass it with a 0.01µF ceramic capacitor to V_{CC}. If not used, leave it open. The V_{BB} reference can source or sink a total of 0.5mA (shared between V_{BB1} and V_{BB2}), which is sufficient to drive five inputs.

Table 1. Mux Select Input Truth Table for MAX9386/MAX9387

SEL2	SEL1	SEL0	DATA OUTPUT
L or open	L or open	L or open	D0*
L or open	L or open	H	D1
L or open	H	L or open	D2
L or open	H	H	D3
H	X	X	D4

**Default output when SEL0, SEL1, and SEL2 are left open.*

Table 2. Mux Select Input Truth Table for MAX9388

SEL1	SEL0	DATA OUTPUT
L or open	L or open	D0*
L or open	H	D1
H	L or open	D2
H	H	D3

**Default output when SEL0 and SEL1 are left open.*

Differential 5:1 or 4:1 ECL/PECL Multiplexers with Single/Dual Output Buffers

Applications Information

Output Termination

Terminate the outputs through 50Ω to V_{CC} - 2V or use equivalent Thevenin terminations. Terminate each Q and $\overline{Q}$ output with identical termination on each for minimal distortion. When a single-ended signal is taken from the differential output, terminate both Q and $\overline{Q}$.

Ensure that output currents do not exceed the current limits as specified in the *Absolute Maximum Ratings* table. Under all operating conditions, the device's total thermal limits should be observed.

Supply Bypassing

Bypass V_{CC} to V_{EE} with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors. For PECL, bypass each V_{CC} to V_{EE}. For ECL, bypass each V_{EE} to V_{CC}. Place the capacitors as close to the device as possible with the 0.01µF capacitor closest to the device pins.

Use multiple vias when connecting the bypass capacitors to ground. When using the V_{BB1} or V_{BB2} reference outputs, bypass each one with a 0.01µF ceramic capacitor to V_{CC}. If the V_{BB1} or V_{BB2} reference outputs are not used, they can be left open.

Traces

Circuit board trace layout is very important to maintain the signal integrity of high-speed differential signals. Maintaining integrity is accomplished in part by reducing signal reflections and skew, and increasing common-mode noise immunity.

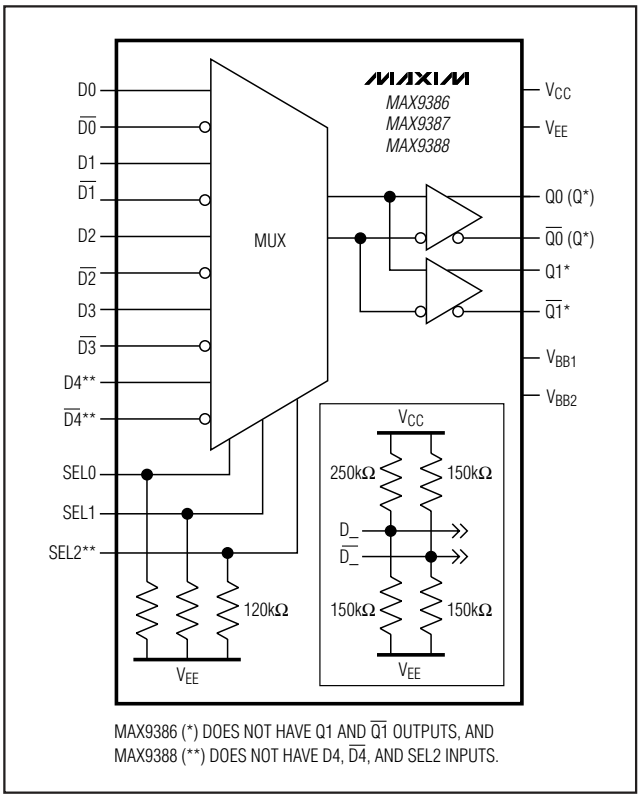
Signal reflections are caused by discontinuities in the 50Ω characteristic impedance of the traces. Avoid discontinuities by maintaining the distance between differential traces, not using sharp corners or using vias. Maintaining distance between the traces also increases common-mode noise immunity. Reducing signal skew is accomplished by matching the electrical length of the differential traces.

Chip Information

TRANSISTOR COUNT: 583

PROCESS: Bipolar

Functional Block Diagram



MAX9386 (*) DOES NOT HAVE Q1 AND $\overline{Q1}$ OUTPUTS, AND
MAX9388 (**) DOES NOT HAVE D4, $\overline{D4}$, AND SEL2 INPUTS.

Ordering Information (continued)

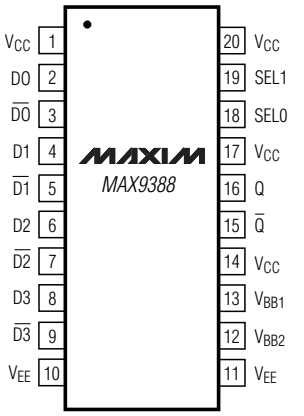
PART	TEMP RANGE	PIN-PACKAGE	SELECTION
MAX9387EUG	-40°C to +85°C	24 TSSOP	5:1 mux with 2 output buffers
MAX9387EEG*	-40°C to +85°C	24 QSOP	5:1 mux with 2 output buffers
MAX9388EUP	-40°C to +85°C	20 TSSOP	4:1 mux with 1 output buffer
MAX9388EEP*	-40°C to +85°C	20 QSOP	4:1 mux with 1 output buffer

**Future product—contact factory for availability.*

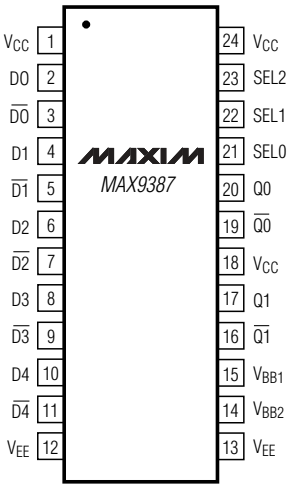
Differential 5:1 or 4:1 ECL/PECL Multiplexers with Single/Dual Output Buffers

Pin Configurations (continued)

TOP VIEW



TSSOP/QSOP

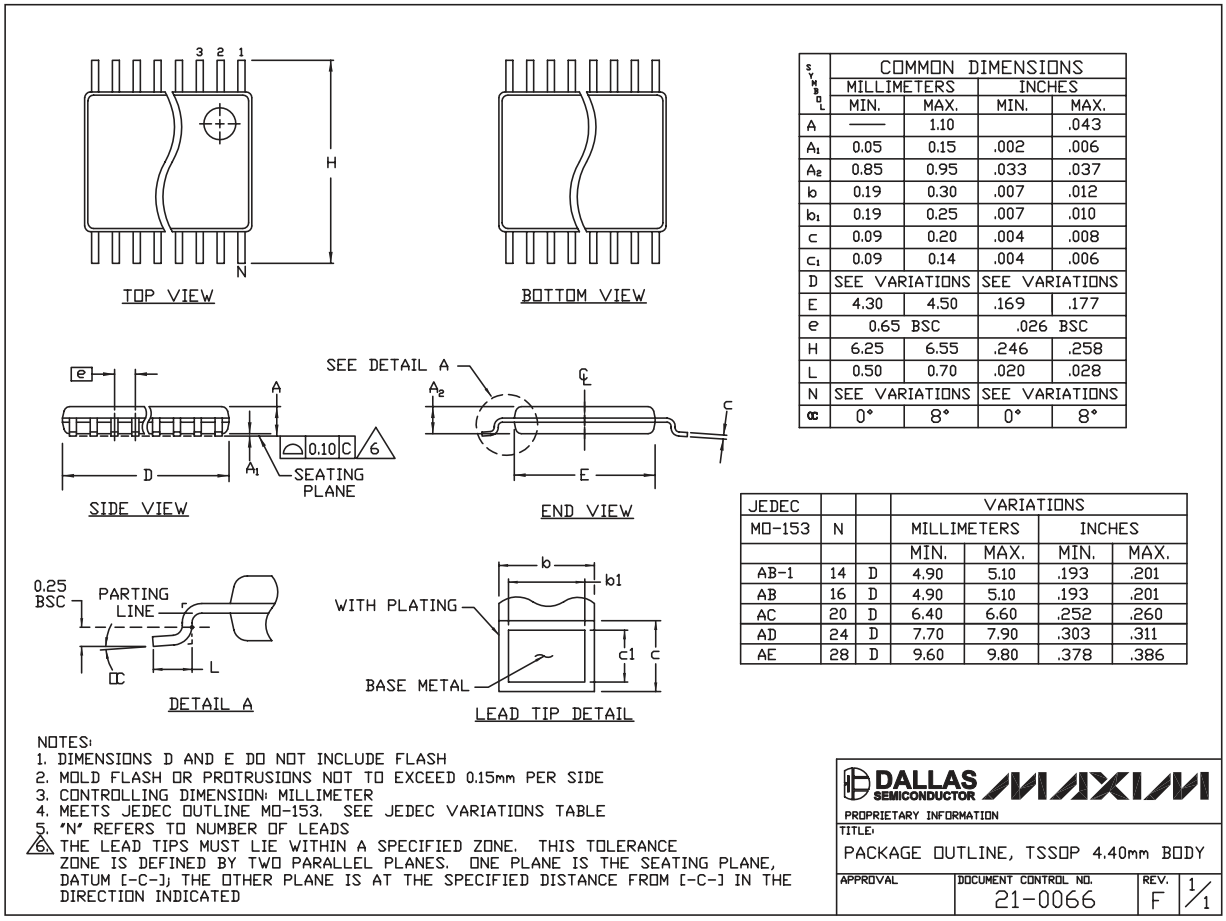


TSSOP/QSOP

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

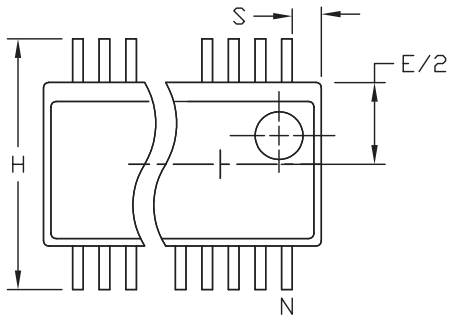
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	F	1/1

Differential 5:1 or 4:1 ECL/PECL Multiplexers with Single/Dual Output Buffers

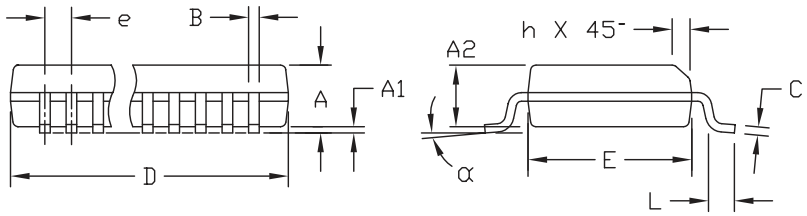
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	D	1/1