FAIRCHILD SEMICONDUCTOR™

June 1998

# FDC655AN

## Single N-Channel, Logic Level, PowerTrench™ MOSFET

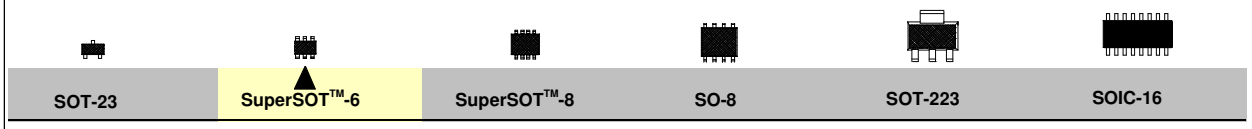
### General Description

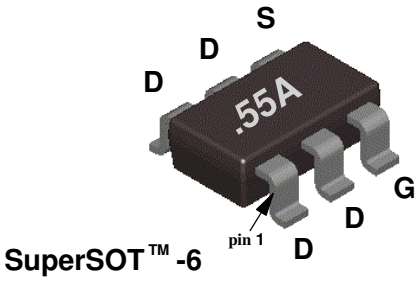
This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

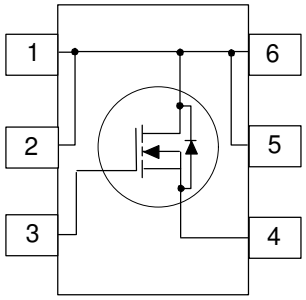
### Features

- 6.3 A, 30 V. $R_{DS(ON)}$ = 0.027 Ω @ $V_{GS}$ = 10 V
  $R_{DS(ON)}$ = 0.035 Ω @ $V_{GS}$ = 4.5 V.
- Fast switching.
- Low gate charge ( typical 9 nC).
- SuperSOT™-6 package: small footprint (72% smaller than SO-8); low profile (1mm thick); pin compatible with TSOP-6.




SuperSOT™ -6




**Absolute Maximum Ratings** $T_A$ = 25°C unless otherwise note

| Symbol | Parameter | | FDC655AN | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 30 | V |
| $V_{GSS}$ | Gate-Source Voltage - Continuous | | ±20 | V |
| $I_D$ | Drain Current - Continuous | (Note 1a) | 6.3 | A |
| | - Pulsed | | 20 | |
| $P_D$ | Maximum Power Dissipation | (Note 1a) | 1.6 | W |
| | | (Note 1b) | 0.8 | |
| $T_J$,$T_{STG}$ | Operating and Storage Temperature Range | | -55 to 150 | °C |
| **THERMAL CHARACTERISTICS** | | | | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 78 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 30 | °C/W |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 30 | | | V |
| $\Delta BV_{DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | $I_D$ = 250 µA, Referenced to 25 °C | | 23 | | mV /°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | | | 1 | µA |
| | | $T_J$ = 55°C | | | 10 | µA |
| $I_{GSSF}$ | Gate - Body Leakage, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | | | 100 | nA |
| $I_{GSSR}$ | Gate - Body Leakage, Reverse | $V_{GS}$ = -20 V, $V_{DS}$= 0 V | | | -100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 1 | 1.6 | 3 | V |
| $\Delta V_{GS(th)}/\Delta T_J$ | Gate Threshold VoltageTemp.Coefficient | $I_D$ = 250 µA, Referenced to 25 °C | | -4.2 | | mV /°C |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 6.3 A | | 0.023 | 0.027 | Ω |
| | | $T_J$ = 125°C | | 0.035 | 0.045 | |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 5.5 A | | 0.029 | 0.035 | |
| $I_{D(on)}$ | On-State Drain Current | $V_{GS}$ = 10 V, $V_{DS}$ = 5 V | 20 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 6.3 A | | 4.5 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, | | 830 | | pF |
| $C_{oss}$ | Output Capacitance | f = 1.0 MHz | | 185 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 80 | | pF |
| **SWITCHING CHARACTERISTICS** (Note 2) | | | | | | |
| $t_{D(on)}$ | Turn - On Delay Time | $V_{DD}$ = 15 V, $I_D$ = 1 A, | | 6 | 12 | ns |
| $t_r$ | Turn - On Rise Time | $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 10 | 18 | ns |
| $t_{D(off)}$ | Turn - Off Delay Time | | | 18 | 29 | ns |
| $t_f$ | Turn - Off Fall Time | | | 5 | 12 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 15 V, $I_D$ = 6.3 A, | | 9 | 13 | nC |
| $Q_{gs}$ | Gate-Source Charge | $V_{GS}$ = 5 V | | 2.8 | | nC |
| $Q_{gd}$ | Gate-Drain Charge | | | 3.1 | | nC |
| **DRAIN-SOURCE DIODE CHARACTERISTICS** | | | | | | |
| $I_S$ | Continuous Source Diode Current | | | | 1.3 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 1.3 A (Note 2) | | 0.73 | 1.2 | V |

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

   a. 78°C/W when mounted on a minimum on a 1 $in^2$ pad of 2oz Cu in FR-4 board.

   b. 156°C/W when mounted on a minimum pad of 2oz Cu in FR-4 board.

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

## Typical Electrical Characteristics

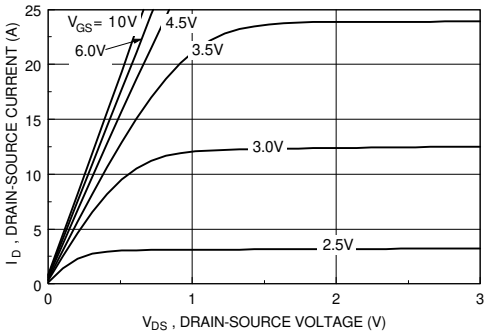



Figure 1. On-Region Characteristics.

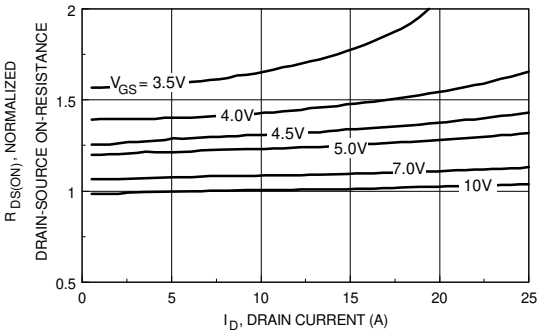



Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

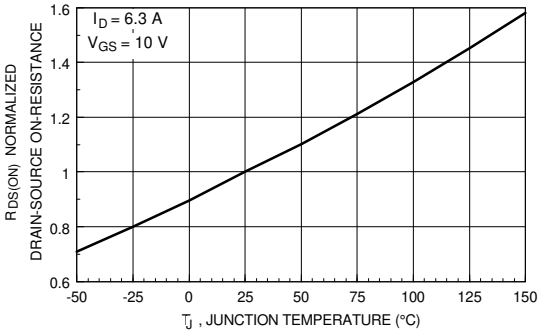



Figure 3. On-Resistance Variation with Temperature.

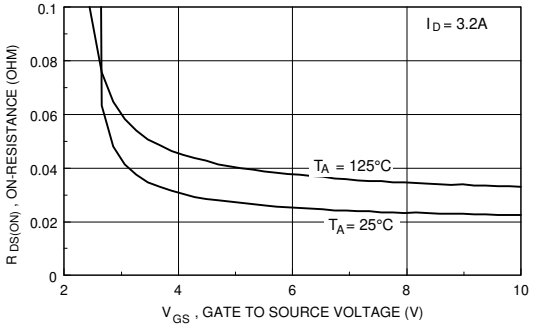



Figure 4. On-Resistance Variation with Gate-To-Source Voltage.

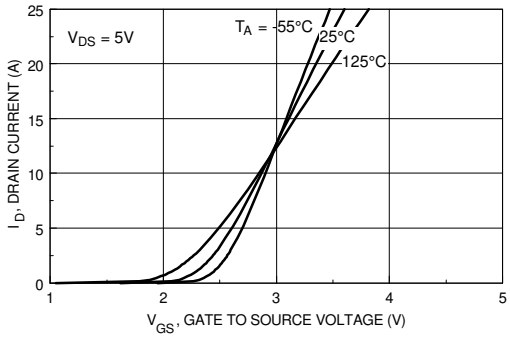



Figure 5. Transfer Characteristics.

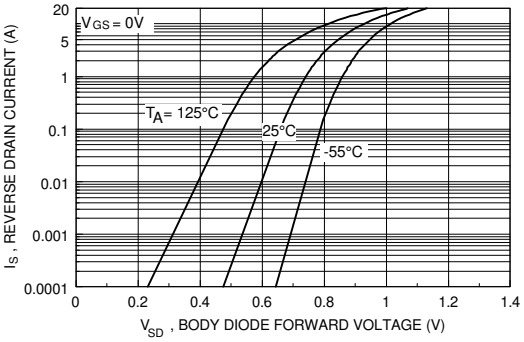



Figure 6. Body Diode Forward Voltage Variation with Source Current

## Typical Electrical Characteristics

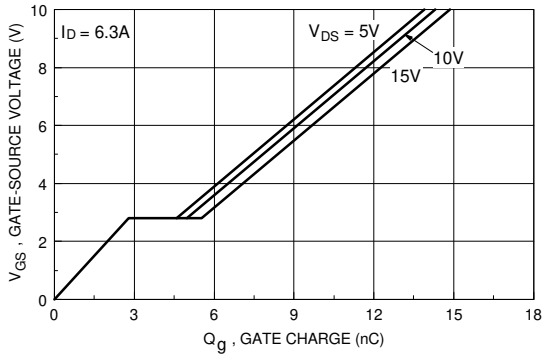



Figure 7. Gate Charge Characteristics.

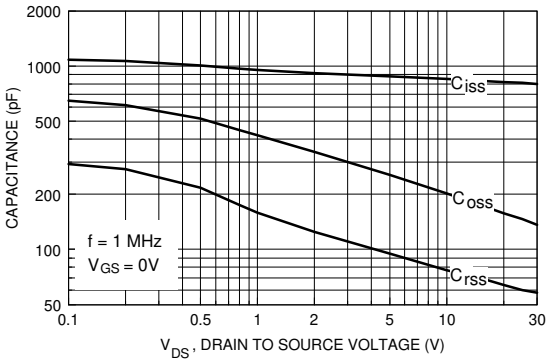



Figure 8. Capacitance Characteristics.

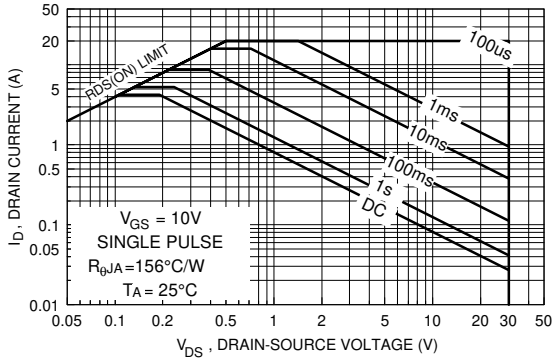



Figure 9. Maximum Safe Operating Area.

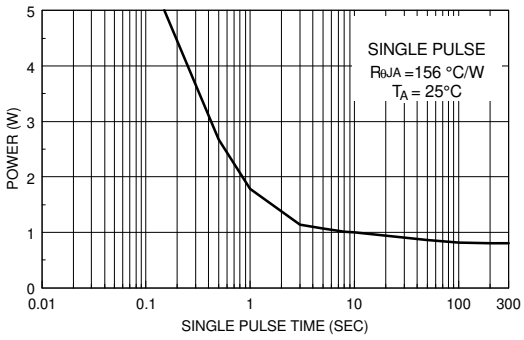



Figure 10. Single Pulse Maximum Power Dissipation.

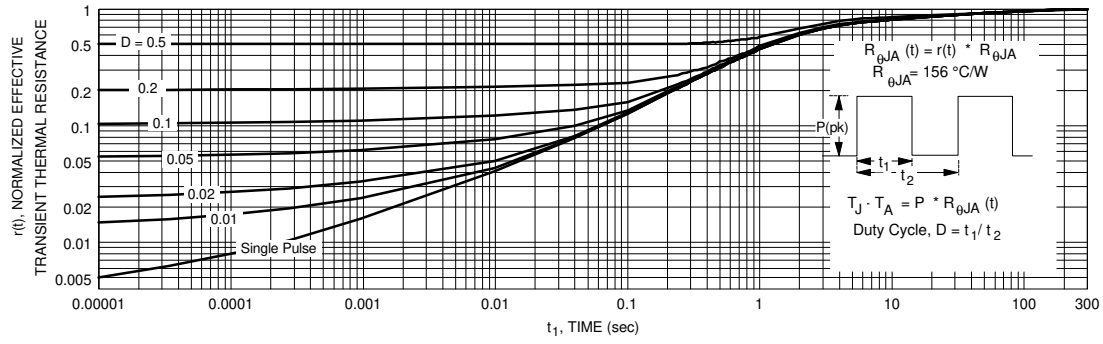



Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in note 1b.
Transient thermal response will change depending on the circuit board design.

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