User's Guide

TPS56C20 Buck Converter Evaluation Module User's Guide

ABSTRACT

This user's guide describes the characteristics, operation, and use of the TPS56C20EVM-614 evaluation module (EVM). The document includes performance specifications, test setup and results, the printed-circuit board (PCB) layout, a schematic, and a bill of materials (BOM).

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1 Introduction

The TPS56C20 is a synchronous DC-DC converter. The TPS56C20 is a buck converter whose output voltage can be adjusted using the feedback resistor divider network or using VID commands from an I2C interface bus. It is a single, adaptive on-time, D-CAP2™ mode converter requiring a very low external component count. The D-CAP2 control circuit is optimized for low-ESR output capacitors such as POSCAP or SP-CAP, or ceramic types. The D-CAP2 control circuit features fast transient response with no external compensation. The reference design internally sets the switching frequency at a nominal 500 kHz. The design integrates the high- and low-side switching MOSFETs and the gate drive circuitry. The low drain-to-source on resistance of the MOSFETs allows the TPS56C20 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The TPS56C20 DC/DC synchronous converter provides up to a 12-A output from an input voltage source of 4.5 V to 17 V. The output voltage range is from 0.6 V to 1.87 V. The rated input voltage and output current range for the evaluation module are given in Table 1-1.

The TPS56C20EVM-614 evaluation module is a single, synchronous buck converter providing 1.1 V at 12 A from 4.5-V to 17-V input.

Table 1-1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS56C20EVM-614	VIN = 4.5V to 17V	0A to 12A

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2 Performance Specification Summary

A summary of the TPS56C20EVM-614 performance specifications is provided in Table 2-1. Specifications are given for an input voltage of VIN = 12V and an output voltage of 1.1V, unless otherwise noted. The ambient temperature is 25°C for all measurement, unless otherwise noted.

Table 2-1. TPS56C20EVM-614 and Performance Specifications Summary

Parameter	Test Conditions	Min	Typ	Max	Units
Input voltage range (V_{IN})		4.5	12	17	V
Output voltage			1.1		V
Operating frequency	V_{IN} = 12 V, I_O = 12 A		500		kHz
Output current range		0		12	A
Over current limit	V_{IN} = 12 V	13.2	20		A
Output ripple voltage	V_{IN} = 12 V, I_O = 12 A		25		mV_{PP}

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3 Modifications

The design of the TPS56C20EVM-614 provides access to all the four devices of the IC family: TPS56520, TPS56720, TPS56920, and TPS56C20. The module ships with a TPS56C20 IC soldered but the user can replace the TPS56C20 with any of the other three ICs to test their performance.

3.1 Output Voltage Set Point

To change the output voltage of the TPS56C20EVM-614, change the value of resistor R7. Calculate the value of R7 for a specific output voltage between 0.6 V to 1.87 V using Equation 1.

$$V_{OUT} = 0.6 \times (1 + R7 / R8) \quad (1)$$

Table 3-1 lists the R7 values for common output voltages. For higher output voltages, a feed forward capacitor (C12) may be required to improve phase margin. The evaluation module provides pads to include the component (C12). NOTE: the values given in Table 3-1 are standard values and not the exact value.

Table 3-1. Output Voltages

Output Voltage (V)	R7 (kΩ)	R8 (kΩ)	C12 (pF)	L1 (µH)			C6 + C7 (µF)
				MIN	TYP	MAX	
0.8	7.33	22					
1	14.7	22		1.0	1.5	2.2	44 – 100
1.1	18.2	22		1.0	1.5	2.2	44 – 100
1.2	22	22		1.0	1.5	2.2	44 – 100
1.5	33	22		1.0	1.5	2.2	44 – 100
1.8	44.2	22	Optional	1.0	1.5	2.2	44 – 100

3.2 Output Voltage Set Point Using I2C Interface

The engineer can change the TPS56C20 output voltage by using an I2C interface which can dynamically scale the output voltage in the range of 0.6 V to 1.87 V. Section 3.2.1, Section 3.2.2, and Section 3.2.3 explain the procedure to download all the software required and how to communicate between the evaluation module and the PC. The design includes an easy-to-use GUI so that the design engineer can test the I2C functionality without much prior experience. The test requires a PC running the Microsoft® Windows® operating system, the TI USB2ANY interface, and USB2ANY_GUI software. The design engineer can purchase the TI USB2ANY interface from the TI website.

3.2.1 PC Preparation

Use the following steps to prepare the PC for use:

1. Turn on the PC and boot up the Windows operating system.
2. Copy the provided file “PC-Software.zip” to a directory on the system hard drive.
3. Uncompress the files to that directory.
4. From the directory listing, unzip the USB2ANY_SDK_SETUP program files and run the USB2ANY_SDK_Setup.exe with the default settings.
5. From the directory listing, unzip the TPS56X20 I2C TEST PANEL file and run the SETUP file from the TPS56X20 I2C TEST PANEL Installer.
6. Reboot the PC after installing both pieces of software.

3.2.2 Connect the PC

Use the following steps to connect the PC to the TI USB2ANY interface:

1. Connect the provided USB cable between the PC USB port and the TI USB2ANY interface as illustrated in Figure 3-1.
2. Connect the supplied 10 conductor ribbon cable between the TI USB2ANY interface and PWR614 J4 connector.
3. Turn on or enable the input voltage power supply.

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Figure 3-1. USB2ANY Connection

3.2.3 Voltage Scaling Procedure

Set voltage scaling by using the following steps:

1. Go to Program Files and click on the TPS56X20 I2C TEST PANEL Application. The TPS56X20 I2C TEST PANEL will load as shown in Figure 3-2.

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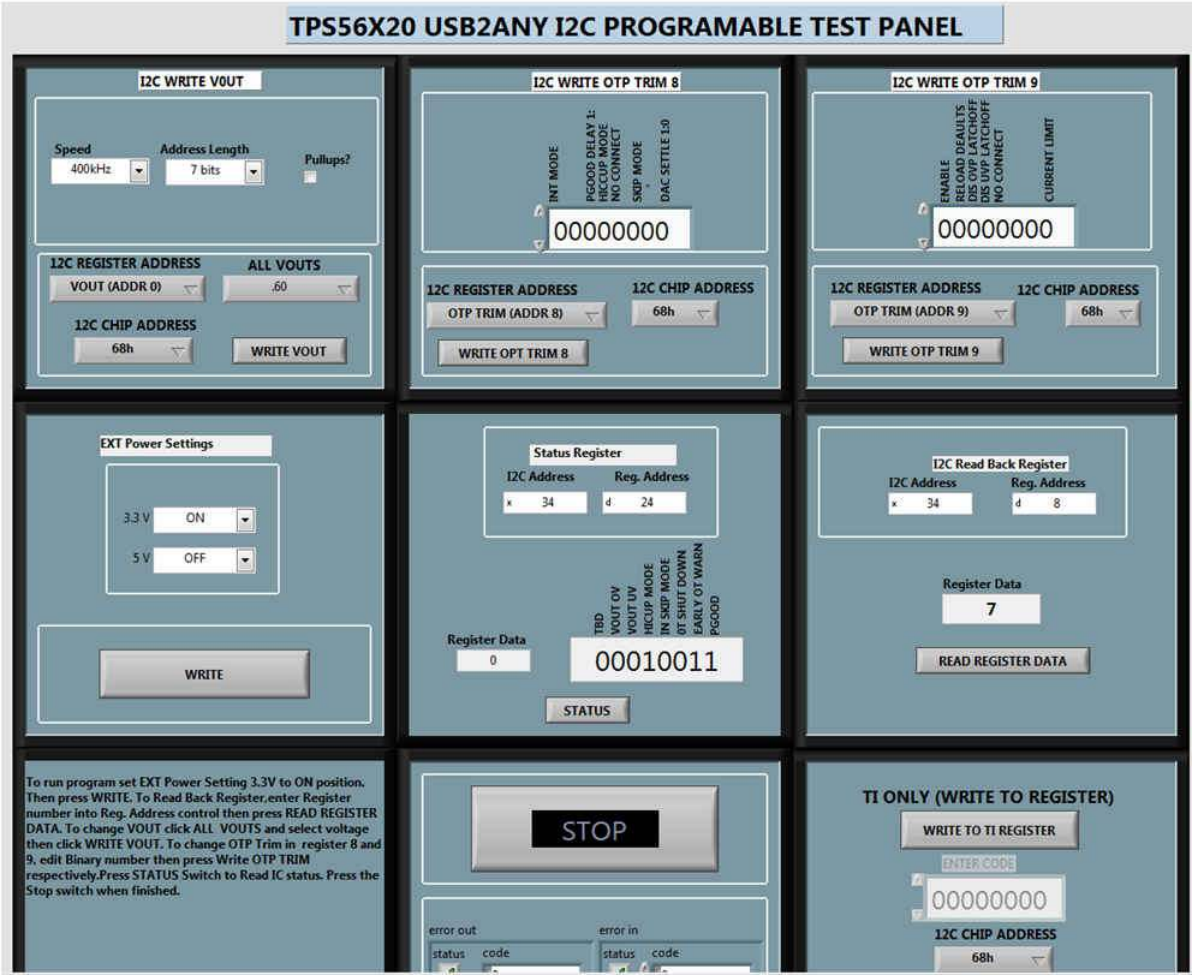

Figure 3-2. TPS56X20 I2C TEST PANEL

2. As a first step before sending a V_{OUT} command, click the write command On the EXT Power Settings block as shown in Figure 3-3.

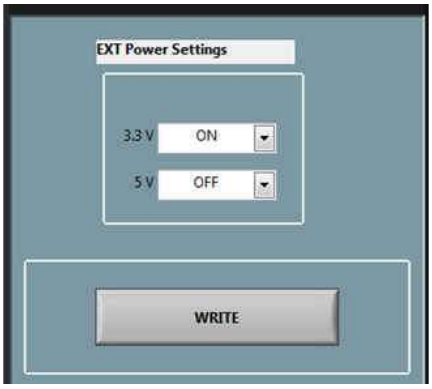

Figure 3-3. EXT Power Settings

3. Go to the VOUTS control block and click on the ALL VOUTS control, illustrated in Figure 3-4. The drop down menu gives an option to select different VOUT.

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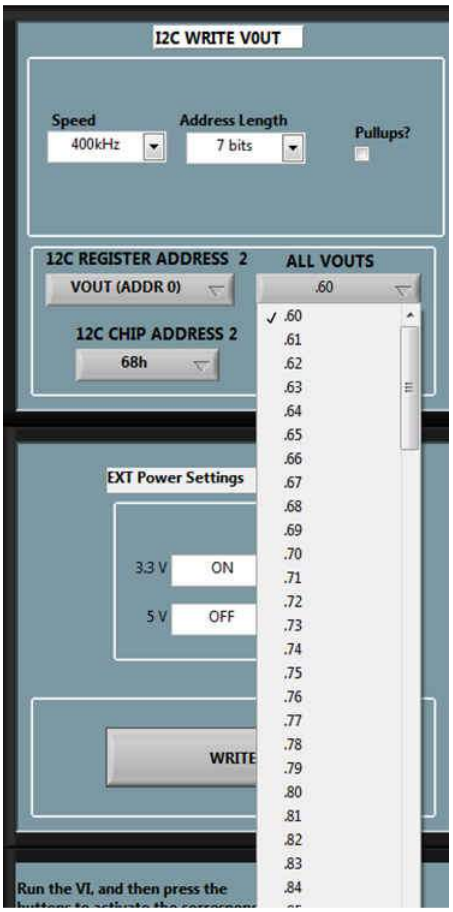

Figure 3-4. ALL VOUTS Control

4. Select a particular value and click on WRITE VOUT switch.

Observe that the Voltage at TP6 relative to TP7 is changed to the programmed VOUT value.

3.3 Output Filter and Closed Loop Response

The TPS56C20 relies on the output filter characteristics to ensure stability of the control loop. The recommended output filter components for common output voltages are in Table 3-1. It may be possible for other output filter component values to provide acceptable closed loop characteristics.

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4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS56C20EVM-614. The section also includes test results typical for the evaluation modules and efficiency, output load regulation, output line regulation, load transient response, output voltage ripple, start-up, and shutdown.

4.1 Input/Output Connections

The TPS56C20EVM-614 provides input/output connectors and test points as shown in Table 4-1. The design requires a power supply capable of supplying 4 A to connect to J1 through a pair of 20-AWG wires. The design requires the load to connect to J3 through a pair of 20-AWG wires. The maximum load current capability is 12 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP3 provides a place to monitor the VIN input voltages with TP4 (which provides a convenient ground reference). The design uses TP6 to monitor the output voltage with TP7 as the ground reference.

Table 4-1. Connection and Test Points

Reference Designator	Function
J1	PVIN input voltage connector (See Table 1-1 for PVIN range)
J2	VIN input voltage connector. Not normally used
J3	VOUT, 1.1V at 12A maximum
JP1	PVIN to VIN jumper. Normally closed
JP2	I2C interface pull up jumper for SDA
JP3	I2C interface pull up jumper for SCL
JP4	I2C interface grounding jumper for A1
JP5	I2C interface grounding jumper for A0
JP6	Enable Jumper. Close to disable, open to enable
TP1	GND test point for VIN connector
TP2	VIN test point
TP3	PVIN test point
TP4	GND test point for PVIN connector
TP5	SW test point
TP6	Output voltage test point at VOUT connector
TP7	GND test point at VOUT connector
TP9	Analog GND test point
TP10	Test point in voltage divider network. Used for loop response measurements

4.2 Start Up Procedure

Using the following procedure ensures a successful start up:

1. Make sure that the Enable jumper JP6 is closed to shunt EN to GND, disabling the output.
2. Apply the appropriate V_{IN} voltage to PVIN (J1-1) and GND (J1-2).

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4.3 Efficiency

Figure 4-1 shows the efficiency for the TPS56C20EVM-614 at an ambient temperature of 25°C.

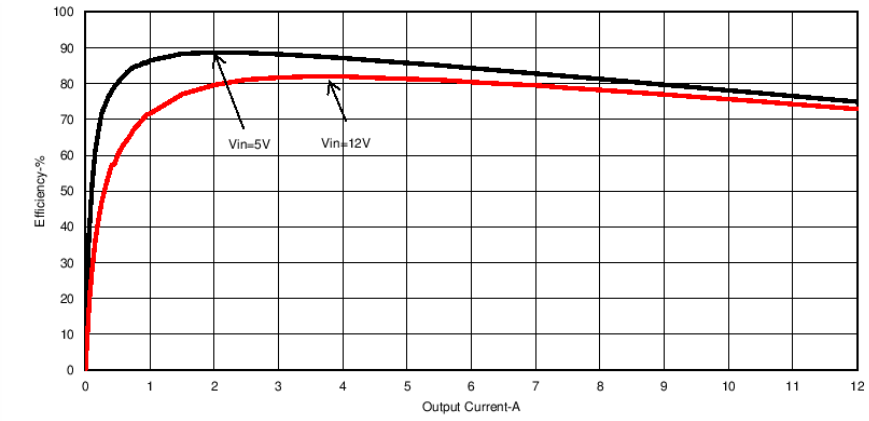

Figure 4-1. TPS56C20EVM-614 Efficiency

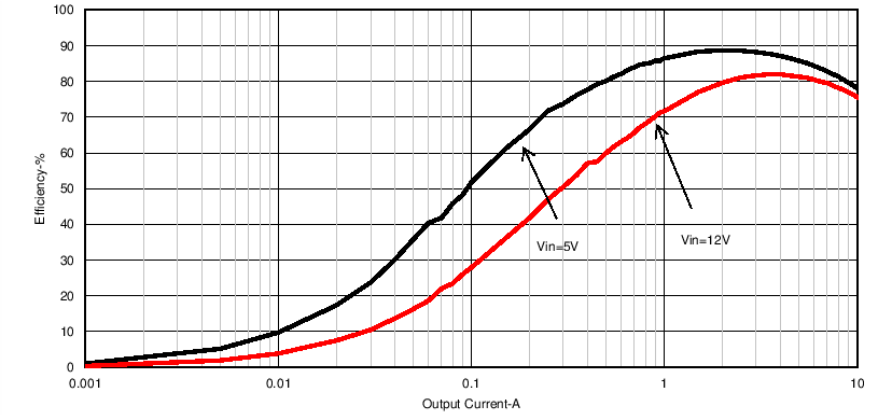

Figure 4-2. TPS56C20EVM-614 Efficiency (Low Current)

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4.4 Load Regulation

Figure 4-3 shows the load regulation for the TPS56C20EVM-614.

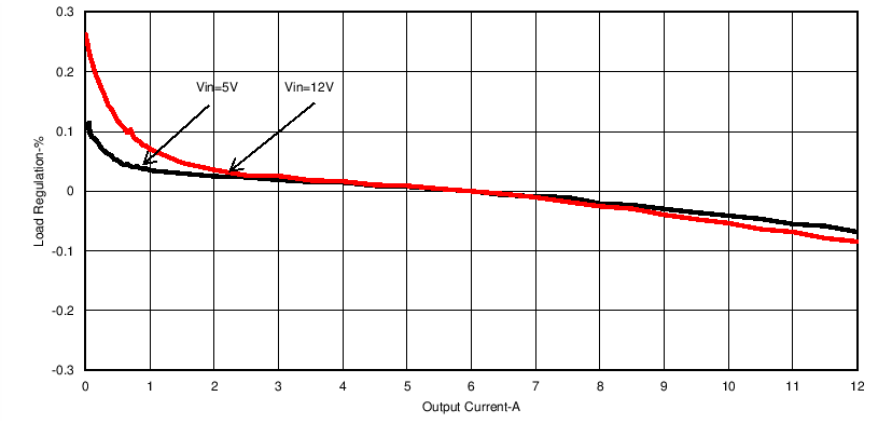

Figure 4-3. TPS56C20EVM-614 Load Regulation

4.5 Line Regulation

Figure 4-4 shows the line regulation for the TPS56C20EVM-614.

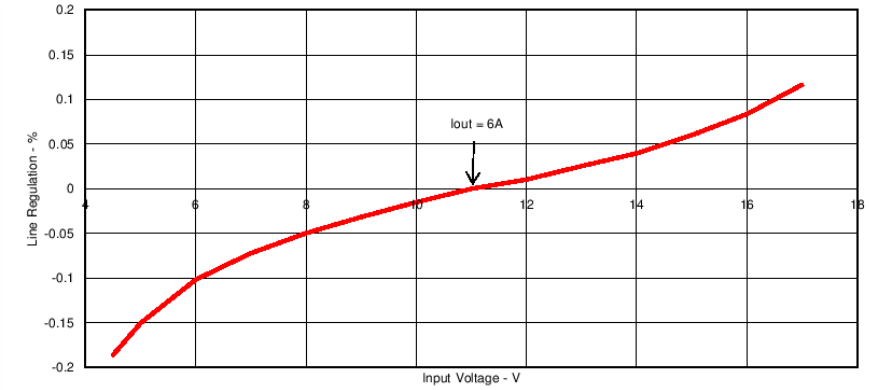

Figure 4-4. TPS56C20EVM-614 Line Regulation

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4.6 Load Transient Response

Figure 4-5 shows the TPS56C20EVM-614 response to load transient. The current step is from 50 mA to 12 A (0% to 100% of rated load), with a slew rate of 500 mA/µs. Figure 4-5 shows the total peak-to-peak output voltage variation.

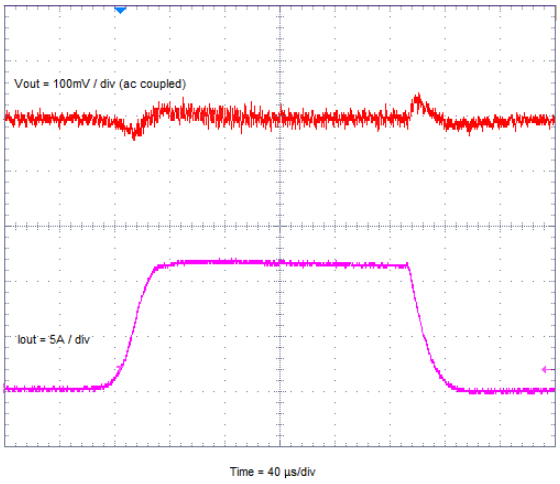

Figure 4-5. TPS56C20EVM-614 Load Transient Response

4.7 Output Voltage Ripple

Figure 4-6 shows the TPS56C20EVM-614 output voltage ripple. The output current is the rated full load of 12 A.

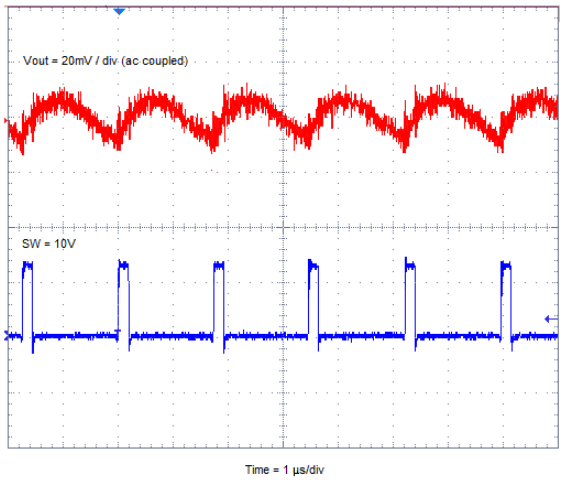

Figure 4-6. TPS56C20EVM-614 Output Voltage Ripple

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4.8 Start Up

Figure 4-7 shows the TPS56C20EVM-614 start up waveform as relative to V_{IN}.

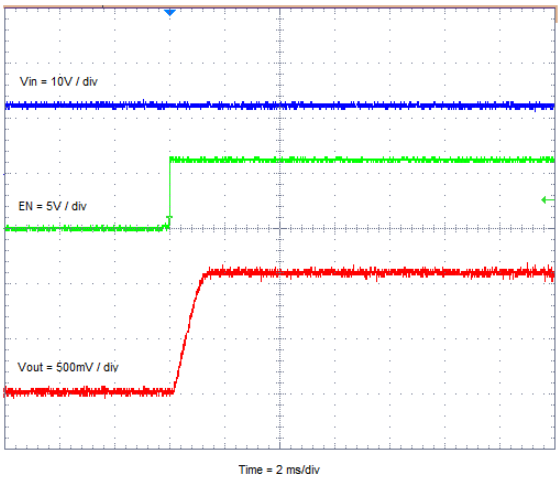

Figure 4-7. TPS56C20EVM-614 Start Up Relative to V_{IN}

Figure 4-8 shows the TPS56C20EVM-614 Start Up waveform is relative to Enable(EN).

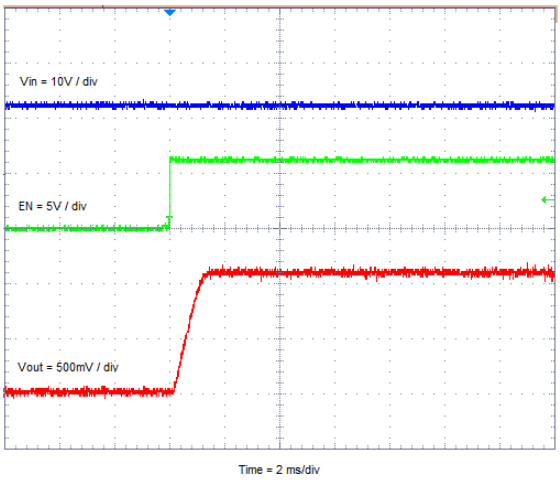

Figure 4-8. TPS56C20EVM-614 Start Up Relative to Enable

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4.9 Shut Down

Figure 4-9 shows the TPS56C20EVM-614 shut down waveform relative to V_{IN}.

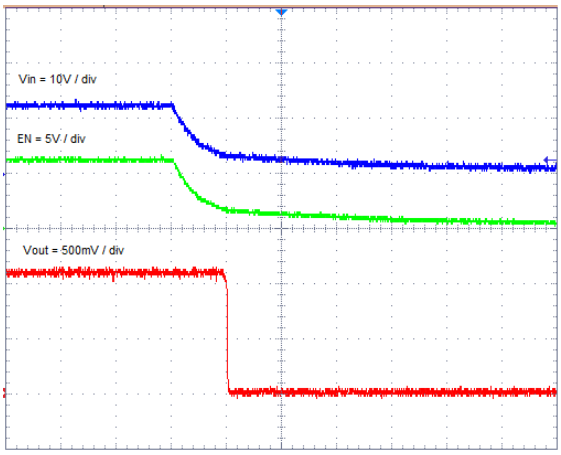

Figure 4-9. TPS56C20EVM-614 Shut Down Relative to V_{IN}

Figure 4-10 shows the TPS56C20EVM-614 Shut Down waveform relative to Enable(EN).

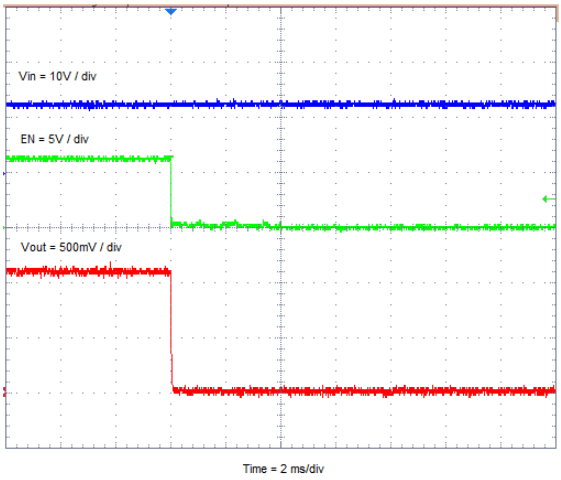

Figure 4-10. TPS56C20EVM-614 Shut Down Relative to Enable

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5 Board Layout

This section provides a description of the TPS56C20EVM-614, PCB layout, and layer illustrations.

5.1 Board Layout

Figure 5-1 through Figure 5-5 show the board layout for the TPS56C20EVM-614. The top layer contains the main power traces for PVIN, VIN, VOUT, SWITCH node, and a huge area filled with ground. Many of the signal traces are also located on the top side. The design locates the input decoupling capacitors and the voltage set point resistor divider network components as close to the IC as possible. The input and output connectors, test points, and most of the components are located on the top side. The analog ground (which is used as a return for the I2C interface signals) connects to the power ground at only one point on the top layer. Internal layer 1 and internal layer 2 are filled with power ground. The bottom layer contains a few traces like the I2C connections and the output voltage trace to the J3 connector.

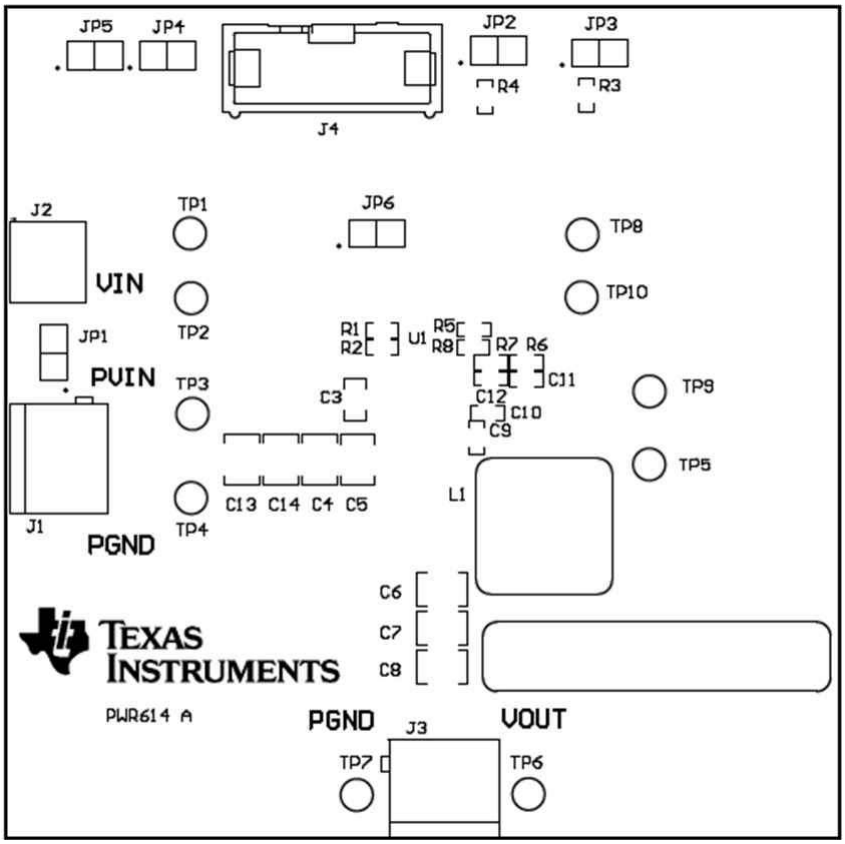

Figure 5-1. Top Assembly

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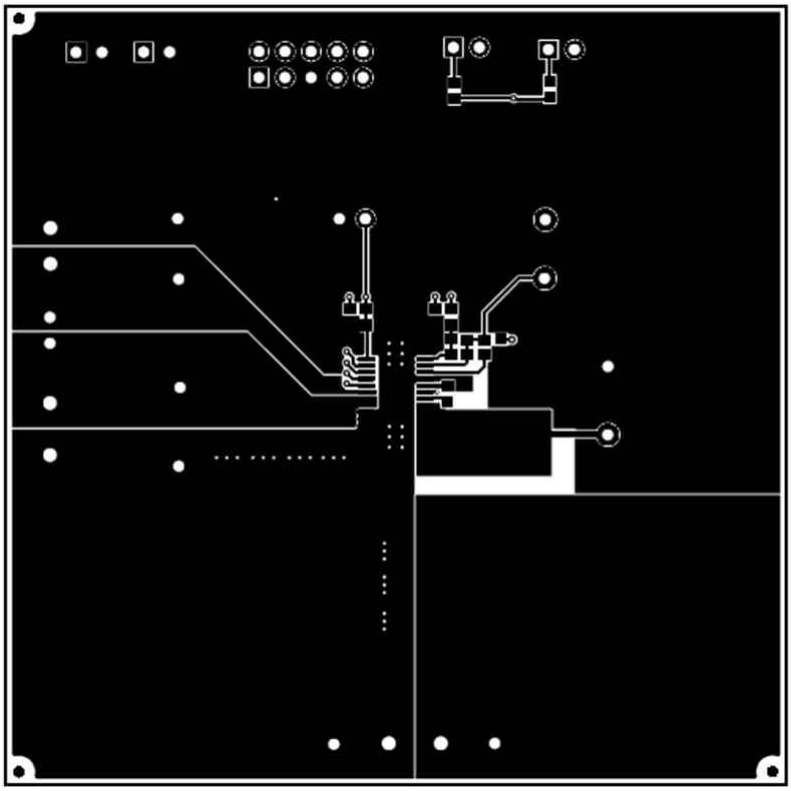

Figure 5-2. Top Layer

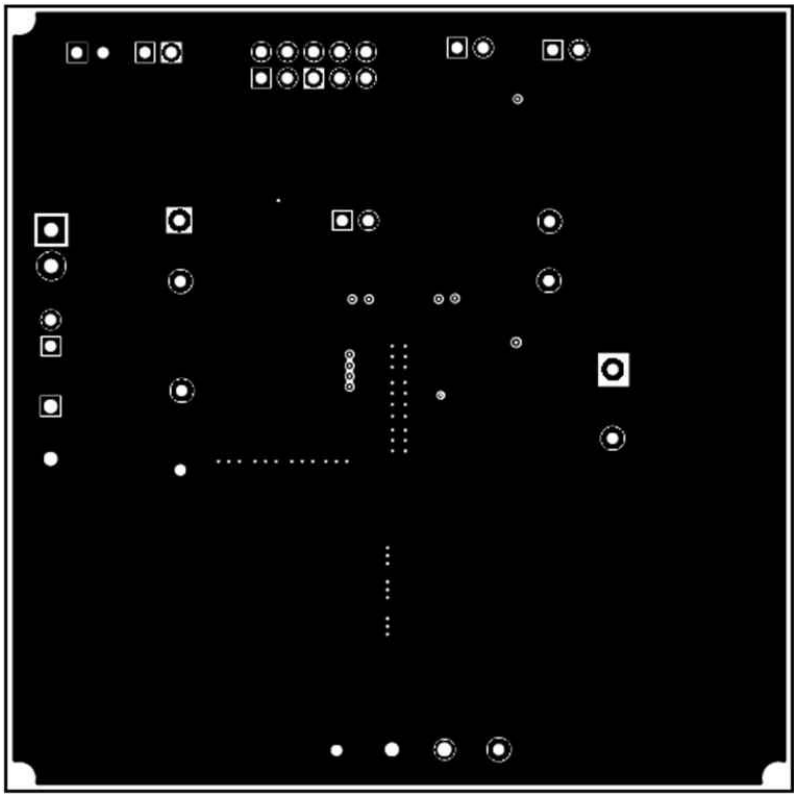

Figure 5-3. Internal Layer 1

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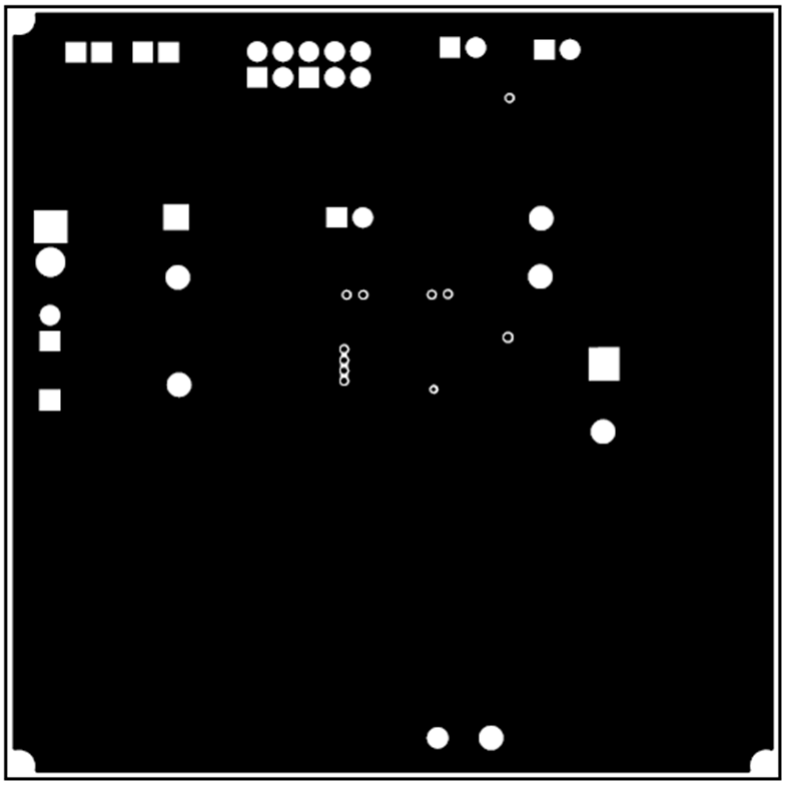

Figure 5-4. Internal Layer 2

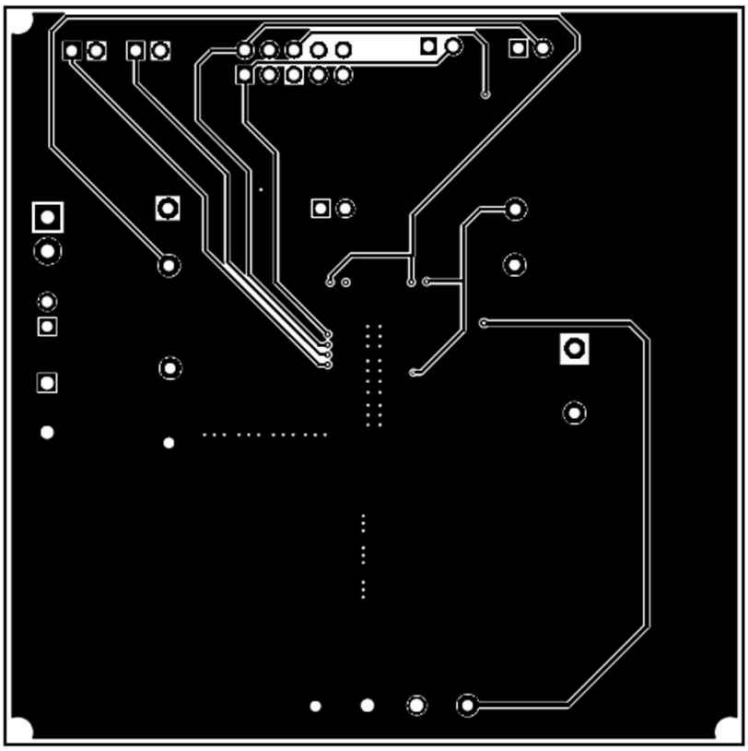

Figure 5-5. Bottom Layer

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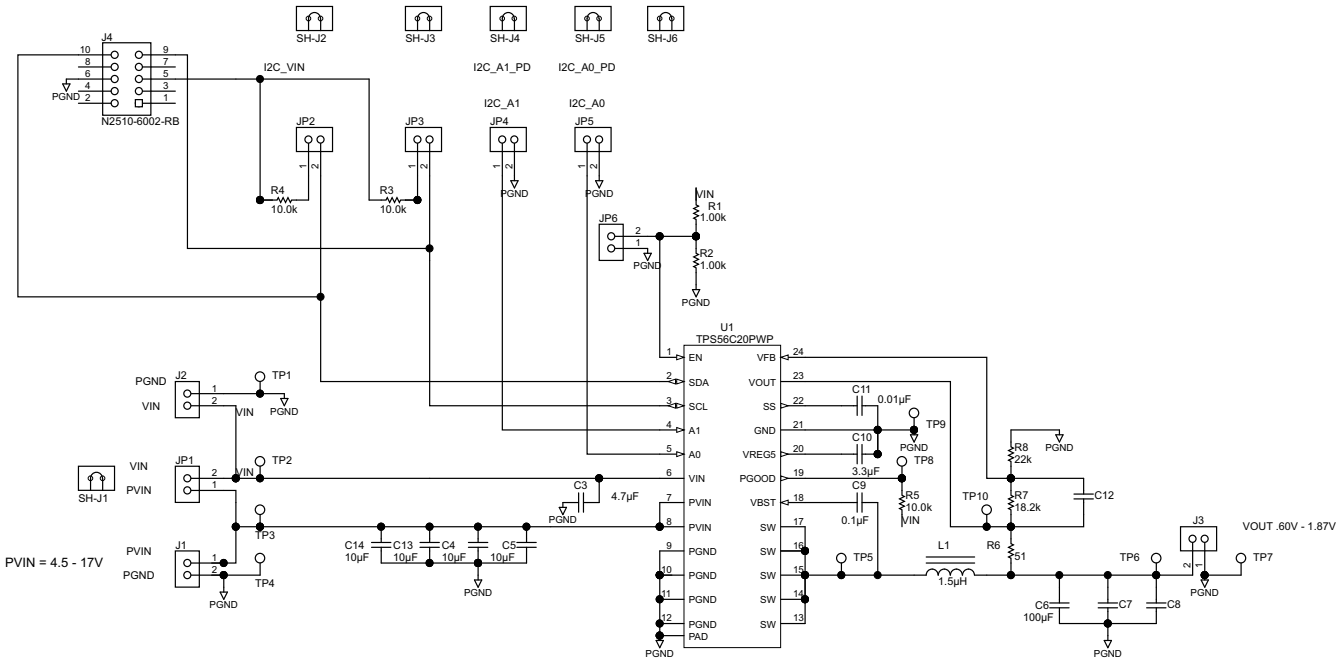
6 Schematic, Bill of Materials and Reference

This section presents the TPS56C20EVM-614 schematic, bill of materials (BOM), and reference.

6.1 Schematic

Figure 6-1 shows the schematic for the TPS56C20EVM.



NOTE: TPS56520,720,920 C10=2.2uF

NOTE: TPS56C20 C10=3.3uF

NOTE: TPS56520: Wurth 1.5uH Inductor:74437346015

NOTE: TPS56720,TPS56920: Wurth 1.5uH Inductor:744311150

NOTE: TPS56C20: Wurth 1.5uH Inductor:744323150

Figure 6-1. TPS56C20EVM-614 Schematic Diagram

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6.2 Bill of Materials

Table 6-1 lists the BOM for the TPS56C20EVM.

Table 6-1. TPS56C20EVM-614 Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C3	1	4.7uF	CAP, CERM, 4.7uF, 10V, +/-10%, X5R, 0805	0805	0805ZD475KAT2A	AVX
C4, C5, C13, C14	4	10uF	CAP, CERM, 10uF, 35V, +/-10%, X7R, 1210	1210	GRM32ER7YA106KA12L	MuRata
C6	1	100uF	CAP, CERM, 100uF, 6.3V, +/-20%, X5R, 1210	1210	C1210C107M9PACTU	Kemet
C9	1	0.1uF	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603	0603	06033C104KAT2A	AVX
C10	1	3.3uF	CAP, CERM, 3.3uF, 25V, +/-10%, X5R, 0603	0603	C1608X5R1E335K080AC	TDK
C11	1	0.01uF	CAP, CERM, 0.01uF, 50V, +/-5%, X7R, 0603	0603	C0603C103J5RACTU	Kemet
J1, J3	2		TERMINAL BLOCK 5.08MM VERT 2POS	TERM_BLK, 2pos, 5.08mm	ED120/2DS	On-Shore Technology, Inc.
J2	1		Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology, Inc.
J4	1		Header (shrouded), 100mil, 5x2, High-Temperature, Gold, TH	5x2 Shrouded header	N2510-6002-RB	3M
JP1, JP2, JP3, JP4, JP5, JP6	6		Header, TH, 100mil, 2x1, Gold plated, 230 mil above insulator	TSW-102-07-G-S	TSW-102-07-G-S	Samtec, Inc.
L1	1	1.5uH	Inductor, Shielded Drum Core, WE-Superflux200, 1.5uH, 12A, 0.0066 ohm, SMD	WE-HC5	744323150	Wurth Elektronik eiSos
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650"H x 0.200"W	THT-14-423-10	Brady
R1, R2	2	1.00k	RES, 1.00k ohm, 1%, 0.1W, 0603	0603	CRCW06031K00FKEA	Vishay-Dale
R3, R4, R5	3	10.0k	RES, 10.0k ohm, 1%, 0.1W, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
R6	1	51	RES, 51 ohm, 5%, 0.1W, 0603	0603	CRCW060351R0JNEA	Vishay-Dale
R7	1	18.2k	RES, 18.2k ohm, 1%, 0.1W, 0603	0603	CRCW060318K2FKEA	Vishay-Dale
R8	1	22k	RES, 22k ohm, 5%, 0.1W, 0603	0603	CRCW060322K0JNEA	Vishay-Dale
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6	6	1x2	Shunt, 100mil, Gold plated, Black	Shunt	969102-0000-DA	3M
TP1	1	Black	Test Point, TH, Miniature, Black	Keystone5001	5001	Keystone
TP2, TP5, TP8, TP10	4	Red	Test Point, TH, Miniature, Red	Keystone5000	5000	Keystone
TP3, TP6	2	Red	Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
TP4, TP7, TP9	3	Black	Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone
U1	1		4.5V to 17V Input, 12A/9A/7A/5A Output, Synchronous Step-Down Voltage Regulator with Voltage Margining, PWP0024G	PWP0024G	TPS56C20PWP	Texas Instruments

6.3 Reference

TPS56C20,TPS56920, TPS56720, TPS56520 data sheet (SLVSCB6).

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2014) to Revision A (May 2021) **Page**

- Changed user's guide title..... 3

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- Updated the numbering format for tables, figures, and cross-references throughout the document. 3

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