- **Correlated Double Sampling (CDS), AGC and High Speed 10-Bit ADC in a Single Package**
- **5-V Analog Power Supply and 3.3-V Digital Power Supply**
- **Power Down Mode**
- **56-Pin TSSOP (DGG) Package with Multichip Module Assembly for Isolation**

CDS/AGC

- **AGC Gain Range of 5 dB to 39 dB**
- **Black Level Clamp Circuit**
- **Direct Connection to ADC Input**
- **Voltage Reference for ADC**

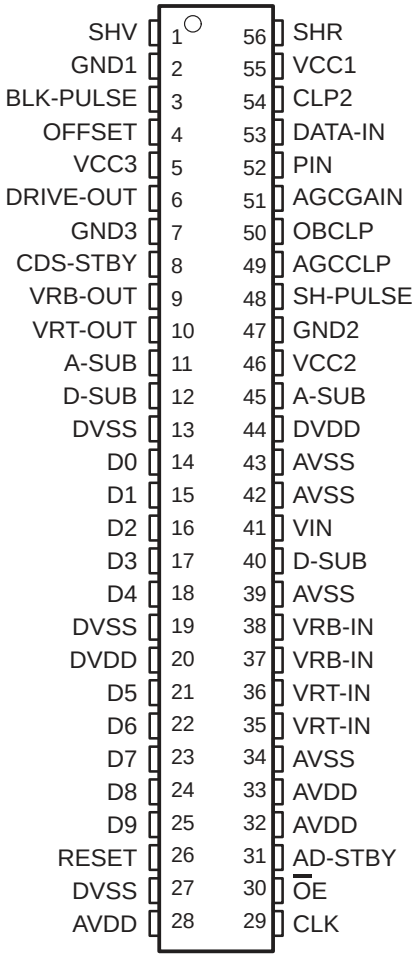
Analog-to-Digital Converter

- **10-Bit Resolution**
- **Maximum Conversion Rate . . . 20 MSPS (MIN)**
- **Differential Nonlinearity . . . 0.75 LSB (TYP)**
- **Analog Input Voltage Range of 2 Vp-p**
- **3.3 V CMOS Digital Interface**

Applications

- **PC Camera**
- **Digital Camera**
- **Camcorder**
- **CCD Scanner**

DGG PACKAGE
(TOP VIEW)



description

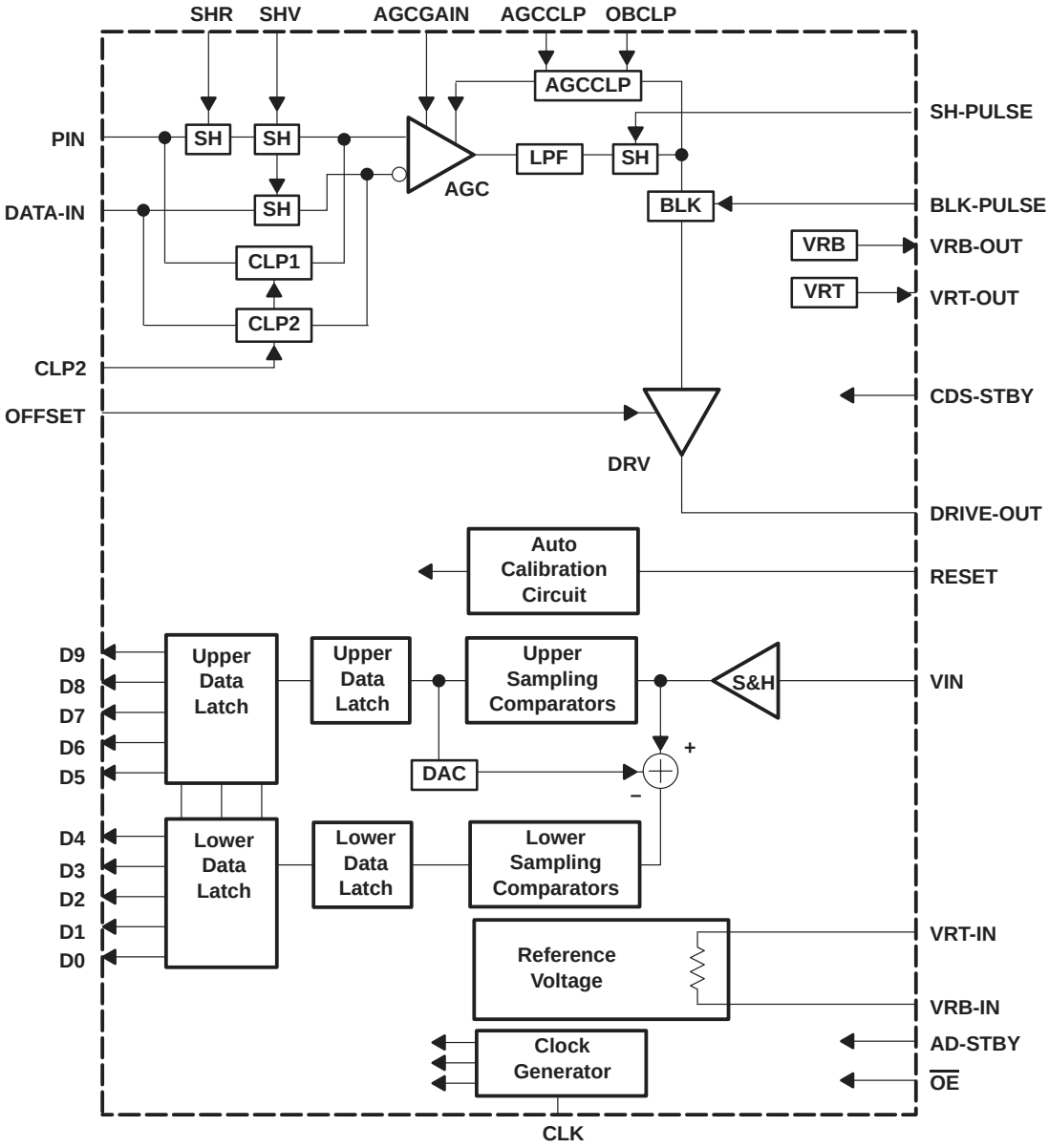
The TLC976 is a multichip module (MCM) subsystem designed for interfacing Charge-Coupled Device (CCD) in camcorder and digital camera systems. The TLC976 includes correlated double sampler (CDS), automatic gain control (AGC), black level clamp circuit, 10 bit, 20 MSPS analog-to-digital converter (ADC), and internal reference voltage generator for ADC.

The CDS/AGC can be connected directly to the ADC input or a separate signal can be connected directly to the ADC input. A power-down mode is provided.

Assembled using the MCM process, the TLC976 provides isolation between the noisy digital domain and the noise sensitive analog signals. The CDS/PGA, black level clamps are on one die and the ADC is on a separate die. The separate dies significantly reduce the substrate noise to the analog section.

The TLC976 comes in a 56-pin TSSOP package with 0,50 mm pin pitch. This is about 25% smaller than using two separate 32-pin quad flat packs (QFP).

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AD-STBY	31	I	ADC standby mode L level in operation H level in standby mode
AGCCLP	49	I	AGC clamp capacitor (connect 0.1 μF to GND)
AGCGAIN	51	I	AGC gain control
A-SUB	11, 45		Analog GND
AVDD	28, 32, 33		ADC analog power supply
AVSS	34, 39, 42, 43		Analog GND for ADC
BLK-PULSE	3	I	DRIVE-OUT terminal is clamped to 1.66 V internally when BLK-PULSE = L.
CDS-STBY	8	I	CDS/AGC standby mode control L level in operation H level in standby mode
CLK	29	I	CLK input for ADC
CLP2	54	I	CCD signal clamp control input
D0–D9	14–18, 21–25	O	Digital data output, D0 (pin 14): LSB, D9 (pin 25): MSB
DATA-IN	53	I	CCD signal input
DRIVE-OUT	6	O	CDS/AGC output
D-SUB	12, 40		Analog GND
DVDD	20, 44		ADC digital power supply
DVSS	13, 19, 27		Digital GND for ADC
GND1	2	I	CDS/AGC analog GND
GND2	47		CDS/AGC analog GND
GND3	7		GND for CDS output circuit
OBCLP	50	I	Control input for clamping optical black level after AGC
$\overline{OE}$	30	I	ADC output enable L level in operation H level in Hi-Z
OFFSET	4	I	CDS/AGC output offset control: DC voltage at OFFSET pin — DRIVE-OUT offset 0 V — –450 mV 0.5 V — –280 mV 3 V — 550 mV
PIN	52	I	CCD signal input
RESET	26	I	Reset for calibration circuit. Restart of startup calibration.
SHV	1	I	CCD signal level sample clock input
SH-PULSE	48	I	Sample and hold pulse input
SHR	56	I	CCD reset level sample clock input
VCC1	55		CDS/AGC analog power supply
VCC2	46		CDS/AGC analog power supply
VCC3	5		CDS/AGC analog power supply
VIN	41	I	ADC analog signal input
VRB-OUT	9	O	ADC bottom reference voltage output (1.5 V typ)
VRB-IN	37, 38	I	Connect to VRB-OUT
VRT-OUT	10	O	ADC top reference voltage output (3.5 V typ)
VRT-IN	35, 36	I	Connect to VRT-OUT

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Analog supply voltage, VCC1, VCC2, VCC3, AVDD (see Note 1) . . . . . –0.4 V to 7 V
Digital supply voltage, DVDD (see Note 1) . . . . . –0.4 V to 7 V
Analog input voltage range, V_I . . . . . –0.4 V to AVCC1, 2,3 + 0.5 V
Continuous total power dissipation (see Note 2) . . . . . 1344 mW
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to GND.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 10.75 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Analog supply voltage, VCC1, VCC2, VCC3, AVDD		4.75	5	5.25	V
ADC digital output supply voltage, DVDD		3	3.3	3.6	V
Difference, AGND to DGND		–100		100	mV
High-level input voltage		2			V
Low-level input voltage				0.8	V
ADC analog input voltage full scale range		2			V
ADC CLK pulse width	High level	25			ns
	Low level	25			
Operating temperature		0		70	°C

electrical characteristics over recommended operating junction temperature range, AVCC = VCC1–3 = 4.75 V, DVDD = 3.3 V, VRT = 3.5 V, VRB = 1.5 V, Fs = 20 MSPS, T_A = 25°C (unless otherwise noted)

total device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CDS/AGC supply current		AGCGAIN = 0 V, VRT = VRB = Open, STBY = 0 V		30	38	mA
ADC supply current	Digital supply	NTSC ramp input		3	6	mA
	Analog supply			32	35	
CDS/AGC standby current		CDS-STBY = High		5.6	11	mA
ADC standby current		AD-STBY = HIGH, CDS STBY = HIGH, (VIN = VRT-IN = VRB-IN = Hi-Z)		0.5	1	mA

electrical characteristics over recommended operating junction temperature range, AVCC = VCC1–3 = 4.75 V, DVDD = 3.3 V, VRT = 3.5 V, VRB = 1.5 V, Fs = 20 MSPS, T_A = 25°C (unless otherwise noted) (continued)

CDS input/AGC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input signal clamp voltage				2.7		V
Input current for SHR, SHV, CLP2	High input	VIN = 3 V			1	A
	Low input	VIN = 0 V			–1	µA
AGC gain	Minimum	AGCGAIN = 0 V		5	7	dB
	Maximum	AGCGAIN = 3 V	34	37	39	
High-level input current, OBCLP, BLK pulse					1	µA
Low-level input current, OBCLP, BLK pulse					–1	µA
CDS input clock frequency				20		MHz

driver output

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output offset voltage	High	OFFSET = 3 V		0.55	0.65	V
	Low	OFFSET = 0 V	–0.35	–0.45		V
Internal black level			1.36	1.66	1.96	V
Nominal signal voltage at DRIVE-OUT				2		Vp-p

reference voltage

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VRT output voltage	300 Ω, AVDD = VCC1–3 = 4.75 V	3.47	3.50	3.53	V
VRB output voltage		1.45	1.50	1.55	V

electrical characteristics over recommended operating junction temperature range, AVCC = VCC1–3 = 4.75 V, DVDD = 3.3 V, VRT = 3.5 V, VRB = 1.5 V, Fs = 20 MSPS, T_A = 25°C (unless otherwise noted) (continued)

A/D converter

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Integral non-linearity	Fs = 20 MSPS,	VIN = 1.8 V – 3.8 V		±1.5	±2.5	LSB
Differential non-linearity				±0.75	±1.25	LSB
Analog input capacitance				10		pF
Reference voltage output current				6.5		mA
Reference voltage output impedance	(VRT IN – VRB IN)			300		Ω
Zero scale offset error				20		mV
Full scale offset error				20		mV
High-level input current	DVDD = MAX,	V_{IH} = DVDD			10	µA
Low-level input current	DVDD = MAX,	V_{IL} = 0 V			10	µA
High-level output current	OE = GND, V_{OH} = DVDD – 0.5 V	DVDD = MIN,		3		mA
Low-level output current	OE = GND, V_{OL} = 0.4 V	DVDD = MIN,		5		mA
High-level output voltage	DVDD = 3 V – 5.25 V,	I_{OH} = 2 mA	VDD– 0.7V			V
Low-level output voltage	DVDD = 3 V – 5.25 V,	I_{OL} = 1 mA			0.8	V
High-level output leakage current	OE = DVDD, V_{OH} = DVDD	DVDD = MAX,			1	µA
Low-level output leakage current	OE = DVDD, V_{OL} = 0 V	DVDD = MIN,			1	µA
Automatic starting calibration voltage	DVDD–DGND			2.5		V
	VRT–VRB			1		

A/D converter operating characteristics

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Sampling rate	V_{IN} = 1.8 V – 3.8 V,	Fin = 1 kHz ramp	0.5		20	MSPS
Analog input bandwidth (–3 dB)				10		MHz
Data output, propagation delay	C_L = 20 pF		15		ns	
Differential gain	NTSC 40 IRE mod ramp, FS = 14.3 MSPS			1%		
Differential phase				0.3		Degree
Sampling delay time				5		ns
Signal to noise ratio	Fin = 1 MHz			55		dB

TYPICAL CHARACTERISTICS

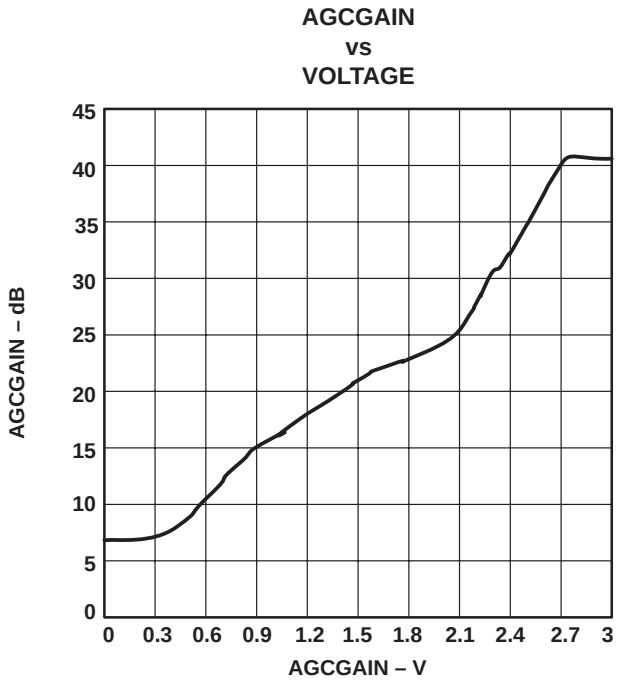


Figure 1. AGC Characteristics

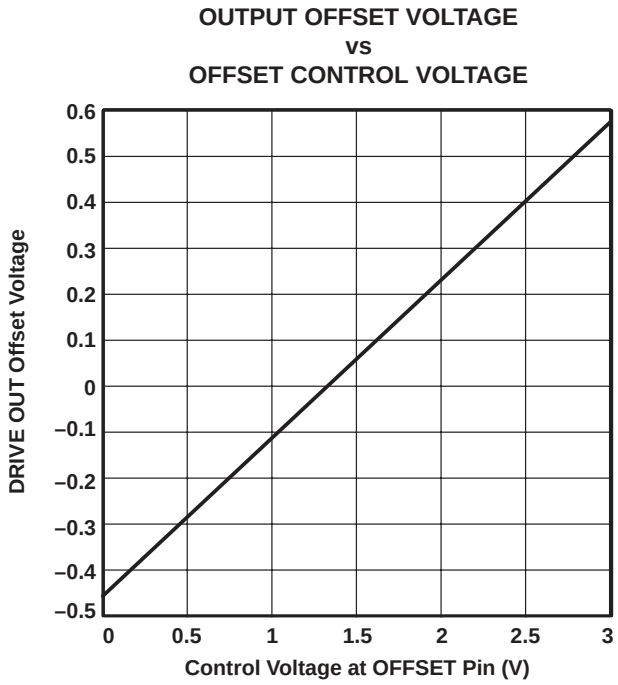


Figure 2. OFFSET IN Terminal Input/Output Characteristics

TYPICAL OPERATION

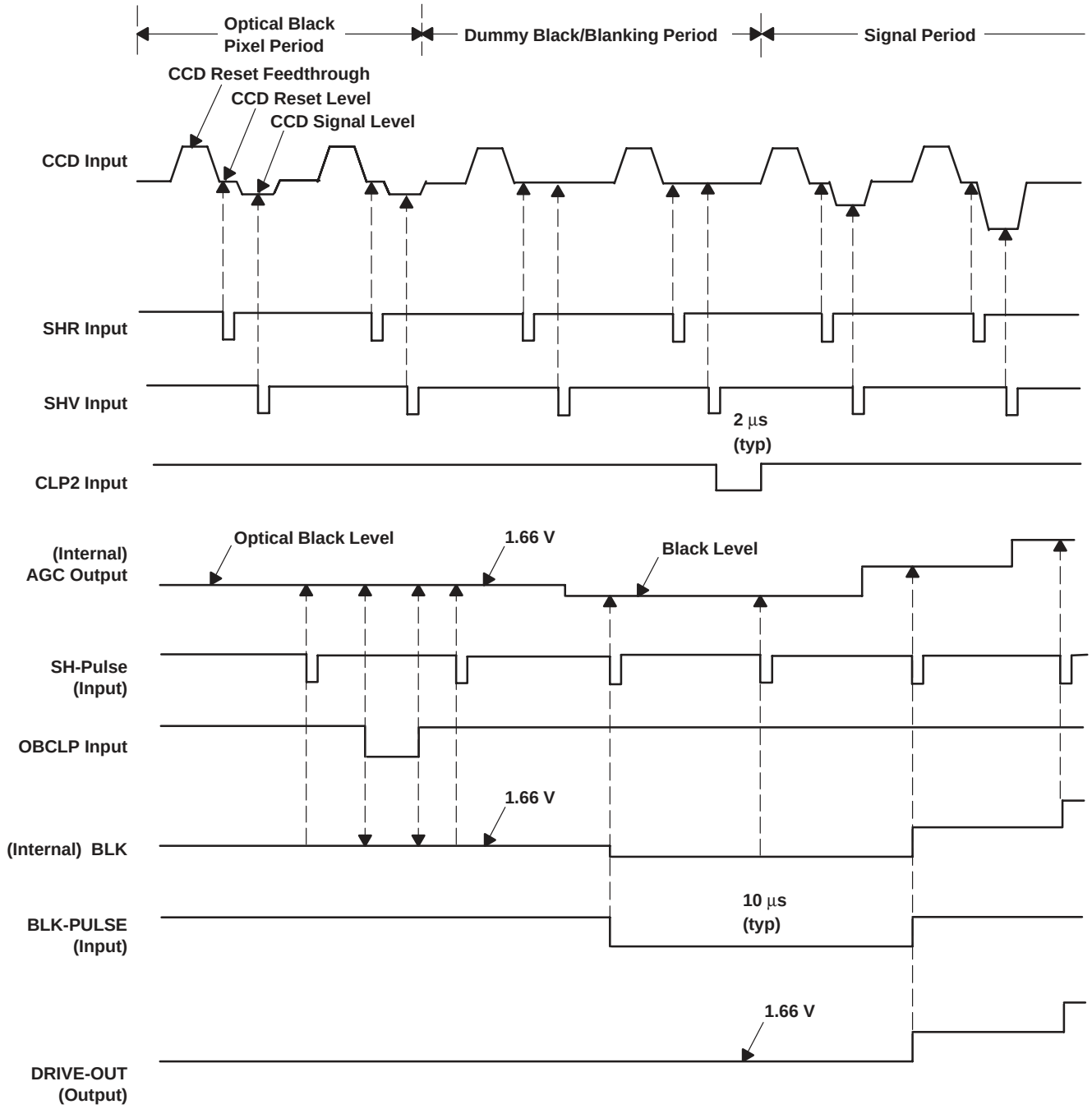
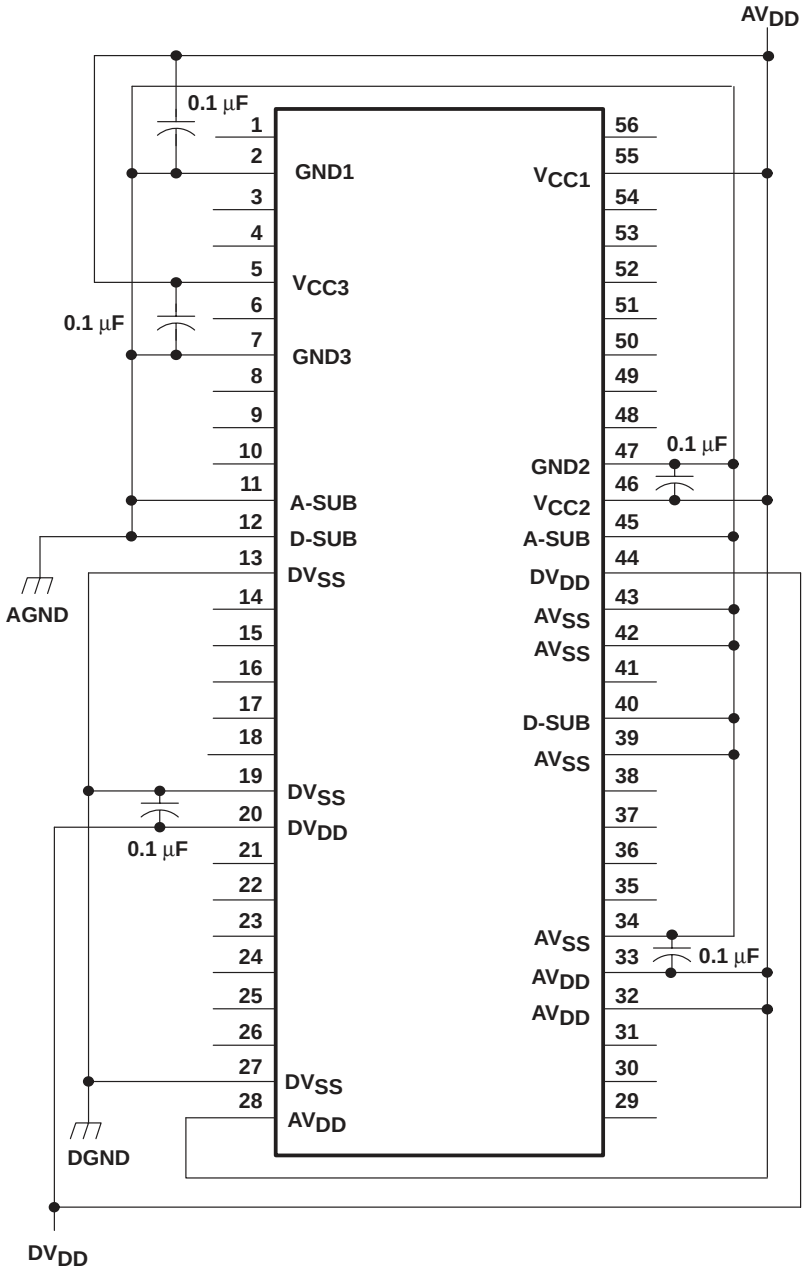


Figure 3. CCD Input Mode Timing Diagram

APPLICATION INFORMATION



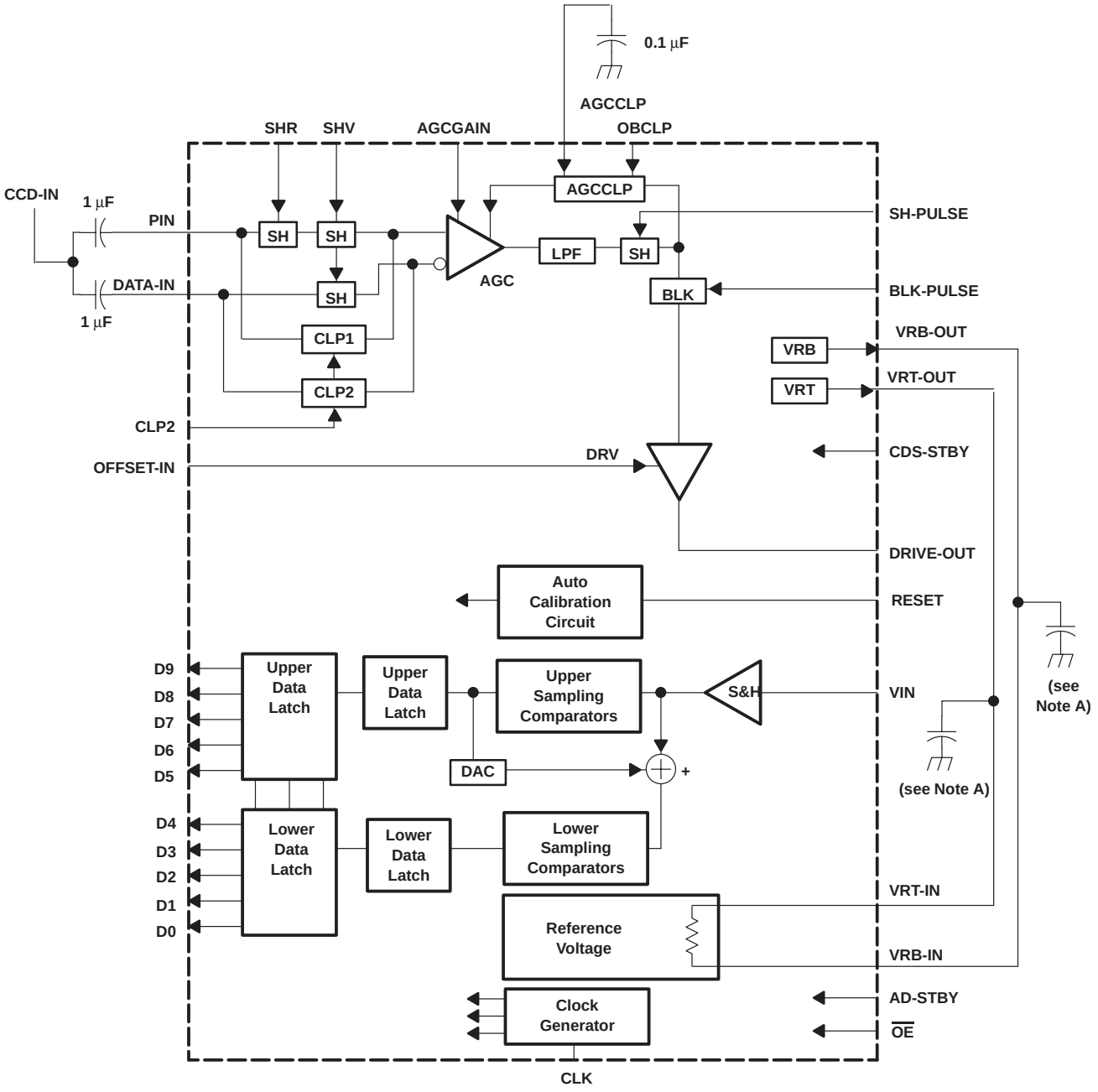
NOTE A: A-SUB and D-SUB should be connected to Analog GND.

Figure 4. Typical Connection Diagram

Table 1. Standby, Output Enable

PIN	PIN NAME	FUNCTION	OPERATION	STAND-BY OR DISABLE
8	CDS-STBY	Standby mode for CDS/AGC	L	H
31	AD-STBY	Standby mode for AD converter	L	H
30	$\overline{OE}$	AD output	L	H

APPLICATION INFORMATION



NOTE A: The 0.1 μF capacitors are necessary when you need to protect the noise.

Figure 5. Typical Application

PRINCIPLES OF OPERATION

CDS/AGC signal processor

The output from the CCD sensor is first fed to a correlated double sampler (CDS). The CCD signal is sampled and held during both the reset reference interval and the video signal interval. By subtracting two resulting voltage levels, the CDS removes low frequency noise from the output of the CCD sensor. Two sample/hold control pulses (SHR and SHV) are required to perform the CDS function.

The CCD output is capacitively coupled to the TLC976. The AC coupling capacitor is clamped to establish proper dc bias during the dummy pixel interval by the CLP2 input. The bias at the input to the TLC976 is set to 2.7 V at V_{CC} = 4.75 V. Normally, the CLP2 is applied at the sensor's line rate.

The signal is sent to AGC after the CDS function is complete. The AGC gain can be adjusted from 5 dB to 39 dB by applying variable dc voltage from 0 V to 3 V at the AGCGAIN terminal.

A low-pass filter is installed at the AGC output to improve signal-to-noise ratio. After its output settles, it is sampled and held by the SH-PULSE input for digitization. The SH-PULSE should synchronize with the ADC clock.

The basic black level reference is established by clamping the AGC output to 1.66 V internally by the OBCLP input during the optical black pixel period. A capacitor of 0.1 μF should be connected to the AGCCLP pin.

To prevent the black level from falling below the basic black level (1.66 V) during the blanking period, the AGC output level is kept at 1.66 V by the BLK PULSE input. It is recommended that the BLK PULSE be kept low during the entire blanking period.

The DRV block drives the ADC and adjusts the signal offset at the DRIVE OUT output. The offset can be adjusted from –450 mV to 550 mV by applying control voltage on the OFFSET pin.

The VRT (3.5 V) and VRB (1.5 V) outputs provide voltage references for the ADC. They should be connected to the VRT-IN and VRB-IN input pins externally.

analog-to-digital converter (ADC)

The A/DC in the TLC976 performs high-speed analog-to-digital conversion with 10-bit resolution using semi-flash technique. The latency of the data output valid is 2.5 clocks.

Table 2. ADC Output Code

INPUT VOLTAGE	STEPS	DIGITAL OUTPUT CODE	
		MSB	LSB
VRT	0	1111111111	
•	•	•	
•	•	•	
•	•	•	
•	•	•	
•	511	1000000000	
•	512	0111111111	
•	•	•	
•	•	•	
•	•	•	
•	•	•	
VRB	1023	0000000000	

PRINCIPLES OF OPERATION

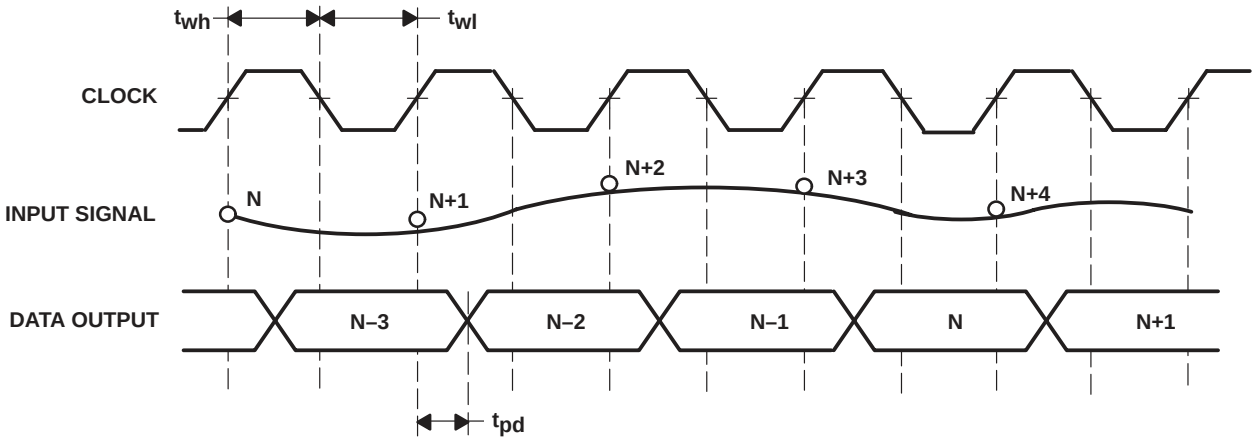


Figure 6. ADC Operation Sequence

PRINCIPLES OF OPERATION

ADC internal calibration

start-up calibration at power up

After power is turned on, the start-up calibration starts under the following conditions:

1. The voltage between VRT and VRB is over 1 V when the voltage between AVDD and AVSS is over 2.5 V.
2. The voltage between DVDD and DVSS is over 2.5 V.
3. The RESET terminal (pin 26) is high.
4. The AD-STBY terminal (pin 31) is low.

The calibration sequence starts after condition 2 is met (see Figure 7). The following equation calculates the time required for the start-up calibration after the above conditions are met.

Start-up calibration time = main clock pulse period $\times$ 16 $\times$ 16384

For example, if the main clock frequency is 15 MHz, the time required for startup calibration is 17.5 ms.

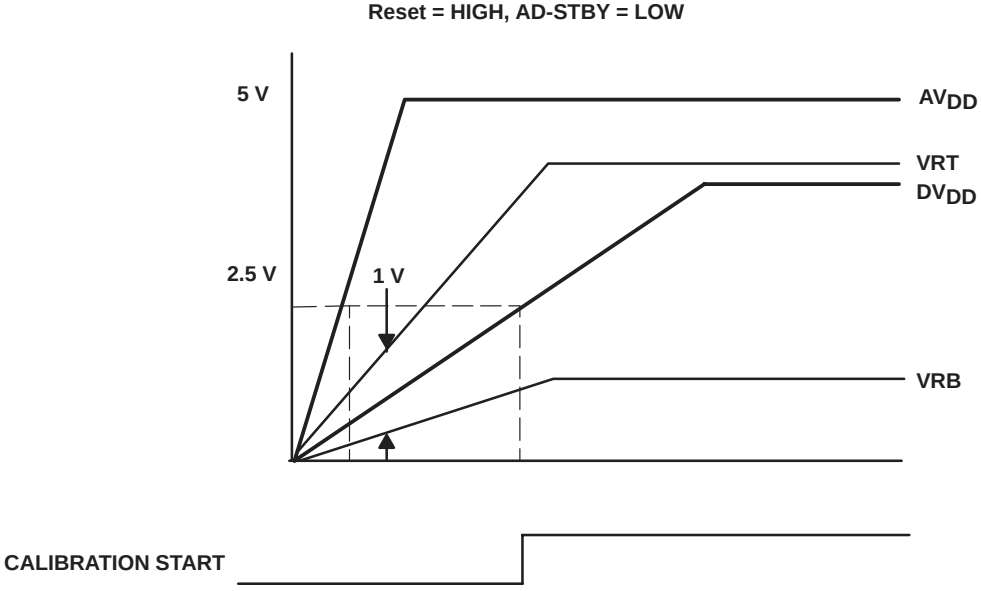


Figure 7. Start-Up Calibration

PRINCIPLES OF OPERATION

start-up calibration using RESET terminal

If start-up characteristics are not stable, the start-up calibration can be performed using the AD-STBY terminal (pin 31) or the RESET terminal (pin 26). Start-up calibration can be initiated properly by connecting RC components to the RESET pin as shown in Figure 8. The RC components delay the start-up until the supply voltage stablizes.

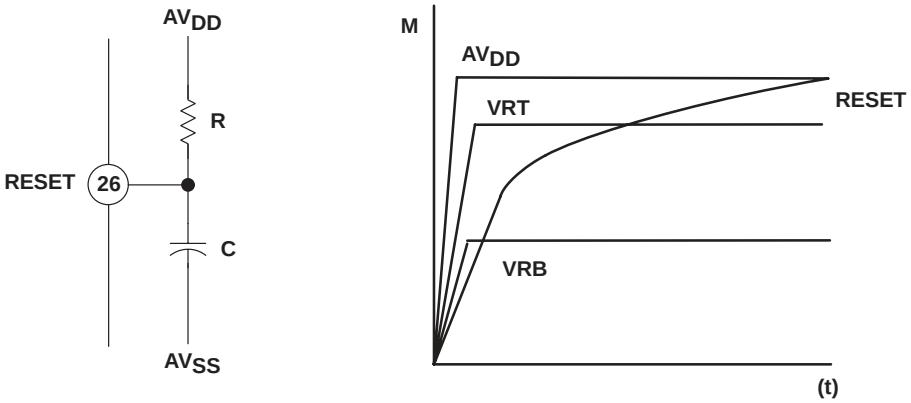
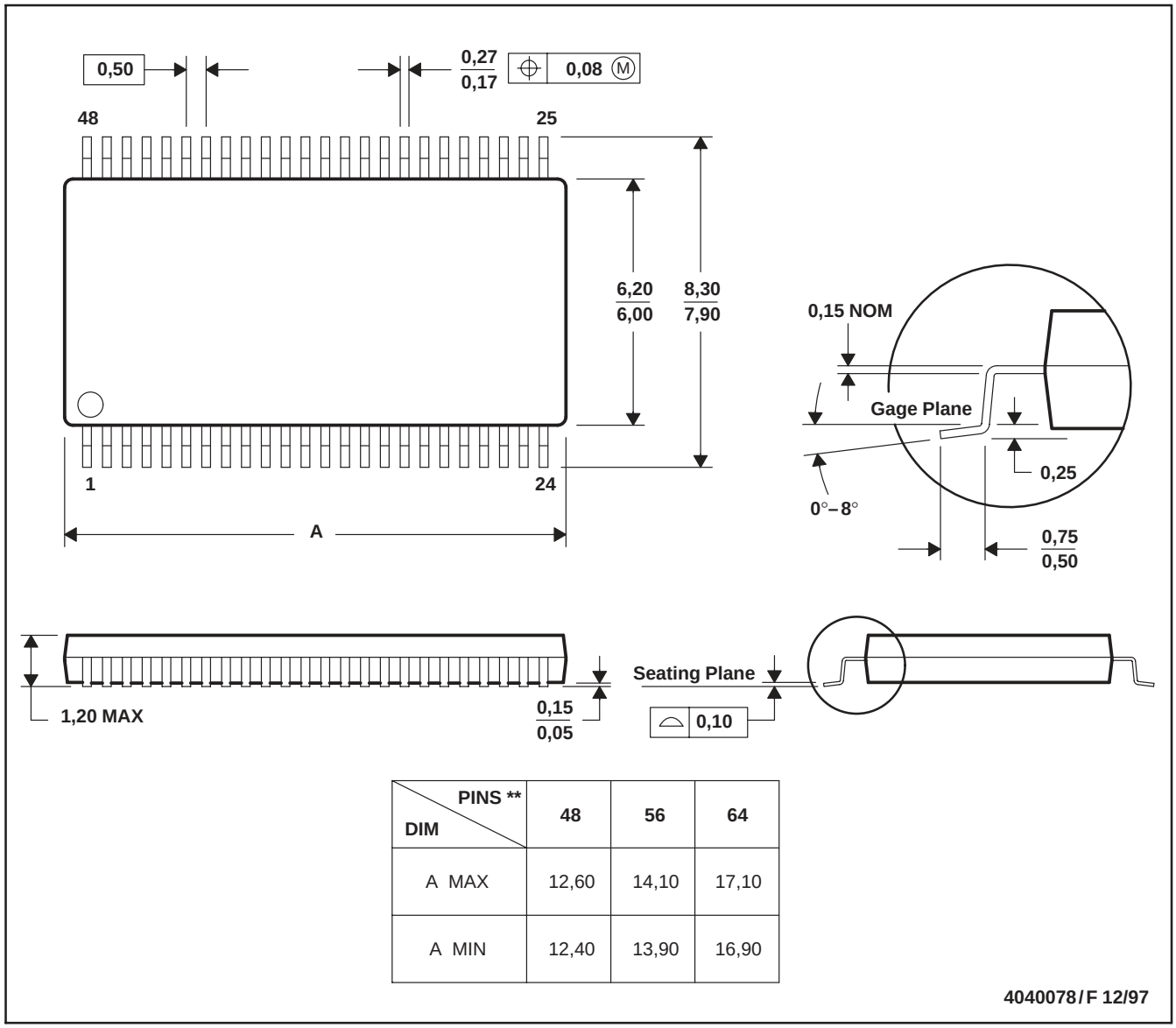


Figure 8. Start-Up Calibration Using RESET Terminal

MECHANICAL DATA

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PIN SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078/F 12/97

NOTES: B. All linear dimensions are in millimeters.
C. This drawing is subject to change without notice.
D. Body dimensions do not include mold protrusion not to exceed 0,15.
E. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLC976CDGG	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
TLC976CDGGR	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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