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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR 2SJ606

SWITCHING P-CHANNEL POWER MOS FET

DESCRIPTION

The 2SJ606 is P-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Super low on-state resistance: $R_{DS(on)1} = 15 \text{ m}\Omega \text{ MAX.}$ (Vgs = -10 V, Ip = -42 A) $R_{DS(on)2} = 23 \text{ m}\Omega \text{ MAX.}$ (Vgs = -4.0 V, Ip = -42 A)
- Low input capacitance: $C_{iss} = 4800 \text{ pF TYP.} (V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V})$
- Built-in gate protection diode

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

-60	V
∓20	V
∓83	А
∓300	А
120	W
1.5	W
150	°C
-55 to +150	°C
-40	А
160	mJ
	∓ 83 ∓ 300 120 1.5 150 -55 to +150 -40

Notes 1. PW \leq 10 μ s, Duty cycle \leq 1%

2. Starting T_{ch} = 25°C, V_{DD} = -30 V, R_G = 25 Ω , V_{GS} = $-20 \rightarrow 0$ V

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SJ606	TO-220AB
2SJ606-S	TO-262
2SJ606-ZJ	TO-263
2SJ606-Z	TO-220SMD Note

Note TO-220SMD package is produced only in Japan



(TO-220AB)

(TO-262)



(TO-263, TO-220SMD)



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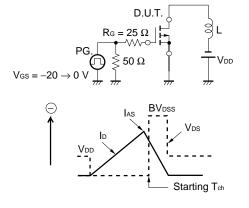
Document No. Date Published Printed in Japan

ELECTRICAL CHARACTERISTICS (TA = 25°C)

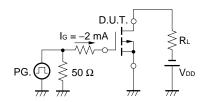
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = -60 V, V_{GS} = 0 V$			-10	μA
Gate Leakage Current	lgss	$V_{GS} = \mp 20 \text{ V}, V_{DS} = 0 \text{ V}$			∓10	μA
Gate Cut-off Voltage	VGS(off)	$V_{DS} = -10 V, I_{D} = -1 mA$	-1.5	-2.0	-2.5	V
Forward Transfer Admittance	y fs	$V_{DS} = -10 V$, $I_{D} = -42 A$	38	74		S
Drain to Source On-state Resistance	RDS(on)1	$V_{GS} = -10 V$, $I_D = -42 A$		12	15	mΩ
	RDS(on)2	$V_{GS} = -4.0 \text{ V}, \text{ Id} = -42 \text{ A}$		16	23	mΩ
Input Capacitance	Ciss	$V_{DS} = -10 V$		4800		pF
Output Capacitance	Coss	$V_{GS} = 0 V$		1200		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		340		pF
Turn-on Delay Time	td(on)	$V_{DD} = -30 \text{ V}, \text{ Id} = -42 \text{ A}$		13		ns
Rise Time	tr	$V_{GS} = -10 V$		13		ns
Turn-off Delay Time	td(off)	$R_G = 0 \Omega$		290		ns
Fall Time	tr			160		ns
Total Gate Charge	QG	V _{DD} = -48 V		120		nC
Gate to Source Charge	Qgs	$V_{GS} = -10 V$		20		nC
Gate to Drain Charge	Qgd	ID = -83 A		30		nC
Body Diode Forward Voltage	V _{F(S-D)}	IF = 83 A, VGS = 0 V		1.1		V
Reverse Recovery Time	trr	IF = 83 A, VGS = 0 V		60		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ µs		120		nC

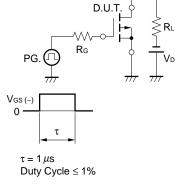
TEST CIRCUIT 1 AVALANCHE CAPABILITY

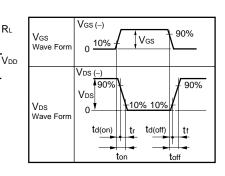
TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



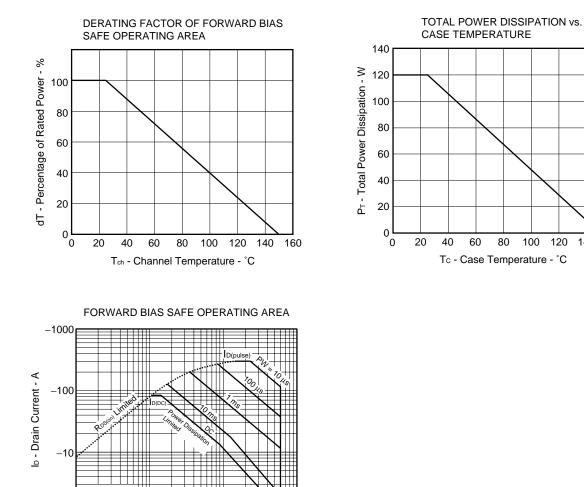




120

140 160

TYPICAL CHARACTERISTICS (TA = 25°C)



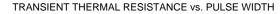
VDS - Drain to Source Voltage - V

-10

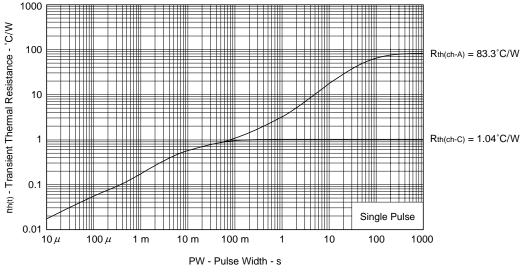
Tc = 25°C Single Pulse

-1

-0.1

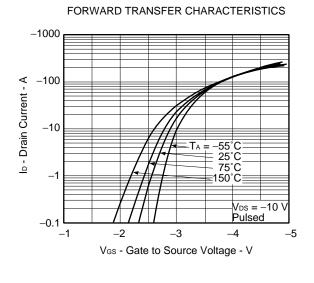


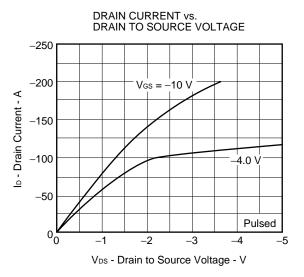
-100

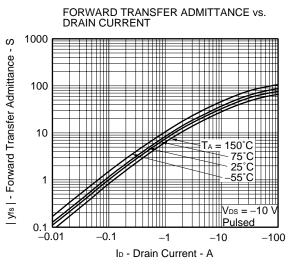


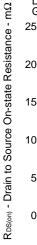
Data Sheet D14654EJ3V0DS



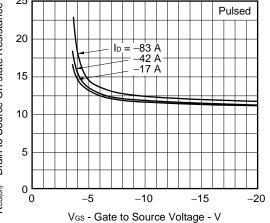


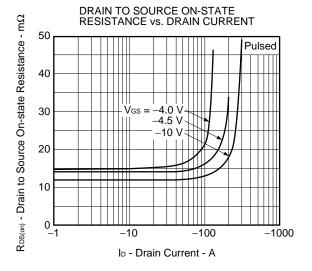


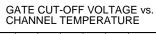


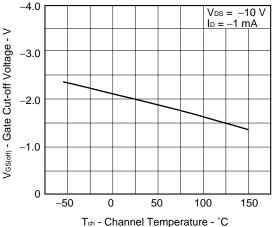


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE





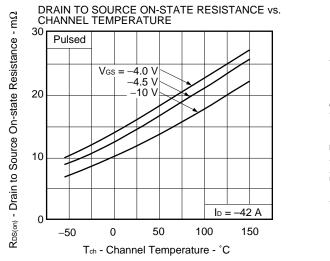


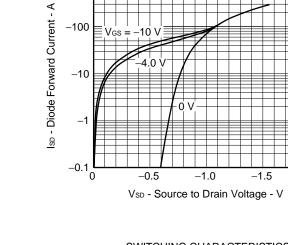


Data Sheet D14654EJ3V0DS

NEC

-2.0





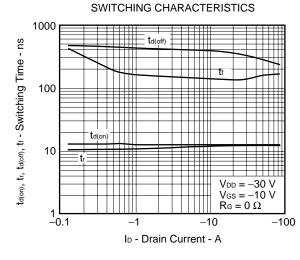
-1000

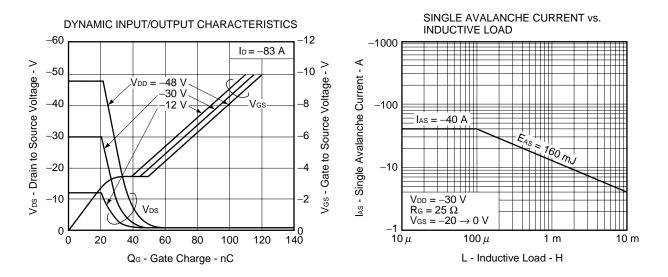
Pulsed

SOURCE TO DRAIN DIODE

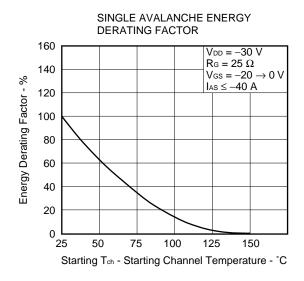
FORWARD VOLTAGE

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE 100000 $V_{GS} = 0 V$ f = 1 MHzCiss, Coss, Crss - Capacitance - pF 10000 Ciss 1000 Ηm 100 –0.1 -1 -10 -100 VDS - Drain to Source Voltage - V



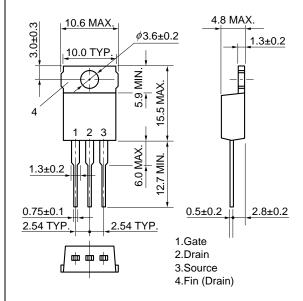


Data Sheet D14654EJ3V0DS

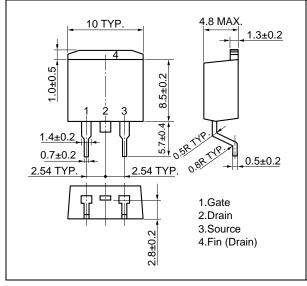


* PACKAGE DRAWINGS (Unit: mm)

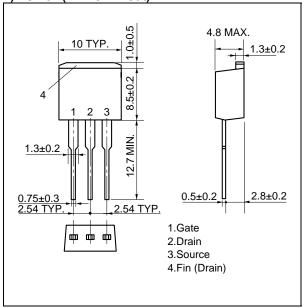
1) TO-220AB (MP-25)



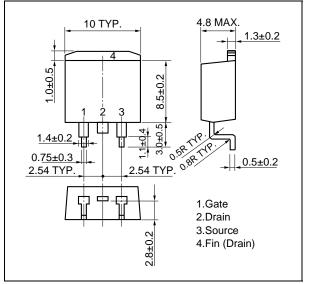
3) TO-263 (MP-25ZJ)



2) TO-262 (MP-25 Fin Cut)

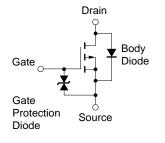


4) TO-220SMD (MP-25Z) Note



Note This package is produced only in Japan.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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