Design Example Report

Title	**30 W USB PD 3.0 Power Supply with 3.3 V–16 V PPS Output Using InnoSwitch™3-PD PowiGaN™ INN3878C-H804**
Specification	90 VAC – 265 VAC Input; 5 V / 3 A, 9 V / 3 A, 12V / 2.5A 15 V / 2 A, 20 V / 1.5 A, 3.3 V – 11 V / 3 A PPS (30 W Power-limited) Output, or 3.3 V – 16V / 2 A PPS
Application	USB PD / PPS Power Adapter
Author	Applications Engineering Department
Document Number	DER-836
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Revision	1.0

Summary and Features

- InnoSwitch3-PD – off-line QR Flyback Switcher IC with Integrated USB Type-C and USB-PD Controller, Integrated High-Voltage Switch, Synchronous Rectification and FluxLinkTM feedback
- Integrated USB Type-C and USB-PD Controller reduces footprint, no external microcontroller required
- Telemetry and comprehensive protection features
  - Meets DOE6 and CoC v5 2016 Average Efficiency requirements with high margin (>3.0%)
    - 5 V Output: 90.72% at 115 VAC (8.88% margin); 90.19% at 230 VAC (8.35%margin)
    - 9 V Output: 92.08% at 115 VAC (4.79% margin); 91.89% at 230 VAC (4.60%margin)
    - 12 V Output: 92.31% at 115 VAC (4.61% margin); 92.26% at 230 VAC (4.56% margin)
    - 15 V Output: 91.59% at 115 VAC (3.89% margin); 91.97% at 230 VAC (4.27%margin)
    - 20 V Output: 90.94% at 115 VAC (3.24% margin); 91.58% at 230 VAC (3.88%margin)
  - < 18 mW no-load input power at 230 VAC
  - Meets CISPR22 / EN55022 Class B Conducted EMI with high margin
    - >6 dB margin at worst case condition (12 V / 2.5 A, 230 VAC)
  - Low component count, high power density
    - Total part count: 59
    - Power density: 12.27 W / inch^3 without enclosure (1.73″ x 1.73″ x 0.817″ formfactor)

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PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at https://www.power.com/company/intellectual-property-licensing/.

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Table of Contents

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a 30 W USB PD 3.0 power supply using InnoSwitch3-PD INN3878C-H804 IC. The USB PD source capabilities of the power supply are listed below.

- PDO1: 5 V / 3 A (Fixed Supply)
- PDO2: 9 V / 3 A (Fixed Supply)
- PDO3: 12 V / 2.5 A (Fixed Supply)
- PDO4: 15 V / 2.0 A (Fixed Supply)
- PDO5: 20 V / 1.5 A (Fixed Supply)
- PDO6: 3.3 V – 11 V / 3 A (Programmable Power Supply, 30 W power-limited)
- PDO7: 3.3 V – 16 V / 2 A (Programmable Power Supply)

This design shows the high power density and efficiency that is possible due to the high level of integration of the InnoSwitch3-PD controller providing exceptional performance.

The report contains the power supply specification, schematic diagram, printed circuit board layout, bill of materials, magnetics specifications, and performance data.

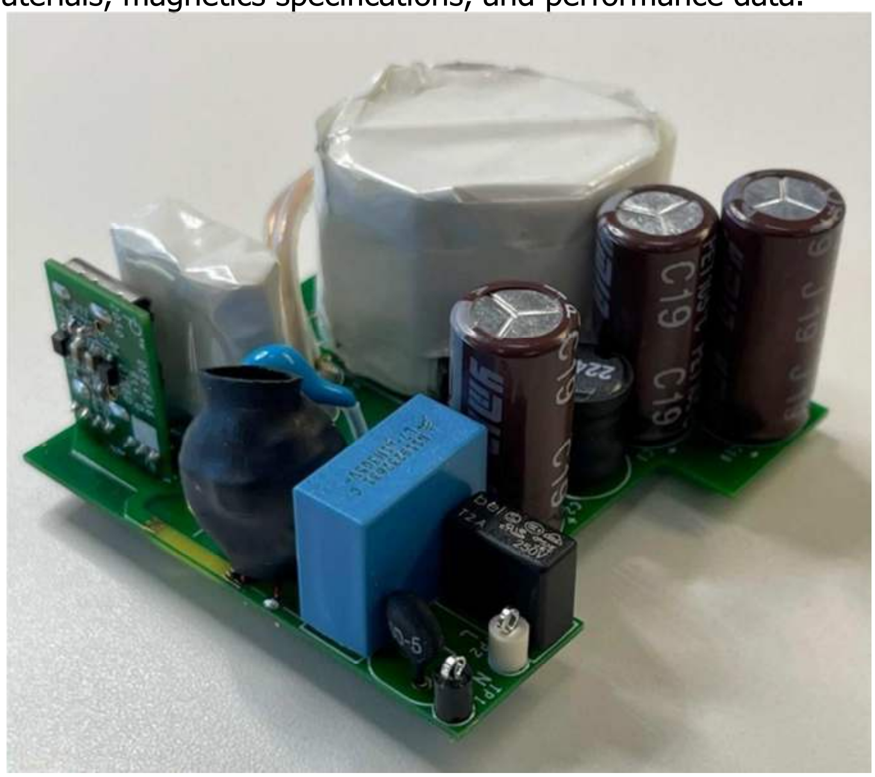


Figure 1 – Populated Circuit Board Photograph, Entire Assembly.

Figure 2 – Populated Circuit Board Photograph – Top.

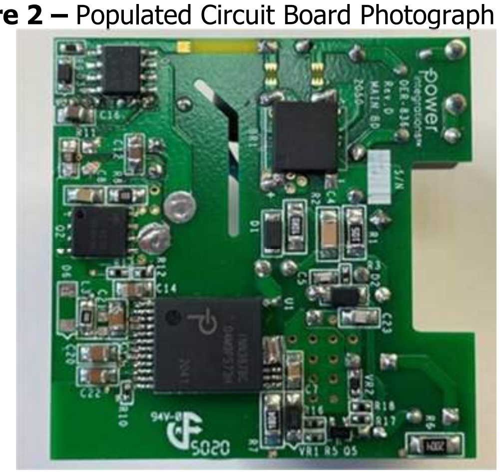


Figure 3 – Populated Circuit Board Photograph – Bottom (L: 44 mm x W 44 mm).

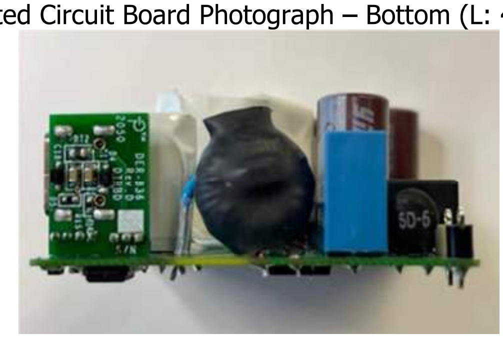


Figure 4 – Populated Circuit Board Photograph – Side (H: 21 mm).

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90	50/60	265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47		64	Hz	
No-load Input Power				18	mW	Measured at 230 VAC
5 V / 3 A Setting						
Output Voltage	$V_{OUT(5\ V)}$		5.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(5\ V)}$			200	mV	Measured at End of 48 mΩ Cable.
Output Current	$I_{OUT(5\ V)}$			3.0	A	±3%
Average Efficiency	$\eta_{(5\ V)}$		90.2		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(5\ V)}$			15	W	
9 V / 3 A Setting						
Output Voltage	$V_{OUT(9\ V)}$		9.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(9\ V)}$			200	mV	Measured at End of 48 mΩ Cable.
Output Current	$I_{OUT(9\ V)}$			3.0	A	±3%
Average Efficiency	$\eta_{(9\ V)}$		91.6		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(9\ V)}$			27	W	
12 V / 2.5 A Setting						
Output Voltage	$V_{OUT(12\ V)}$		12.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(12\ V)}$			200	mV	Measured at End of 48 mΩ Cable.
Output Current	$I_{OUT(12\ V)}$			2.5	A	±3%
Average Efficiency	$\eta_{(12\ V)}$		91.8		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(12\ V)}$			30	W	
15 V / 2 A Setting						
Output Voltage	$V_{OUT(15\ V)}$		15.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(15\ V)}$			200	mV	Measured at End of 48 mΩ Cable.
Output Current	$I_{OUT(15\ V)}$			2.0	A	±3%
Average Efficiency	$\eta_{(15\ V)}$		91.1		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(15\ V)}$			30	W	
20 V / 1.5 A Setting						
Output Voltage	$V_{OUT(20\ V)}$		20.0		V	
Output Voltage Ripple	$V_{RIPPLE(20\ V)}$			200	mV	±3%
Output Current	$I_{OUT(20\ V)}$			1.5	A	Measured at End of 48 mΩ Cable.
Average Efficiency	$\eta_{(20\ V)}$		90.4		%	
Continuous Output Power	$P_{OUT(20\ V)}$			30	W	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
3.3 – 11 V PPS Setting						
Maximum Programmable Output Voltage	$V_{OUT(MAX)}$			11	V	APDO Maximum Voltage.
Minimum Programmable	$V_{OUT(MIN)}$	3.3			V	APDO Minimum Voltage.

Output Voltage						
Output Current	**$I_{OUT(PPS)}$**			3.0	A	±3%
PPS Voltage Step	**$V_{STEP(PPS)}$**		20		mV	PPS Voltage Step (USB PD 3.0).
PPS Current Step	**$I_{STEP(PPS)}$**		50		mA	PPS Current Step (USB PD 3.0).
Continuous Output Power	**P_{OUT}**			30	W	PPS Power Limited bit = 1 (USB PD 3.0).
3.3 – 16 V PPS Setting						
Maximum Programmable Output Voltage	**$V_{OUT(MAX)}$**			16	V	APDO Maximum Voltage.
Minimum Programmable Output Voltage	**$V_{OUT(MIN)}$**	3.3			V	APDO Minimum Voltage.
Output Current	**$I_{OUT(PPS)}$**			2.0	A	±3%
PPS Voltage Step	**$V_{STEP(PPS)}$**		20		mV	PPS Voltage Step (USB PD 3.0).
PPS Current Step	**$I_{STEP(PPS)}$**		50		mA	PPS Current Step (USB PD 3.0).
Continuous Output Power	**P_{OUT}**			32	W	PPS Power Limited bit = 0 (USB PD 3.0).
Conducted EMI Margin		6			dB	Meets CISPR22B / EN55022B
Ambient Temperature	**T_{AMB}**	0		45	ºC	Open Frame, Sea Level.

Note: To use this design for a charger/adapter with a different shape and form factor, the changes in the circuit board layout must be carefully evaluated to meet the target specifications for EMI, ESD, and Line Surge performance.

3 Schematic

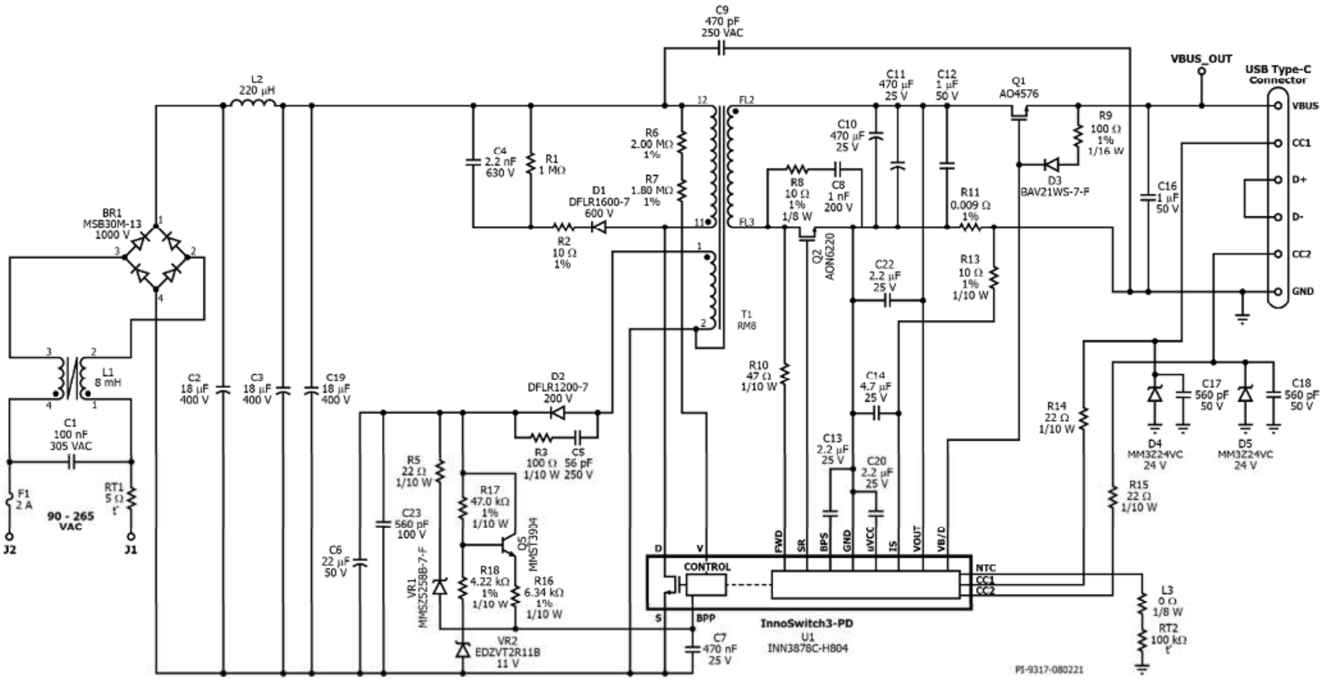


Figure 5 – DER-836 Rev D Schematic.

4 Circuit Description

4.1 *Input Rectifier and EMIFilter*

The input fuse F1 isolates the circuit and provides protection from component failure. NTC thermistor RT1 limits the inrush current when the input AC supply is connected. Common mode choke L1, differential mode choke L2, with capacitors C1, C2, C3, and Y-cap C9 provide common mode and differential mode noise filtering for EMI attenuation. Bridge rectifier BR1 rectifies the AC line voltage to have a full wave rectified DC, which is filtered by the bulk capacitors C2, C3, and C19.

4.2 *InnoSwitch3-PD IC Primary*

One end of the flyback transformer T1 primary winding is connected to the rectified DC bus and the other end is connected to the drain terminal of the switch inside the InnoSwitch3-PD IC U1. Resistors R6 and R7 provide input voltage sensing for protection in case of AC input undervoltage or overvoltage.

A low-cost R2CD clamp formed by diode D1, resistors R1, and R2, and capacitor C4 limits the peak drain-source voltage of U1 at the instant the switch inside U1 turns off. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor C7 when AC is first applied. During normal operation, the primary side block is powered from an auxiliary winding on the transformer T1. The output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C6 and C23. Resistor R16 limits the current being supplied to the BPP pin of the InnoSwitch3-PD IC U1. A linear regulator comprising resistor R17, R18, BJT Q5 and Zener diode VR2 ensures sufficient current flows through R16 such that the internal current source of U1 is not required to charge C7 during normal operation. The RC network consisting of resistor R3 and capacitor C5 offers damping of the high frequency ringing in the voltage across diode D2 to reduce radiated EMI.

Zener diode VR1 offers primary sensed output overvoltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at output of the converter, the auxiliary winding voltage increases and causes breakdown of VR2 which then causes excess current to flow into the BPP pin of InnoSwitch3-PD IC U1. If the current flowing into the BPP pin increases above the ISD threshold, the InnoSwitch3-PD controller will latch off and prevent any further increase in output voltage. Resistor R5 limits the current injected to BPP pin when the output overvoltage protection is triggered.

4.3 *InnoSwitch3-Pro IC Secondary and USB Power Delivery Controller*

The secondary-side of the InnoSwitch3-PD IC provides output voltage and current sensing and a gate drive to a FET for synchronous rectification. The voltage across the transformer secondary winding is rectified by the secondary-side synchronous rectifier FET (SR FET) Q2 and filtered by capacitors C10, C11 and C12. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a RC snubber, R8 and C8.

The gate of Q2 is turned on by secondary-side controller inside IC U1, based on the secondary winding voltage sensed via resistor R10 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the SR FET is turned off just prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous mode of operation, the SR FET is turned off when the magnitude of the voltage drop across the SR FET falls below a threshold of approximately VSR(TH). Secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switches and provides extremely reliable synchronous rectifier operation.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C13 connected to the BPS pin of InnoSwitch3- PD IC U1 provides decoupling for the internal circuitry.

The output current is sensed by monitoring the voltage drop across resistor R11. The current measurement is filtered with decoupling capacitor C14 and R13; it is monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold of approximately 32 mV is used to reduce losses. Once the threshold is exceeded, the InnoSwitch3-PD IC U1 regulates the number of switch pulses to maintain a fixed output current.

During constant current (CC) operation, when the output voltage falls, the secondary side controller inside InnoSwitch3-PD IC U1 will power itself from the secondary winding directly. During the on-time of the primary-side power switch, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS pin decoupling capacitor C13 via resistor R10 and an internal regulator. This allows output current regulation to be maintained down to the minimum UV threshold. Below this level the unit enters auto-restart until the output load is reduced.

When the output current is below the CC threshold, the converter operates in constant voltage mode. The output voltage is monitored by the VOUT pin of the InnoSwitch3-PD IC. Similar with current regulation, the output voltage is also compared to an internal voltage threshold and the controller inside IC U1 regulates the output voltage by controlling the number of switch pulses. Capacitor C22 is needed between the VOUT pin and the SECONDARY GROUND pin for ESD protection of the VOUT pin.

N-channel MOSFET Q1 functions as the bus switch which connects or disconnects the output of the flyback converter from the USB Type-C receptacle. MOSFET Q1 is controlled by the VB/D pin on the InnoSwitch3-PD IC. Resistor R9 and diode D3 are connected across the Source and Gate terminals of Q1 to provide a discharge path for the bus voltage when the Q1 is turned off. Capacitor C16 is used at the output for ESD protection and output voltage ripple reduction.

The InnoSwitch3-PD IC U1 integrates the USB Power Delivery (USB PD) controller and is internally powered through the µVCC pin. USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which Type-C plug is connected.

The InnoSwitch3-PD IC sets the CV, CC, VKP, OVA and UVA parameters via programmed firmware. These parameters correspond to the output voltage, constant output current, constant output power voltage threshold, output overvoltage threshold, and output undervoltage threshold registers of the InnoSwitch3-Pro PD, respectively.

Capacitor C20 provides decoupling to the µVCC of the InnoSwitch3-PD IC. Capacitors C17 and C18, resistors R14 and R15, and zener diodes D4, and D5 provide protection from ESD to pins CC1 and CC2.

5 PCB Layout

PCB copper thickness is 0.031 inches.

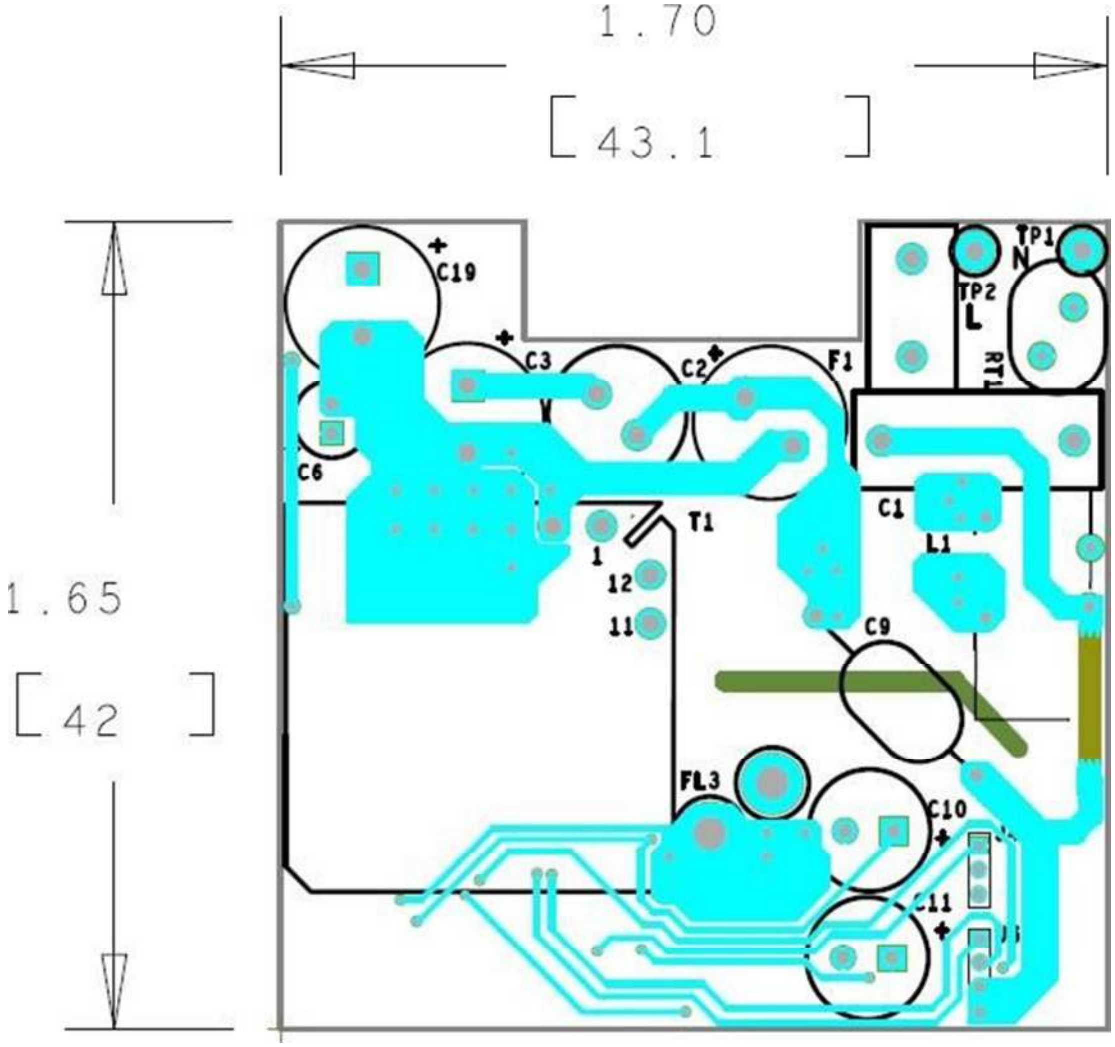


Figure 6 – DER-836 Rev D PCB Layout, Top.

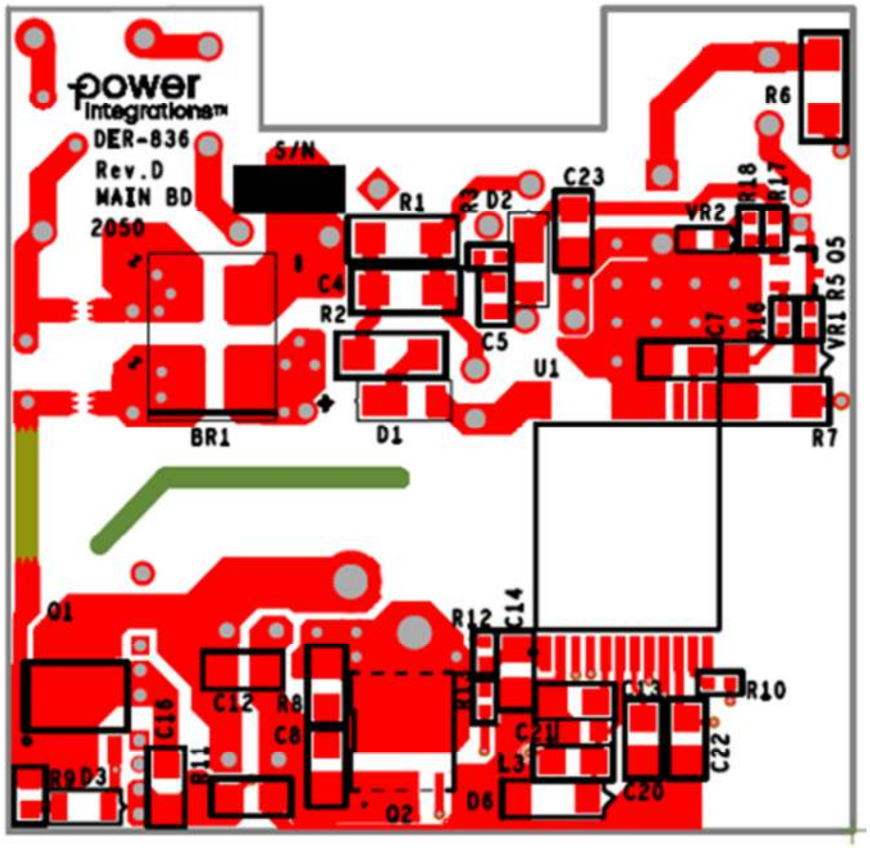


Figure 7 – DER-836 Rev D PCB Layout, Bottom.

Note: Component references R12, C21, and D6, although present in the layout, should not be populated.

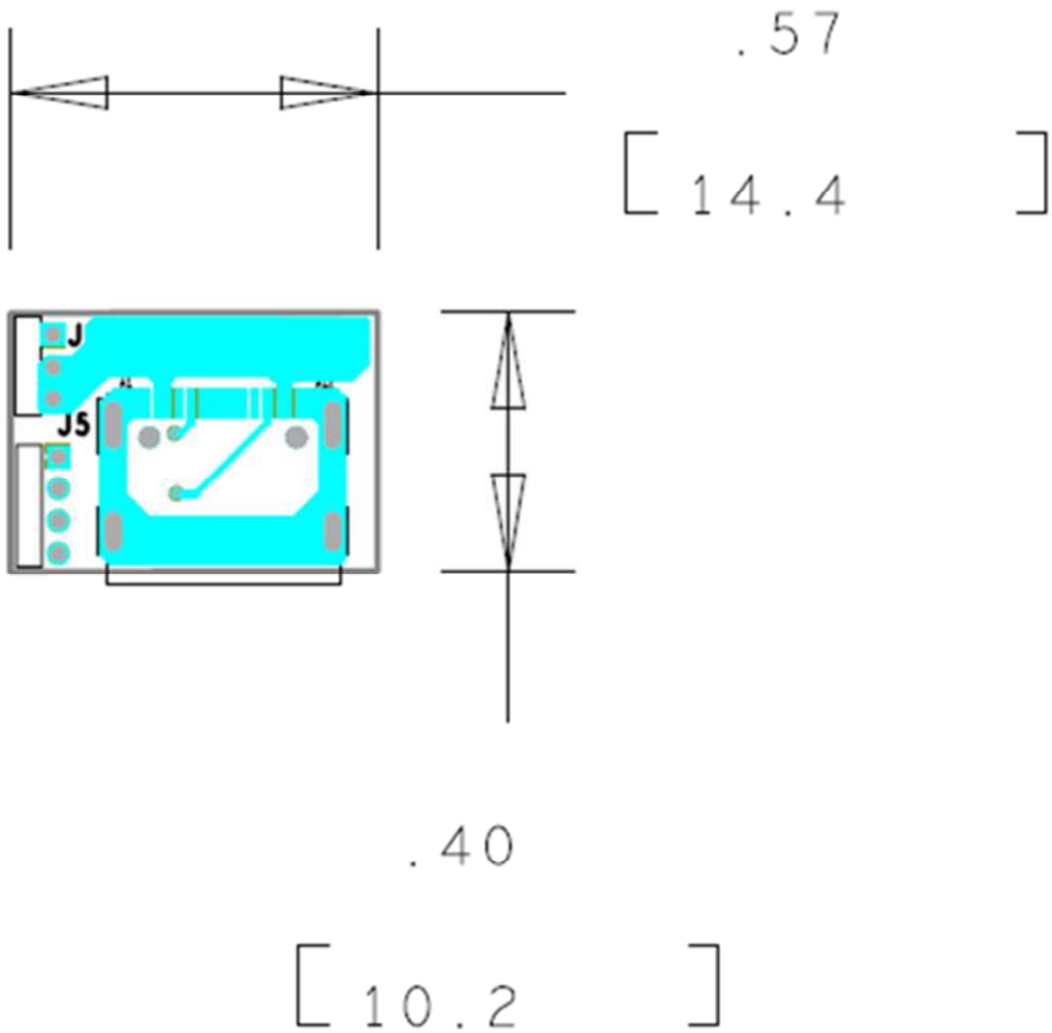


Figure 8 – USB Type-C Connector PCB Layout, Top.

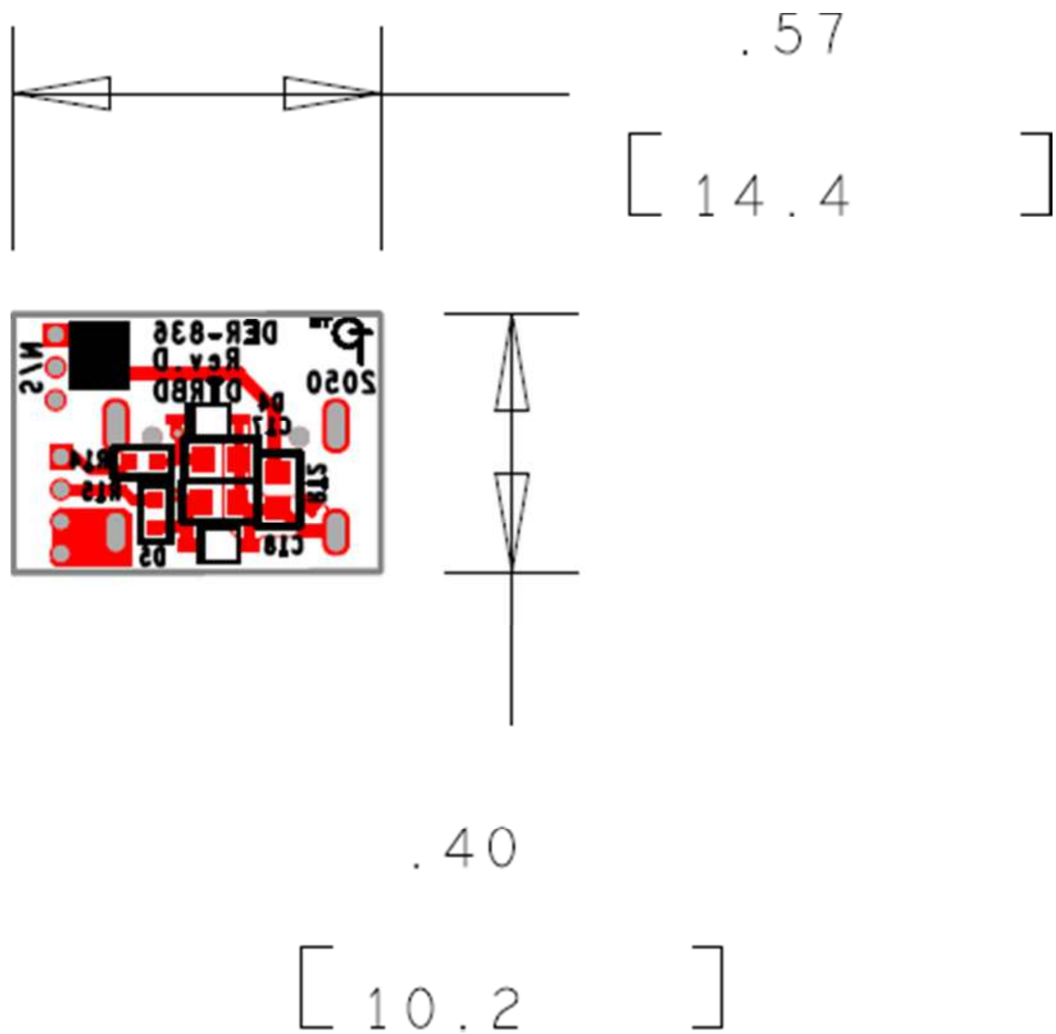


Figure 9 – USB Type-C Connector PCB Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	Bridge Rectifier, Single Phase, Standard, 1 kV, 3 A, SMT, 4-MSBL, 4-SMD, Flat Leads	MSB30M-13	Diodes, Inc.
2	1	C1	100 nF, 305 VAC, Polypropylene Film, X2	MK61104-P24M	Sichuan Zhongxing
3	3	C2 C3 C19	18 µF, 400 V, Electrolytic, (8 x 17)	KCXD1702G180MF	Shanghai Yongming
4	1	C4	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K	TDK
5	1	C5	56 pF, 250 V, Ceramic, NP0, 0603	GQM1875C2E560JB12D	Murata
6	1	C6	Cap Alum 22µF 20% 50V Radial	UVR1H220MDD1TD	Nichicon
7	1	C7	0.47 µF, ±10%,25 V, Ceramic, X7R, 0805	CGA4J2X7R1E474K125AA	TDK
8	1	C8	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
9	1	C9	470 pF, ±10%, 250VAC, X1, Y1, Ceramic, B, Radial, Disc	DE1B3RA471KA4BN01F	Murata
10	2	C10 C11	470 µF, 25 V, Electrolytic with polymer electrolyte, (6.3 x 14)	CRS-FX-1805078	AISHI
11	2	C12 C16	1 µF, ±20% ,50 V, Ceramic, X7R, Boardflex Sensitive, 0805	CGA4J3X7R1H105M125AE	TDK
12	3	C13 C20 C22	2.2 µF, ±10%, 25V, X7R, r, -55°C ~125°C, 0805	CL21B225KAFVPNE	Samsung
13	1	C14	4.7 µF ±10%, 25V, X7R, 0805,-55°C ~ 125°C	TMK212AB7475KG-T	Taiyo Yuden
14	2	C17 C18	560 pF, 50V, Ceramic, X7R, 0603, 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	CC0603KRX7R9BB561	Yageo
15	0	C21	Do Not Populate		
16	1	C23	560 pF, ±5%, 100V, General Purpose, Ceramic, C0G, NP0, 0805	CC0805JRNPO0BN561	Yageo Corp
17	1	D1	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
18	1	D2	200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes, Inc.
19	1	D3	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
20	2	D4 D5	DIODE, ZENER, 24 V, 200 mW, SC-90, SOD-323F	MM3Z24VC	ON Semi
21	0	D6	Do Not Populate		
22	1	F1	2 A, 250 V, Slow, Long Time Lag,RST	RST 2	Belfuse
23	1	J2	Connector, "Certified", USB - C, USB 3.1, For 0.031" PCB Material!, Superspeed+, Receptacle Connector, 16 Position, SMT, RA, TH	LM-U3231-096	LM-Link Precise
24	1	J4	3 Position (1 x 3) header, 0.050" (1.27 mm) pitch, Gold, R/A	M50-3930342	Harwin
25	1	J6	4 Position (1 x 4) header, 0.050" (1.27 mm) pitch, Gold, R/A	M50-3930442	Harwin
26	1	L1	CMC, 8 mH ±25% @ 100 kHz, Toroidal, wound on 32-00376-00 toroidal core, using #30 AWG wire, and Cable Tie PI # 75-00202-00	30-04109-00	Power Integrations
27	1	L2	Inductor, Fixed, 220 µH 0.43 A 5.4 MHz, Radial Lead	22R224C	Murata
28	1	Q1	MOSFET, N-Channel 30 V 20 A (Ta) 3.1 W (Ta) Surface Mount 8-SOIC	AO4576	Alpha & Omega Semi
29	1	Q2	MOSFET, N-CH, 100 V, 48 A (Tc), 113.5 W (Tc), DFN5X6, 8-DFN (5x6)	AON6220	Alpha & Omega Semi
30	1	Q5	NPN, Small Signal BJT, 40 V, 0.2 A, SOT-323	MMST3904-7-F	Diodes, Inc.
31	1	R1	RES, 1.0 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ105V	Panasonic
32	1	R2	RES, 10 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF10R0V	Panasonic
33	1	R3	RES, 100 Ω, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ101X	Panasonic
34	3	R5 R14 R15	RES, 22 Ω, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ220X	Panasonic
35	1	R6	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
36	1	R7	RES, 1.80 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1804V	Panasonic
37	1	R8	RES, 10 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF10R0V	Panasonic
38	1	R9	RES, 100 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1000V	Panasonic
39	1	R10	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ470X	Panasonic
40	1	R11	RES, 0.009 Ω, ±1%, 0.5 W, 0805, Current Sense, Moisture Resistant, Metal Element	CRF0805-FZ-R009ELF	Bourns
41	0	R12	Do Not Populate		
42	1	R13	RES, 10 Ω, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF10R0X	Panasonic
43	1	R16	RES, 6.34 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF6341X	Panasonic

44	1	R17	RES, 47.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF4702X	Panasonic
45	1	R18	RES, 4.22 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF4221X	Panasonic
46	1	L3	RES, 0 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEY0R00V	Panasonic
47	1	RT1	NTC Thermistor, 5 Ω, 1 A	MF72-005D5	Cantherm
48	1	RT2	NTC Thermistor, 100 kΩ, 1%,4250K, 0603	NCU18WF104F60RB	Murata
49	1	T1	DER-836 Rev D Transformer Rev 6	25-01185-00	Power Integrations
50	1	U1	InnoSwitch3-PD	INN3878C-H804	Power Integrations
51	1	VR1	DIODE ZENER 36 V 500 mW SOD123	MMSZ5258B-7-F	Diodes, Inc.
52	1	VR2	Zener Diode 11 V 150 mW ±2% SMT EMD2, SC-79, SOD-523	EDZVT2R11B	Rohm

7 Transformer Design Spreadsheet

1	ACDC_InnoSwitch3-PD_Flyback_032521; Rev.0.4; Copyright Power Integrations 2021	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-PD Flyback Design Spreadsheet
2	APPLICATION VARIABLES					
3	VAC_MIN	90		90	V	Minimum AC line voltage
4	VAC_MAX			265	V	Maximum AC input voltage
5	VAC_RANGE			UNIVERSAL		AC line voltage range
6	FLINE			60	Hz	AC line voltage frequency
7	CAP_INPUT	54.0		54.0	uF	Input capacitance
9	SET-POINT 1					
10	VOUT1	20.00		20.15	V	Output voltage 1, should be the highest output voltage required
11	IOUT1	1.500		1.500	A	Output current 1
12	POUT1			30.23	W	Output power 1
13	EFFICIENCY1	0.91		0.91		Converter efficiency for output 1
14	Z_FACTOR1	0.50		0.50		Z-factor for output 1
15	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object
17	SET-POINT 2					
18	VOUT2	16.00		16.00	V	Output voltage 2
19	IOUT2	2.000		2.000	A	Output current 2
20	POUT2			32.00	W	Output power 2
21	EFFICIENCY2	0.91		0.91		Converter efficiency for output 2
22	Z_FACTOR2	0.50		0.50		Z-factor for output 2
23	TYPE	APDO		APDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object
25	SET-POINT 3					
26	VOUT3	15.00		15.20	V	Output voltage 3
27	IOUT3	2.000		2.000	A	Output current 3
28	POUT3			30.40	W	Output power 3
29	EFFICIENCY3	0.92		0.92		Converter efficiency for output 3
30	Z_FACTOR3	0.50		0.50		Z-factor for output 3
31	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object
33	SET-POINT 4					
34	VOUT4	12.00		12.25	V	Output voltage 4
35	IOUT4	2.500		2.500	A	Output current 4
36	POUT4			30.63	W	Output power 4
37	EFFICIENCY4	0.92		0.92		Converter efficiency for output 4
38	Z_FACTOR4	0.50		0.50		Z-factor for output 4
39	TYPE	PDO	Info	PDO		The voltage entered is not a standard PDO(Power Delivery Object)
41	SET-POINT 5					
42	VOUT5	10.00		10.30	V	Output voltage 5
43	IOUT5	3.000		3.000	A	Output current 5
44	POUT5			30.90	W	Output power 5
45	EFFICIENCY5	0.92		0.92		Converter efficiency for output 5
46	Z_FACTOR5	0.50		0.50		Z-factor for output 5
47	TYPE	PDO	Info	PDO		The voltage entered is not a standard PDO(Power Delivery Object)
49	SET-POINT 6					
50	VOUT6	9.00		9.30	V	Output voltage 6

51	IOUT6	3.000		3.000	A	Output current 6
52	POUT6			27.90	W	Output power 6
53	EFFICIENCY6	0.92		0.92		Converter efficiency for output 6
54	Z_FACTOR6			0.50		Z-factor for output 6
55	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object
57	**SET-POINT 7**					
58	VOUT7	5.00		5.30	V	Output voltage 7
59	IOUT7	3.000		3.000	A	Output current 7
60	POUT7			15.90	W	Output power 7
61	EFFICIENCY7	0.90		0.90		Converter efficiency for output 7
62	Z_FACTOR7			0.50		Z-factor for output 7
63	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object
65	**SET-POINT 8**					
66	VOUT8	3.30		3.30	V	Output voltage 8
67	IOUT8	3.000		3.000	A	Output current 8
68	POUT8			9.90	W	Output power 8
69	EFFICIENCY8	0.90		0.90		Converter efficiency for output 8
70	Z_FACTOR8			0.50		Z-factor for output 8
71	TYPE	APDO		APDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object
73	**SET-POINT 9**					
74	VOUT9			0.00	V	Output voltage 9
75	IOUT9			0.000	A	Output current 9
76	POUT9			0.00	W	Output power 9
77	EFFICIENCY9			0.00		Converter efficiency for output 9
78	Z_FACTOR9			0.00		Z-factor for output 9
79	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object
81	VOLTAGE_CDC	0.300		0.300	V	Cable drop compensation desired at maximum output current
85	**PRIMARY CONTROLLER SELECTION**					
86	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
87	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
88	VDRAIN_BREAKDOWN	750		750	V	Device breakdown voltage
89	DEVICE_GENERIC	INN38X8		INN38X8		Device selection
90	DEVICE_CODE			INN3878C		Device code
91	PDEVICE_MAX			55	W	Device maximum power capability
92	RDSON_25DEG			0.68	Ω	Primary switch on-time resistance at 25°C
93	RDSON_100DEG			1.02	Ω	Primary switch on-time resistance at 100°C
94	ILIMIT_MIN			1.581	A	Primary switch minimum current limit
95	ILIMIT_TYP			1.700	A	Primary switch typical current limit
96	ILIMIT_MAX			1.819	A	Primary switch maximum current limit
97	VDRAIN_ON_PRSW			0.38	V	Primary switch on-time voltage drop
98	VDRAIN_OFF_PRSW			585.31	V	Peak drain voltage on the primary switch during turn-off
102	**WORST CASE ELECTRICAL PARAMETERS**					
103	FSWITCHING_MAX	54730	Info	54730	Hz	The worst case minimum operating frequency is less than 25kHz: may result in audible noise
104	VOR	142.0		142.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
105	VMIN			90.03	V	Valley of the rectified minimum input AC voltage at

						full load
106	KP			0.888		Measure of continuous/discontinuous mode of operation
107	MODE_OPERATION			CCM		Mode of operation
108	DUTYCYCLE			0.522		Primary switch duty cycle
109	TIME_ON			11.27	us	Primary switch on-time
110	TIME_OFF			8.87	us	Primary switch off-time
111	LPRIMARY_MIN			578.6	uH	Minimum primary magnetizing inductance
112	LPRIMARY_TYP			609.0	uH	Typical primary magnetizing inductance
113	LPRIMARY_TOL			5.0	%	Primary magnetizing inductance tolerance
114	LPRIMARY_MAX			639.5	uH	Maximum primary magnetizing inductance
116	**PRIMARY CURRENT**					
117	IAVG_PRIMARY			0.375	A	Primary switch average current
118	IPEAK_PRIMARY			1.607	A	Primary switch peak current
119	IPEDESTAL_PRIMARY			0.160	A	Primary switch current pedestal
120	IRIPPLE_PRIMARY			1.607	A	Primary switch ripple current
121	IRMS_PRIMARY			0.633	A	Primary switch RMS current
123	**SECONDARY CURRENT**					
124	IPEAK_SECONDARY			11.476	A	Secondary winding peak current
125	IPEDESTAL_SECONDARY			1.145	A	Secondary winding pedestal current
126	IRMS_SECONDARY			4.899	A	Secondary winding RMS current
127	IRIPPLE_CAP_OUT			3.873	A	Output capacitor ripple current
131	**TRANSFORMER CONSTRUCTION PARAMETERS**					
132	**CORE SELECTION**					
133	CORE	RM8	Info	RM8		Refer to the Transformer Parameters tab to verify fit factor
134	CORE NAME			B65811J0000R095		Core code
135	AE			64.0	mm^2	Core cross sectional area
136	LE			38.0	mm	Core magnetic path length
137	AL			4100	nH	Ungapped core effective inductance per turns squared
138	VE			2430	mm^3	Core volume
139	BOBBIN NAME			B65812N1012D001		Bobbin name
140	AW			30.0	mm^2	Bobbin window area
141	BW	9.25		9.25	mm	Bobbin width
142	MARGIN			0.0	mm	Bobbin safety margin
144	**PRIMARY WINDING**					
145	NPRIMARY			50		Primary winding number of turns
146	BPEAK			3720	Gauss	Peak flux density
147	BMAX			3157	Gauss	Maximum flux density
148	BAC			1579	Gauss	AC flux density (0.5 x Peak to Peak)
149	ALG			244	nH	Typical gapped core effective inductance per turns squared
150	LG			0.311	mm	Core gap length
151	LAYERS_PRIMARY			2		Primary winding number of layers
152	AWG_PRIMARY	28		28		Primary wire gauge
153	OD_PRIMARY_INSULATED			0.375	mm	Primary wire insulated outer diameter
154	OD_PRIMARY_BARE			0.321	mm	Primary wire bare outer diameter
155	CMA_PRIMARY			252.3	Cmils/A	Primary winding wire CMA
157	**SECONDARY WINDING**					
158	NSECONDARY	7		7		Secondary winding number of turns
159	AWG_SECONDARY	20		20		Secondary wire gauge
160	OD_SECONDARY_INSULATED			1.118	mm	Secondary wire insulated outer diameter
161	OD_SECONDARY_BARE			0.812	mm	Secondary wire bare outer diameter
162	CMA_SECONDARY			208.5	Cmils/A	Secondary winding wire CMA
164	**BIAS WINDING**					

165	NBIAS			14		Bias winding number of turns
169	**PRIMARY COMPONENTS SELECTION**					
170	**LINE UNDERVOLTAGE**					
171	BROWN-IN REQURED			72.00	V	Required line brown-in threshold
172	RLS			3.82	MΩ	Connect two 1.91 MOhm resistors to the V-pin for the required UV/OV threshold
173	BROWN-IN ACTUAL			72.58	V	Actual brown-in threshold using standard resistors
174	BROWN-OUT ACTUAL			63.94	V	Actual brown-out threshold using standard resistors
176	**LINE OVERVOLTAGE**					
177	OVERVOLTAGE_LINE		Warning	319.20	V	The device voltage stress will be higher than 650V when overvoltage is triggered
179	**BIAS WINDING**					
180	VBIAS			9.00	V	Rectified bias voltage at the cable disconnect (5V) set-point
181	VF_BIAS			0.70	V	Bias winding diode forward drop
182	VREVERSE_BIASDIODE			113.53	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
183	CBIAS			22	uF	Bias winding rectification capacitor
184	CBPP			0.47	uF	BPP pin capacitor
188	**SECONDARY COMPONENTS SELECTION**					
189	**RECTIFIER**					
190	VDRAIN_OFF_SRFET			72.41	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
191	SRFET	AON6220		AON6220		Secondary rectifier (Logic MOSFET)
192	VBREAKDOWN_SRFET			100	V	Secondary rectifier breakdown voltage
193	RDSON_SRFET			7.4	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V

Note: The warning on item number 177 above has been verified to not be an issue for this design (INN3878C is a 750 V rating device).

8 Transformer Specification (T1)

8.1 *Electrical Diagram*

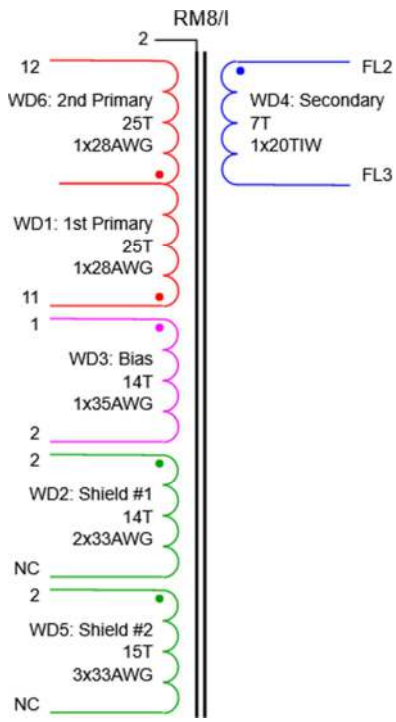


Figure 10 – Transformer Electrical Diagram.

8.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Across pin 11 to pin 12, with all other windings open, 100 kHz, 1.0 V test level.	609 μH ±3%
Primary Leakage Inductance	Across pin 11 to pin 12, with FL2 and FL3 shorted, 100 kHz, 1.0 V test level.	7 μH (Max.)
Resonant Frequency	Across pin 11 to pin 12, with all other windings open.	1,200 kHz (Min.)
Electrical Strength (Primary to Secondary)	Across shorted primary windings (pins 11, 12, 1, 2) to shorted secondary winding (FL2, FL3).	3000 VAC, 10 mA 200 V / s ramp rate, 60 s soak

8.3 *Transformer Build Diagram*

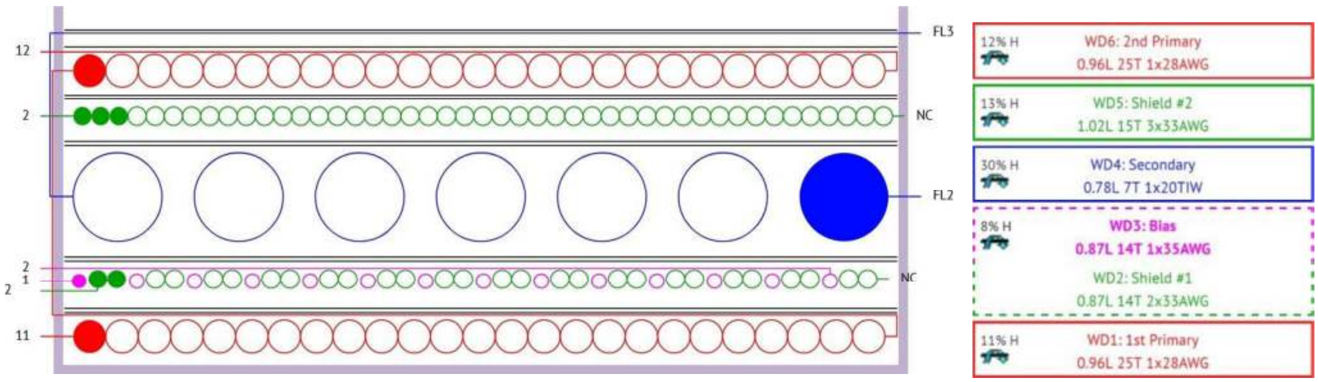


Figure 11 – Transformer Build Diagram.

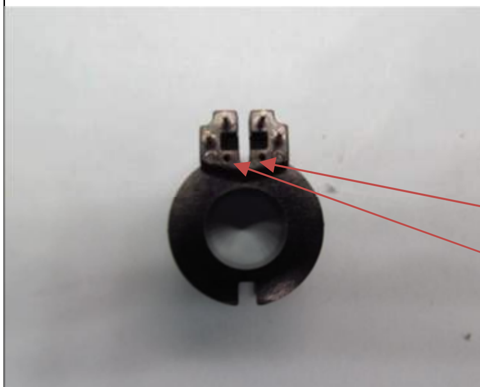
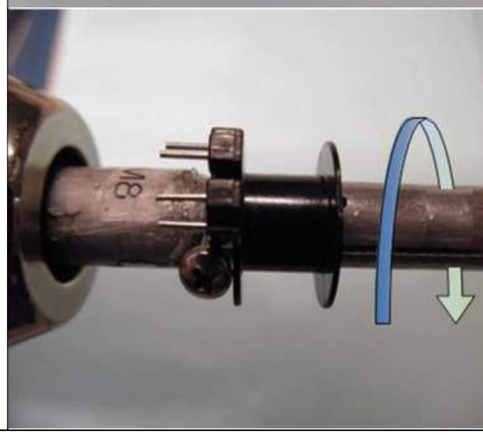
8.4 *Material List*

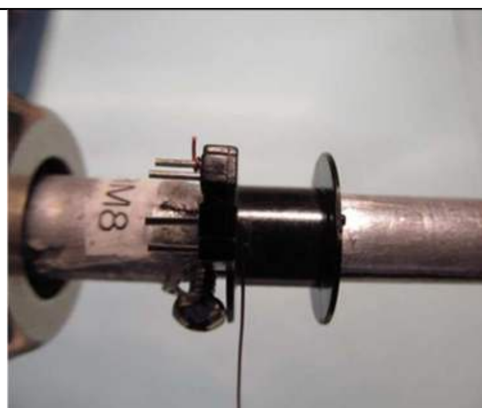
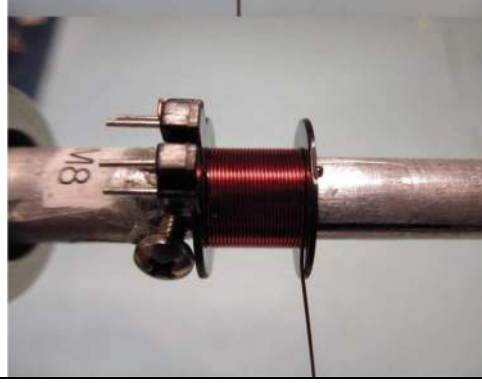
Item	Description
[1]	Core: RM8 TDK-PC95.
[2]	Bobbin: RM8, Vertical, 6pins (6/0), PI#: 25-01147-00.
[3]	Clip: RM8, MHW Int Corp; or equivalent.
[4]	Magnet Wire: #28 AWG, Double Coated.
[5]	Magnet Wire: #32 AWG, Double Coated.
[6]	Magnet Wire: #33 AWG, Double Coated.
[7]	Magnet Wire: #35 AWG, Double Coated.
[8]	Magnet Wire: #20 AWG, Triple Insulated Wire.
[9]	Bus Wire: #28 AWG, Alpha Wire, Tinned Copper.
[10]	Tape: 3M 1350-F, Polyester Film, 1 mil Thickness, 9.3 mm Width.
[11]	Tape: 3M 1350-F, Polyester Film, 1 mil Thickness, 24 mm x 52 mm.
[12]	Varnish: Dolph BC-359.
[13]	Teflon tube: #20 AWG, AlphaWire TFT-200-20; or equivalent.

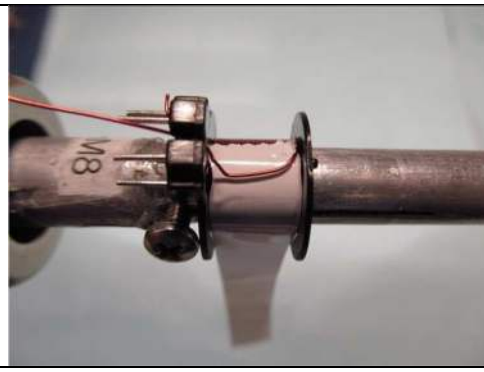
8.5 *Transformer Winding Summary Instructions*

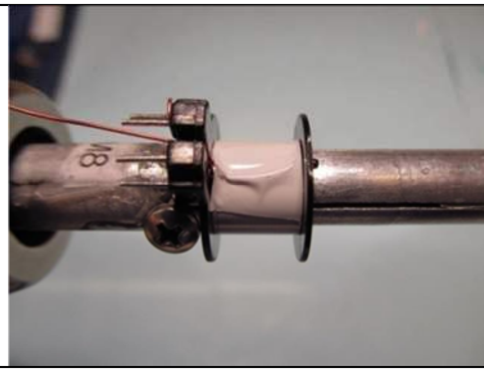
Winding Preparation	Remove pin 3 and 10 of bobbin Item [2], and place on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.
WD1 1ST Primary	Start at pin 11, wind 25 turns of wire Item [4] in 1 layer, with tight tension, from left to right. At the last turn, bring the wire back to left, and leave enough length of wire-floating for 2nd Primary.
Insulation	1 layer of tape Item [10].
WD2: Bias & WD3: Shield1	Use single wire Item [7] start at pin 1 for Bias winding, also use 2 wires same Item [5] start at pin 2 for Shield1 winding. Wind all 3 wires in parallel, at the 14th turn: - bring single wire for Bias winding to the left and terminate at pin 2, - cut short 2 wires for Shield1 Winding as No-Connect.
Insulation	2 layers of tape Item [10].
WD4 Secondary	Start at right slot of secondary side, use wire Item [8], leaving ~30.0 mm floating, and mark as FL2.Wind 7 turns in 1 layer, from right to left, at the last turn bring exit at the left slot, also leaving ~40.0 mm floating, and mark FL3.
Insulation	2 layers of tape Item [10].
WD5 Shield2	Start at pin 2, wind 15 tri-filar turns of wire Item [6], from left to right. At the last turn, cut short to leave as No-Connect.
Insulation	1 layer of tape Item [10].
WD6 2ND Primary	Use floating wire from winding 1st Primary, continue to wind 25 turns from left to right. At the last turn, bring the wire back to the left and finish at pin 12.
Insulation	1 layer of tape Item [10]. Bring floating wire FL3 to the right and continue securing with 2 layers.
Finish	Gap core halves to get 609 μH, secure with clips Item [3], and cut short GND tips. Solder pin 2 with bus-wire Item [9] and solder to top of either clip Item [3]. Varnish with Item [12]. Place 2 layers of tape Item [11] at the bottom then wrap up to the body of transformer, also place 1 layer surround and wrap on top to cover the cores. Tape around 1turn of tape Item [10]. Insert Teflon tubes Item [13] to secondary leads and twist. (*See pictures below).*

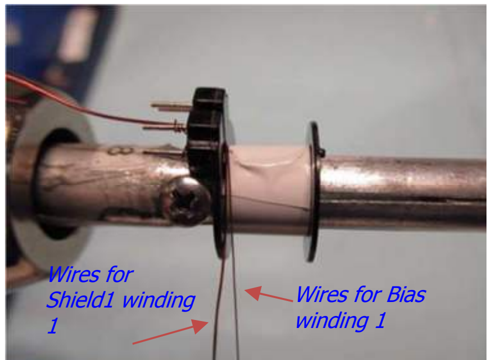
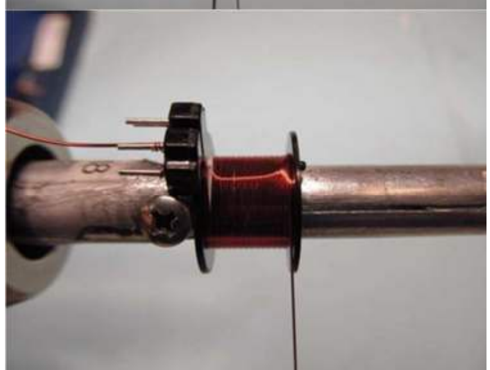
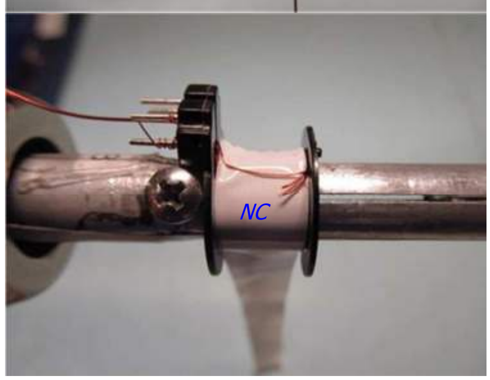
8.6 *Transformer Winding Step-By-Step Instructions*

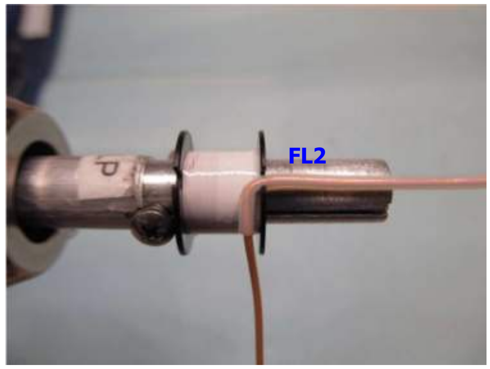
Bobbin and Winding Preparation	 	Remove pin 3 and 10 of bobbin Item [2], and place on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.

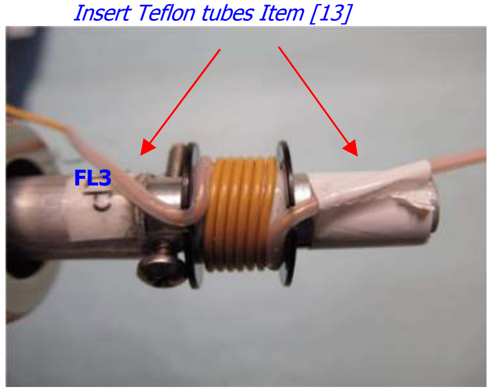
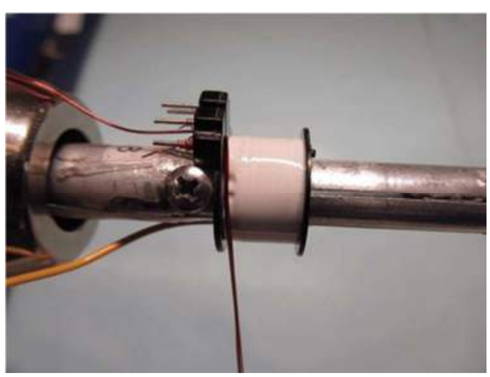
WD1 **1st Primary**	 	Start at pin 11, wind 25 turns of wire Item [4] in 1 layer, with tight tension, from left to right. At the last turn, bring the wire back to left, and leave enough length of wire-floating for 2nd Primary.

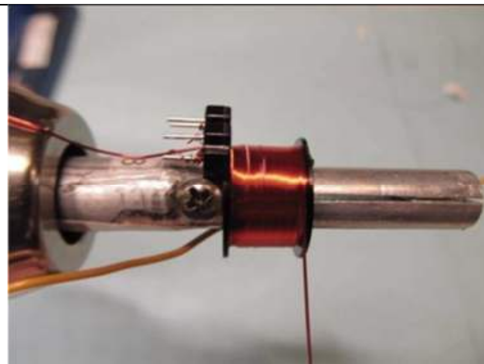
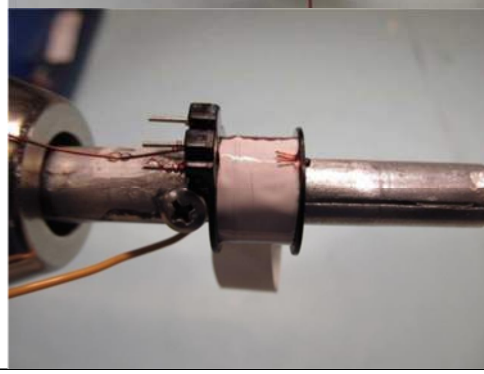
		

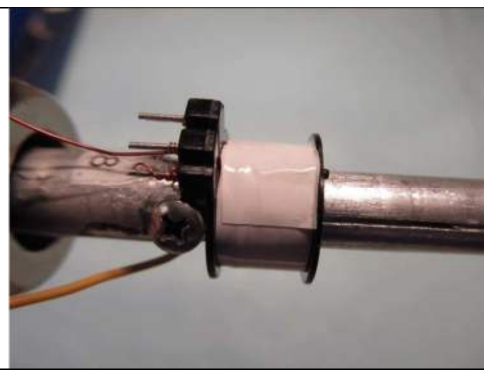
Insulation		1 layer of tape Item [10].

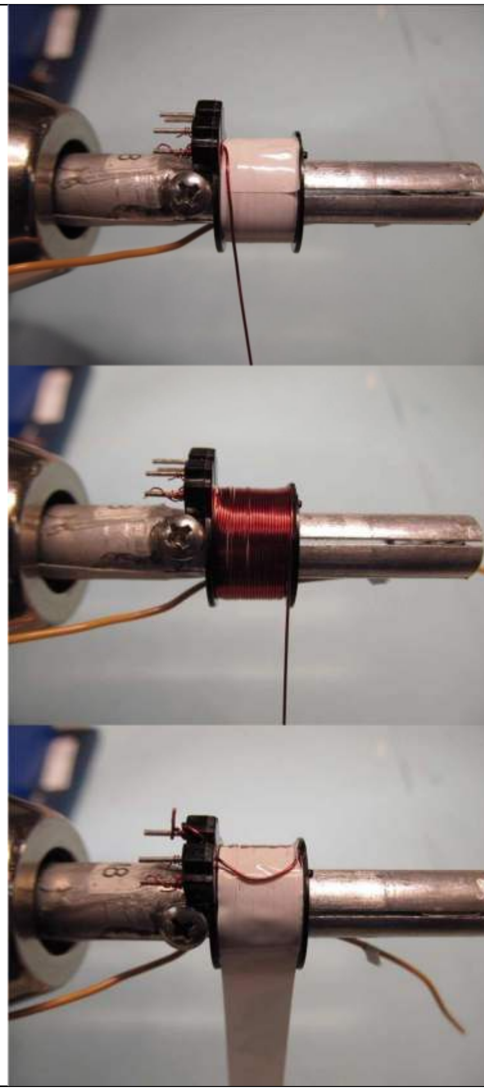
WD2: Bias & WD3: Shield #1	  	Start at pin 2, with 1 wire Item [4] for WD2 (Bias). Use single wire Item [7] start at pin 1 for Bias winding, also use 2 wires same Item [5] start at pin 2 for Shield1 winding. Wind all 3 wires in parallel, at the 14th turn: - bring single wire for Bias winding to the left and terminate at pin 2, - cut short 2 wires for Shield1 Winding as No-Connect.
Insulation		2 layers of tape Item [10].

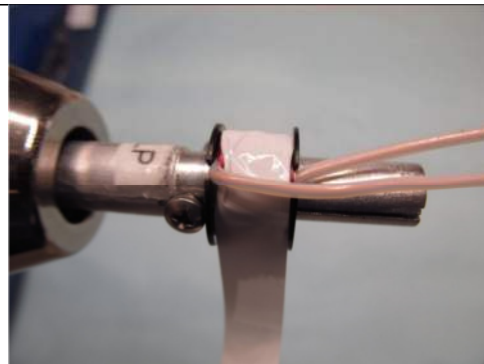
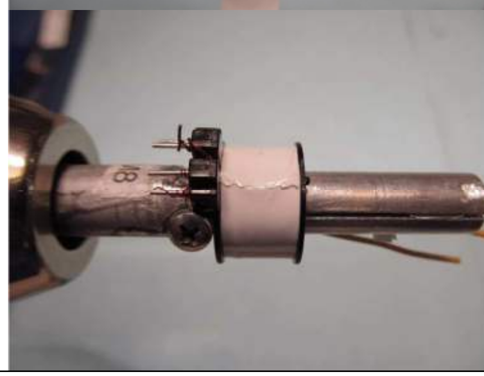
<table>
<tr><td>WD4:
Secondary</td><td>

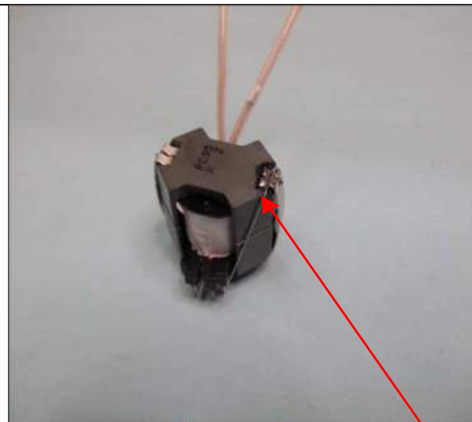
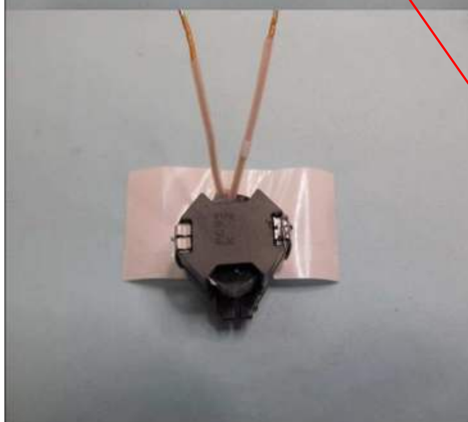
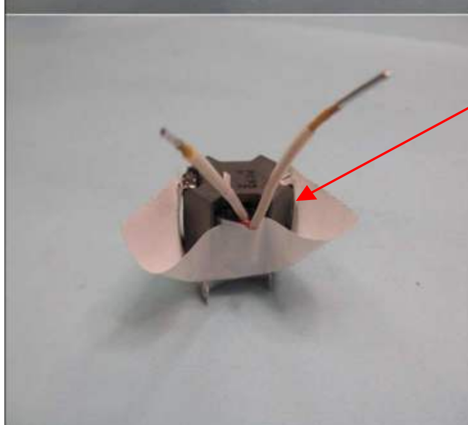
Insert Teflon tubes Item [13]

</td><td>Start at right slot of secondary side, use wire Item [8], leaving ~ 30 mm floating, insert Teflon tube item {13] also ~30 mm long reach inside to bobbin ~ 3mm and mark as FL2.Wind 7 turns in 1 layer, from right to left, at the last turn exit the wire at the left slot, leaving ~ 40.0mm floating and also insert Teflon tube same as FL2, and mark FL3.</td></tr>
<tr><td>Insulation</td><td></td><td>2 layers of tape Item [10].</td></tr>
<tr><td>WD5: Shield #2</td><td></td><td>Start at pin 2, wind 15 tri-filar turns of wire Item [6], from left to right. At the last turn, cut short to leave as No-Connect.</td></tr>
</table>

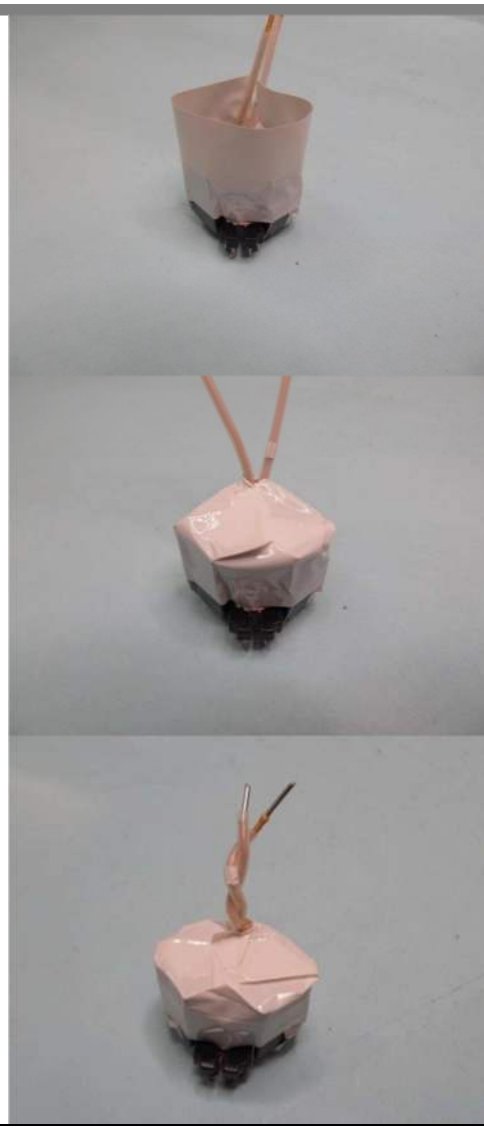
	 	

Insulation		1 layer of tape Item [10].

WD6: 2nd Primary		Use floating wire from winding 1st Primary, continue to wind 25 turns from left to right. At the last turn, bring the wire back to the left and finish at pin 12.

Insulation	 	1 layer of tape Item [10]. Bring floating wire FL3 to the right and continue securing with 2 layers.

Finish Assembly	   	Gap core halves to get 609 uH, secure with clips Item [3], and cut short GND tips. <u>Solder pin 2 with bus-wire Item [9] and solder to top of either clip Item [3].</u> Varnish with Item [12]. <u>Place 3 layers of tape Item [11] at</u> the bottom then wrap up to the body of transformer.
		Also place 1 layer surround and wrap on top to cover the cores. Tape around 1turn of tape Item [10]. (*See pictures beside).*

Completed Transformer		

9 Common Mode Choke Specifications

9.1 *8 mH Common Mode Choke (L1)*

9.2 *Electrical Diagram*

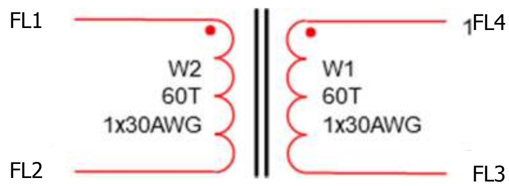


Figure 12 – Choke Electrical Diagram.

9.3 *Electrical Specifications*

Inductance	Across FL1 to FL2 (or FL3 to FL4) with the other winding open.	8 mH ±10%
Leakage Inductance	Across FL1 to FL2 (or FL3 to FL4) with the other winding shorted.	0.3 µH (Max.)
LCR Meter Setting	L_S measurement, 100 kHz switching frequency, 1.0 V test level.	

9.4 *Material List*

Item	Description
[1]	Toroidal Core: TDK , T10 X 6X X 4 T46, Mfg P/N: B64290L0038X046 PI#: 32-00376-00.
[2]	Magnet Wire: #30 AWG, Double Coated.
[3]	Cable Tie PI # 75-00202-00.
[4]	Heat Shrink: Heat Shrink 1” Inner diameter, 0.035” Wall Thickness. PI#: 62-00002-00; cut to 0.75” length.

9.5 *Winding Instructions*

	Prepare core Item [1], ~4ft of 2 wires Item [2]. Insert Cable Tie [3] in to core Item [1].
	Start as FL1 for Item [2] and wind 19 turns for 1^{st} layer. Continue winding another 13 turns in 2^{nd} layer and 8 turns in 3^{rd} layer and 8 turns in 4 layer, 7 turns in layer 5 and backward to start point for 5 turns and finish as FL2 for Item [2].
	Continue to wind the same the second half of core start as FL4 and finish as FL3.
	Add Item [4] to the common-mode choke.

10 Assembly Details

10.1 *C9 Y Capacitor Teflon Sleeving*

	Before soldering to the board, cut the length of the C9 capacitor wire to about 1.5 cm. Use #20 AWG AlphaWire TFT-200-20 or equivalent and add sleeves to the wire connections to prevent ESD arcing.

10.2 *C10 and C11 Output Capacitor Insulation*

	Before soldering output capacitors C10 and C11, use 8.43 mm width tape and place on top of both capacitors as shown on the left. Then, use 13.7 mm width tape and wrap the capacitors as shown.

11 Performance Data

Note:

1. Output voltage measured on the PCB unless otherwise specified.
2. Measurements taken at room temperature ambient (approximately 25 °C) unless otherwise specified.

11.1 *No-Load Input Power at 5V$_{OUT}$*

Note:

1. Unit tested without Type-C cable connected to output.
2. For each line voltage, soak time = 15 min and integration time = 15 min.

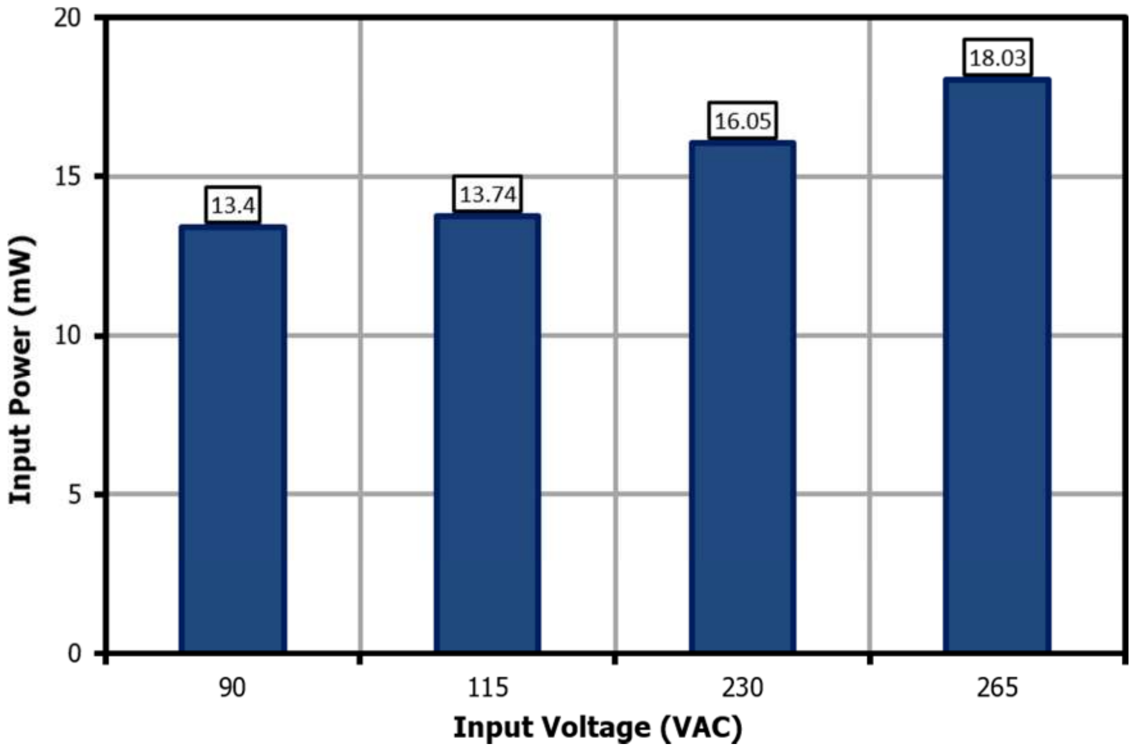


Figure 13 – No-Load Input Power vs. Input Line Voltage.

11.2 *Full Load Efficiency*

V_{OUT} (V)	Load (A)	Power (W)	Full Load Efficiency (%)			
			90 VAC	115 VAC	230 VAC	265 VAC
5	3.0	15	89.15	90.11	90.83	90.42
9	3.0	27	90.17	91.42	91.97	92.49
12	2.5	30	90.47	91.62	92.81	91.21
15	2.0	30	90.40	91.59	92.37	92.92
20	1.5	30	90.37	91.57	92.71	92.55

11.3 *Average and 10% LoadEfficiency*

11.3.1 Efficiency Requirements

		Test	Average	Average	10% Load
		Effective	2016	Jan-16	Jan-16
V_{OUT} (V)	Model (V)	Power (W)	New EISA2007	CoC v5 Tier 2	CoC v5 Tier 2
5	<6	15	81.39%	81.84%	72.48%
9	>6	27	86.62%	87.30%	77.30%
12	>6	30	86.95%	87.70%	77.70%
15	>6	30	86.95%	87.70%	77.70%
20	>6	30	86.95%	87.70%	77.70%

11.3.2 Efficiency Performance Summary (On Board)

V_{OUT} (V)	Power (W)	Average Efficiency (%)		10% Load Efficiency (%)	
		115 VAC	230 VAC	115 VAC	230 VAC
5	15	90.72	90.19	90.35	85.19
9	27	92.08	91.89	90.51	88.04
12	30	92.31	92.26	89.23	86.98
15	30	91.59	91.97	87.27	85.69
20	30	90.94	91.22	82.80	81.24

11.3.3 Average and 10% Load Efficiency Measurements

11.3.3.1 *Output: 5 V / 3 A*

Input (VAC)	Load (%)	POUT (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)	Remarks
115	100	15.54	90.11	90.72	81.39	81.84	PASS
	75	11.55	90.55				
	50	7.62	91.02				
	25	3.75	91.18				
	10	1.47	90.35			72.48	PASS
230	100	15.63	90.83	90.19	81.39	81.84	PASS
	75	11.58	90.57				
	50	7.62	90.27				
	25	3.75	89.10				
	10	1.48	85.19			72.48	PASS

11.3.3.2 *Output: 9 V / 3 A*

Input (VAC)	Load (%)	POUT (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)	Remarks
115	100	27.53	91.42	92.08	86.62	87.30	PASS
	75	20.54	91.64				
	50	13.60	91.96				
	25	6.74	93.32				
	10	2.65	90.51			77.30	PASS
230	100	27.67	91.97	91.89	86.62	87.30	PASS
	75	20.58	92.36				
	50	13.63	92.23				
	25	6.74	91.03				
	10	2.65	88.04			77.30	PASS

11.3.3.3 *Output: 12 V/ 2.5 A*

Input (VAC)	Load (%)	POUT (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)	Remarks
115	100	30.34	91.62	92.31	86.95	87.70	PASS
	75	22.70	91.88				
	50	15.07	92.16				
	25	7.47	93.58				
	10	2.92	89.23			77.70	PASS
230	100	30.42	92.81	92.26	86.95	87.70	PASS
	75	22.74	92.69				
	50	15.07	92.39				
	25	7.47	91.16				
	10	2.93	86.98			77.70	PASS

11.3.3.4 *Output: 15 V / 2 A*

Input (VAC)	Load (%)	POUT (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)	Remarks
115	100	30.19	91.59	91.59	86.95	87.70	PASS
	75	22.57	91.80				
	50	14.99	91.95				
	25	7.43	91.02				
	10	2.93	87.27			77.70	PASS
230	100	30.22	92.37	91.97	86.95	87.70	PASS
	75	22.60	92.61				
	50	15.01	92.29				
	25	7.43	90.60				
	10	2.93	85.69			77.70	PASS

11.3.3.5 *Output: 20 V / 1.5 A*

Input (VAC)	Load (%)	POUT (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)	Remarks
115	100	30.03	91.57	90.94	86.95	87.70	PASS
	75	22.44	91.54				
	50	14.90	91.49				
	25	7.37	89.15				
	10	2.89	82.80			77.70	PASS
230	100	30.06	92.71	91.22	86.95	87.70	PASS
	75	22.47	92.43				
	50	14.90	91.82				
	25	7.37	89.34				
	10	2.89	81.24			77.70	PASS

11.4 *Efficiency Across Line at 100% Load (On Board)*

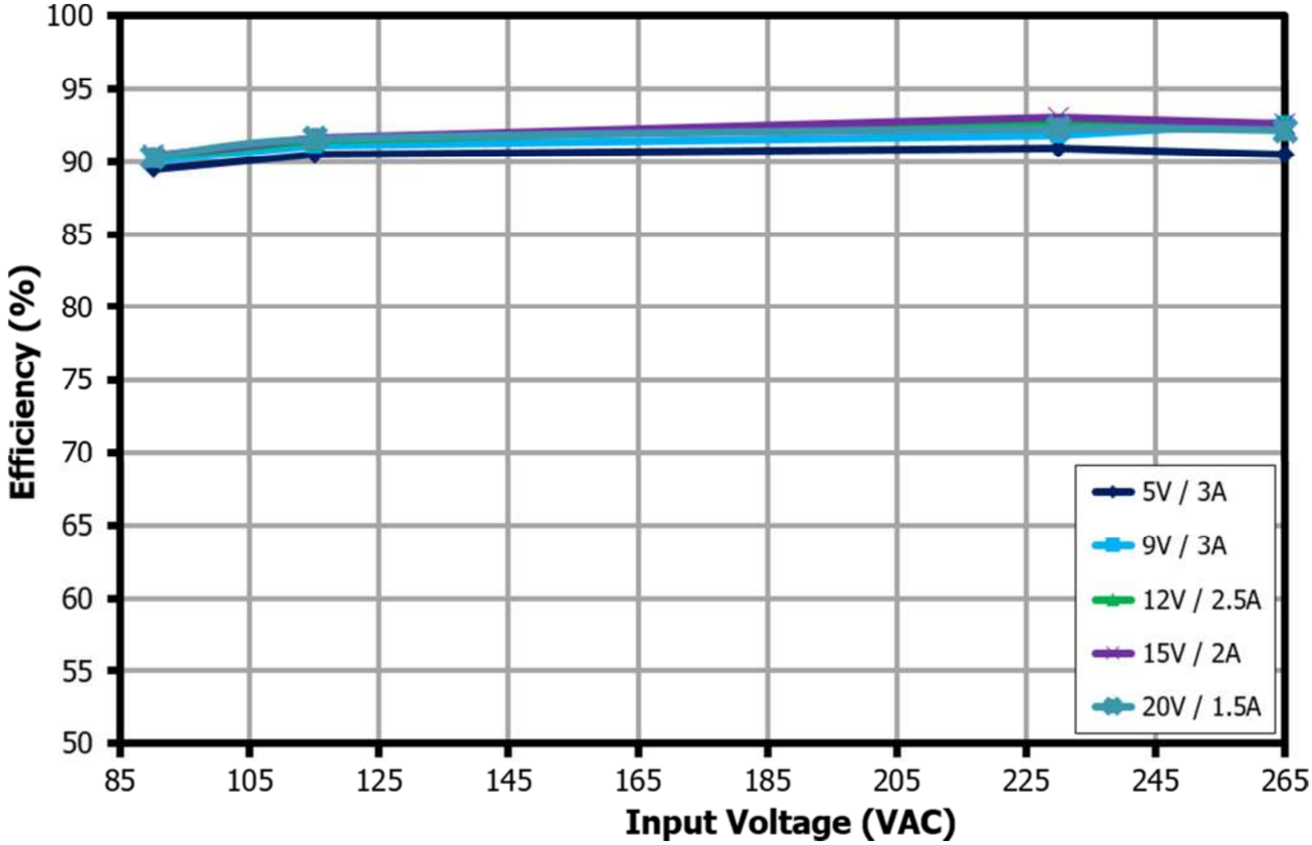


Figure 14 – Full Load Efficiency vs. Input Line for 5 V, 9 V, 12 V, 15 V, and 20 V Output, Room Temperature.

11.5 ***Efficiency Across Load (On Board)***

11.5.1 Output: 5 V / 3 A

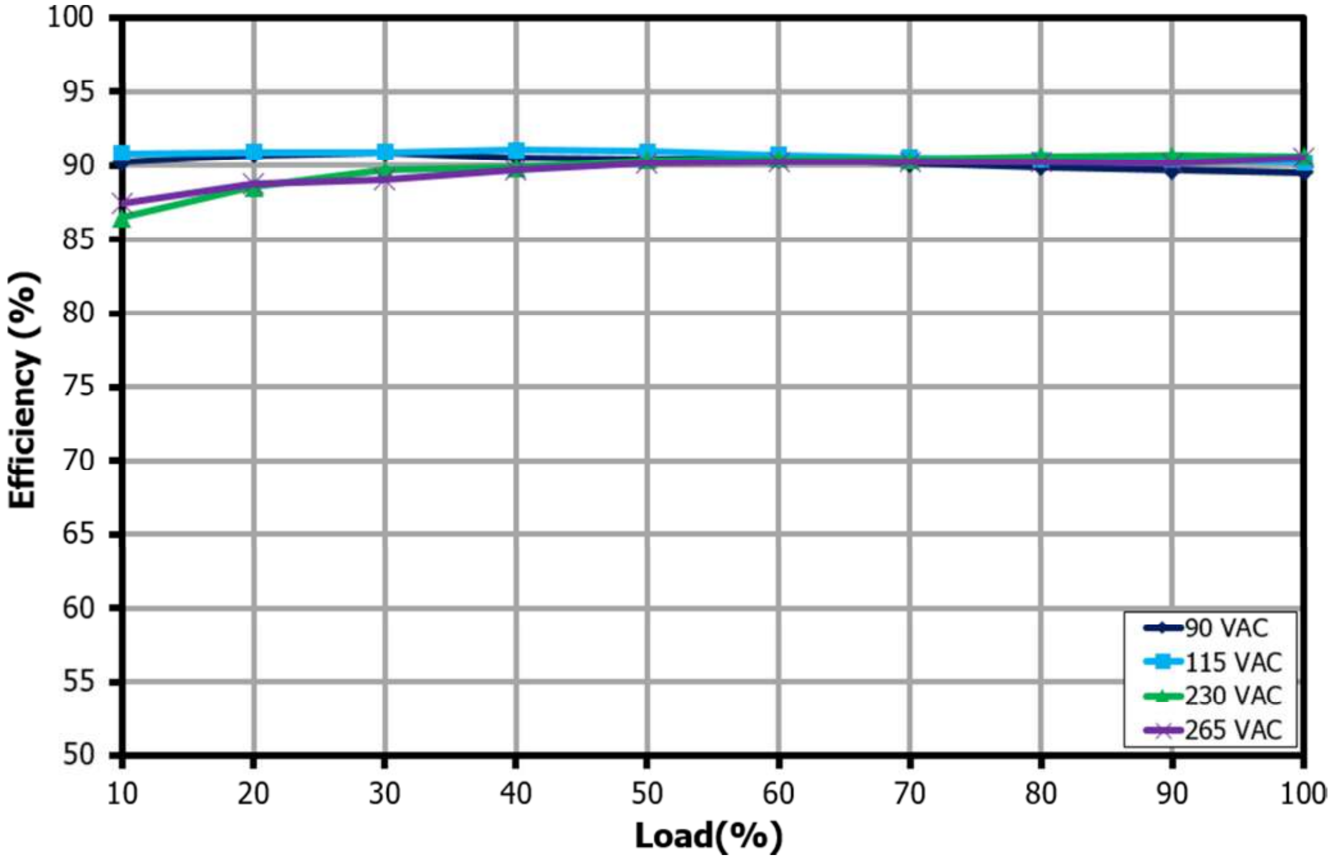


Figure 15 – Efficiency vs. Load for 5 V Output, Room Temperature.

11.5.2 Output: 9 V / 3 A

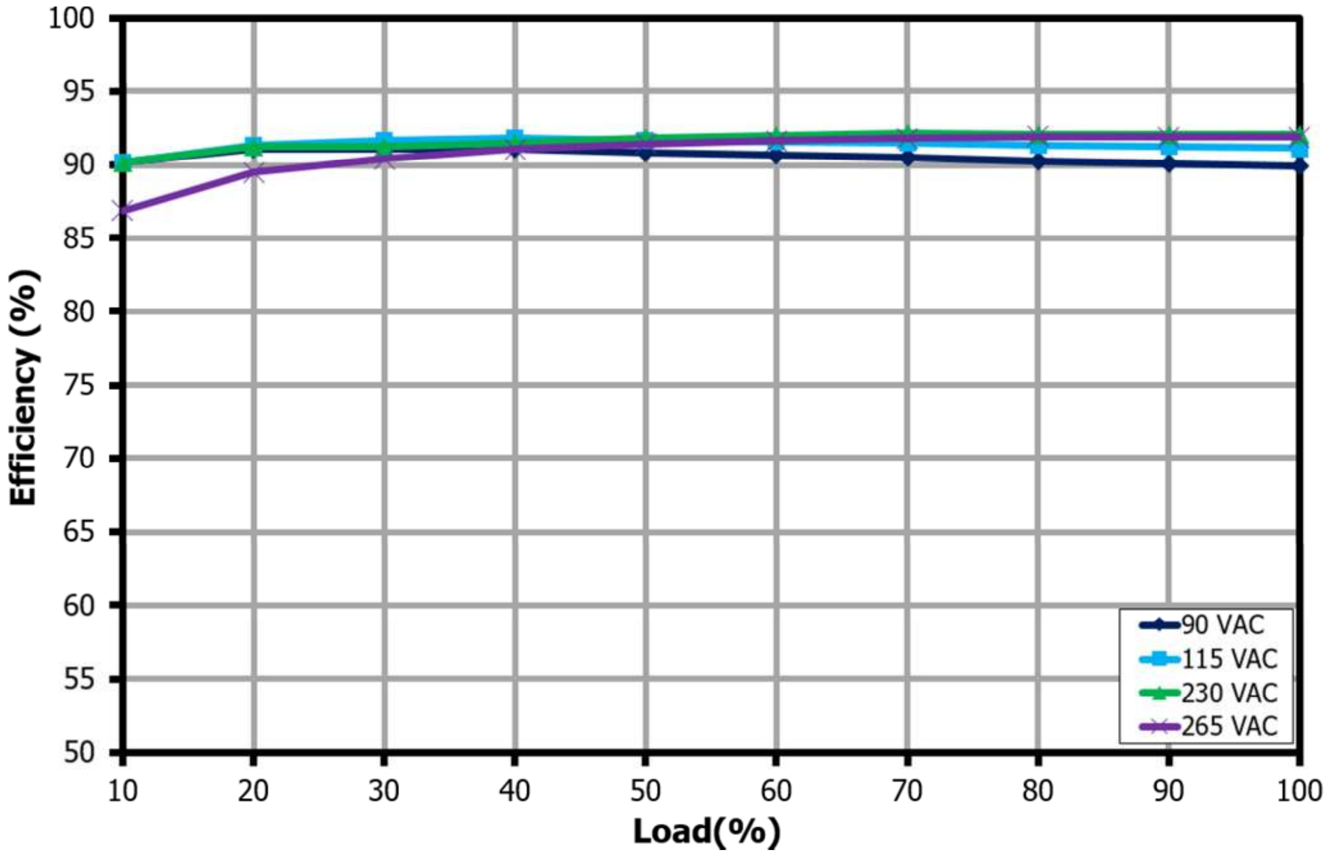


Figure 16 – Efficiency vs. Load for 9 V Output, Room Temperature.

11.5.3 Output: 12 V / 2.5 A

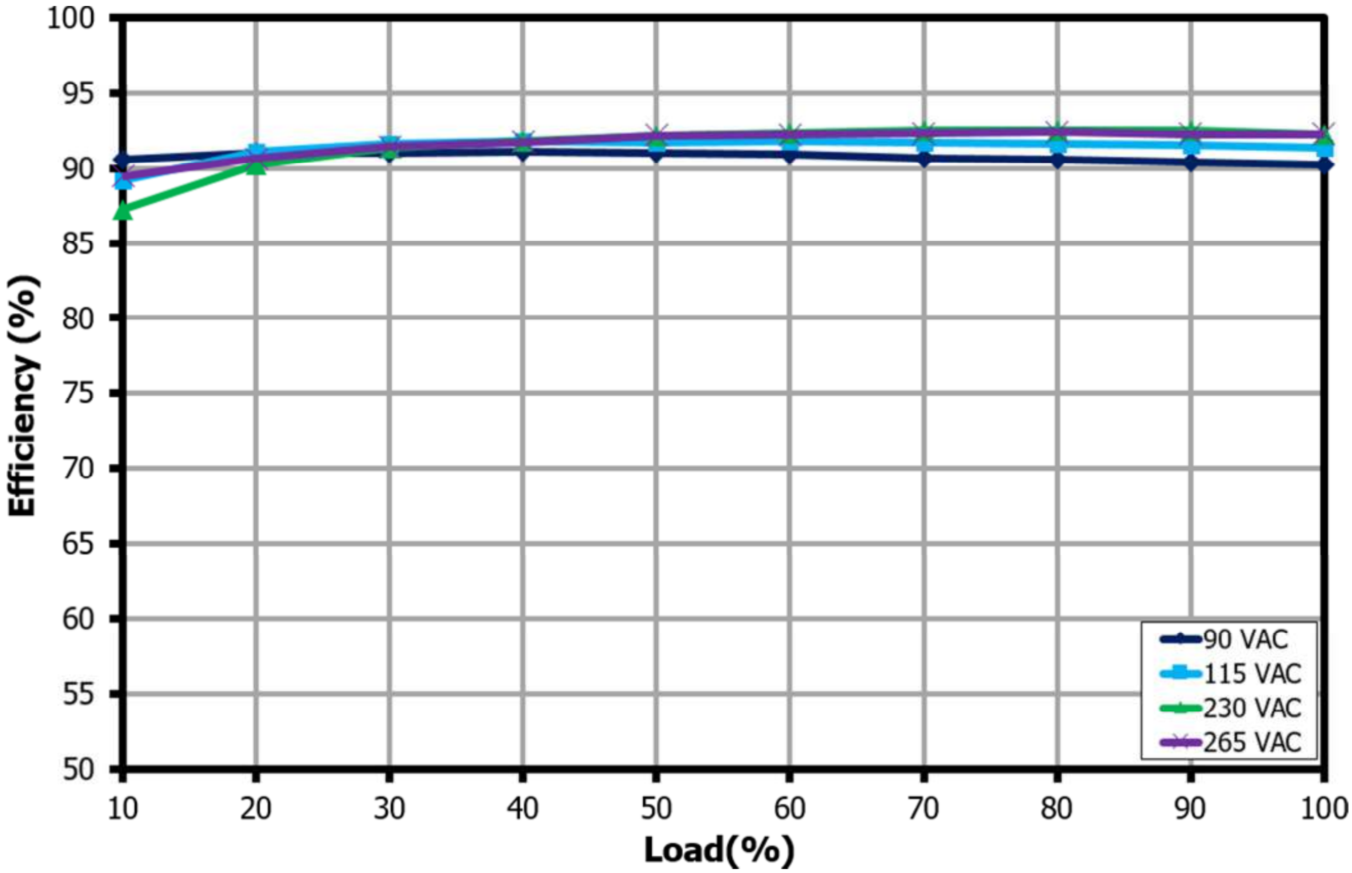


Figure 17 – Efficiency vs. Load for 12 V Output, Room Temperature.

11.5.4 Output: 15 V / 2 A

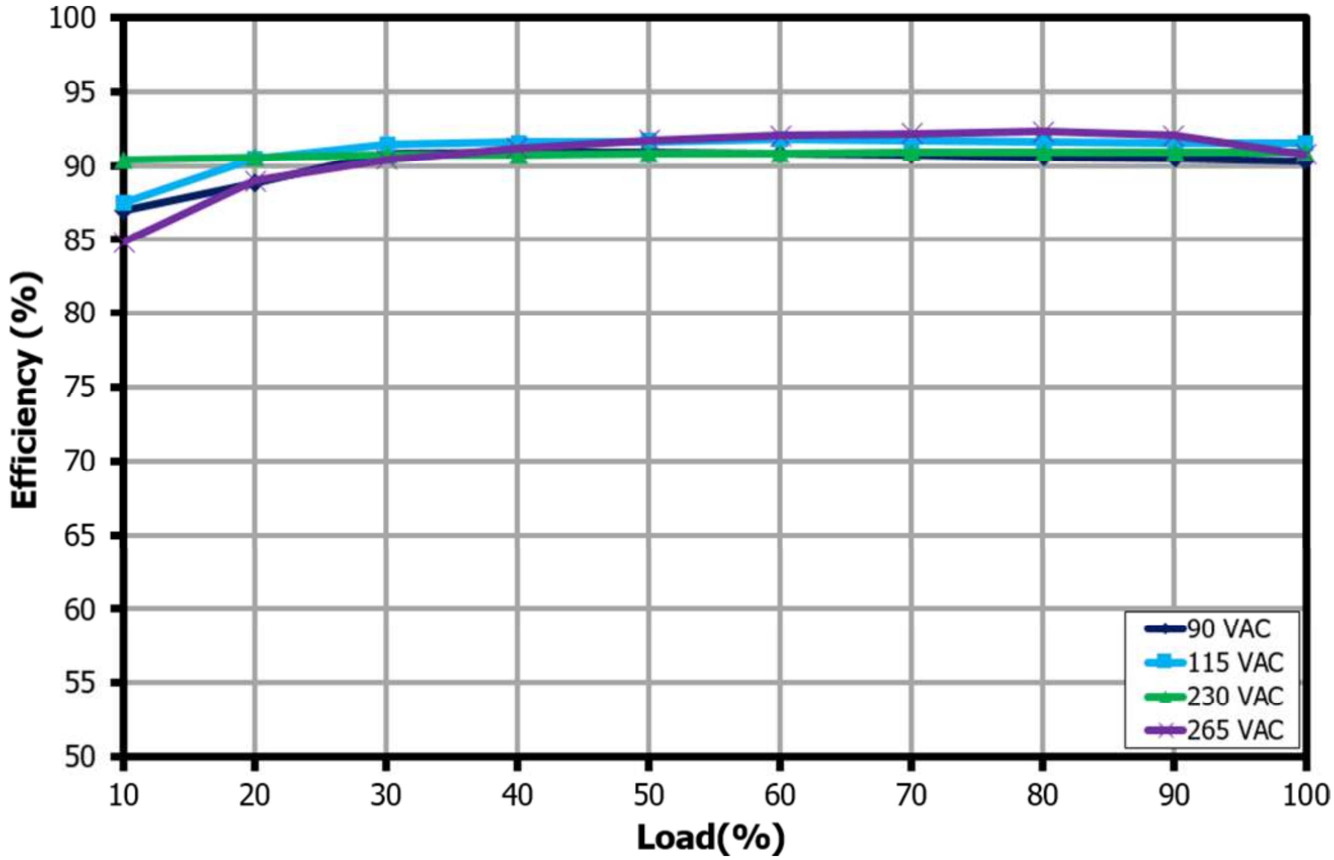


Figure 18 – Efficiency vs. Load for 15 V Output, Room Temperature.

11.5.5 Output: 20 V / 1.5 A

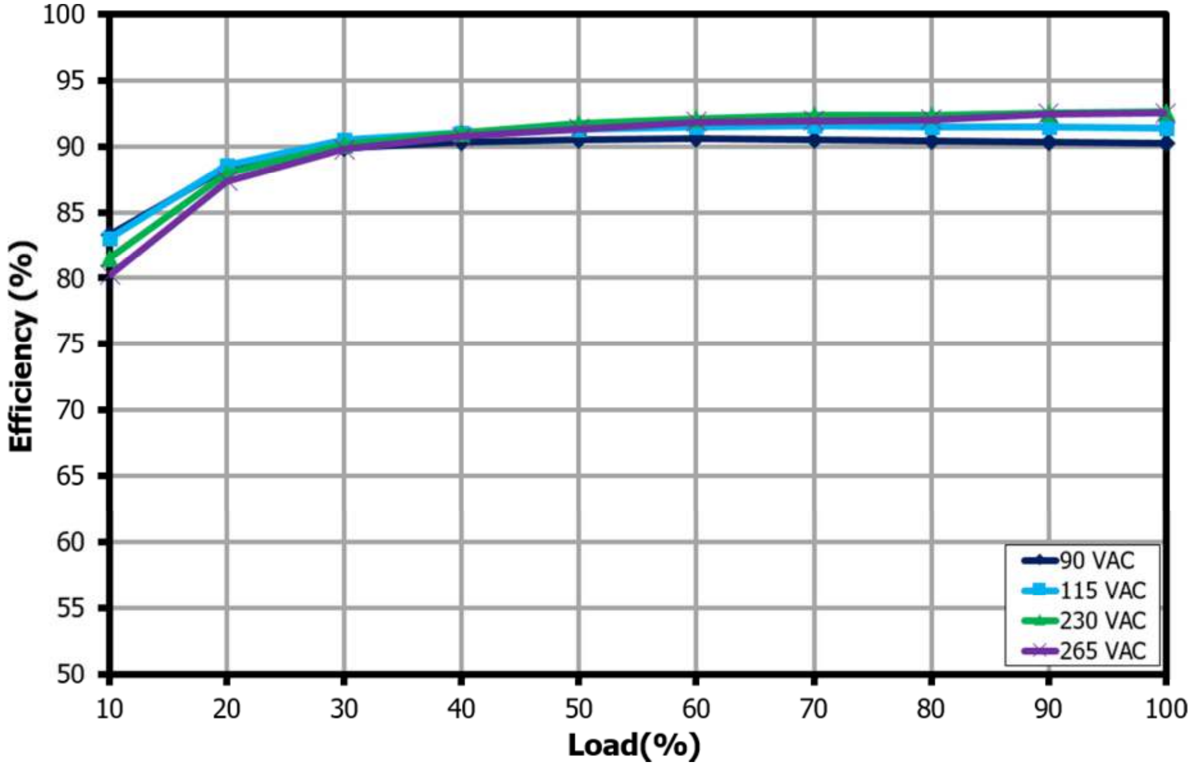


Figure 19 – Efficiency vs. Load for 20 V Output, Room Temperature.

11.6 *Load Regulation (End of Cable)*

11.6.1 Output: 5 V / 3 A

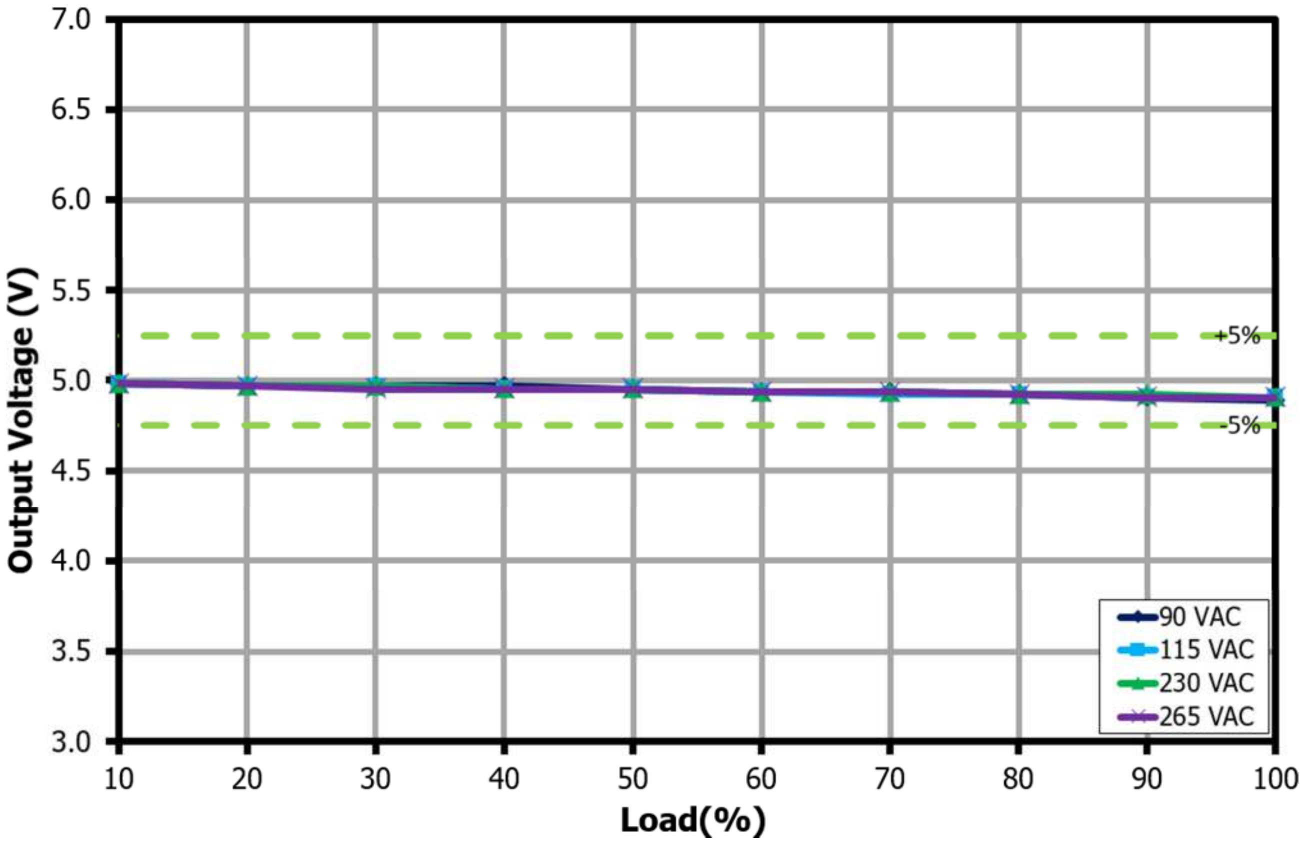


Figure 20 – Output Voltage vs. Output Load for 5 V Output, Room Temperature.

11.6.2 Output: 9 V / 3 A

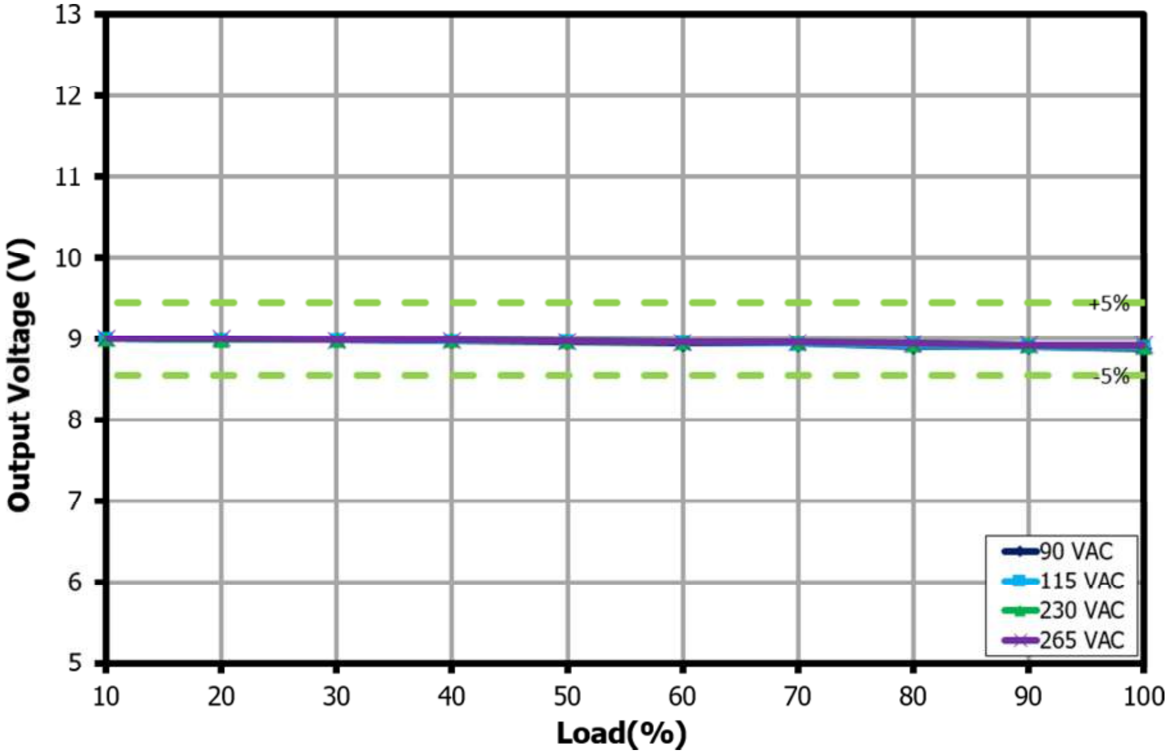


Figure 21 – Output Voltage vs. Output Load for 9 V Output, Room Temperature.

11.6.3 Output: 12 V / 2.5 A

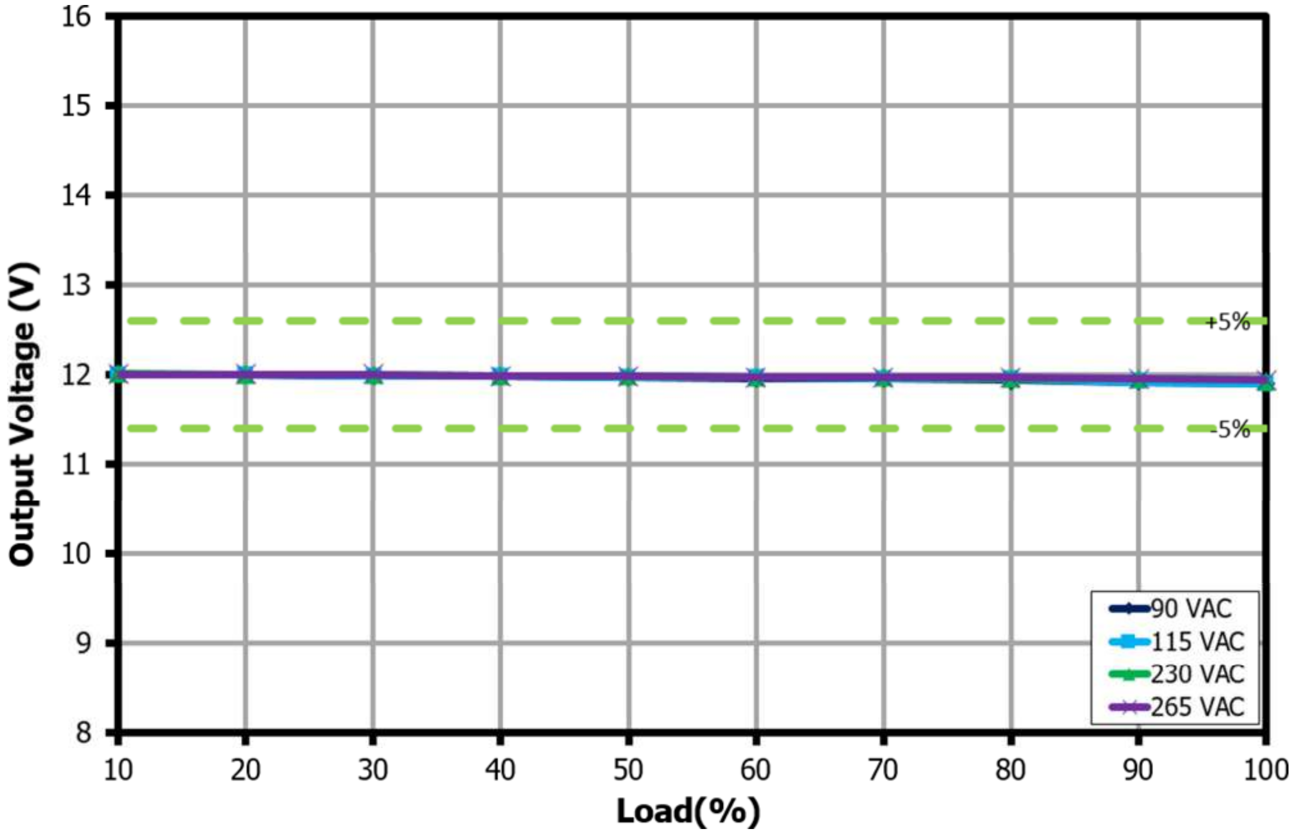


Figure 22 – Output Voltage vs. Output Load for 12 V Output, Room Temperature.

11.6.4 Output: 15 V / 2 A

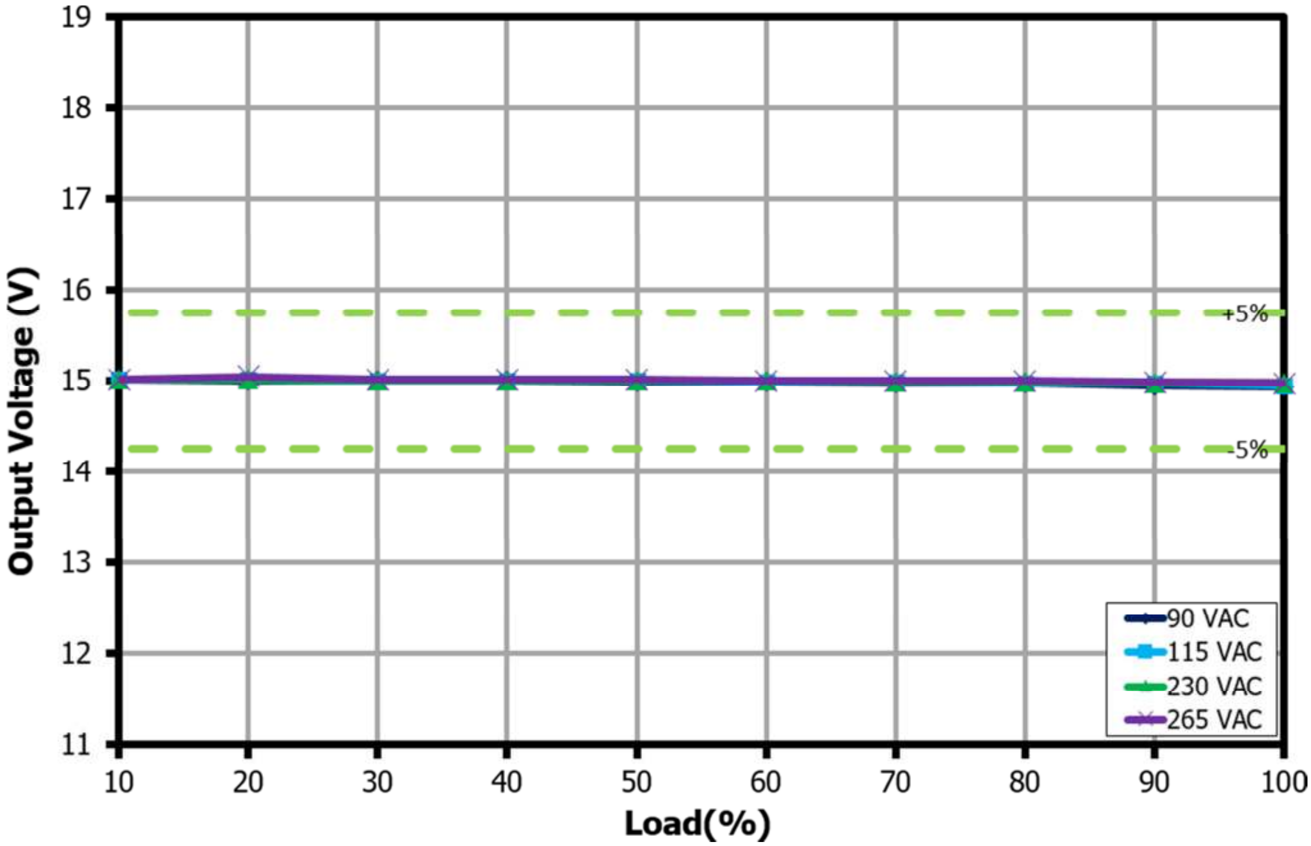


Figure 23 – Output Voltage vs. Output Load for 15 V Output, Room Temperature.

11.6.5 Output: 20 V / 1.5 A

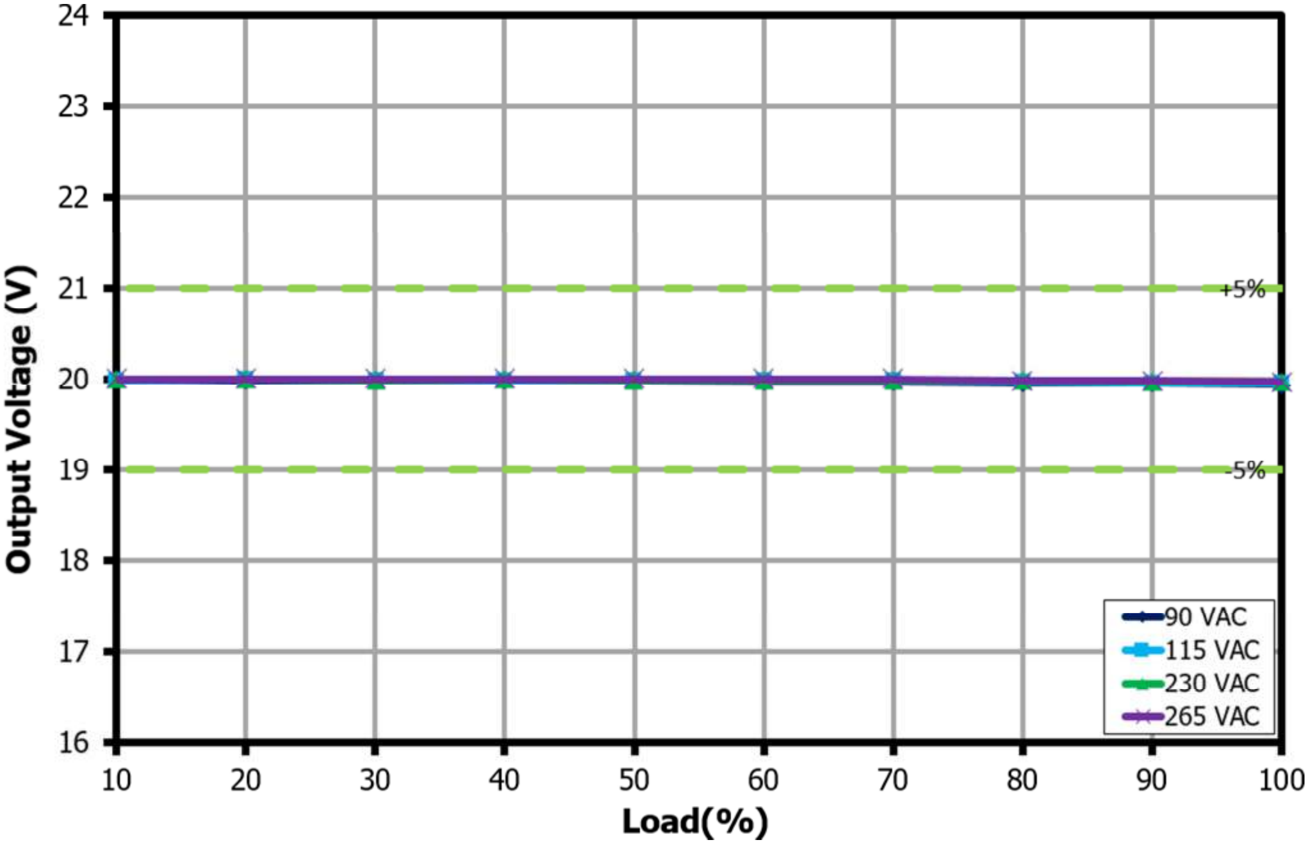


Figure 24 – Output Voltage vs. Output Load for 20 V Output, Room Temperature.

11.7 ***Line Regulation (End of Cable)***

11.7.1 Output: 5 V / 3 A

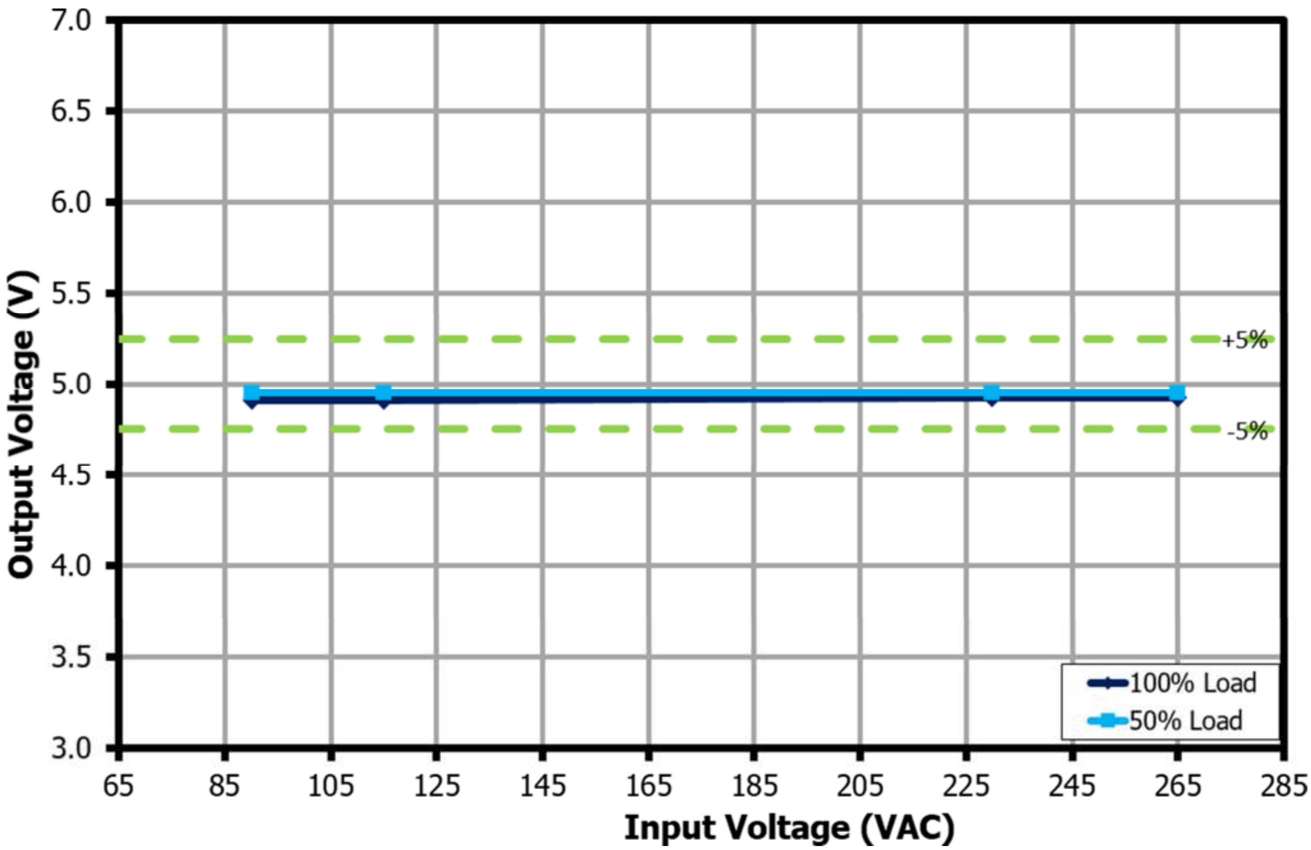


Figure 25 – Output Voltage vs. Input Line Voltage for 5 V Output, Room Temperature.

11.7.2 Output: 9 V / 3 A

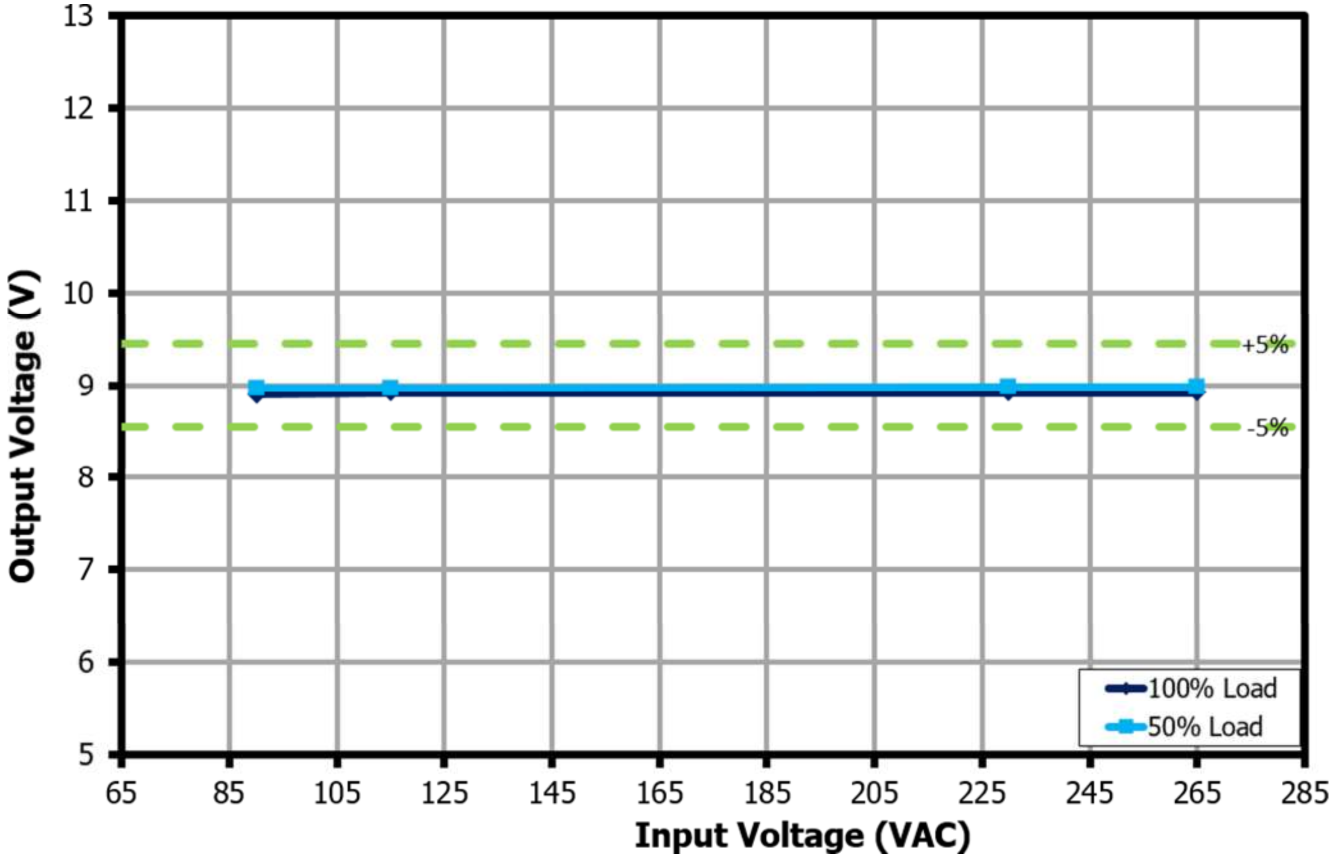


Figure 26 – Output Voltage vs. Input Line Voltage for 9 V Output, Room Temperature.

11.7.3 Output: 12 V / 2.5 A

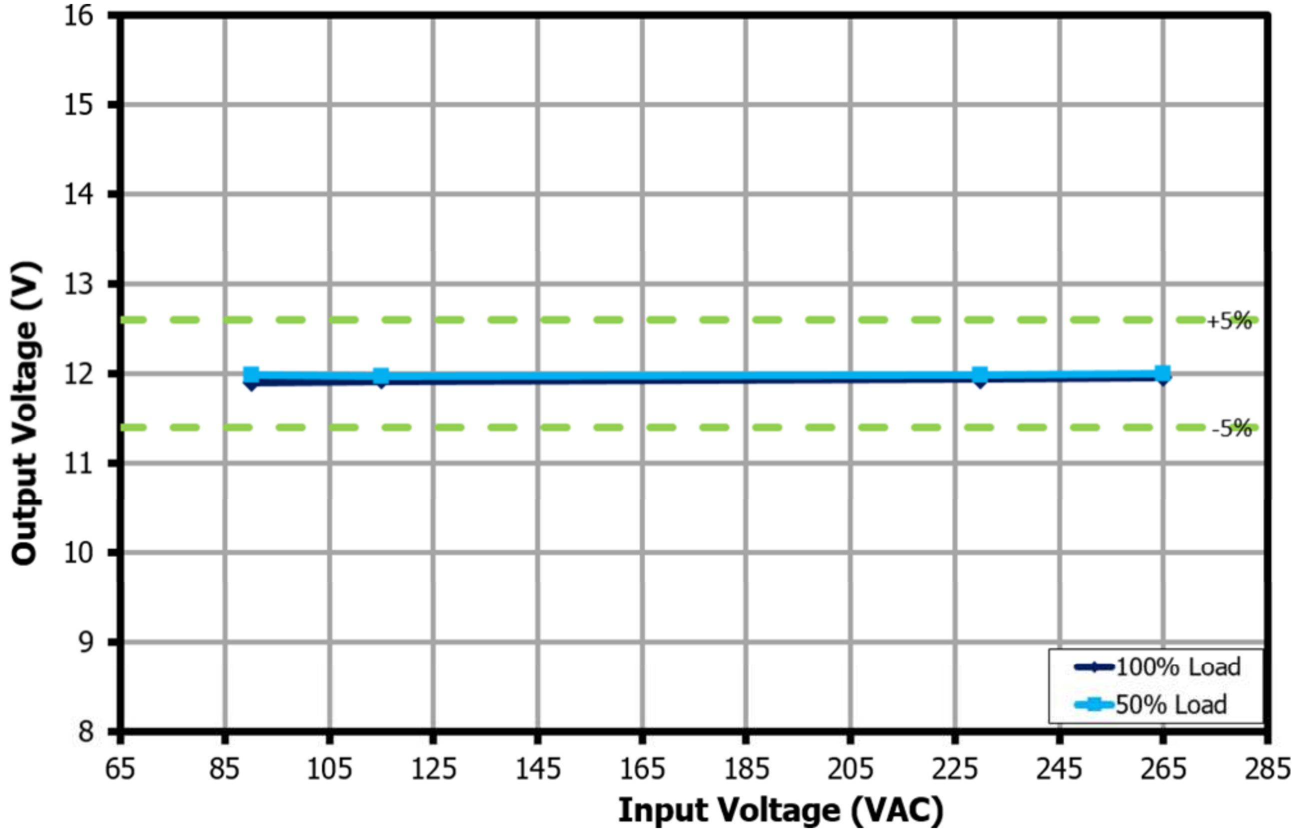


Figure 27 – Output Voltage vs. Input Line Voltage for 12 V Output, Room Temperature.

11.7.4 Output: 15 V / 2 A

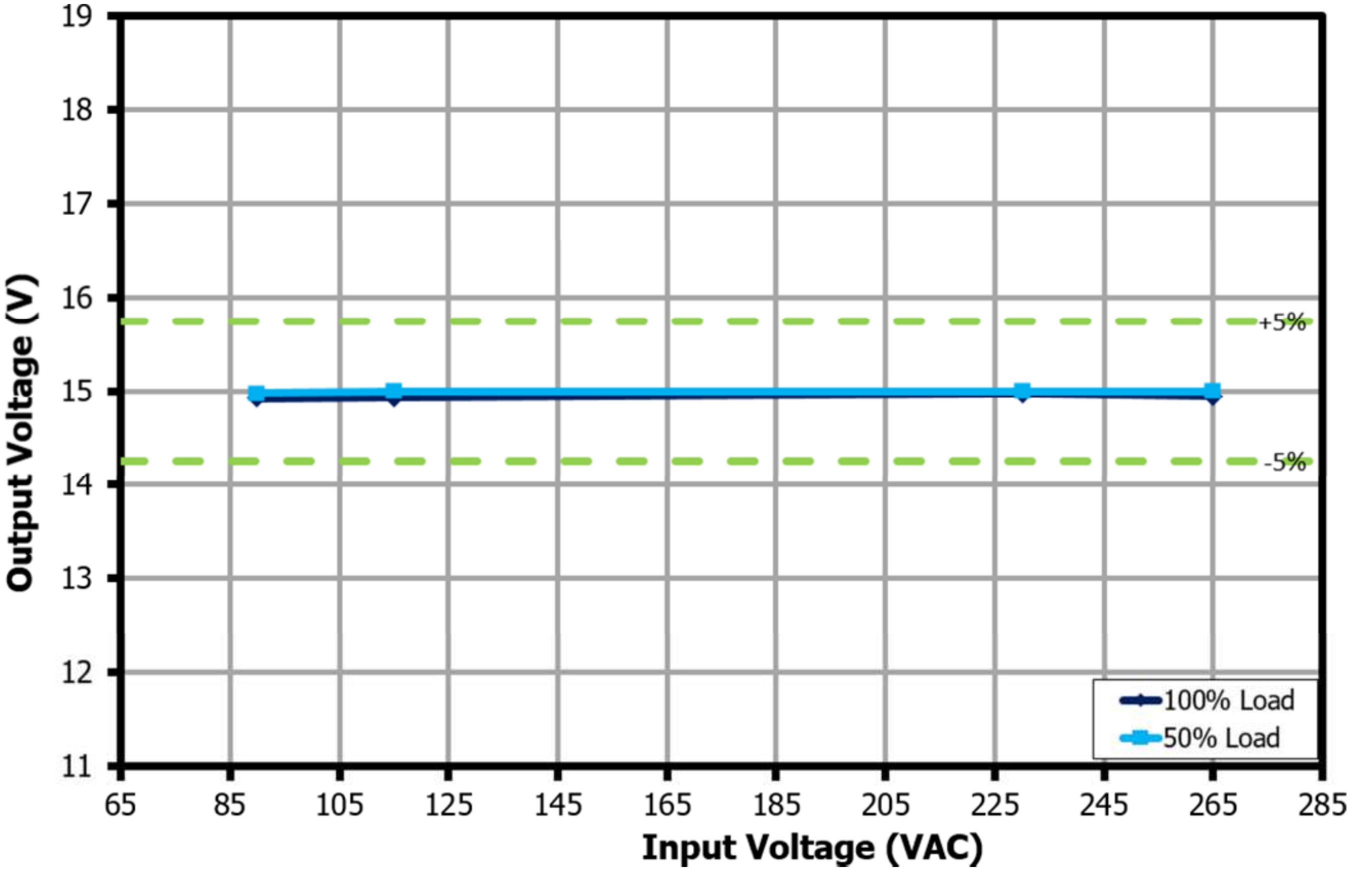


Figure 28 – Output Voltage vs. Input Line Voltage for 15 V Output, Room Temperature.

11.7.5 Output: 20 V / 1.5 A

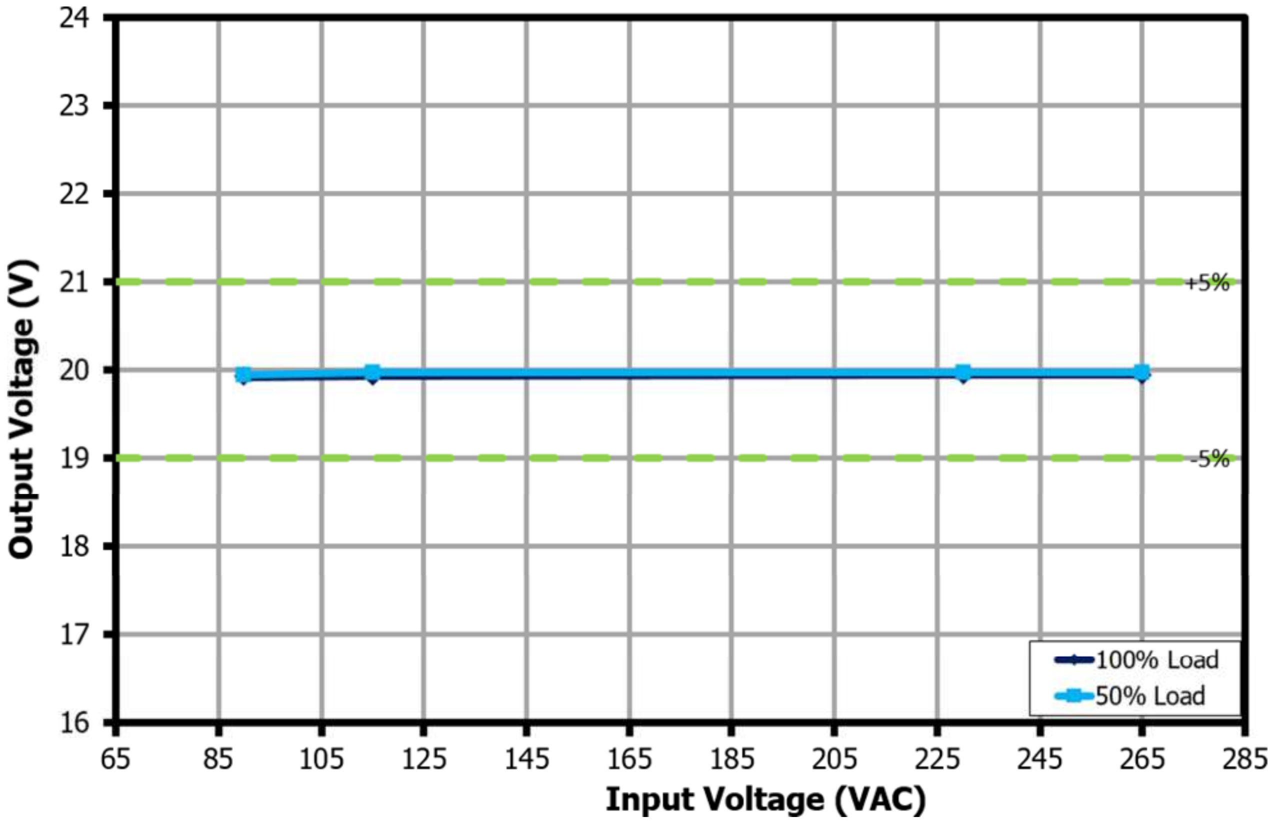


Figure 29 – Output Voltage vs. Input Line Voltage for 20 V Output, Room Temperature.

12 Thermal Performance

12.1 *Thermal Performance in Open Case, 25 ºC Ambient*

Note: Measurements taken at room temperature ambient.

12.1.1 Output: 5 V / 3 A (90 VAC)

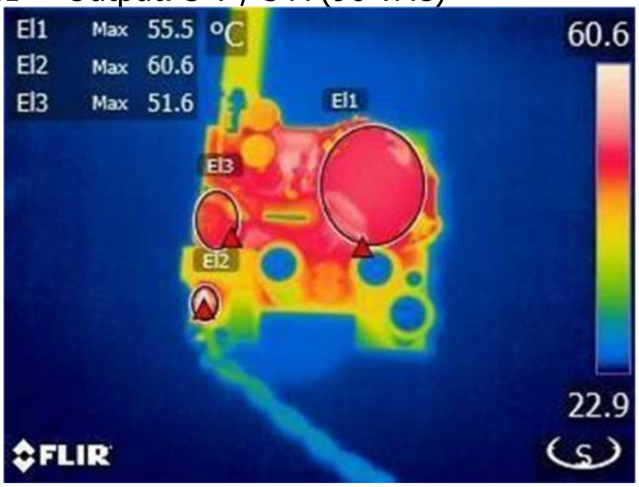


Figure 30 – Top Thermal Image, T_{AMB} = 23.1 ºC.
El1: Transformer, T1 = 55.5 ºC.
El2: Thermistor, RT1 = 60.6 ºC.
El3: CMC, L1 = 51.6 ºC.

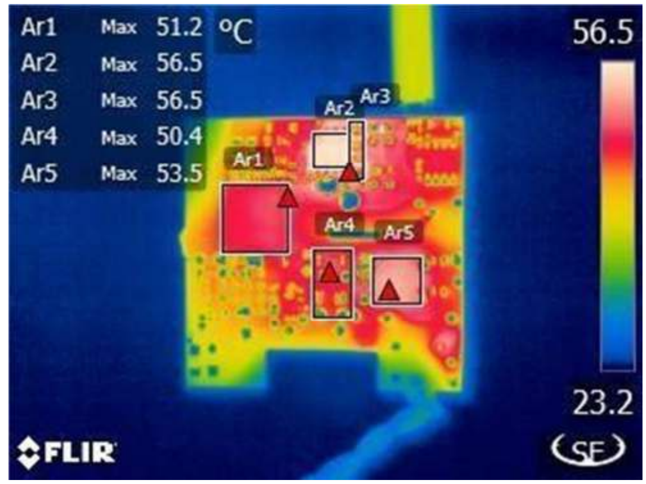


Figure 31 – Bottom Thermal Image, T_{AMB} = 23.1 ºC.
Ar1: InnoSwitch3-PD, U1 = 51.2 ºC.
Ar2: SR FET, Q2 = 56.5 ºC.
Ar3: SR FET Snubber = 56.5 ºC.
Ar4: Primary Snubber = 50.4 ºC.
Ar5: Bridge Rectifier, BR1 = 53.5 ºC.

12.1.2 Output: 5 V / 3 A (265 VAC)

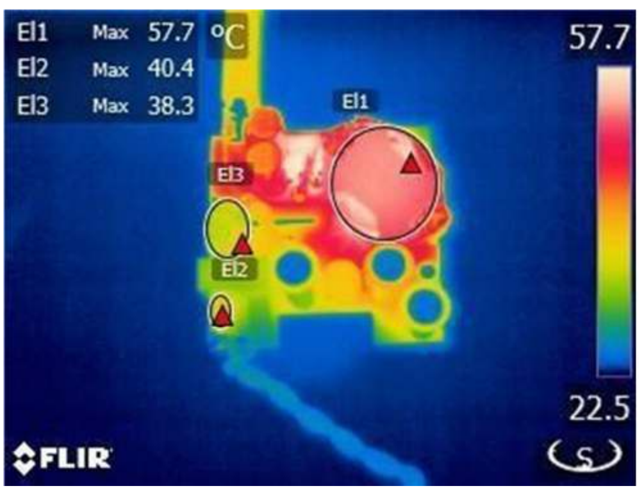


Figure 32 – Top Thermal Image, T_{AMB} = 22.7 ºC.
El1: Transformer, T1 = 57.7 ºC.
El2: Thermistor, RT1 = 40.4 ºC.
El3: CMC, L1 = 38.3 ºC.

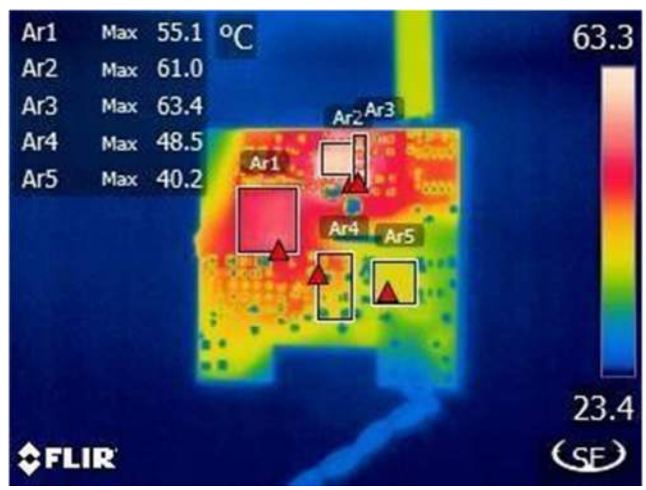


Figure 33 – Bottom Thermal Image, T_{AMB} = 22.7 ºC.
Ar1: InnoSwitch3-PD, U1 = 55.1 ºC.
Ar2: SR FET, Q2 = 61.0 ºC.
Ar3: SR FET Snubber = 63.4 ºC.
Ar4: Primary Snubber = 48.5 ºC.
Ar5: Bridge Rectifier, BR1 = 40.2 ºC.

12.1.3 Output: 9 V / 3 A (90 VAC)

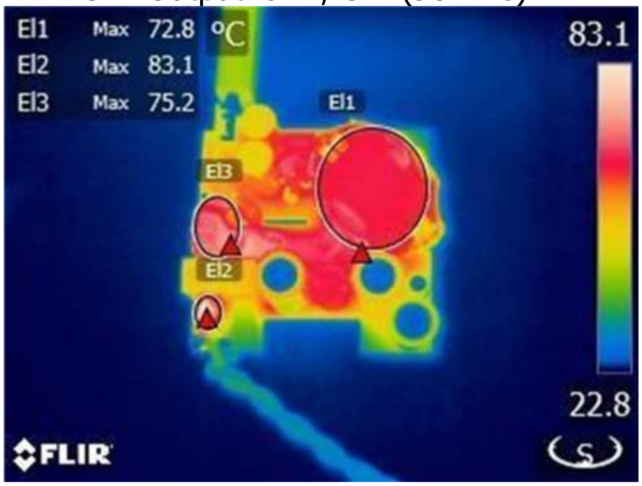


Figure 34 – Top Thermal Image, T_{AMB} = 23.3 °C.
El1: Transformer, T1 = 72.8 °C.
El2: Thermistor, RT1 = 83.1 °C.
El3: CMC, L1 = 75.2 °C.

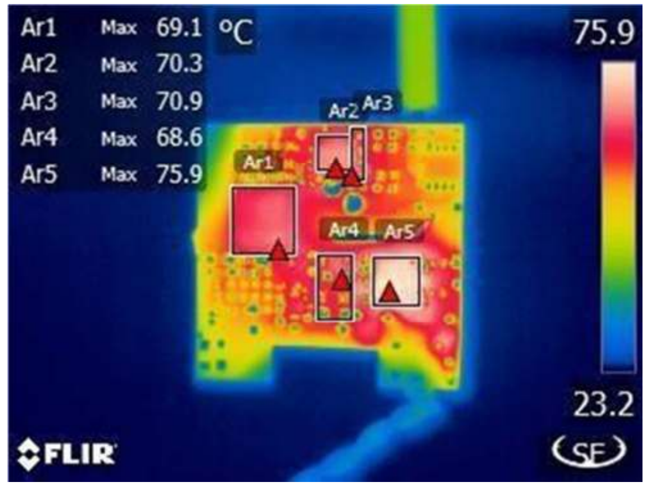


Figure 35 – Bottom Thermal Image, T_{AMB} = 23.1 °C.
Ar1: InnoSwitch3-PD, U1 = 69.1 °C.
Ar2: SR FET, Q2 = 70.3 °C.
Ar3: SR FET Snubber = 70.9 °C.
Ar4: Primary Snubber = 68.6 °C.
Ar5: Bridge Rectifier, BR1 = 75.9 °C.

12.1.4 Output: 9 V / 3 A (265 VAC)

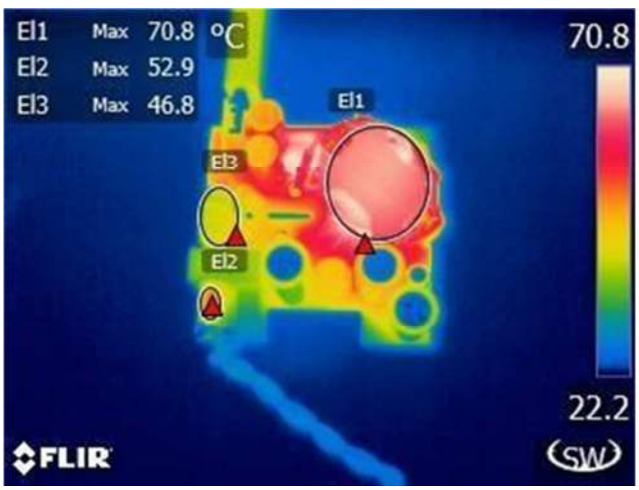


Figure 36 – Top Thermal Image, T_{AMB} = 22.6 °C.
El1: Transformer, T1 = 70.8 °C.
El2: Thermistor, RT1 = 52.9 °C.
El3: CMC, L1 = 46.8 °C.

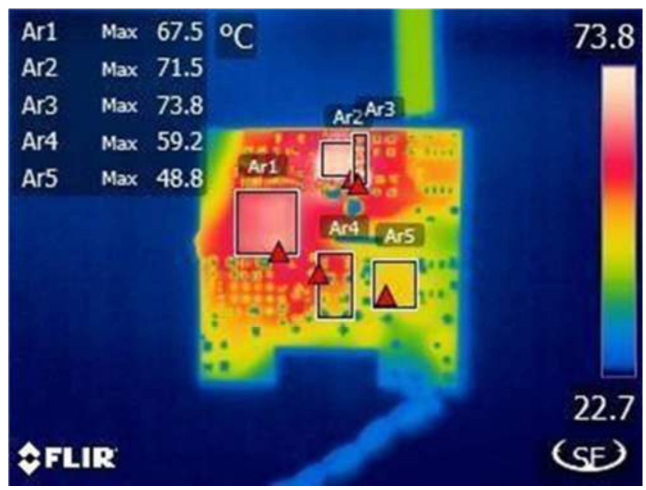


Figure 37 – Bottom Thermal Image, T_{AMB} = 22.6 °C.
Ar1: InnoSwitch3-PD, U1 = 67.5 °C.
Ar2: SR FET, Q2 = 71.5 °C.
Ar3: SR FET Snubber = 73.8 °C. Ar4: Primary Snubber = 59.2 °C. Ar5: Bridge Rectifier, BR1 = 48.8 °C.

12.1.5 Output: 12 V / 2.5 A (90 VAC)

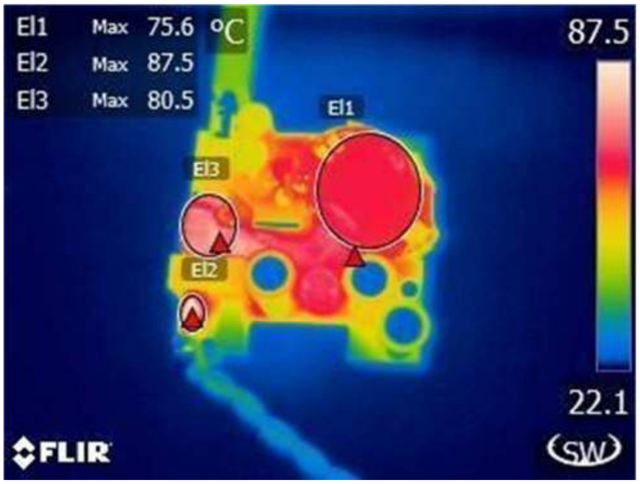


Figure 38 – Top Thermal Image, T_{AMB} = 22.8 ºC.
El1: Transformer, T1 = 75.6 ºC.
El2: Thermistor, RT1 = 87.5 ºC.
El3: CMC, L1 = 80.5 ºC.

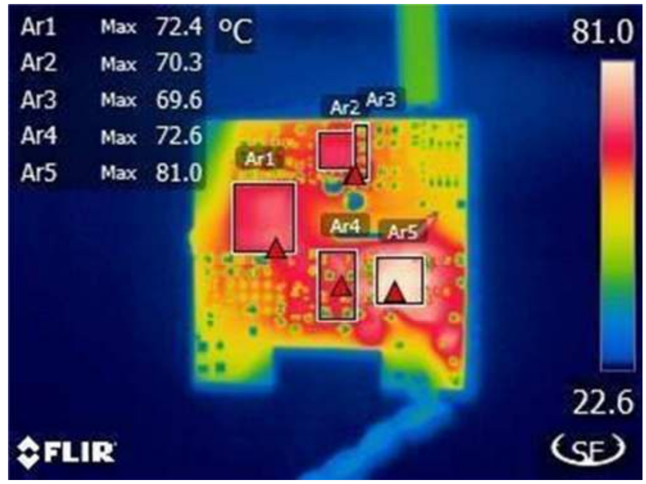


Figure 39 – Bottom Thermal Image, T_{AMB} = 22.8 ºC.
Ar1: InnoSwitch3-PD, U1 = 72.4 ºC.
Ar2: SR FET, Q2 = 70.3 ºC.
Ar3: SR FET Snubber = 69.6 ºC.
Ar4: Primary Snubber = 72.6 ºC.
Ar5: Bridge Rectifier, BR1 = 81.0 ºC.

12.1.6 Output: 12 V / 2.5 A (265 VAC)

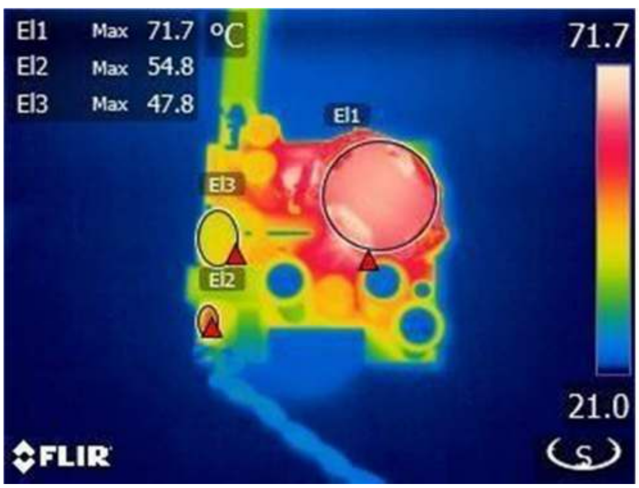


Figure 40 – Top Thermal Image, T_{AMB} = 21.4 ºC.
El1: Transformer, T1 = 71.7 ºC.
El2: Thermistor, RT1 = 54.8 ºC.
El3: CMC, L1 = 47.8 ºC.

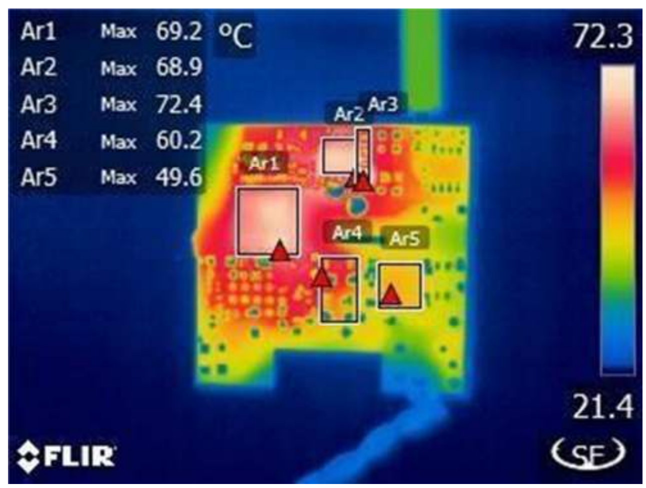


Figure 41 – Bottom Thermal Image, T_{AMB} = 21.4 ºC.
Ar1: InnoSwitch3-PD, U1 = 69.2 ºC.
Ar2: SR FET, Q2 = 68.9 ºC.
Ar3: SR FET Snubber = 72.4 ºC.
Ar4: Primary Snubber = 60.2 ºC.
Ar5: Bridge Rectifier, BR1 = 49.6 ºC.

12.1.7 Output: 15 V / 2 A (90 VAC)

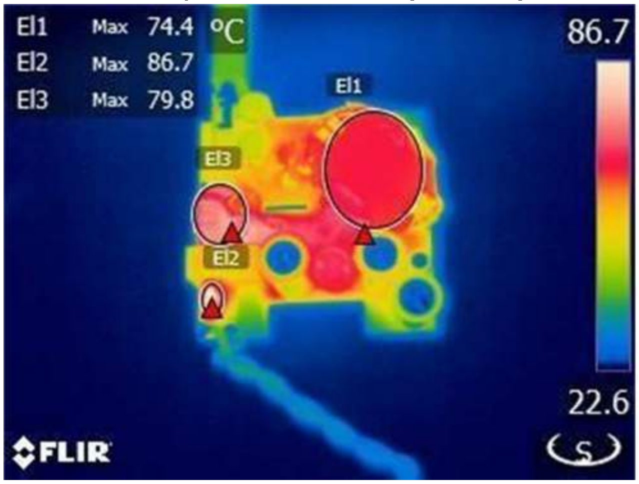


Figure 42 – Top Thermal Image, T_{AMB} = 23.0 ºC.
El1: Transformer, T1 = 74.4 ºC.
El2: Thermistor, RT1 = 86.7 ºC.
El3: CMC, L1 = 79.8 ºC.

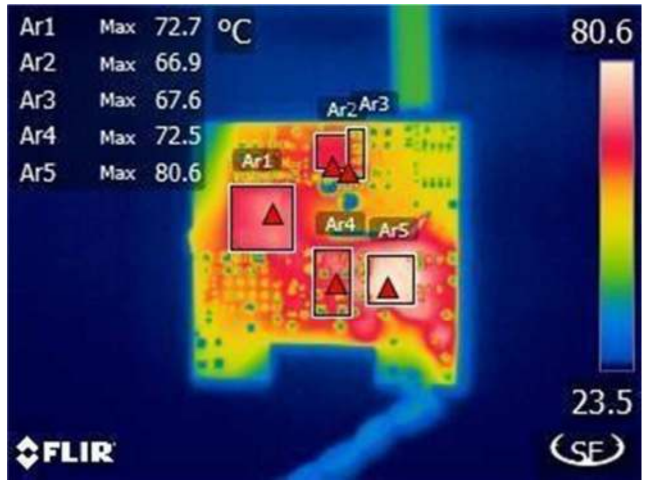


Figure 43 – Bottom Thermal Image, T_{AMB} = 23.0 ºC.
Ar1: InnoSwitch3-PD, U1 = 72.7 ºC.
Ar2: SR FET, Q2 = 66.9 ºC.
Ar3: SR FET Snubber = 67.6 ºC.
Ar4: Primary Snubber = 72.5 ºC.
Ar5: Bridge Rectifier, BR1 = 80.6 ºC.

12.1.7 Output: 15 V / 2 A (265 VAC)

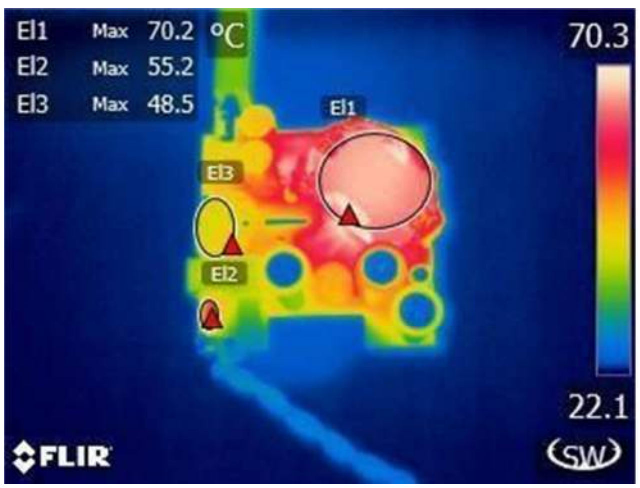


Figure 44 – Top Thermal Image, T_{AMB} = 22.8 ºC.
El1: Transformer, T1 = 70.2 ºC.
El2: Thermistor, RT1 = 55.2 ºC.
El3: CMC, L1 = 48.5 ºC.

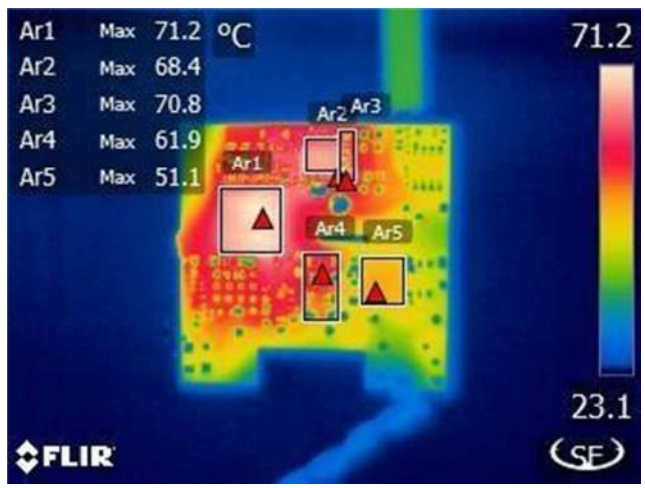


Figure 45 – Bottom Thermal Image, T_{AMB} = 22.8 ºC.
Ar1: InnoSwitch3-PD, U1 = 71.2 ºC.
Ar2: SR FET, Q2 = 68.4 ºC.
Ar3: SR FET Snubber = 70.8 ºC.
Ar4: Primary Snubber = 61.9 ºC.
Ar5: Bridge Rectifier, BR1 = 51.1 ºC.

12.1.8 Output: 20 V / 1.5 A (90 VAC)

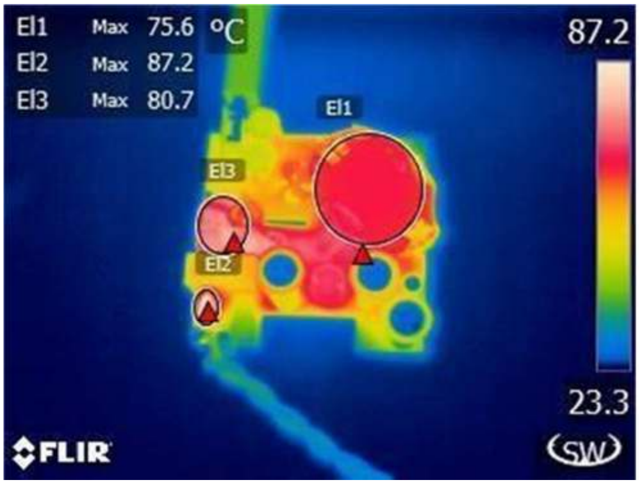


Figure 46 – Top Thermal Image, T_{AMB} = 23.7 ºC.
El1: Transformer, T1 = 75.6 ºC.
El2: Thermistor, RT1 = 87.2 ºC.
El3: CMC, L1 = 80.7 ºC.

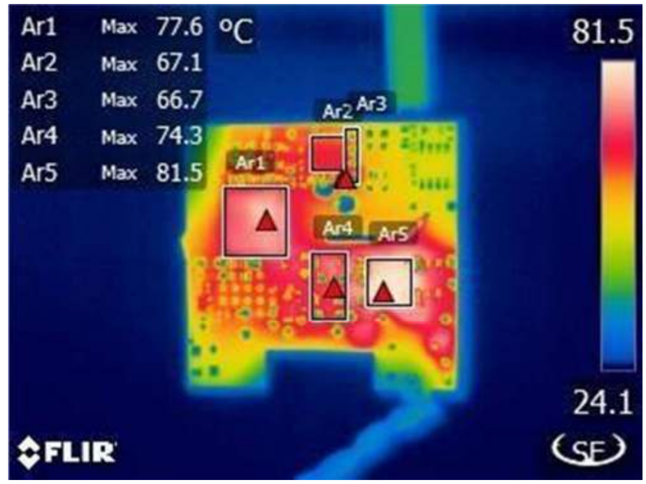


Figure 47 – Bottom Thermal Image, T_{AMB} = 23.7 ºC.
Ar1: InnoSwitch3-PD, U1 = 77.6 ºC.
Ar2: SR FET, Q2 = 67.1 ºC.
Ar3: SR FET Snubber = 66.7 ºC.
Ar4: Primary Snubber = 74.3 ºC.
Ar5: Bridge Rectifier, BR1 = 81.5 ºC.

12.1.9 Output: 20 V / 1.5 A (265 VAC)

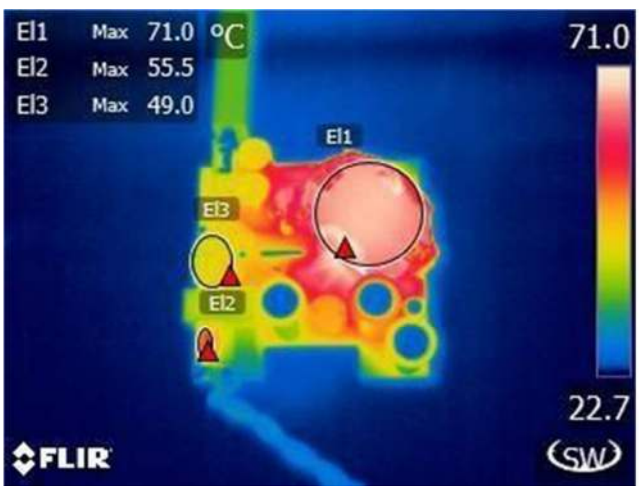


Figure 48 – Top Thermal Image, T_{AMB} = 23.3 ºC.
El1: Transformer, T1 = 71.0 ºC.
El2: Thermistor, RT1 = 55.5 ºC.
El3: CMC, L1 = 49.0 ºC.

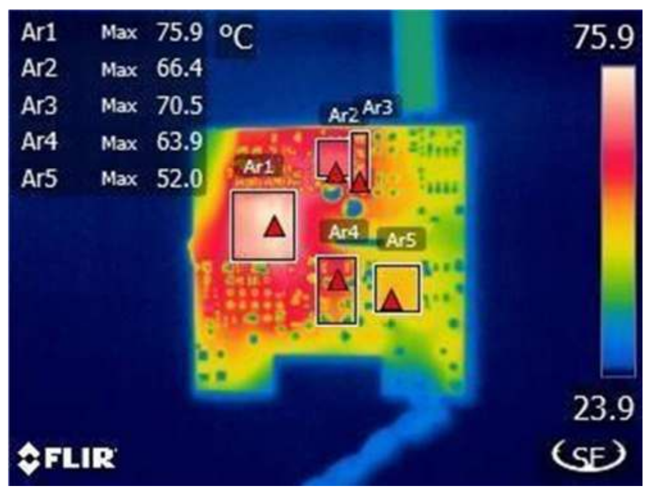


Figure 49 – Bottom Thermal Image, T_{AMB} = 23.3 ºC.
Ar1: InnoSwitch3-PD, U1 = 75.9 ºC.
Ar2: SR FET, Q2 = 66.4 ºC.
Ar3: SR FET Snubber = 70.5 ºC.
Ar4: Primary Snubber = 63.9 ºC.
Ar5: Bridge Rectifier, BR1 = 52.0 ºC.

12.1.10 Output: 16 V / 2.0 A (90 VAC)

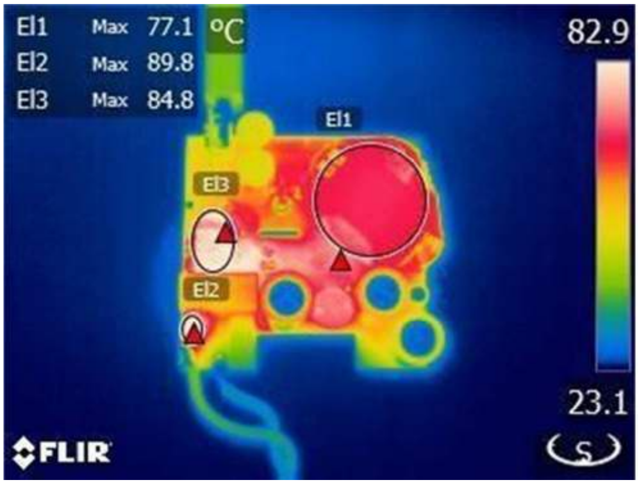


Figure 50 – Top Thermal Image, T_{AMB} = 23.5 ºC.
El1: Transformer, T1 = 77.1 ºC.
El2: Thermistor, RT1 = 89.8 ºC.
El3: CMC, L1 = 84.8 ºC.

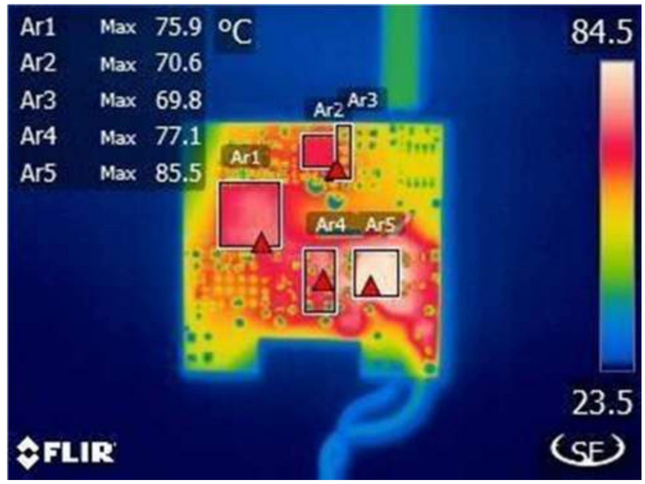


Figure 51 – Bottom Thermal Image, T_{AMB} = 23.5 ºC.
Ar1: InnoSwitch3-PD, U1 = 75.9 ºC.
Ar2: SR FET, Q2 = 70.6 ºC.
Ar3: SR FET Snubber = 69.78 ºC.
Ar4: Primary Snubber = 77.1 ºC.
Ar5: Bridge Rectifier, BR1 = 85.5 ºC.

12.1.11 Output: 16 V / 2.0 A (265 VAC)

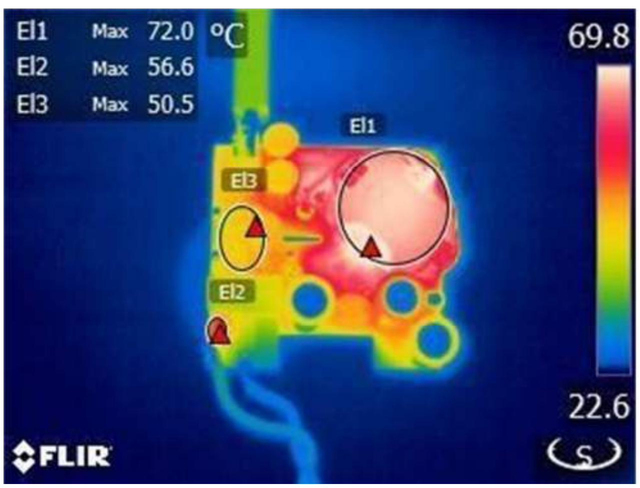


Figure 52 – Top Thermal Image, T_{AMB} = 23.5 ºC.
El1: Transformer, T1 = 72.0 ºC.
El2: Thermistor, RT1 = 56.6 ºC.
El3: CMC, L1 = 50.5 ºC.

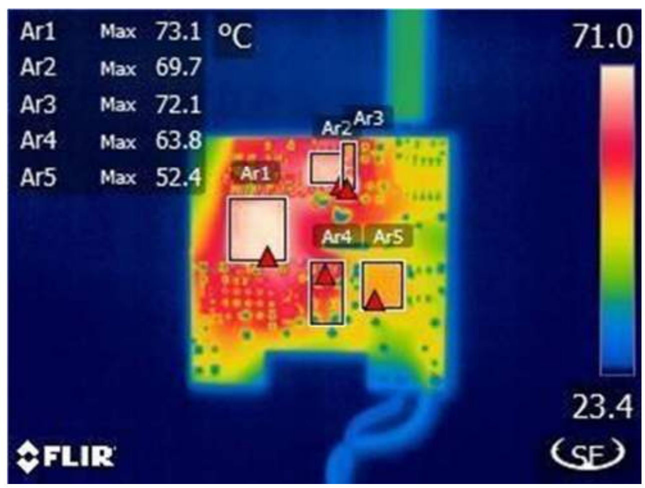


Figure 53 – Bottom Thermal Image, T_{AMB} = 23.5 ºC.
Ar1: InnoSwitch3-PD, U1 = 73.1 ºC.
Ar2: SR FET, Q2 = 69.7 ºC.
Ar3: SR FET Snubber = 72.1 ºC.
Ar4: Primary Snubber = 63.8 ºC.
Ar5: Bridge Rectifier, BR1 = 52.4 ºC.

12.2 *Thermal Performance in Open Case, 45 ºCAmbient*

Note: Measurements taken using Type-T thermocouple and with the board inside a thermal chamber.

12.2.1 Components Temperature Summary

Condition	**Component**	**Temperature (°C)**			
		5 V / 3 A (90 VAC)	**5 V / 3 A (265 VAC)**	**9 V / 3 A (90 VAC)**	**9 V / 3 A (265 VAC)**
Open Frame Unit 45 °C Ambient	INN3878 (U1)	69	73	90.1	87.7
	Primary Snubber (D1)	68	66.5	88.4	79.5
	SR FET (Q2)	72.5	76.9	87.9	88.4
	SR FET Snubber (R8)	71.4	76.6	86.8	87.9
	Bridge Rectifier (BR1)	68.7	58.3	92.3	68.3
	Transformer (T1)	66.4	68.9	80.6	80.2
	Thermistor (RT1)	66.9	52.6	85.9	63.2
	Ambient	48.2	42.9	44.1	46.9

Condition	**Component**	**Temperature (°C)**			
		12 V / 2.5 A (90 VAC)	**12 V / 2.5 A (265 VAC)**	**15 V / 2.0 A (90 VAC)**	**15 V / 2.0 A (265 VAC)**
Open Frame Unit 45 °C Ambient	INN3878 (U1)	94.1	90.7	98.3	94.3
	Primary Snubber (D1)	92.3	81.7	95.6	85.1
	SR FET (Q2)	87.8	87.8	89	89.8
	SR FET Snubber (R8)	86.6	87.6	88	89.6
	Bridge Rectifier (BR1)	97.3	70.3	100.3	75.1
	Transformer (T1)	82.6	81.7	85.5	81.5
	Thermistor (RT1)	88.7	64.9	91.1	69.4
	Ambient	43.5	43.6	49	42.5

Condition	**Component**	**Temperature (°C)**			
		20 V / 1.5 A (90 VAC)	**20 V / 1.5 A (265 VAC)**	**16 V / 2.0 A (90 VAC)**	**16 V / 2.0 A (265 VAC)**
Open Frame Unit 45°C Ambient	INN3878 (U1)	101.3	97.4	92.8	90.5
	Primary Snubber (D1)	96.6	86.1	94.3	87.1
	SR FET (Q2)	88	88.5	87.5	88.1
	SR FET Snubber (R8)	86.8	87.9	87.1	90.8
	Bridge Rectifier (BR1)	100.4	75.8	104.8	76.9
	Transformer (T1)	85.5	82	91.8	90.3
	Thermistor (RT1)	91.4	69.9	98.3	69.6
	Ambient	49.1	43.3	46.5	45.6

12.2.2 Output: 5 V / 3 A (90 VAC and 265VAC)

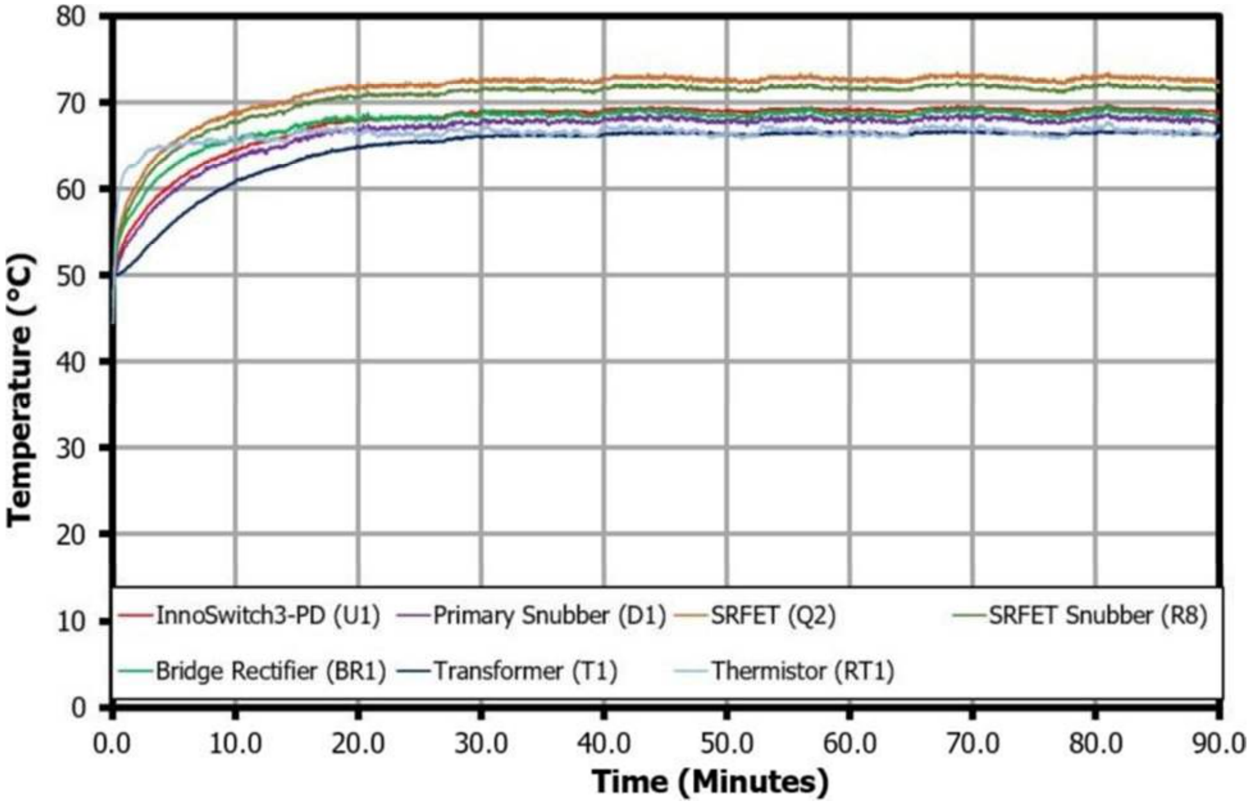


Figure 54 – Enclosed Unit Thermal Performance at 5 V / 3 A Output, 90 VAC, 45 °C Ambient.

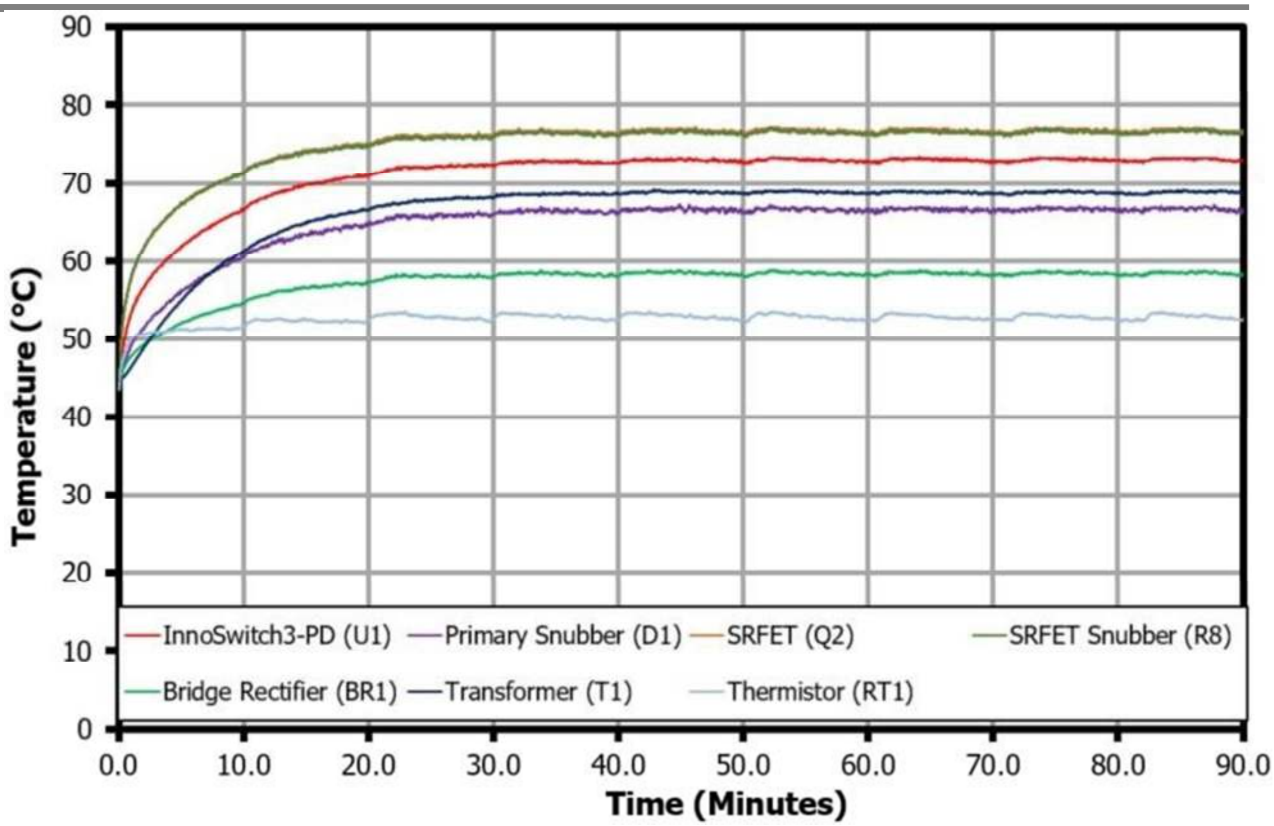


Figure 55 – Enclosed Unit Thermal Performance at 5 V / 3 A Output, 265 VAC, 45 °C Ambient.

12.2.3 Output: 9 V / 3 A (90 and 265 VAC)

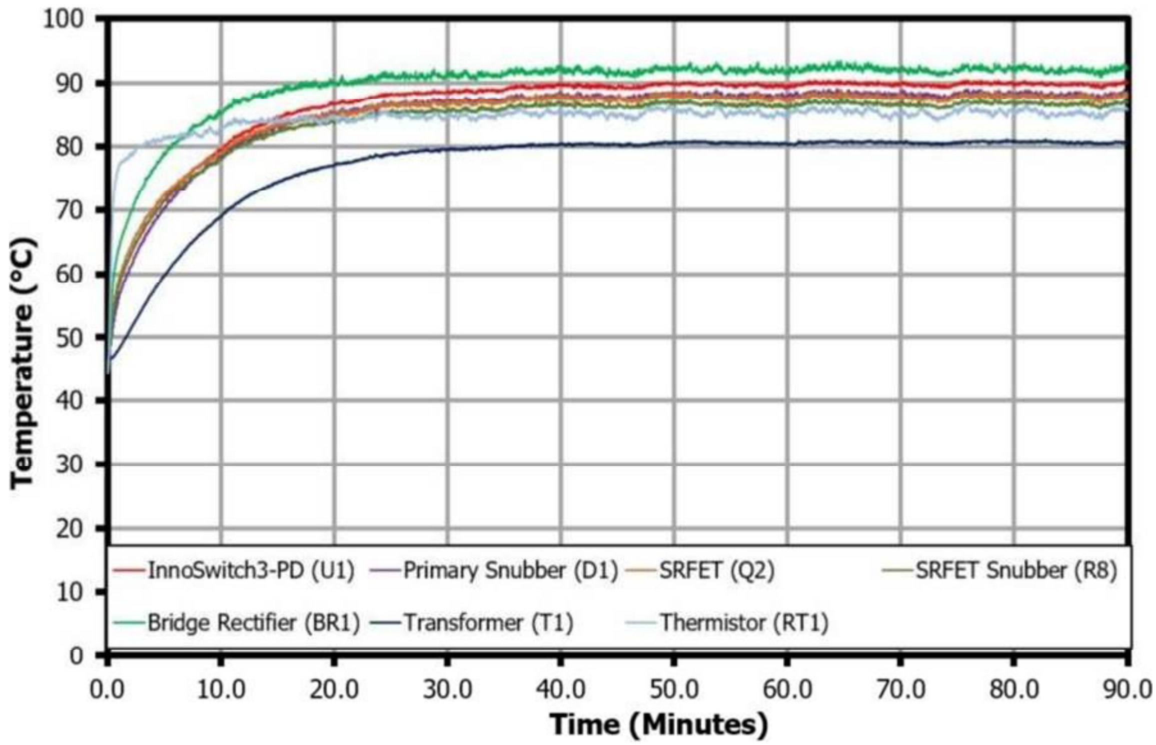


Figure 56 – Enclosed Unit Thermal Performance at 9 V / 3 A Output, 90 VAC, 45 °C Ambient.

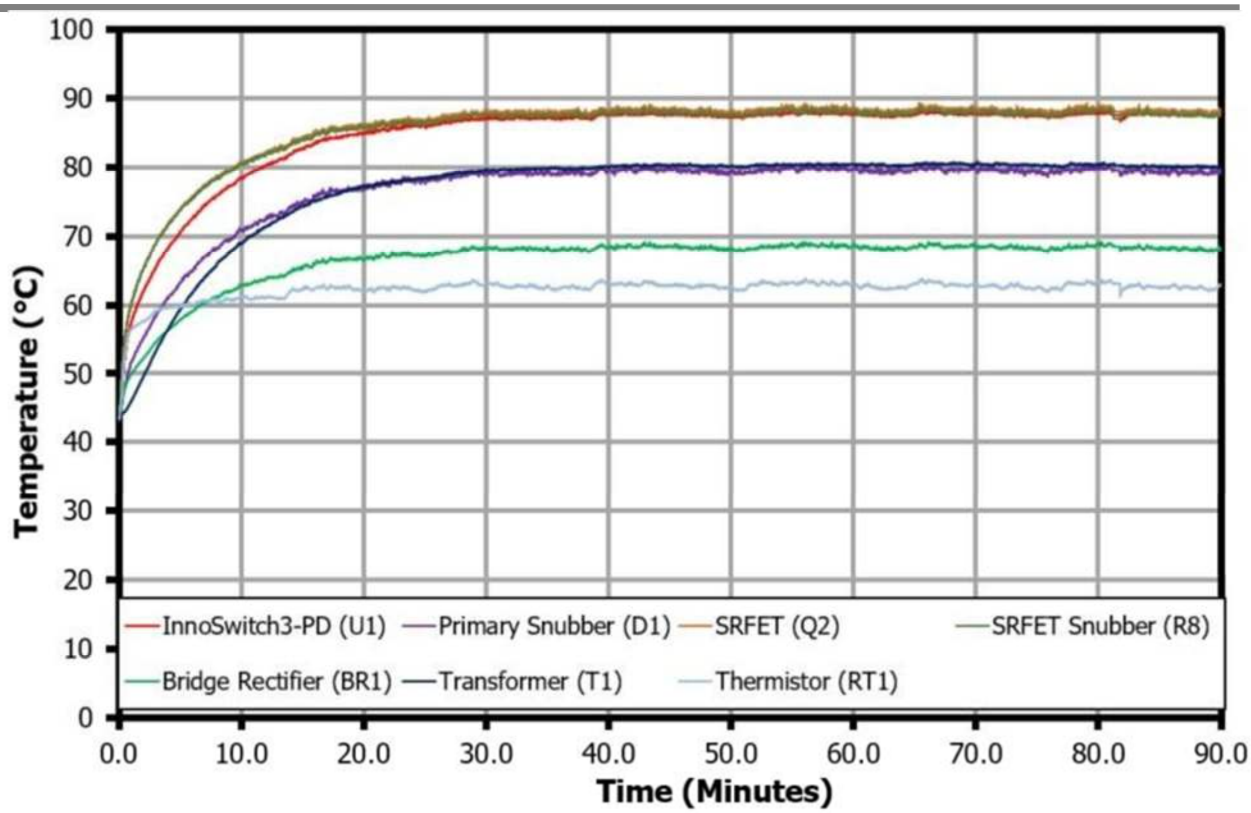


Figure 57 – Enclosed Unit Thermal Performance at 9 V / 3 A Output, 265 VAC, 45 °C Ambient.

12.2.4 Output: 12 V / 2.5 A (90 VAC and 265 VAC)

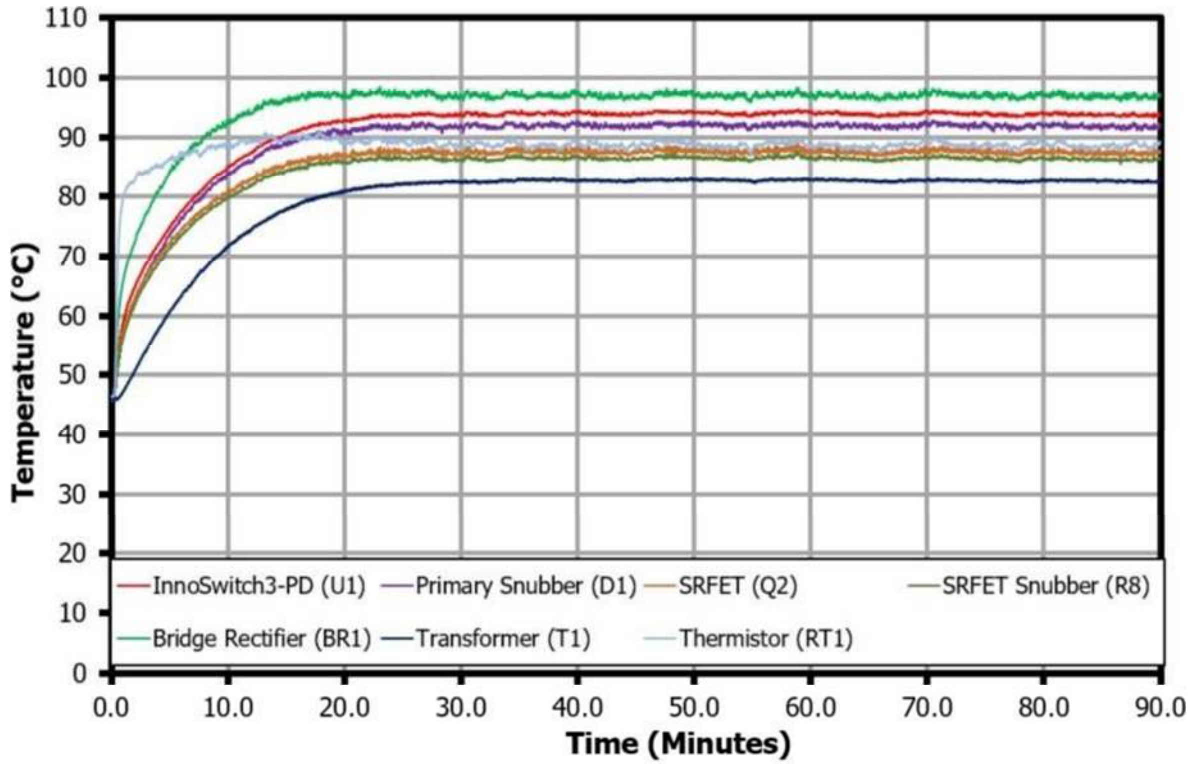


Figure 58 – Enclosed Unit Thermal Performance at 12 V / 1.5 A Output, 90 VAC, 45 °C Ambient.

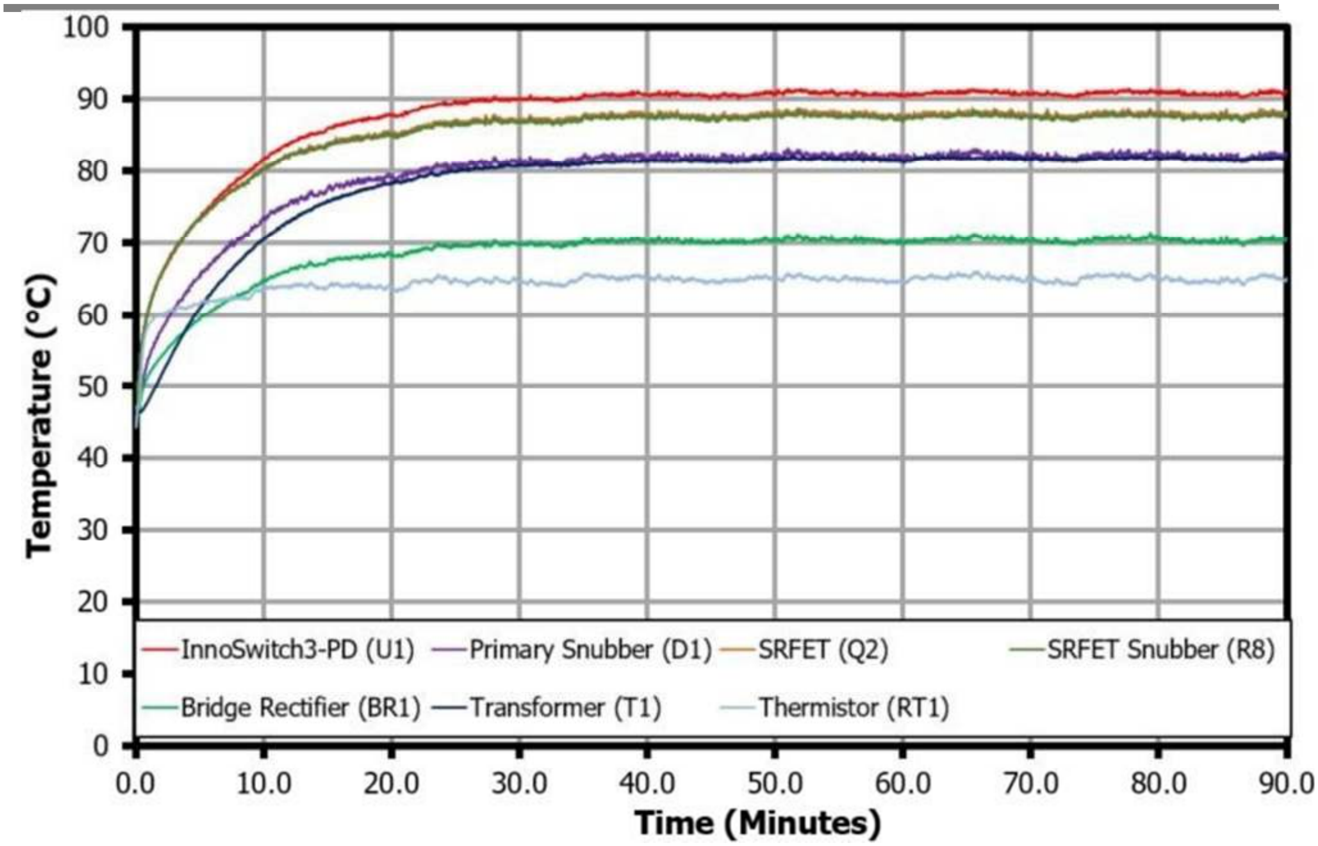


Figure 59 – Enclosed Unit Thermal Performance at 12 V / 2.5 A Output, 265 VAC, 45 °C Ambient.

12.2.5 Output: 15 V / 2.0 A (90 VAC and 265 VAC)

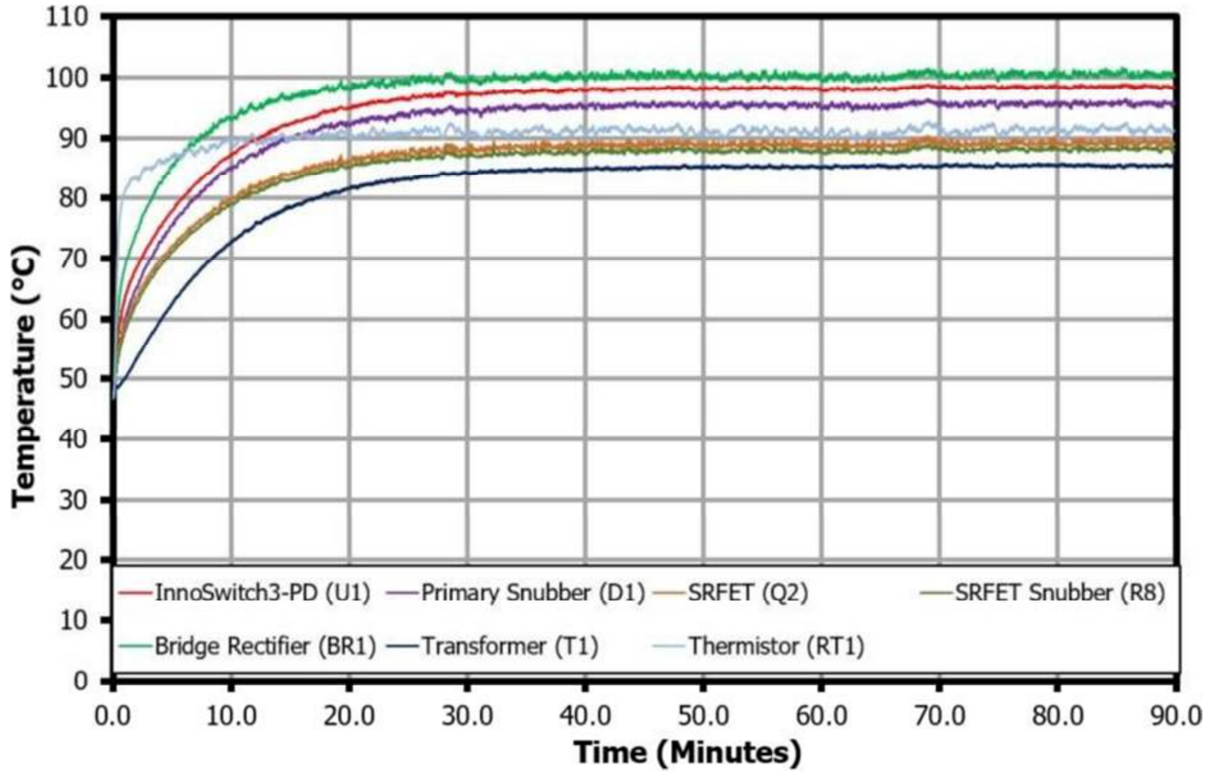


Figure 60 – Enclosed Unit Thermal Performance at 15 V / 2 A Output, 90 VAC, 45 °C Ambient.

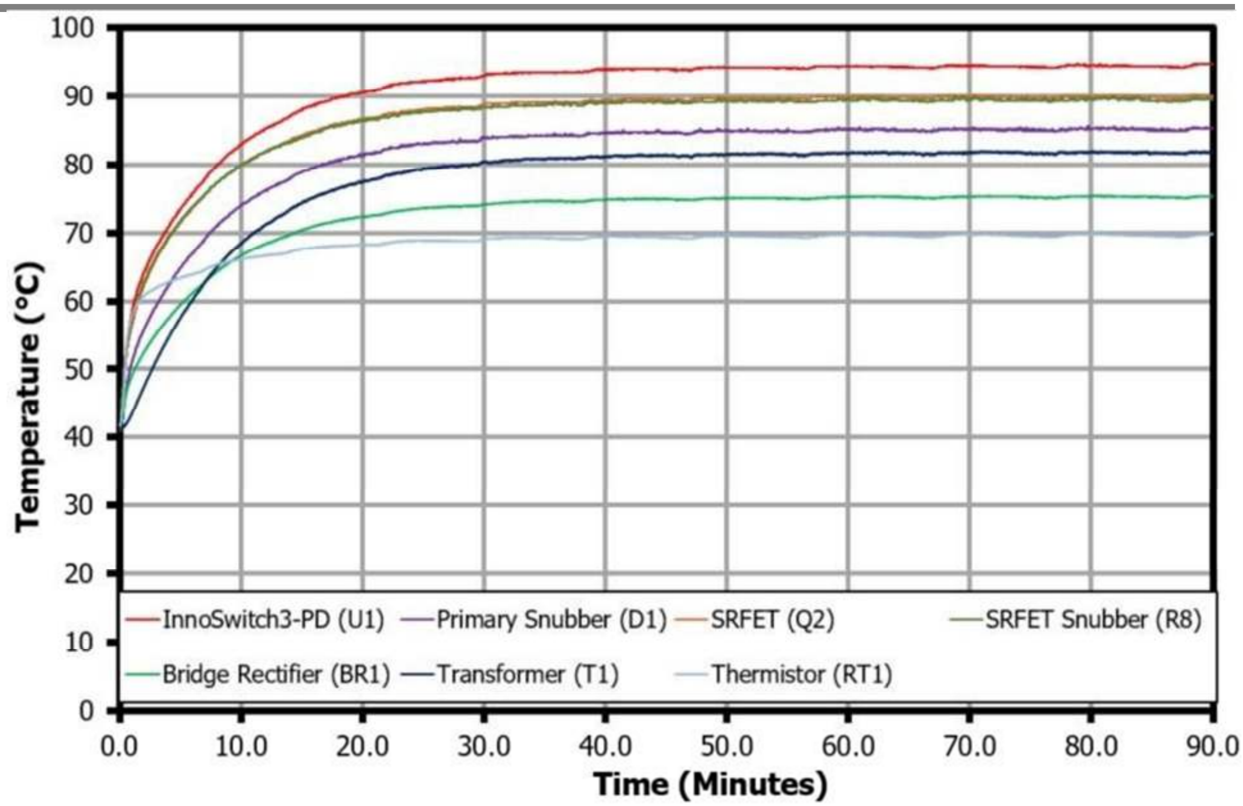


Figure 61 – Enclosed Unit Thermal Performance at 15 V / 2 A Output, 265 VAC, 45 °C Ambient.

12.2.6 Output: 20 V / 1.5 A (90 VAC and 265 VAC)

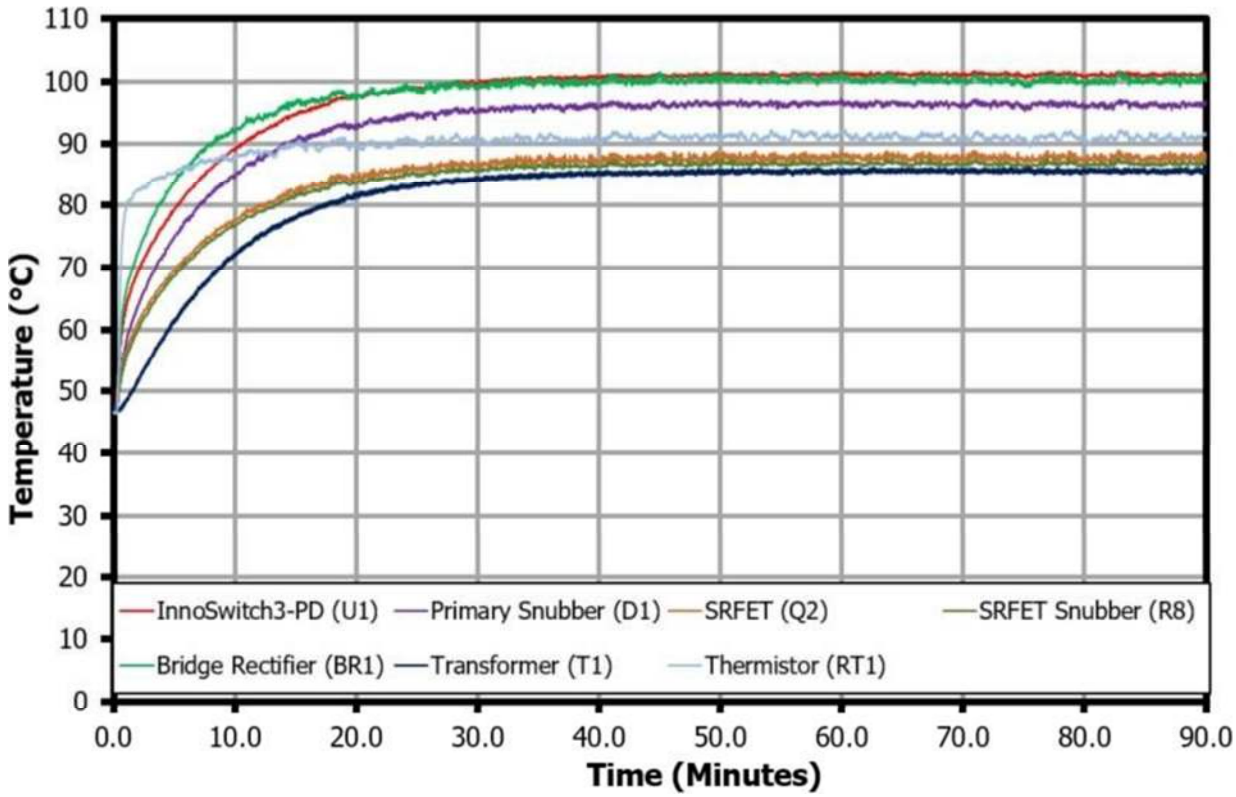


Figure 62 – Enclosed Unit Thermal Performance at 20 V / 1.5 A Output, 90 VAC, 45 °C Ambient

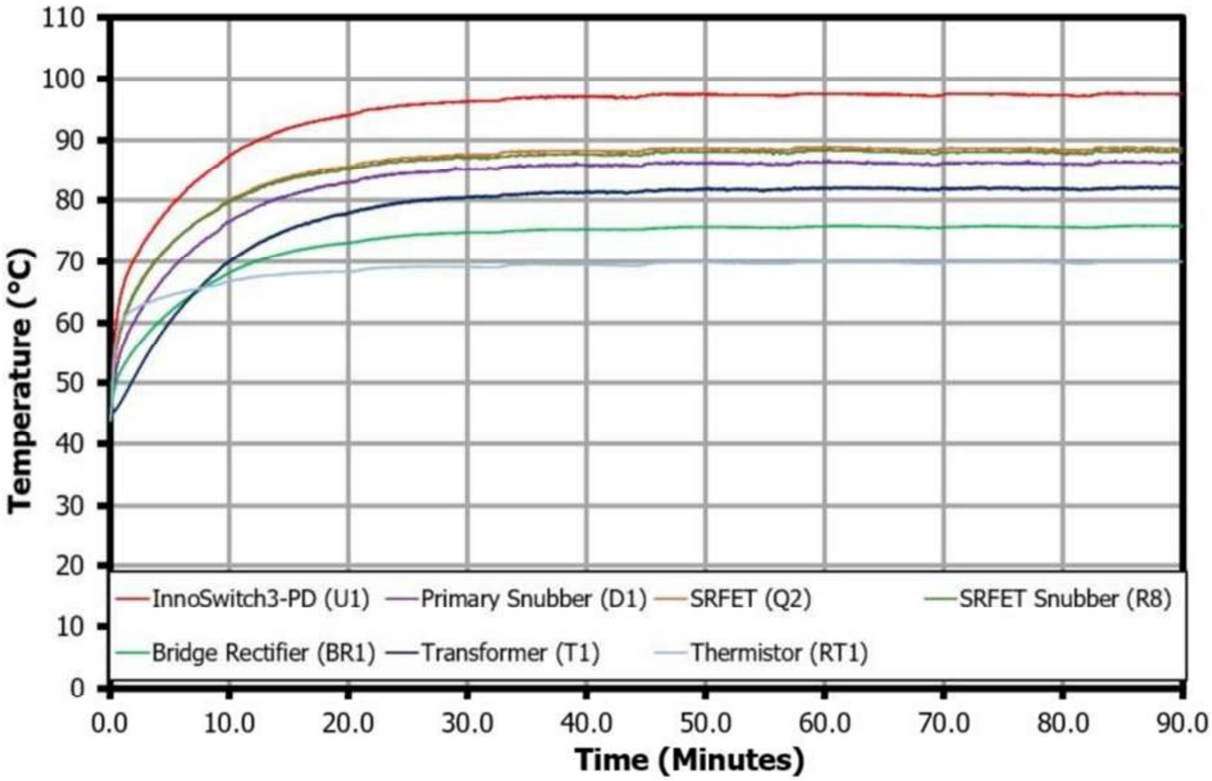


Figure 63 – Enclosed Unit Thermal Performance at 20 V / 1.5 A Output, 265 VAC, 45 °C Ambient.

12.2.7 Output: 16 V / 2.0 A (90 VAC and 265 VAC)

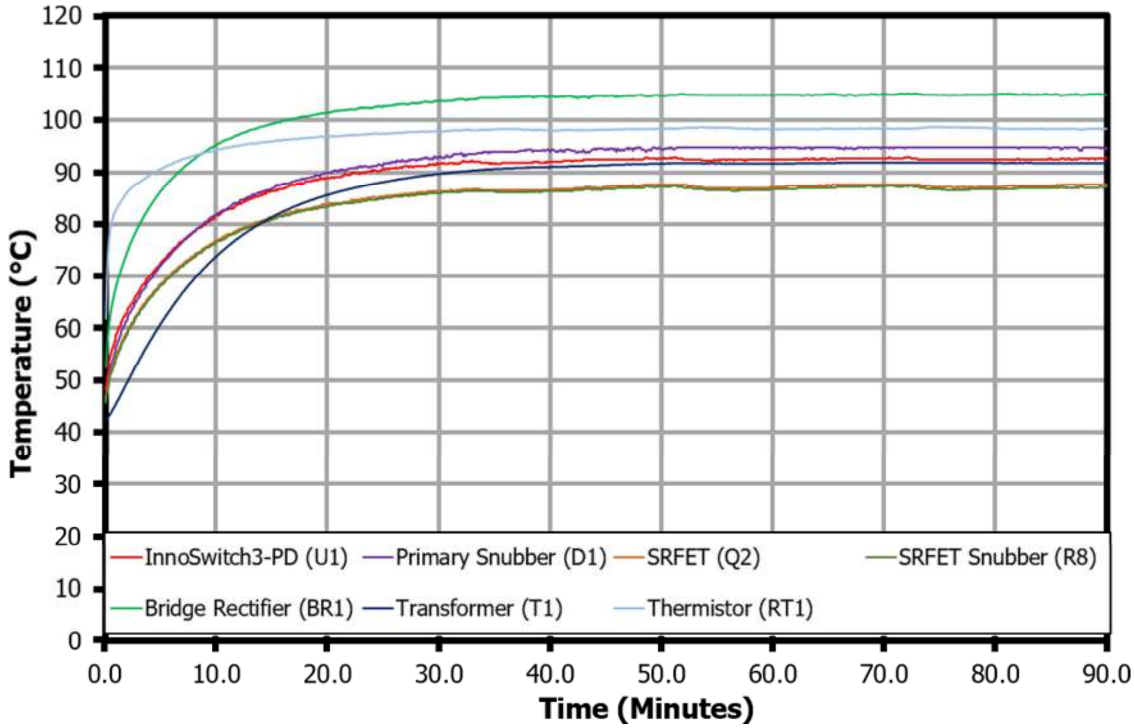


Figure 64 – Enclosed Unit Thermal Performance at 16 V / 2.0 A Output, 90 VAC, 45 °C Ambient.

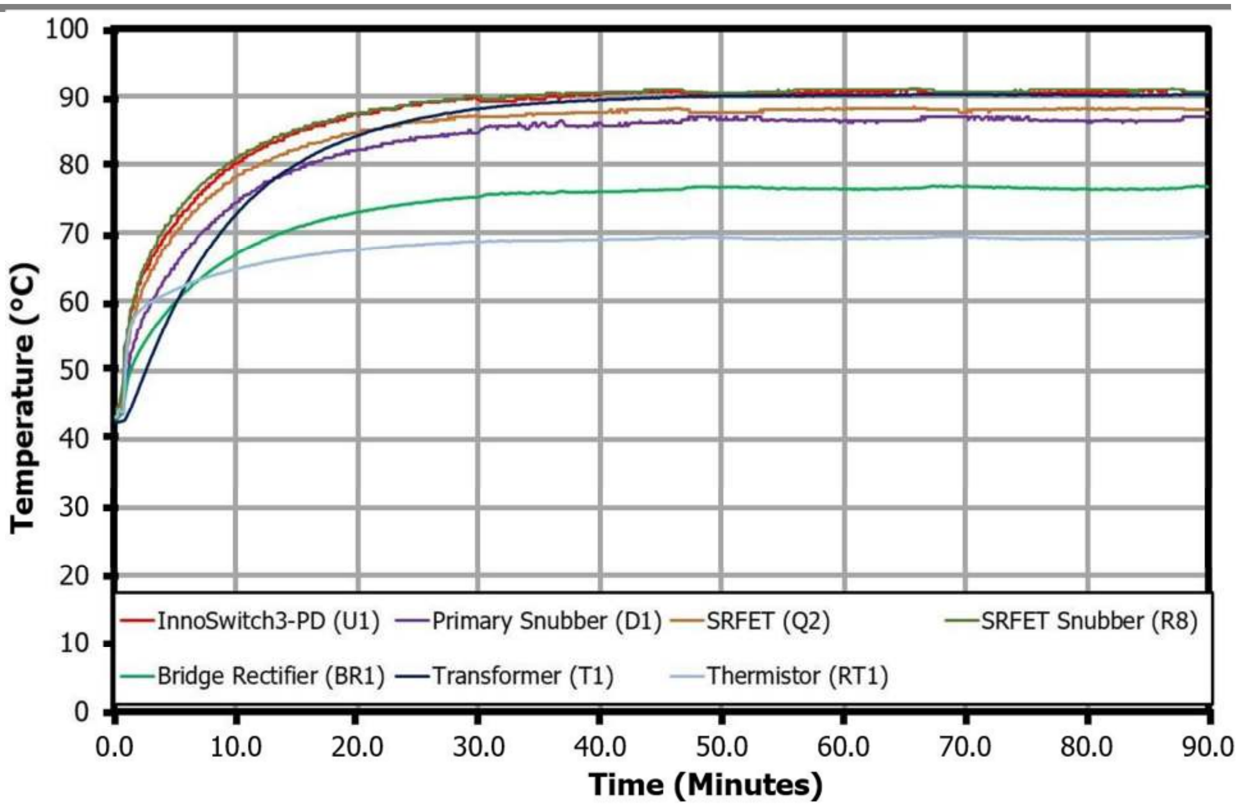


Figure 65 – Enclosed Unit Thermal Performance at 16 V / 2.0 A Output, 265 VAC, 45 °C Ambient.

13 Waveforms

Note: Waveforms taken at room temperature ambient (approximately 25 °C)

13.1 *Start-up Waveforms*

13.1.1 Output Voltage and Current

Note: Output voltage waveforms captured at the end of 48 mΩ cable.

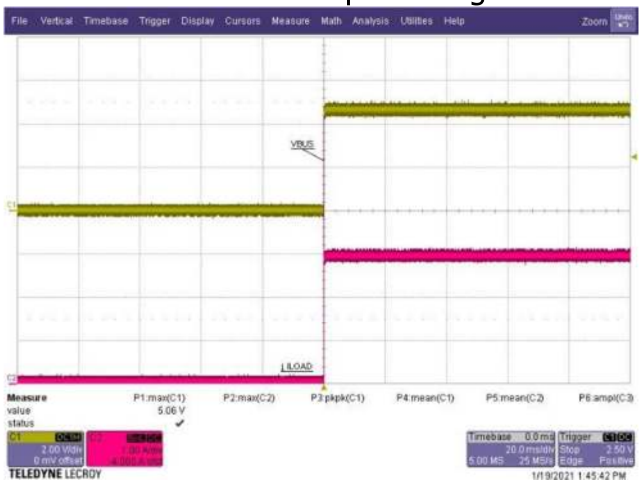


Figure 66 – Output Voltage and Current.
90 VAC, 5.0 V, 3 A Load (CR Mode).
V_{OUT} = 5.06 V Maximum. CH1:
V_{OUT}, 2 V / div.
CH2: I_{LOAD}, 1 A / div.
Time: 20 ms / div.

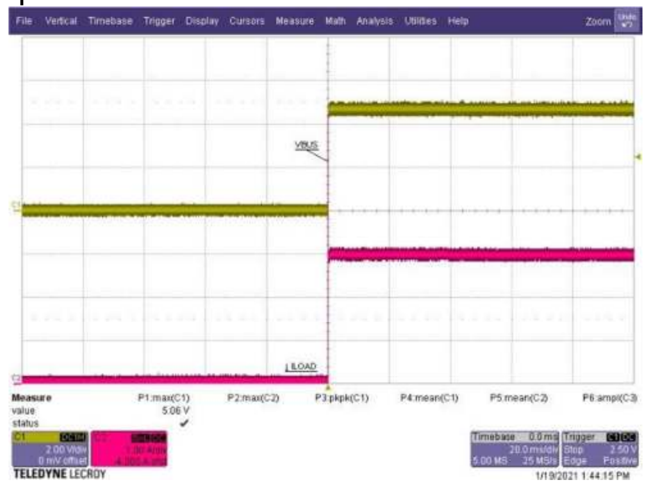


Figure 67 – Output Voltage and Current.
265 VAC, 5.0 V, 3 A Load (CR Mode).
V_{OUT} = 5.059 V Maximum.
CH1: V_{OUT}, 2 V / div.
CH2: I_{LOAD}, 1 A / div.
Time: 20 ms / div.

13.1.2 Primary Drain Voltage and Current

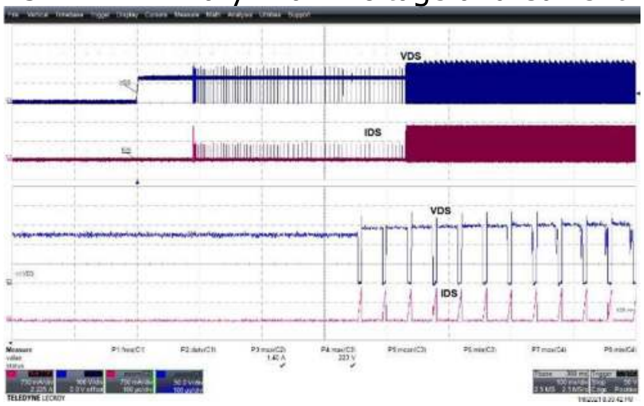


Figure 68 – Primary Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load.
V_{DS_PRI} = 223 V Maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 750 mA / div.
Time: 100 ms / div. (100 µs / div. Zoom)

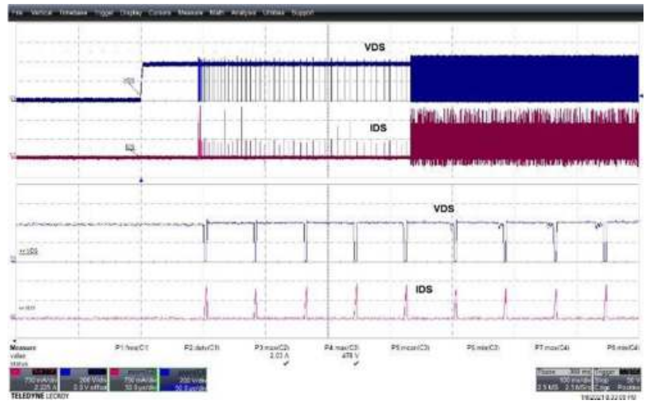


Figure 69 – Primary Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load.
V_{DS_PRI} = 478 V Maximum.
CH1: V_{DS_PRI}, 200 V / div.
CH2: I_{DS_PRI}, 750 mA / div.
Time: 100 ms / div. (50 µs / div. Zoom)

13.1.3 SR FET Drain Voltage and Current

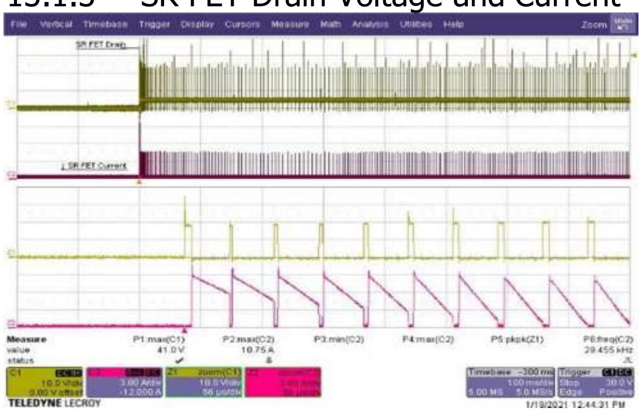


Figure 70 – SR FET Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load.
V_{DS_SRFET} = 41 V Maximum.
CH1: V_{DS_SRFET}, 10 V / div.
CH2: I_{DS_SRFET}, 3 A / div.
Time: 100 ms / div. (56 µs / div. Zoom)

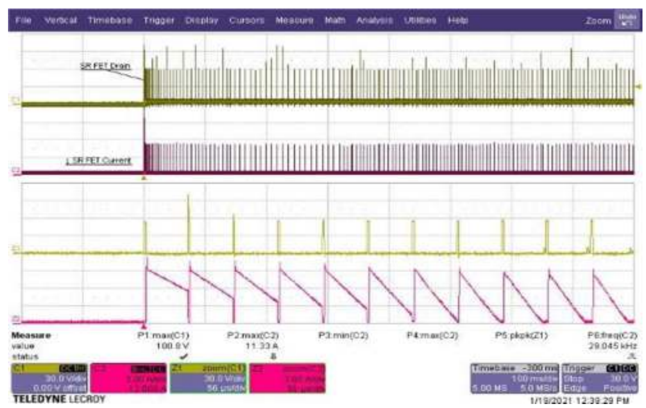


Figure 71 – SR FET Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load.
V_{DS_SRFET} = 101 V Maximum.
CH1: V_{DS_SRFET}, 30 V / div.
CH2: I_{DS_SRFET}, 3 A / div.
Time: 100 ms / div. (56 µs / div. Zoom)

13.2 *Primary Drain Voltage and Current (Steady-State)*

13.2.1 Output: 5 V / 3 A

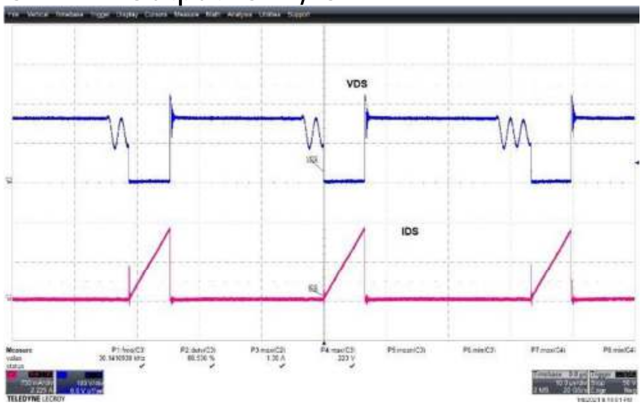


Figure 72 – Primary Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load.
V_{DS_PRI} = 223 V Maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 750 mA / div.
Time: 10 μs / div.

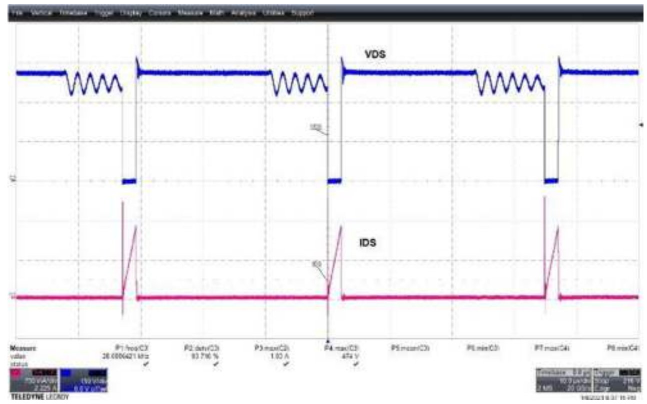


Figure 73 – Primary Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load.
V_{DS_PRI} = 474 V Maximum.
CH1: V_{DS_PRI}, 150 V / div.
CH2: I_{DS_PRI}, 750 mA / div.
Time: 10 μs / div.

13.2.2 Output: 9 V / 3 A

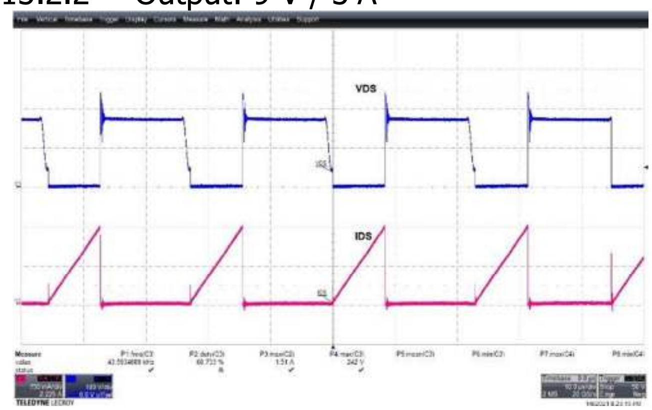


Figure 74 – Primary Drain Voltage and Current.
90 VAC, 9.0 V, 3 A Load.
V_{DS_PRI} = 242 V Maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 750 mA / div.
Time: 10 μs / div.

Figure 75 – Primary Drain Voltage and Current.
265 VAC, 9.0 V, 3 A Load.
V_{DS_PRI} = 509 V Maximum.
CH1: V_{DS_PRI}, 150 V / div.
CH2: I_{DS_PRI}, 750 mA / div.
Time: 10 μs / div.

13.2.3 Output: 12 V / 2.5 A

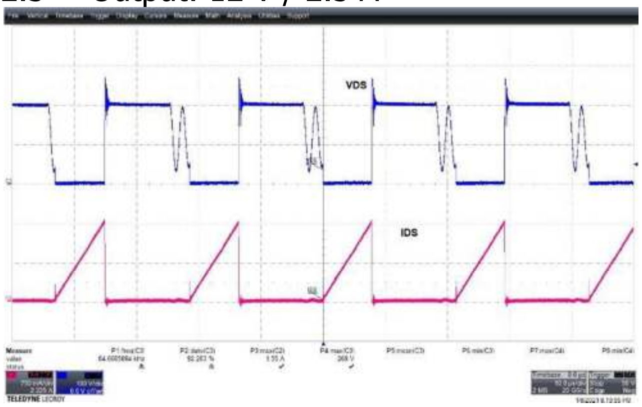


Figure 76 – Primary Drain Voltage and Current.
90 VAC, 12.0 V, 2.5 A Load.
V_{DS_PRI} = 269 V Maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 750 mA / div.
Time: 10 μs / div.

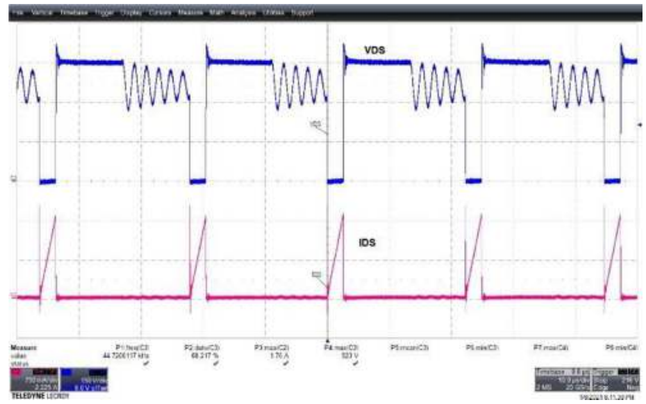


Figure 77 – Primary Drain Voltage and Current.
265 VAC, 12.0 V, 2.5 A Load.
V_{DS_PRI} = 523 V Maximum.
CH1: V_{DS_PRI}, 150 V / div.
CH2: I_{DS_PRI}, 750 mA / div.
Time: 10 μs / div.

13.2.4 Output: 15 V / 2 A

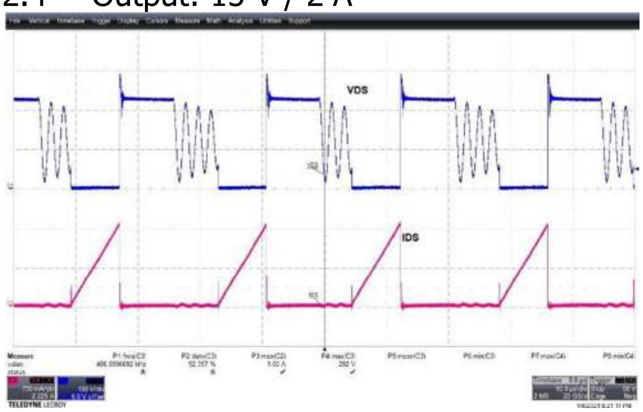


Figure 78 – Primary Drain Voltage and Current.
90 VAC, 15.0 V, 2 A Load.
V_{DS_PRI} = 292 V Maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 750 mA / div.
Time: 10 μs / div.

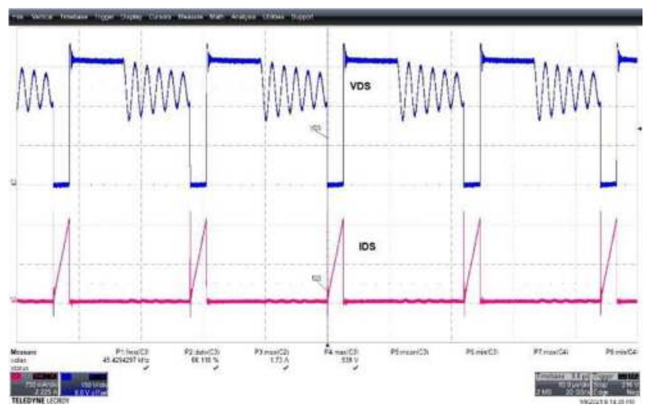


Figure 79 – Primary Drain Voltage and Current.
265 VAC, 15.0 V, 2 A Load.
V_{DS_PRI} = 539 V Maximum.
CH1: V_{DS_PRI}, 150 V / div.
CH2: I_{DS_PRI}, 750 mA / div.
Time: 10 μs / div.

13.2.5 Output: 20 V / 1.5 A

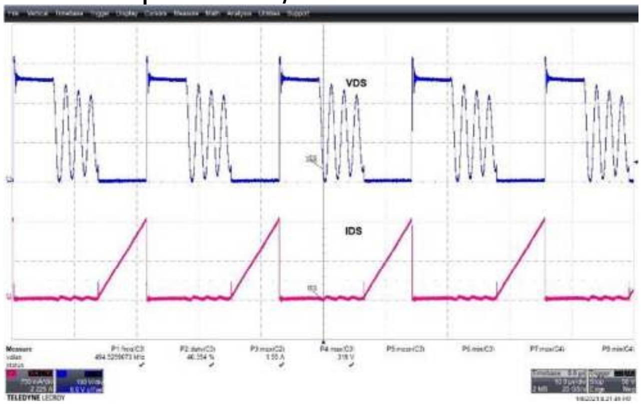


Figure 80 – Primary Drain Voltage and Current.
90 VAC, 20.0 V, 1.5 A Load.
V_{DS_PRI} = 319 V Maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 750 mA / div.
Time: 10 µs / div.

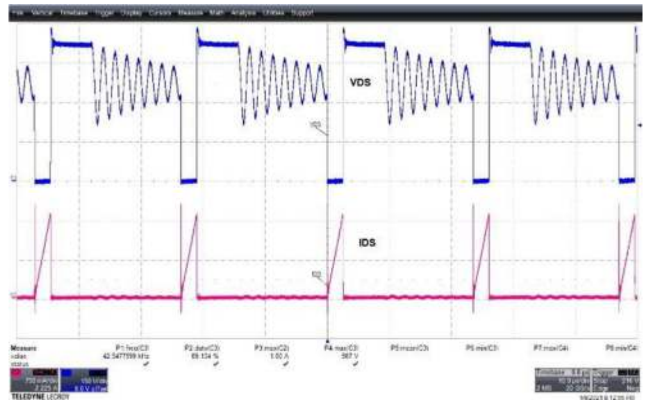


Figure 81 – Primary Drain Voltage and Current.
265 VAC, 20.0 V, 1.5 A Load.
V_{DS_PRI} = 587 V Maximum.
CH1: V_{DS_PRI}, 150 V / div.
CH2: I_{DS_PRI}, 750 mA / div.
Time: 10 µs / div.

13.3 *SR FET Drain Voltage and Current (Steady-State)*

13.3.1 Output: 5 V / 3 A

Figure 82 – SR FET Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load.
V_{DS_SRFET} = 28.0 V Maximum.
CH1: V_{DS_SRFET}, 12 V / div.
CH2: I_{DS_SRFET}, 3 A / div.
Time: 10 µs / div.

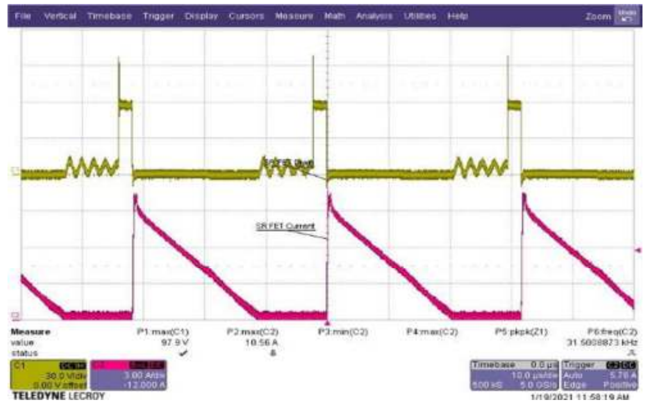


Figure 83 – SR FET Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load.
V_{DS_SRFET} = 97.9 V Maximum.
CH1: V_{DS_SRFET}, 30 V / div.
CH2: I_{DS_SRFET}, 3 A / div.
Time: 10 µs / div.

13.3.2 Output: 9 V / 3 A

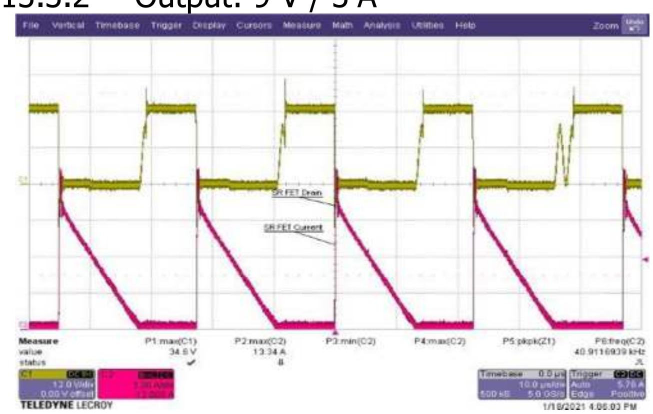


Figure 84 – SR FET Drain Voltage and Current.
90 VAC, 9.0 V, 3 A Load.
V_{DS_SRFET} = 34.6 V Maximum.
CH1: V_{DS_SRFET}, 12 V / div.
CH2: I_{DS_SRFET}, 3 A / div.
Time: 10 µs / div.

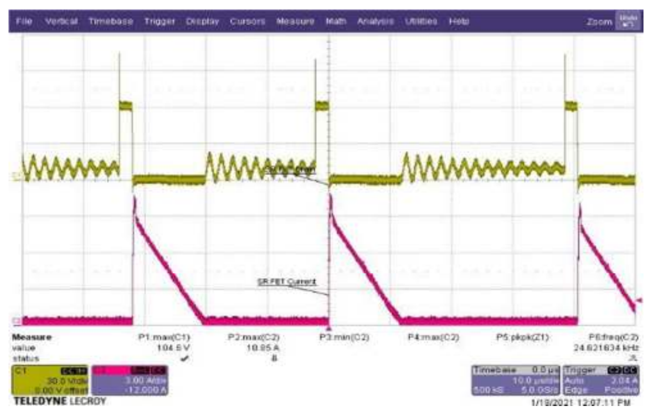


Figure 85 – SR FET Drain Voltage and Current.
265 VAC, 9.0 V, 3 A Load.
V_{DS_SRFET} = 105 V Maximum.
CH1: V_{DS_SRFET}, 30 V / div.
CH2: I_{DS_SRFET}, 3 A / div.
Time: 10 µs / div.

13.3.3 Output 12 V / 2.5 A

Figure 86 – SR FET Drain Voltage and Current.
90 VAC, 15.0 V, 2 A Load.
V_{DS_SRFET} = 31.5 V Maximum.
CH1: V_{DS_SRFET}, 12 V / div.
CH2: I_{DS_SRFET}, 3 A / div.
Time: 10 µs / div.

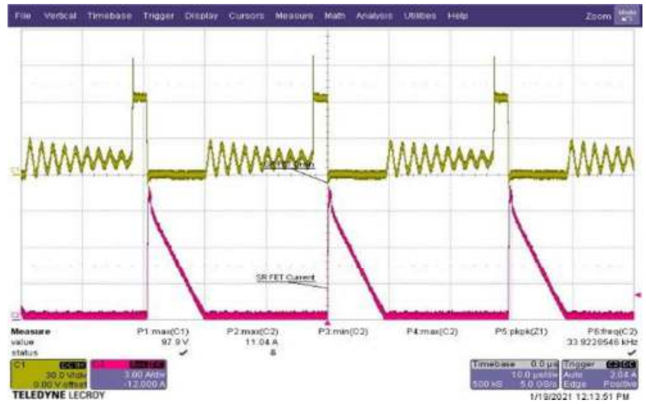


Figure 87 – SR FET Drain Voltage and Current.
265 VAC, 15.0 V, 2 A Load.
V_{DS_SRFET} = 97.9 V Maximum.
CH1: V_{DS_SRFET}, 30 V / div.
CH2: I_{DS_SRFET}, 3 A / div.
Time: 10 µs / div.

13.3.4 Output: 15 V / 2 A

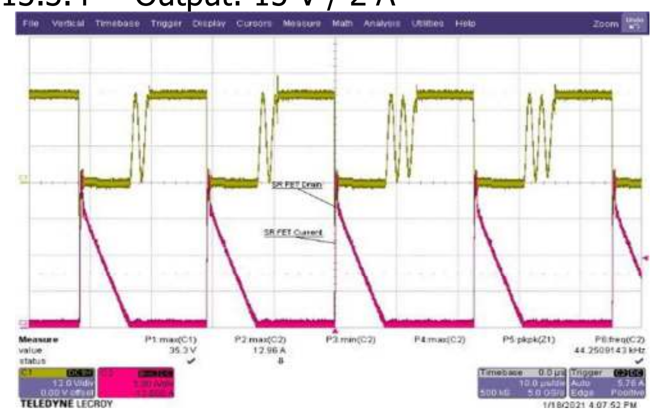


Figure 88 – SR FET Drain Voltage and Current.
90 VAC, 15.0 V, 2 A Load.
V_{DS_SRFET} = 35.3 V Maximum.
CH1: V_{DS_SRFET}, 12 V / div.
CH2: I_{DS_SRFET}, 3 A / div.
Time: 10 µs / div.

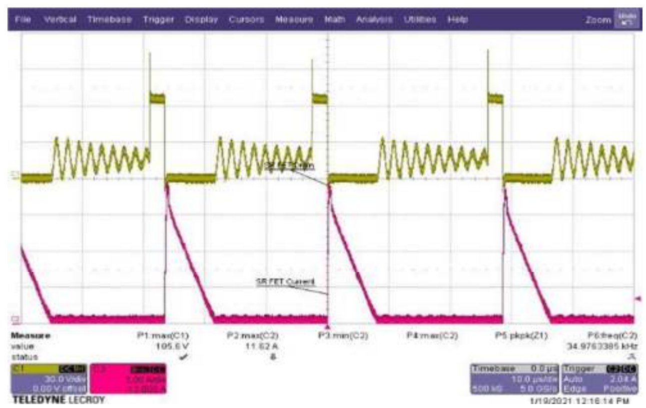


Figure 89 – SR FET Drain Voltage and Current.
265 VAC, 15.0 V, 2 A Load.
V_{DS_SRFET} = 105 V Maximum.
CH1: V_{DS_SRFET}, 30 V / div.
CH2: I_{DS_SRFET}, 3 A / div.
Time: 10 µs / div.

13.3.5 Output: 20 V / 1.5 A

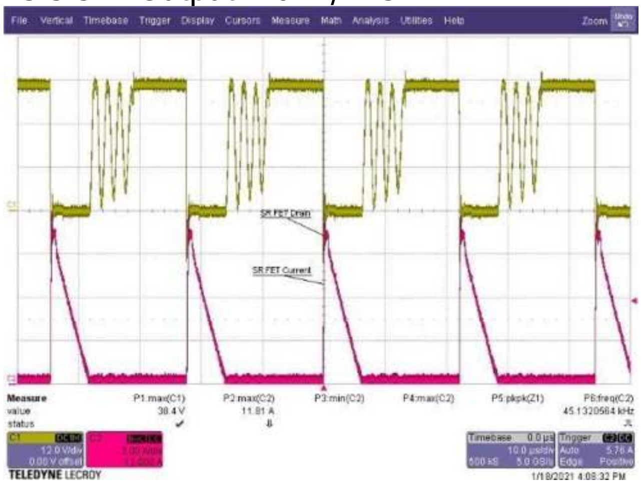


Figure 90 – SR FET Drain Voltage and Current.
90 VAC, 20.0 V, 1.5 A Load.
V_{DS_SRFET} = 38.4 V Maximum.
CH1: V_{DS_SRFET}, 12 V / div.
CH2: I_{DS_SRFET}, 3 A / div.
Time: 10 µs / div.

Figure 91 – SR FET Drain Voltage and Current.
265 VAC, 20.0 V, 1.5 A Load.
V_{DS_SRFET} = 103 V Maximum.
CH1: V_{DS_SRFET}, 30 V / div.
CH2: I_{DS_SRFET}, 3 A / div.
Time: 10 µs / div.

13.4 *Primary and SR FET Drain Voltage and Current (during Output Voltage Transition)*

13.4.1 Primary Drain Voltage and Current, 3.3 V to 11 V Transition / 2.727 A Load

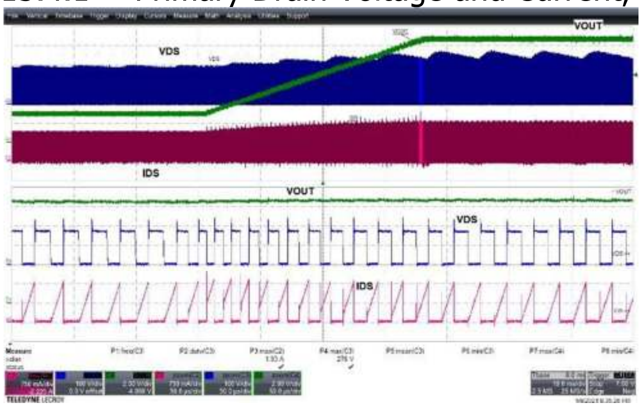


Figure 92 – Primary Drain Voltage and Current.
90 VAC, 3.3 V to 20 V V_{OUT} Transition,
2.727 A Load.
V_{DS_PRI} = 276 V Maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 750 mA / div.
CH4: V_{OUT}, 2 V / div.
Time: 10 ms / div. (50 µs / div. Zoom)

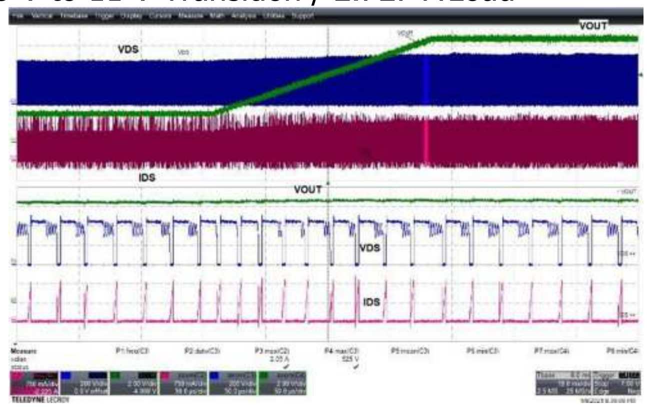


Figure 93 – Primary Drain Voltage and Current.
265 VAC, 3.3 V to 20 V V_{OUT} Transition,
2.727 A Load.
V_{DS_PRI} = 525 V Maximum.
CH1: V_{DS_PRI}, 200 V / div.
CH2: I_{DS_PRI}, 750 mA / div.
CH4: V_{OUT}, 2 V / div.
Time: 10 ms / div. (50 µs / div. Zoom)

13.4.2 Primary Drain Voltage and Current, 3.3 V to 16 V Transition / 8 Ω Load

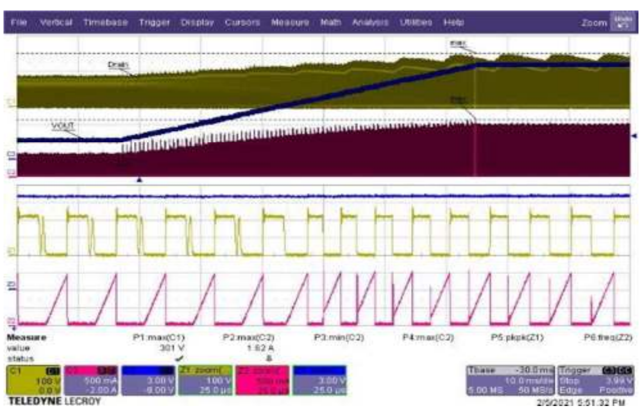


Figure 94 – Primary Drain Voltage and Current.
90 VAC, 3.3 V to 20 V V_{OUT} Transition,
2.727 A Load.
V_{DS_PRI} = 301 V Maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 500 mA / div.
CH4: V_{OUT}, 3 V / div.
Time: 10 ms / div. (25 µs / div. Zoom)

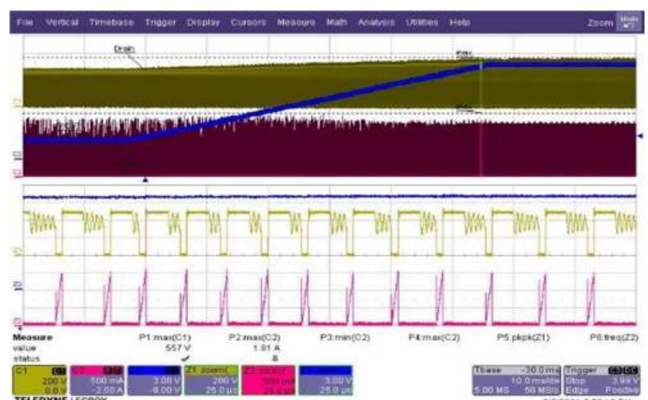


Figure 95 – Primary Drain Voltage and Current.
265 VAC, 3.3 V to 20 V V_{OUT} Transition,
2.727 A Load.
V_{DS_PRI} = 557 V Maximum.
CH1: V_{DS_PRI}, 200 V / div.
CH2: I_{DS_PRI}, 500 mA / div.
CH4: V_{OUT}, 3 V / div.
Time: 10 ms / div. (25 µs / div. Zoom)

13.4.3 SR FET Drain Voltage and Current, 3.3 V to 11 V Transition / 2.727 A Load

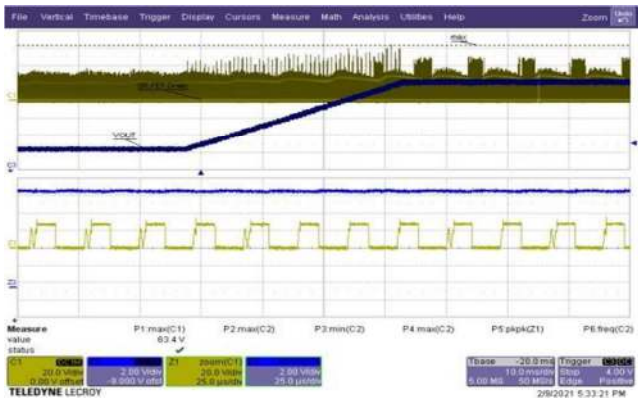


Figure 96 – SR FET Drain Voltage and Current.
90 VAC, 3.3 V to 20 V V_{OUT} Transition,
2.727 A Load.
V_{DS_SRFET} = 68.5 V Maximum.
CH1: V_{DS_SRFET}, 20 V / div.
CH2: I_{DS_SRFET}, 3 A / div.
CH4: V_{OUT}, 2 V / div.
Time: 10 ms / div. (50 μs / div. Zoom)

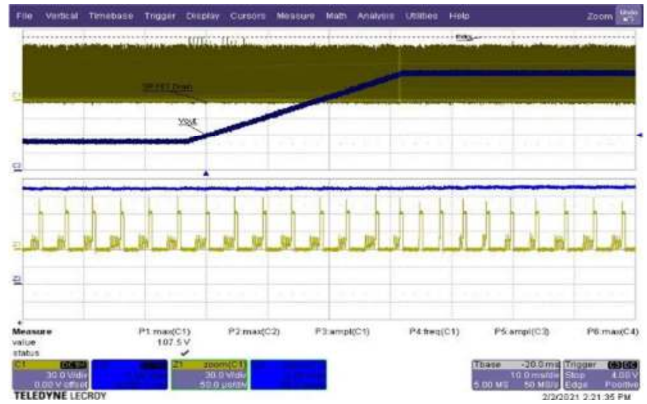


Figure 97 – SR FET Drain Voltage and Current.
265 VAC, 3.3 V to 20 V V_{OUT} Transition,
2.727 A Load.
V_{DS_SRFET} = 107.5 V Maximum.
CH1: V_{DS_SRFET}, 30V / div.
CH4: V_{OUT}, 2 V / div.
Time: 10 ms / div. (50 μs / div. Zoom)

13.4.4 SR FET Drain Voltage and Current, 3.3 V to 16 V Transition / 8 Ω Load

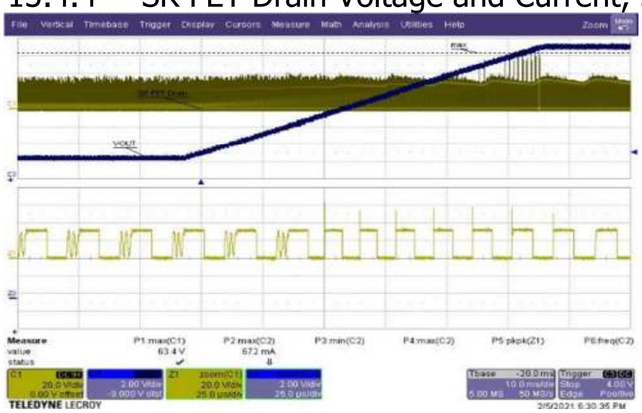


Figure 98 – SR FET Drain Voltage and Current.
90 VAC, 3.3 V to 20 V V_{OUT} Transition,
2.727 A Load.
V_{DS_SRFET} = 63.4 V Maximum.
CH1: V_{DS_SRFET}, 20 V / div.
CH4: V_{OUT}, 2 V / div.
Time: 10 ms / div. (25 μs / div. Zoom)

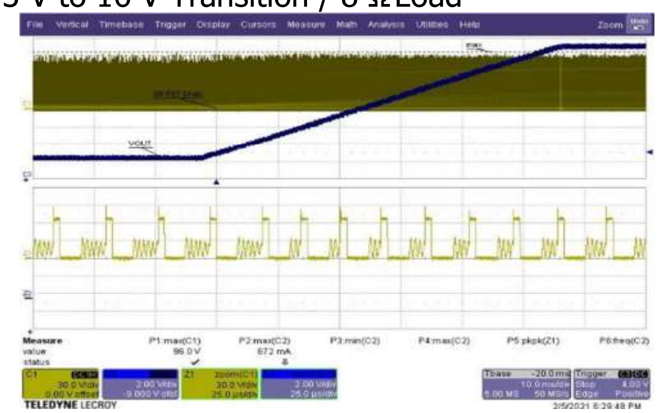


Figure 99 – SR FET Drain Voltage and Current.
265 VAC, 3.3 V to 20 V V_{OUT} Transition,
2.727 A Load.
V_{DS_SRFET} = 96.0 V Maximum.
CH1: V_{DS_SRFET}, 30V / div.
CH4: V_{OUT}, 2 V / div.
Time: 10 ms / div. (25 μs / div. Zoom)

13.5 ***Load Transient and Output Ripple Measurements***

13.5.1 Ripple Measurement Technique

For load transient response and DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

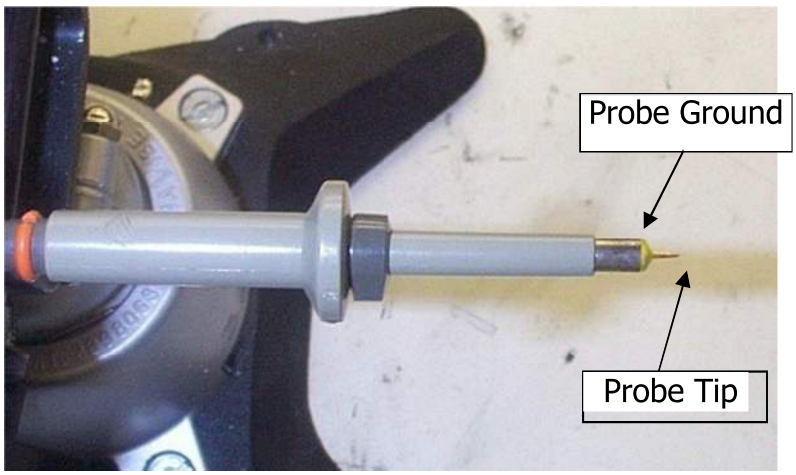


Figure 100 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

Figure 101 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

13.6 *Load Transient Response*

Note: 1. Output voltage waveforms captured at the end of 48 mΩ cable using the ripple measurement probe with decoupling capacitors.

2. Duration for load states (high = 50 ms; low = 50 ms) are chosen to show steady- state for each load condition.

3. Load slew rate (150 mA / μs) is based on USB PD 3.0 PPS specification.

13.6.1 Output: 5 V / 3 A

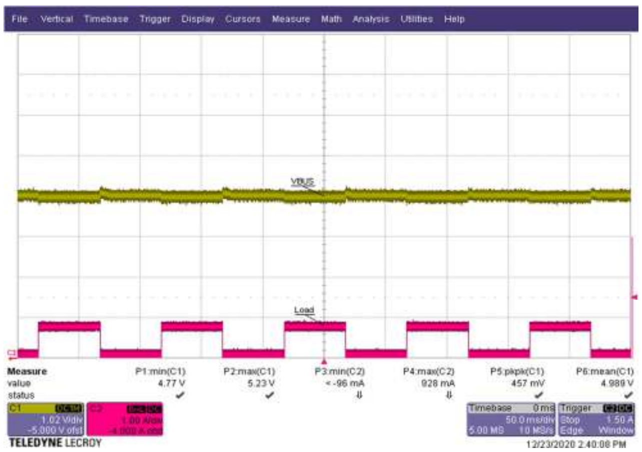


Figure 102 – Transient Response.
90 VAC, 5 V, 0 to 25% Load.
V_{OUT} = 5.23 V max., 4.77 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

Figure 103 – Transient Response.
265 VAC, 5 V, 0 to 25% Load.
V_{OUT} = 5.23 V max., 4.77 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

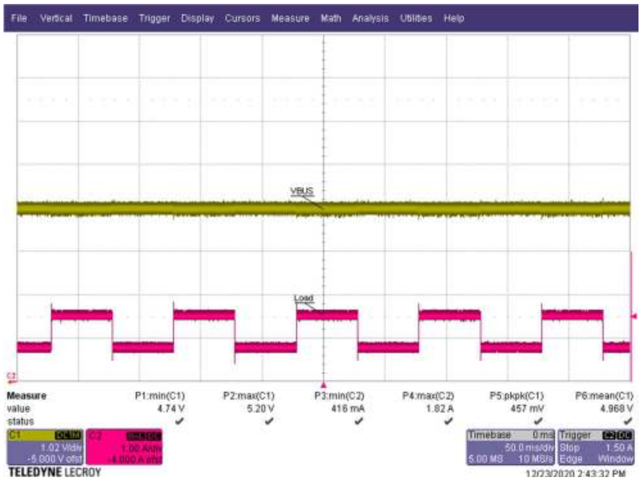


Figure 104 – Transient Response.
90 VAC, 5 V, 25% to 50% Load.
V_{OUT} = 5.20 V max., 4.74 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

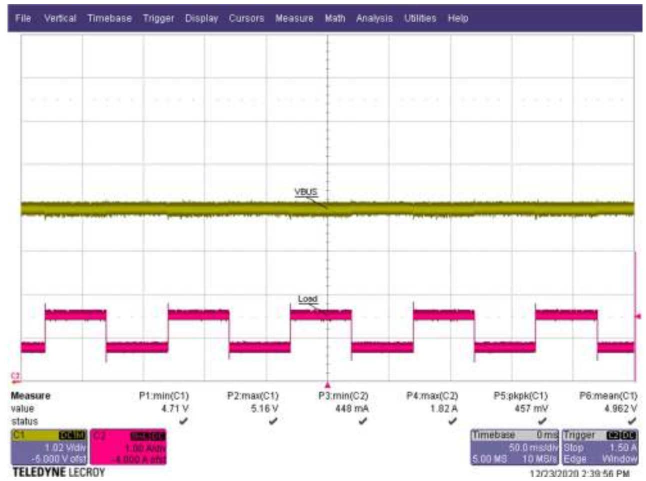


Figure 105 – Transient Response.
265 VAC, 5 V, 25% to 50% Load. V_{OUT} = 5.16 V max., 4.71 V min. CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

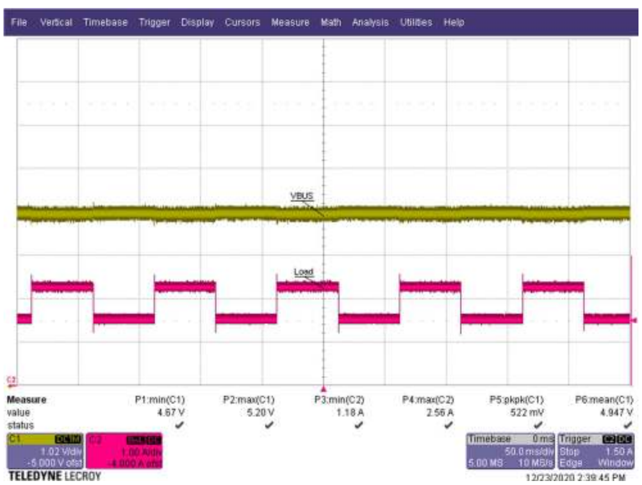


Figure 106 – Transient Response.
90 VAC, 5.0 V, 50% to 75% Load.
V_{OUT} = 5.20 V max., 4.67 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

Figure 107 – Transient Response.
265 VAC, 5.0 V, 50% to 75% Load.
V_{OUT} = 5.20 V max., 4.71 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

Figure 108 – Transient Response.
90 VAC, 5.0 V, 75% to 100% Load.
V_{OUT} = 5.16 V max., 4.67 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

Figure 109 – Transient Response.
265 VAC, 5.0 V, 75% to 100% Load.
V_{OUT} = 5.33 V max., 4.67 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

13.6.2 Output: 9 V / 3 A

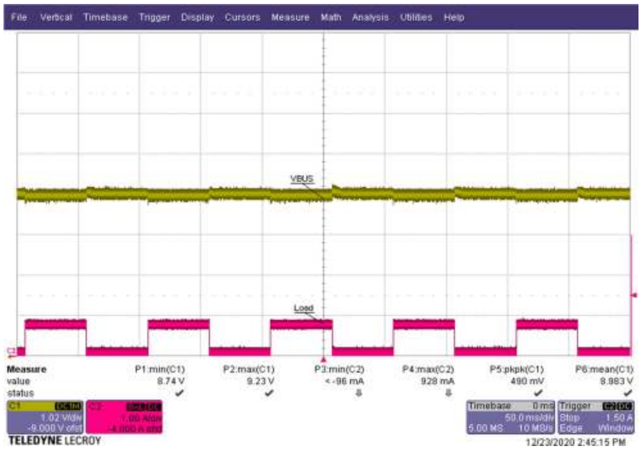


Figure 110 – Transient Response.
90 VAC, 9.0 V, 0 to 25% Load.
V_{OUT} = 9.23 V max., 8.74 V min. CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

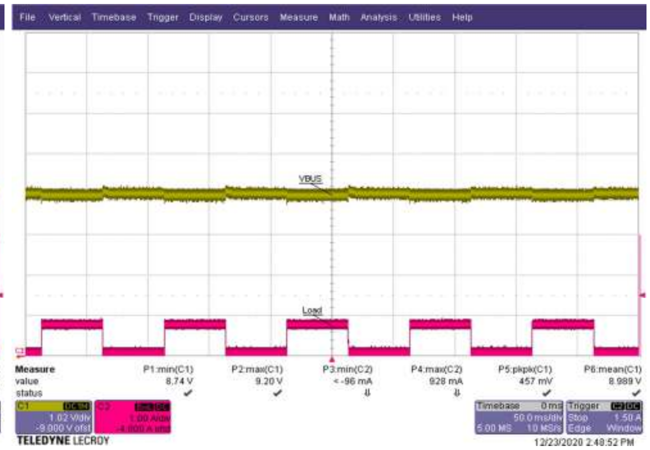


Figure 111 – Transient Response.
265 VAC, 9.0 V, 0 to 25% Load.
V_{OUT} = 9.20 V max., 8.74 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

Figure 112 – Transient Response.
90 VAC, 9.0 V, 25% to 50% Load.
V_{OUT} = 9.16 V max., 8.67 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

Figure 113 – Transient Response.
265 VAC, 9.0 V, 25% to 50% Load.
V_{OUT} = 9.20 V max., 8.71 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

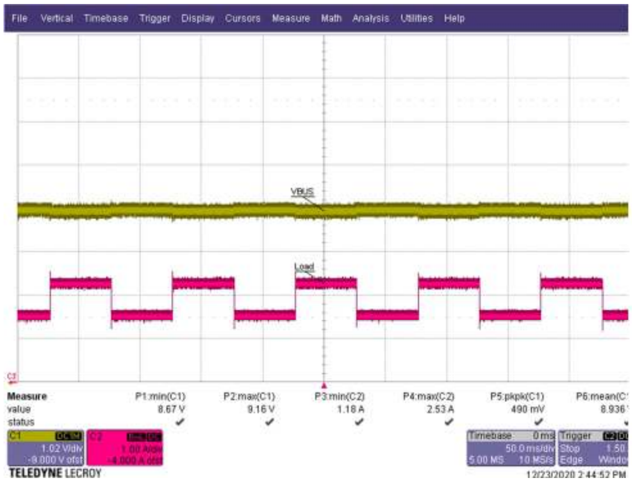


Figure 114 – Transient Response.
90 VAC, 9.0 V, 50% to 75% Load.
V_{OUT} = 9.16 V max., 8.67 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

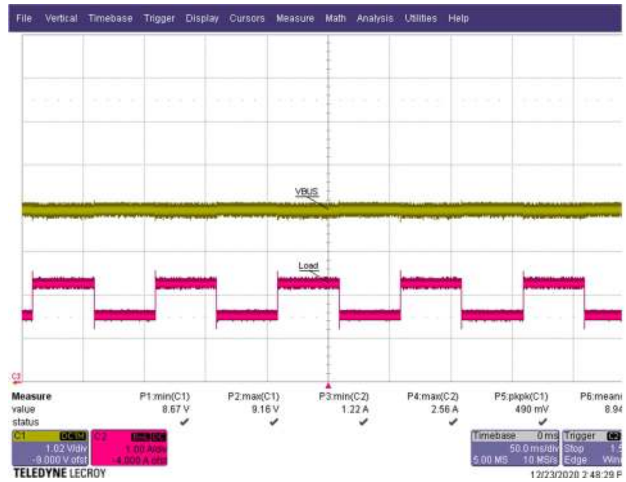


Figure 115 – Transient Response.
265 VAC, 9.0 V, 50% to 75% Load.
V_{OUT} = 9.16 V max., 8.67 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

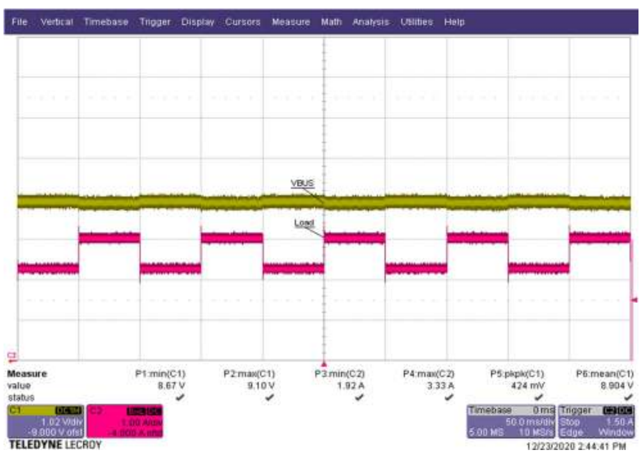


Figure 116 – Transient Response.
90 VAC, 9.0 V, 75% to 100% Load.
V_{OUT} = 9.10 V max., 8.67 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

Figure 117 – Transient Response.
265 VAC, 9.0 V, 75% to 100% Load.
V_{OUT} = 9.13 V max., 8.67 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

13.6.3 Output: 12 V / 2A

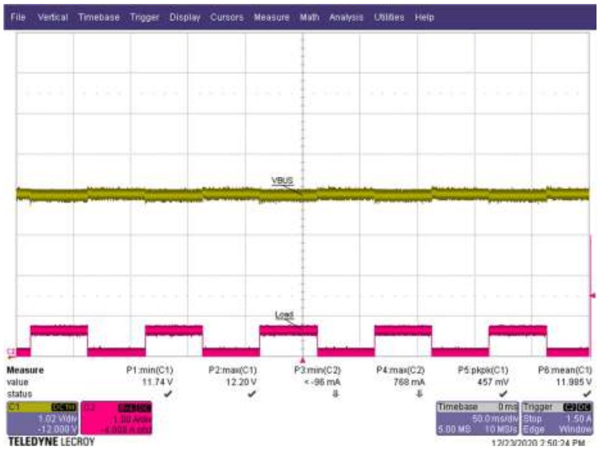


Figure 118 – Transient Response.
90 VAC, 12.0 V, 0 to 25% Load.
VOUT = 12.20 V max., 11.74 V min. CH1: VOUT, 1.02 V / div.
CH2: IOUT, 1 A / div.
Time: 50 ms / div.

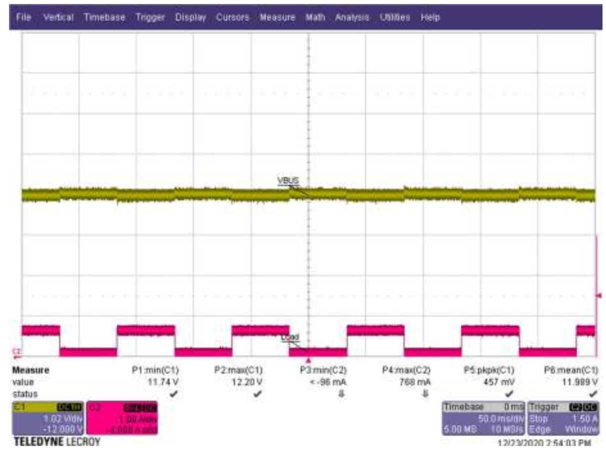


Figure 119 – Transient Response.
265 VAC, 12.0 V, 0 to 25% Load.
VOUT = 12.20 V max., 11.74 V min. CH1: VOUT, 1.02 V / div.
CH2: IOUT, 1 A / div.
Time: 50 ms / div.

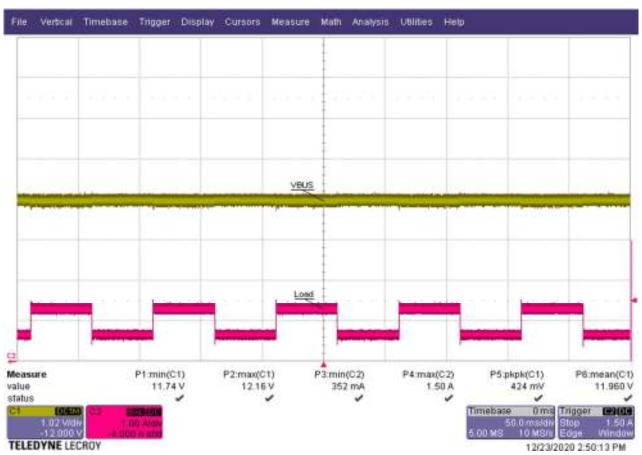


Figure 120 – Transient Response.
90 VAC, 12.0 V, 25% to 50% Load.
VOUT = 12.16 V max., 11.74 V min.
CH1: VOUT, 1.02 V / div.
CH2: IOUT, 1 A / div.
Time: 50 ms / div.

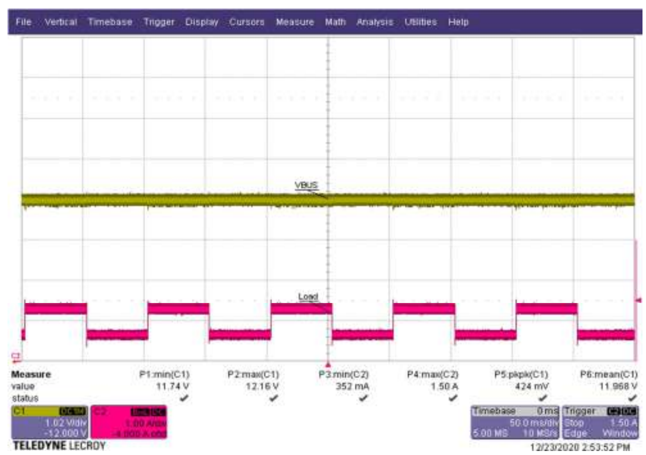


Figure 121 – Transient Response.
265 VAC, 12.0 V, 25% to 50% Load.
VOUT = 12.16 V max., 11.74 V min.
CH1: VOUT, 1.02 V / div.
CH2: IOUT, 1 A / div.
Time: 50 ms / div.

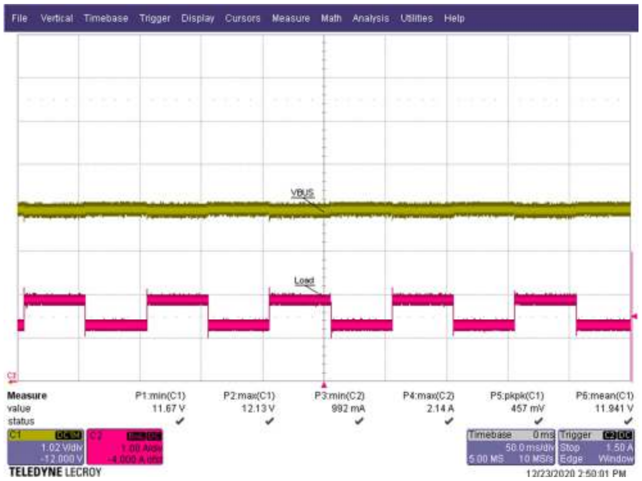


Figure 122 – Transient Response.
90 VAC, 12.0 V, 50 to 75% Load.
V_{OUT} = 12.13 V max., 11.67 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

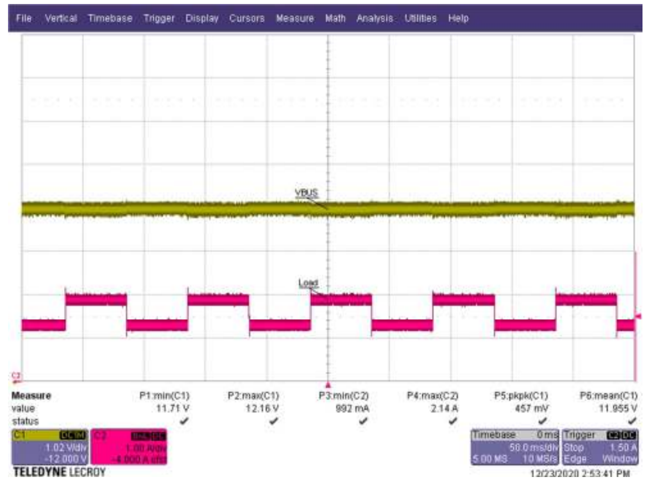


Figure 123 – Transient Response.
265 VAC, 12.0 V, 50 to 75% Load.
V_{OUT} = 12.16 V max., 11.71 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

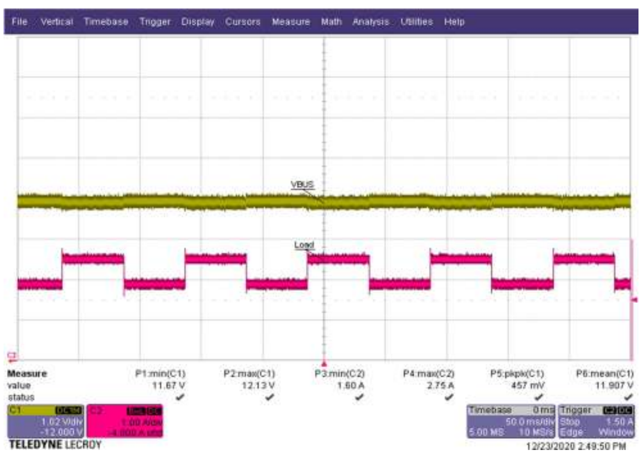


Figure 124 – Transient Response.
90 VAC, 12.0 V, 75% to 100% Load.
V_{OUT} = 12.13 V max., 11.67 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

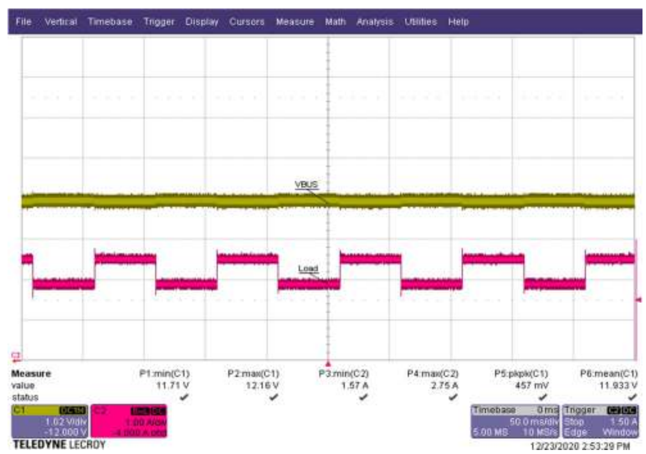


Figure 125 – Transient Response.
265 VAC, 12.0 V, 75% to 100% Load.
V_{OUT} = 12.16 V max., 11.71 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

13.6.4 Output: 15 V / 2 A

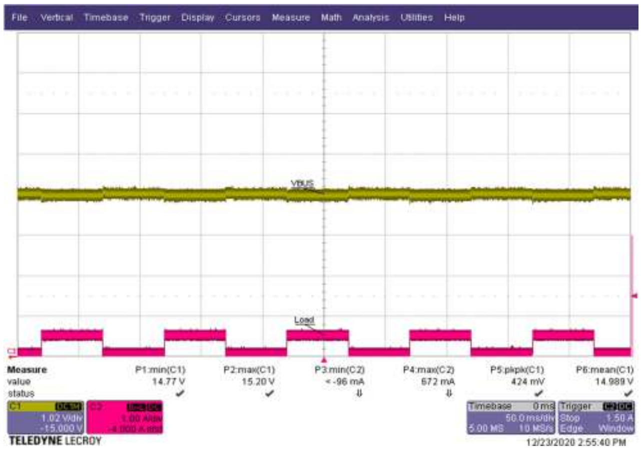


Figure 126 – Transient Response.
90 VAC, 15.0 V, 0 to 25% Load.
V_{OUT} = 15.20 V max., 14.77 V min. CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

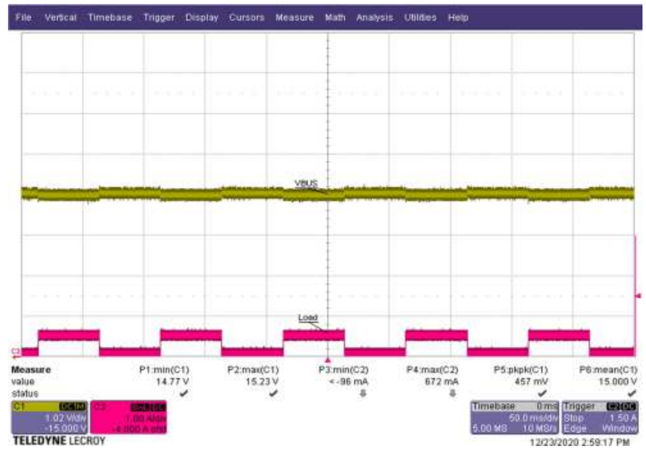


Figure 127 – Transient Response.
265 VAC, 15.0 V, 0 to 25% Load.
V_{OUT} = 15.23 V max., 14.77 V min. CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

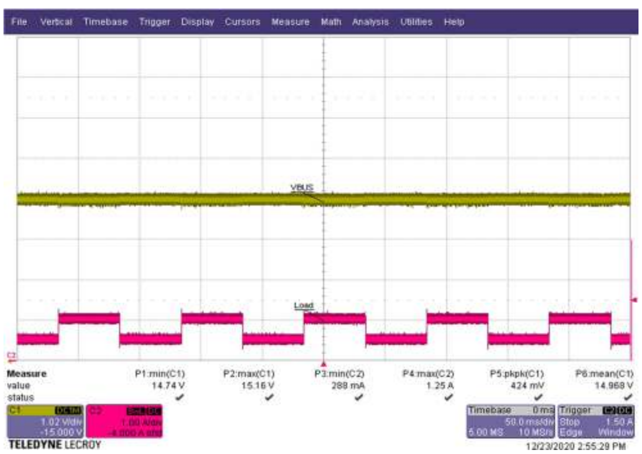


Figure 128 – Transient Response.
90 VAC, 15.0 V, 25% to 50% Load.
V_{OUT} = 15.16 V max., 14.74 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

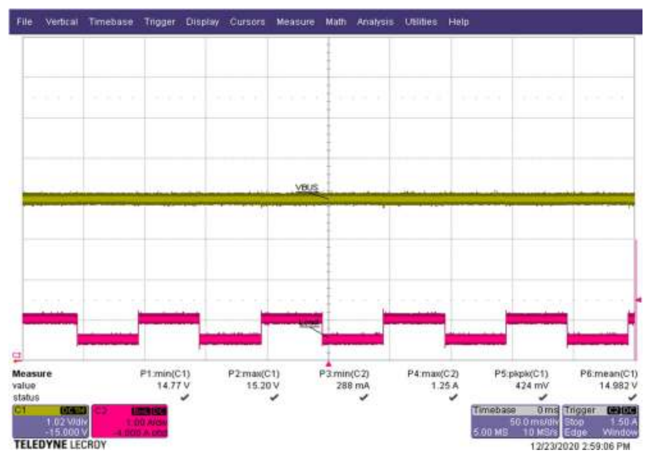


Figure 129 – Transient Response.
265 VAC, 15.0 V, 25% to 50% Load.
V_{OUT} = 15.20 V max., 14.77 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

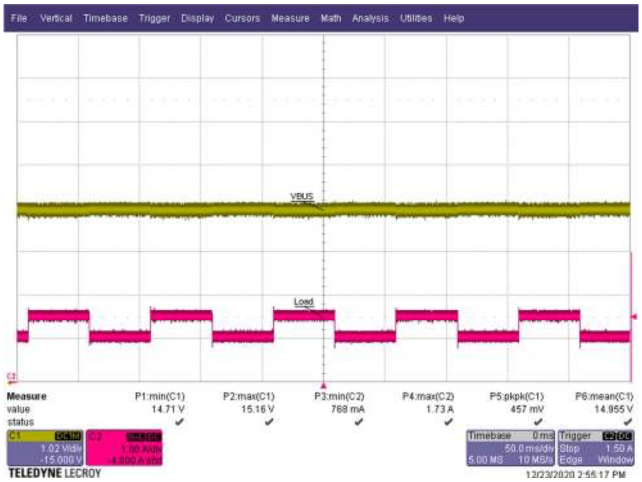


Figure 130 – Transient Response.
90 VAC, 15.0 V, 50% to 75% Load.
V_{OUT} = 15.16 V max., 14.71 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

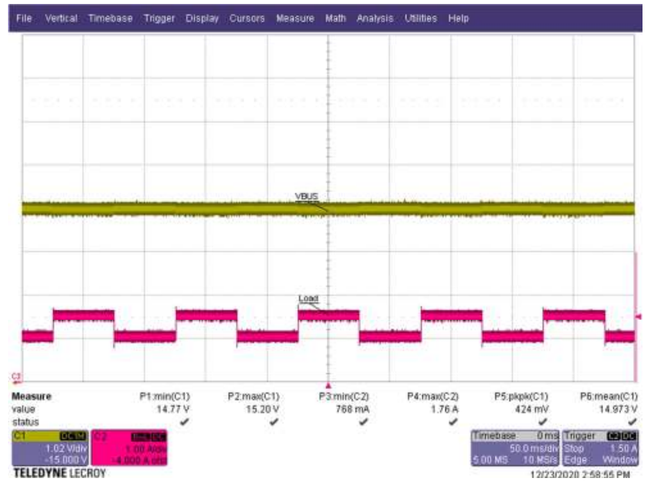


Figure 131 – Transient Response.
265 VAC, 15.0 V, 50% to 75% Load.
V_{OUT} = 15.20 V max., 14.77 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

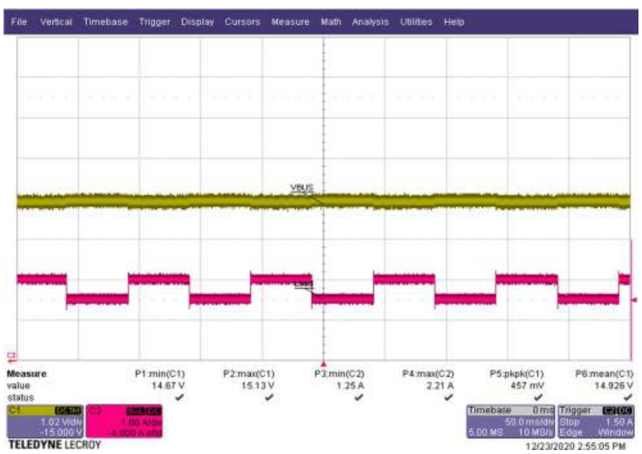


Figure 132 – Transient Response.
90 VAC, 15.0 V, 75% to 100% Load.
V_{OUT} = 15.13 V max., 14.67 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

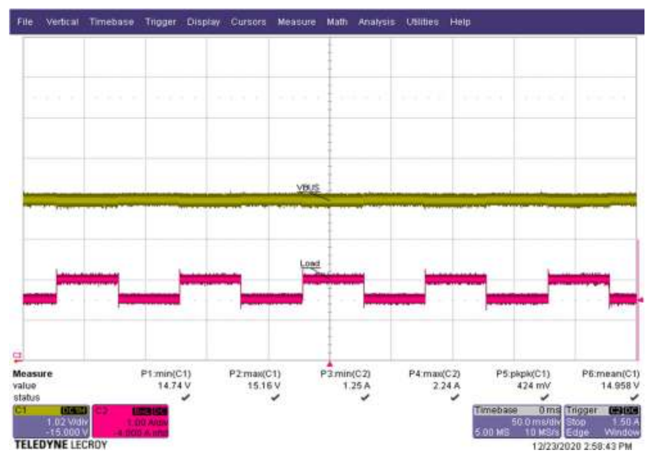


Figure 133 – Transient Response.
265 VAC, 15.0 V, 75% to 100% Load.
V_{OUT} = 15.16 V max., 14.74 V min.
CH1: V_{OUT}, 1.02V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

13.6.5 Output: 20 V / 1.5 A

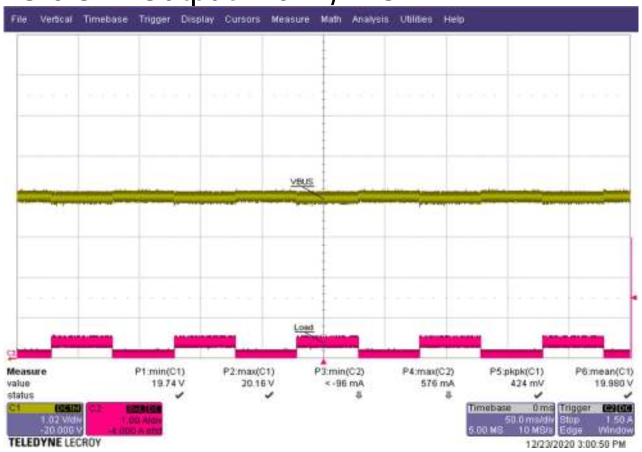


Figure 134 – Transient Response.
90 VAC, 20.0 V, 0 to 25% Load.
V_{OUT} = 20.16 V max., 19.74 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

Figure 135 – Transient Response.
265 VAC, 20.0 V, 0 to 25% Load.
V_{OUT} = 20.20 V max., 19.80 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

Figure 136 – Transient Response.
90 VAC, 20.0 V, 25% to 50% Load.
V_{OUT} = 20.16V max., 19.74 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

Figure 137 – Transient Response.
265 VAC, 20.0 V, 25% to 50% Load.
V_{OUT} = 20.16 V max., 19.80 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

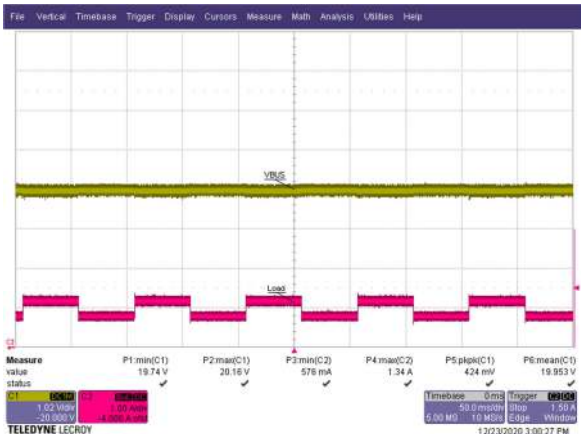


Figure 138 – Transient Response.
90 VAC, 20.0 V, 50% to 75% Load.
V_{OUT} = 20.16 V max., 19.74 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

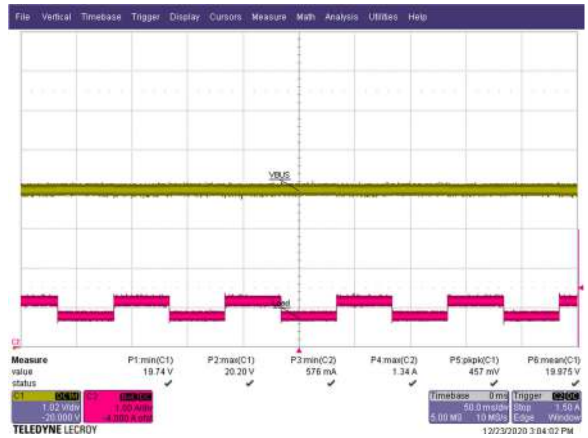


Figure 139 – Transient Response.
265 VAC, 20.0 V, 50% to 75% Load.
V_{OUT} = 20.20 V max., 19.74 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

Figure 140 – Transient Response.
90 VAC, 20.0 V, 75% to 100% Load.
V_{OUT} = 20.13 V max., 19.71 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

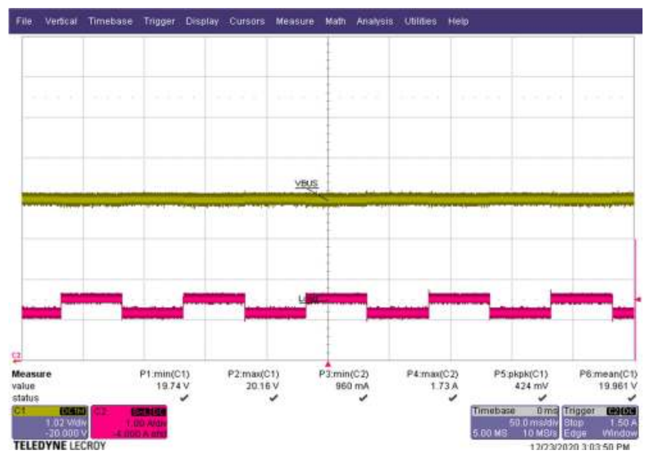


Figure 141 – Transient Response.
265 VAC, 20.0 V, 75% to 100% Load.
V_{OUT} = 20.16 V max., 19.74 V min.
CH1: V_{OUT}, 1.02 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 50 ms / div.

13.7 *Output Voltage Ripple Waveforms*

Note: 1. Output voltage waveforms captured at the end of 96 mΩ cable using the ripple measurement probe with decoupling capacitors.

Output: 5 V / 3 A

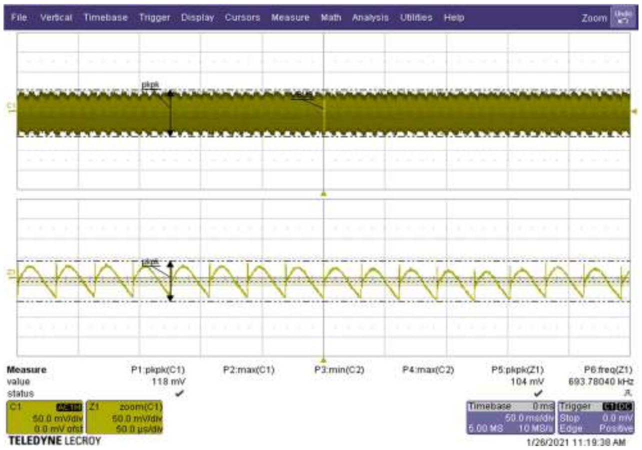


Figure 142 – Output Voltage Ripple.
90 VAC, 5.0 V, 3 A Load.
$V_{OUT(AC)}$ = 118 mV peak-to-peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 50 ms / div. (50 µs / div. Zoom)

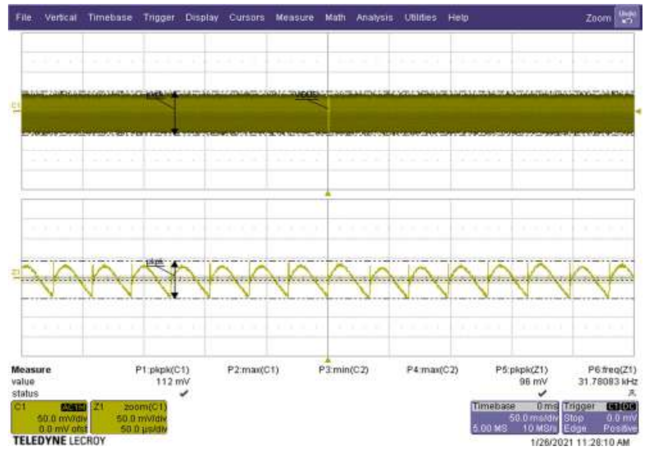


Figure 143 – Output Voltage Ripple.
265 VAC, 5.0 V, 3 A Load.
$V_{OUT(AC)}$ = 112 mV peak-to-peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 50 ms / div. (50 µs / div. Zoom)

13.7.1 Output: 9 V / 3 A

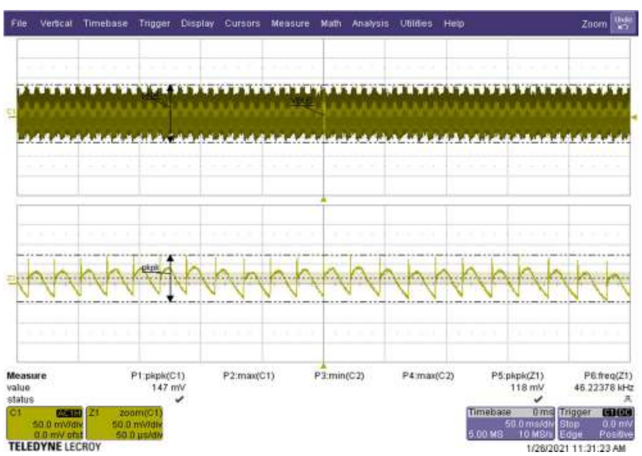


Figure 144 – Output Voltage Ripple.
90 VAC, 9.0 V, 3 A Load.
$V_{OUT(AC)}$ = 147 mV peak-to-peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 50 ms / div. (50 µs / div. Zoom)

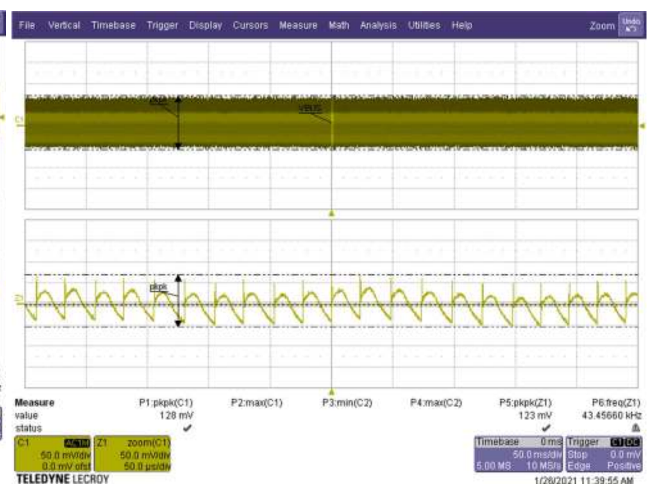


Figure 145 – Output Voltage Ripple.
265 VAC, 9.0 V, 3 A Load.
$V_{OUT(AC)}$ = 128 mV peak-to-peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 50 ms / div. (50 µs / div. Zoom)

13.7.2 Output: 12 V / 2.5 A

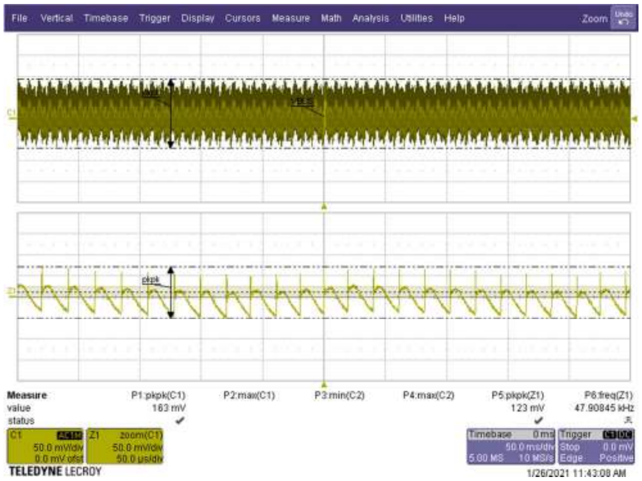


Figure 146 – Output Voltage Ripple.
90 VAC, 15.0 V, 2 A Load.
$V_{OUT(AC)}$ = 163 mV peak-to-peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 50 ms / div. (50 µs / div. Zoom)

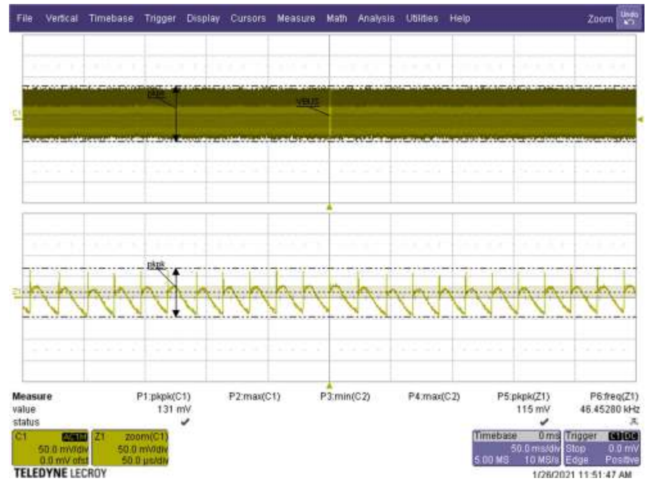


Figure 147 – Output Voltage Ripple.
265 VAC, 15.0 V, 2 A Load.
$V_{OUT(AC)}$ = 131 mV peak-to-peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 50 ms / div. (50 µs / div. Zoom)

13.7.3 Output: 15 V / 2 A

Figure 148 – Output Voltage Ripple.
90 VAC, 15.0 V, 2 A Load.
$V_{OUT(AC)}$ = 170 mV peak-to-peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 50 ms / div. (50 µs / div. Zoom)

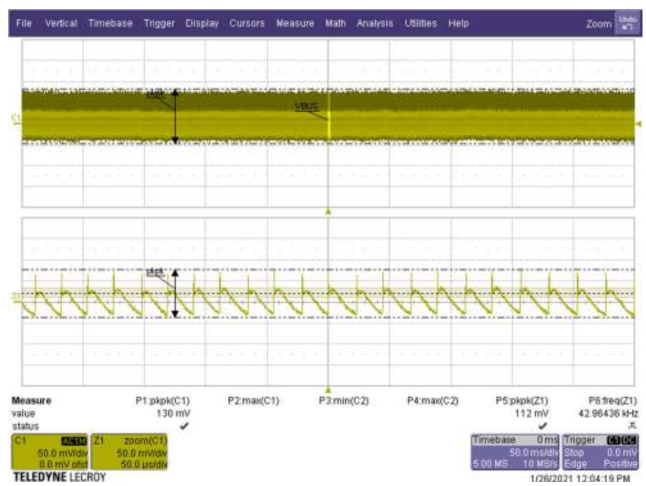


Figure 149 – Output Voltage Ripple.
265 VAC, 15.0 V, 2 A Load.
$V_{OUT(AC)}$ = 130 mV peak-to-peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 50 ms / div. (50 µs / div. Zoom)

13.7.4 Output: 20 V / 1.5 A

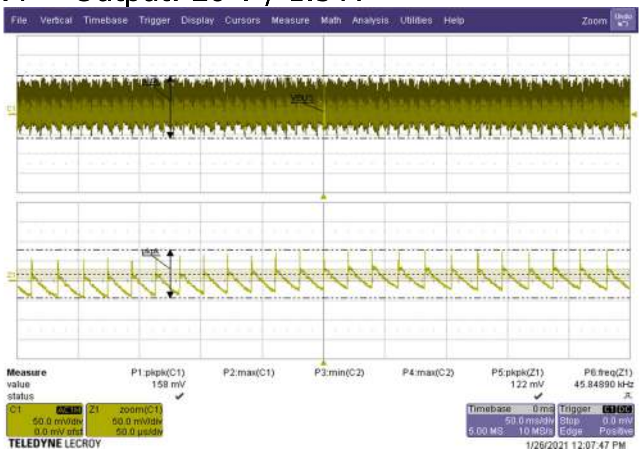


Figure 150 – Output Voltage Ripple.
90 VAC, 20.0 V, 1.5 A Load.
$V_{OUT(AC)}$ = 158 mV peak-to-peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 50 ms / div. (50 µs / div. Zoom)

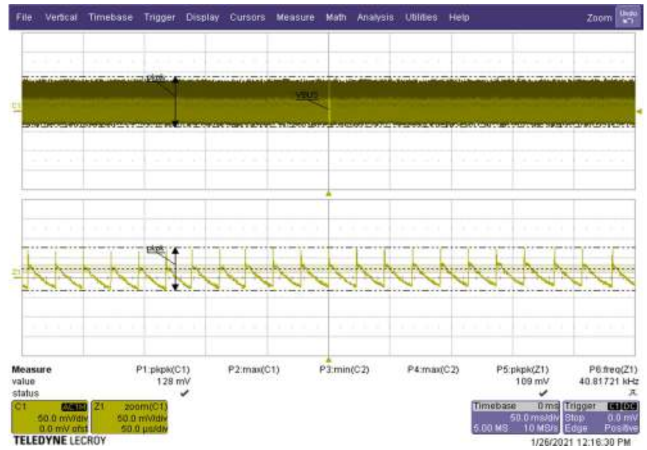


Figure 151 – Output Voltage Ripple.
265 VAC, 20.0 V, 1.5 A Load.
$V_{OUT(AC)}$ = 128 mV peak-to-peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 50 ms / div. (50 µs / div. Zoom)

13.8 ***Output Voltage Ripple Amplitude vs. Load (End of Cable)***

13.8.1 Output: 5 V / 3 A

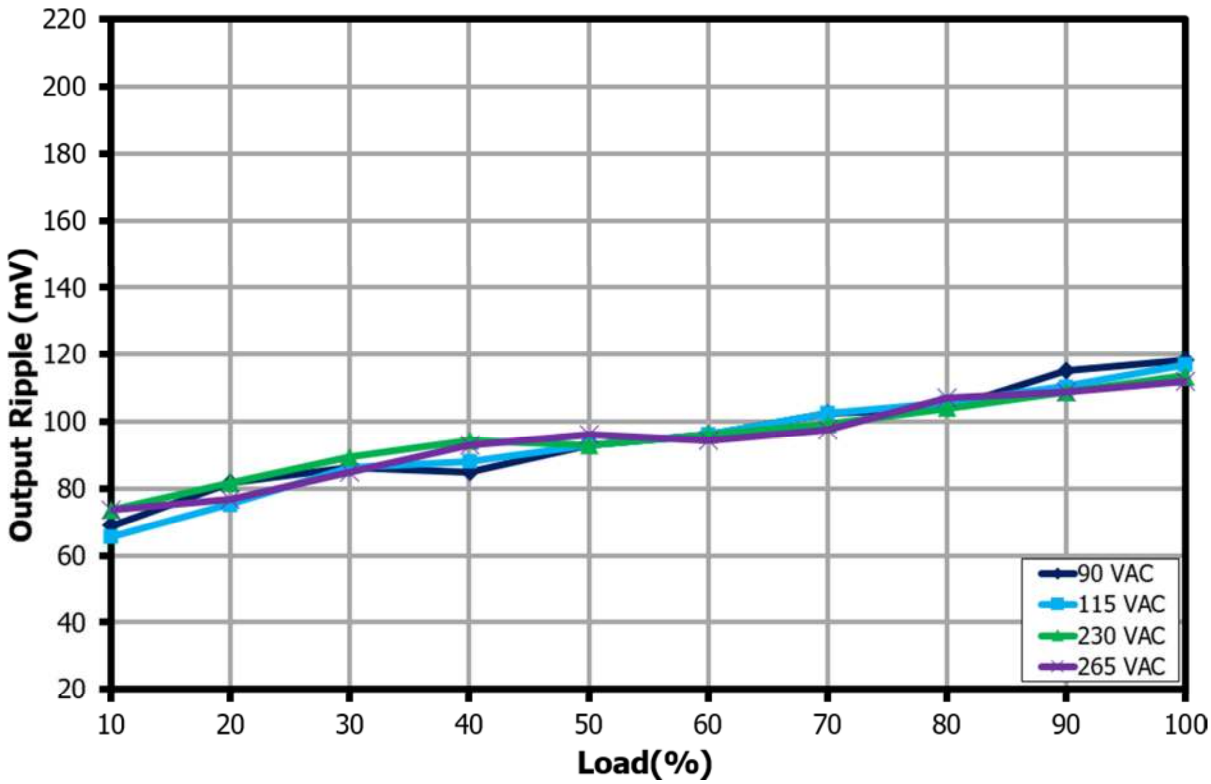


Figure 152 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 5 V Output.

13.8.2 Output: 9 V / 3 A

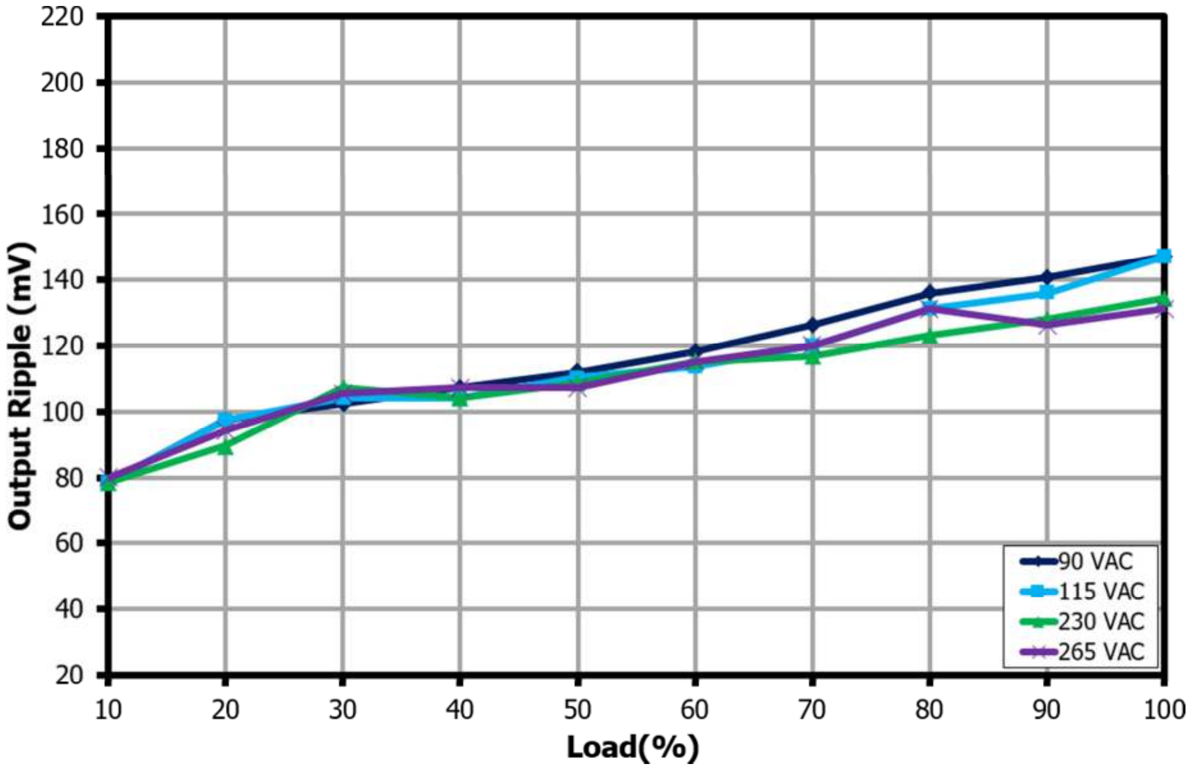


Figure 153 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 9 V Output.

13.8.3 Output: 12 V / 2.5A

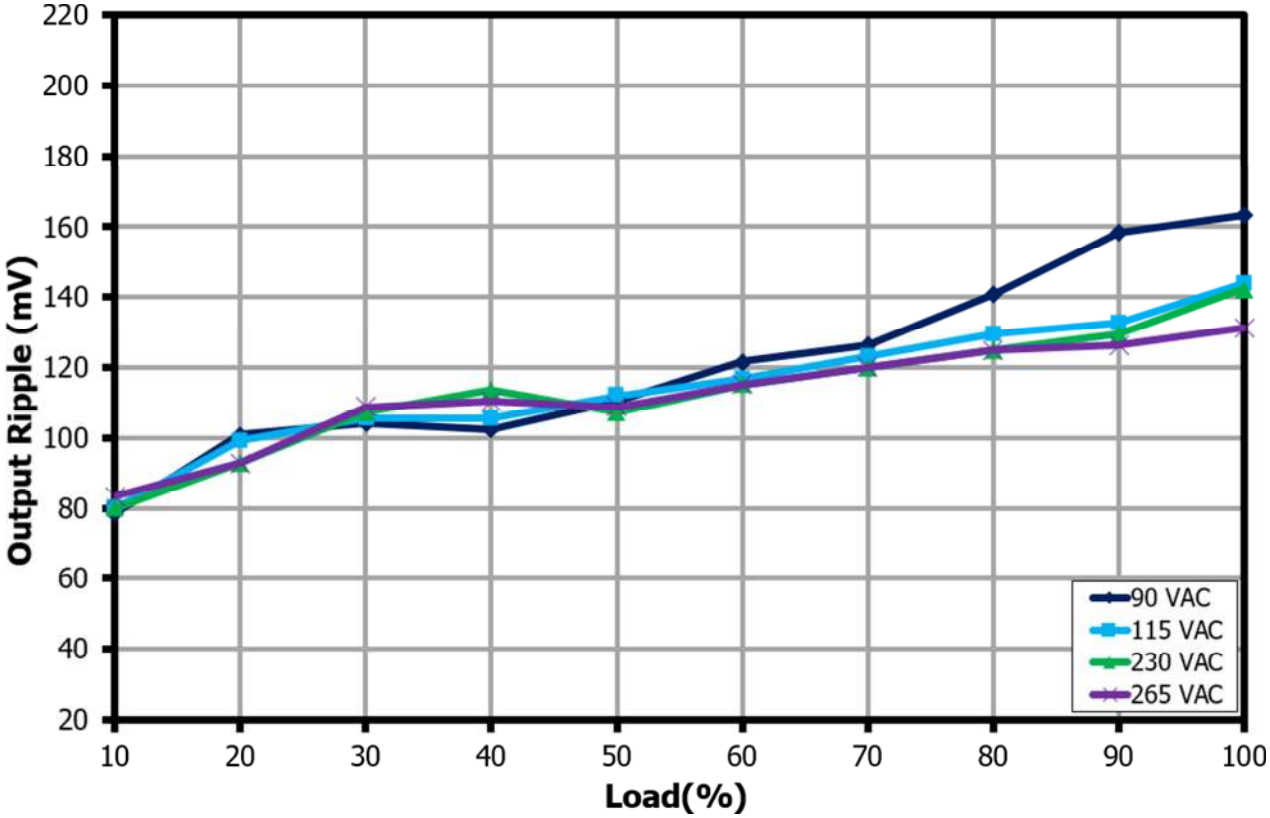


Figure 154 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 12 V Output.

13.8.4 Output: 15 V / 2 A

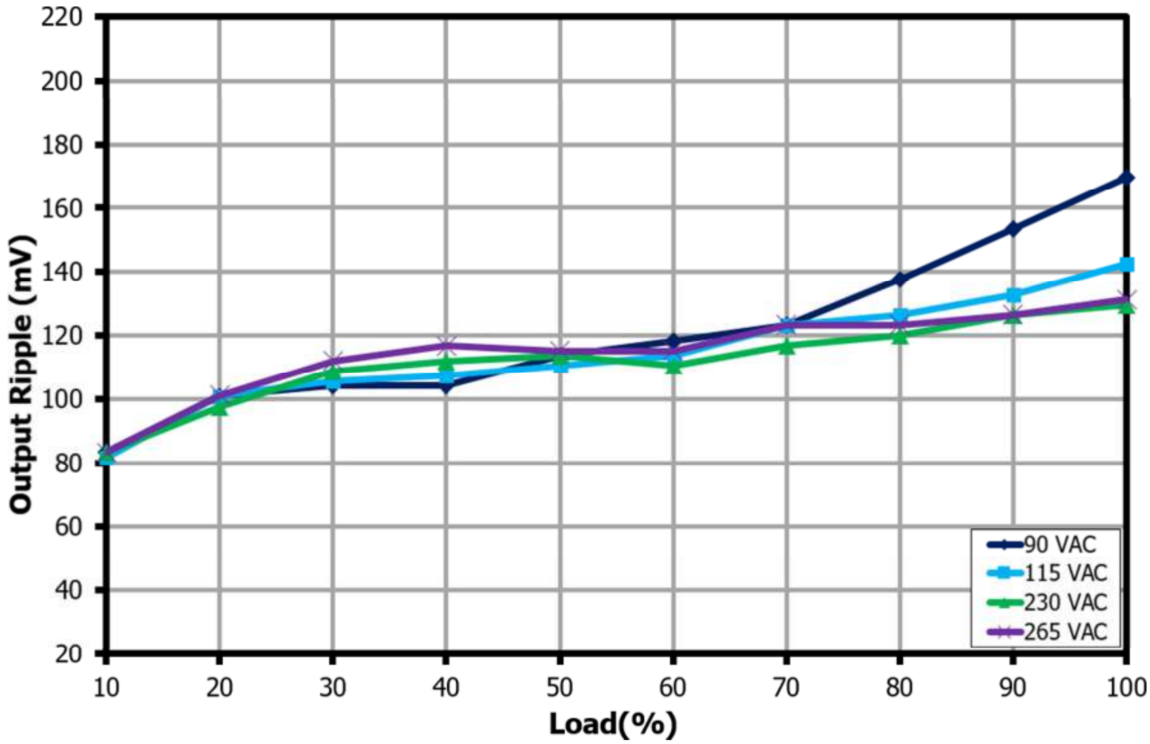


Figure 155 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 15 V Output.

13.8.5 Output: 20 V / 1.5 A

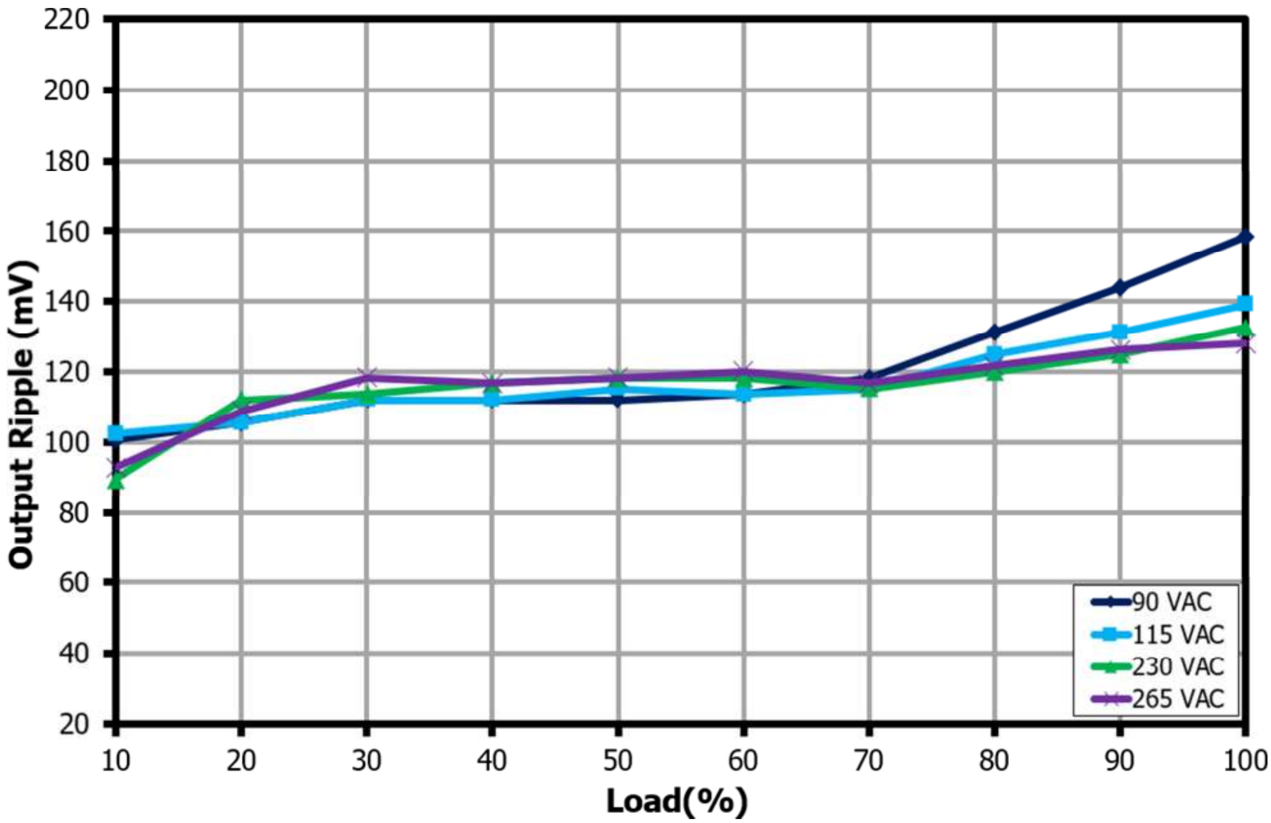


Figure 156 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 20 V Output.

14 CV/CC Profile

Note: 1. Two Programmable Power Supply (PPS) Augmented Power Data Objects (APDO) are supported in this design:

- PDO6: 3.3 V – 11 V / 3.0 A PPS (30 W power-limited)
- PDO7: 3.3 V – 16 V / 2.0 A PPS

14.1 *Output: 10 V / 3 A PPS Request, PDO6 (30 W Power-Limited)*

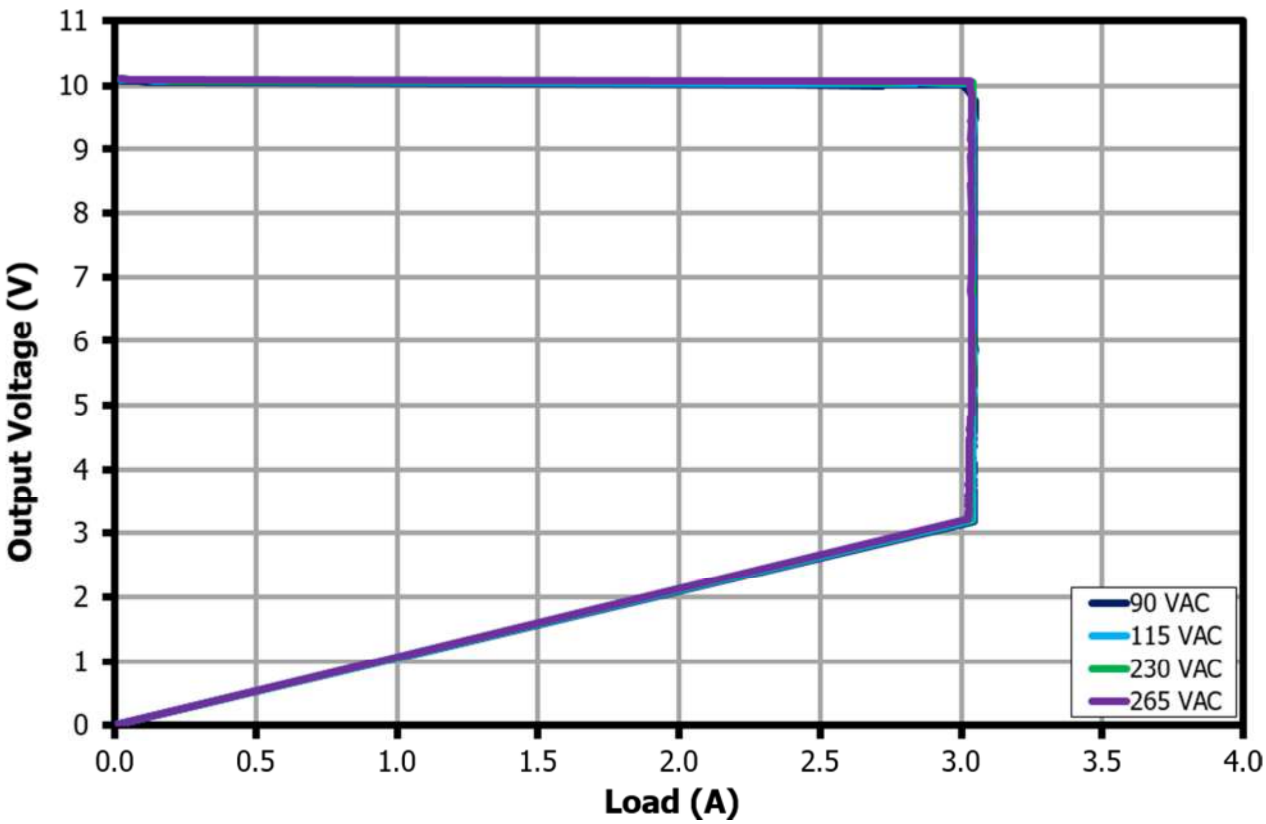


Figure 157 – CV/CC Profile for 10 V / 3 A PPS Request.

14.2 *Output: 11 V / 3 A PPS Request, PDO6 (30 W Power-Limited)*

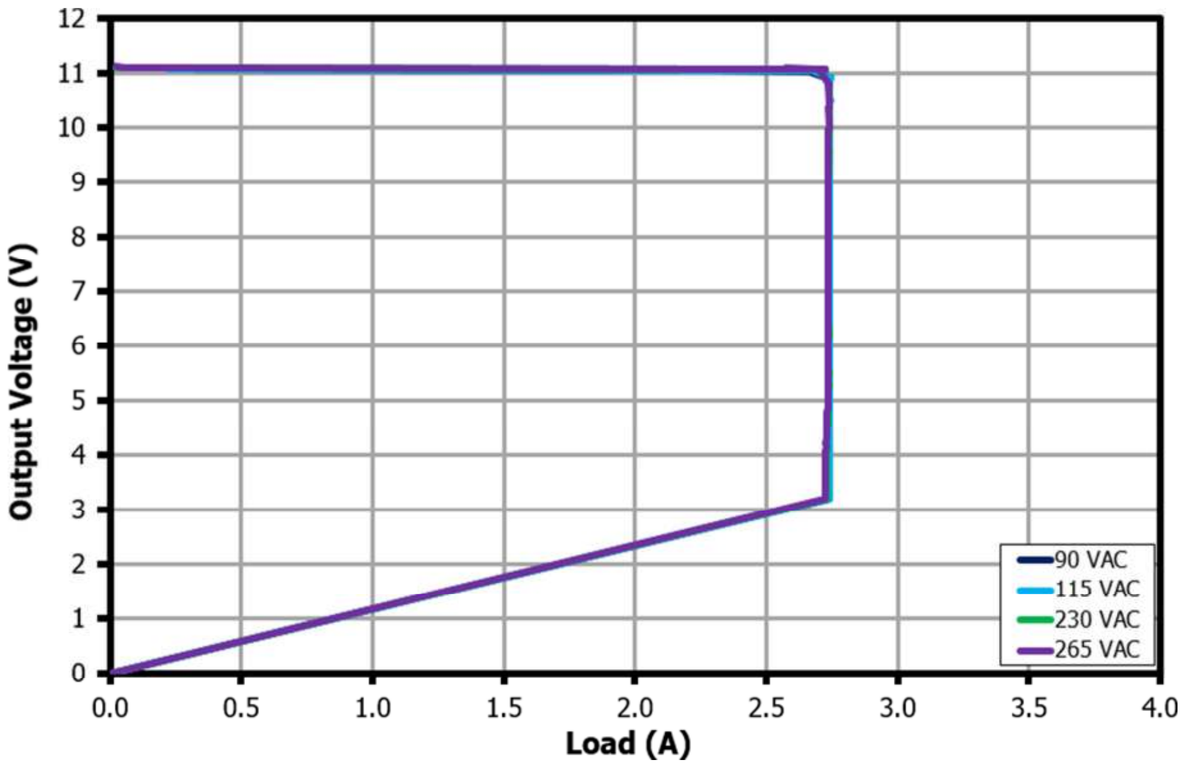


Figure 158 – CV/CC Profile for 11 V / 3 A PPS Request.

14.3 ***Output: 15 V / 2 A PPS Request, PDO7***

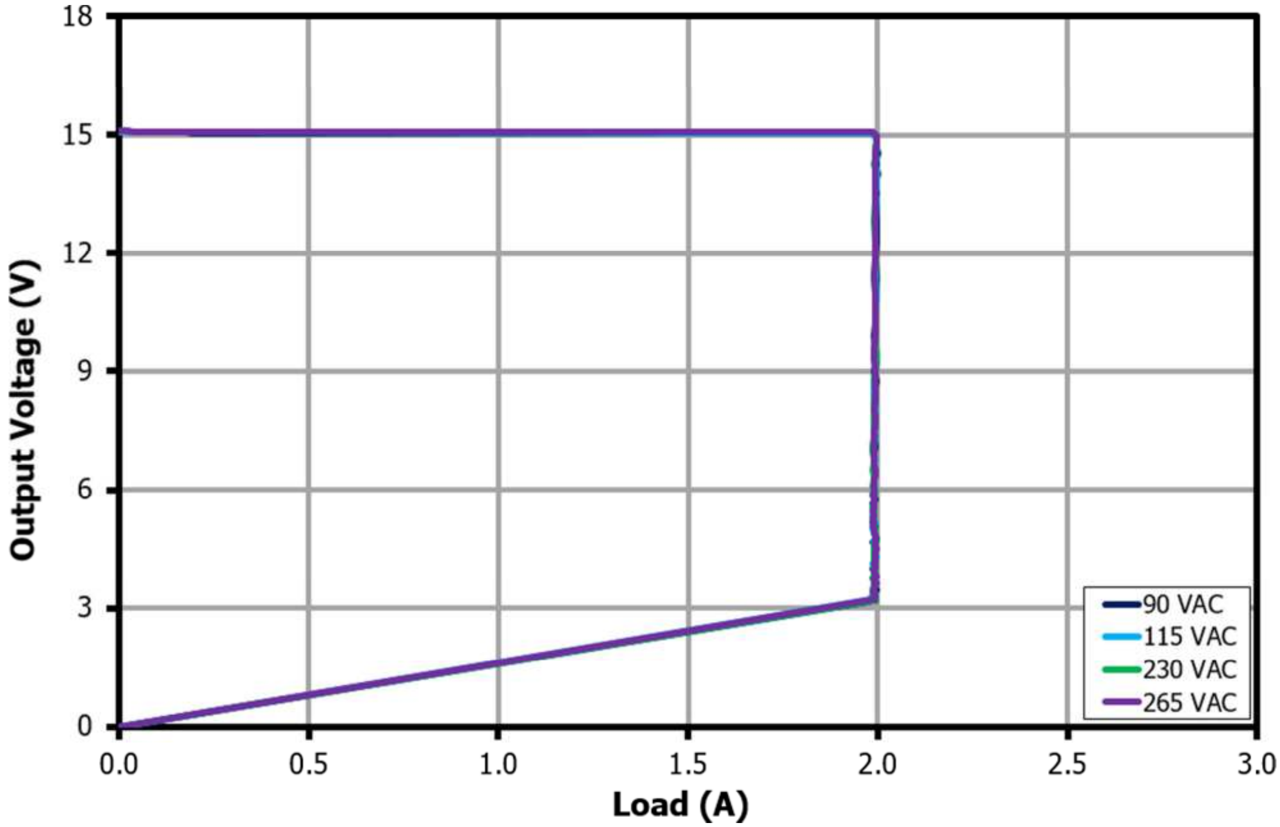


Figure 159 – CV/CC Profile for 15 V / 2 A PPS Request.

14.4 ***Output: 16 V / 2 A PPS Request, PDO7***

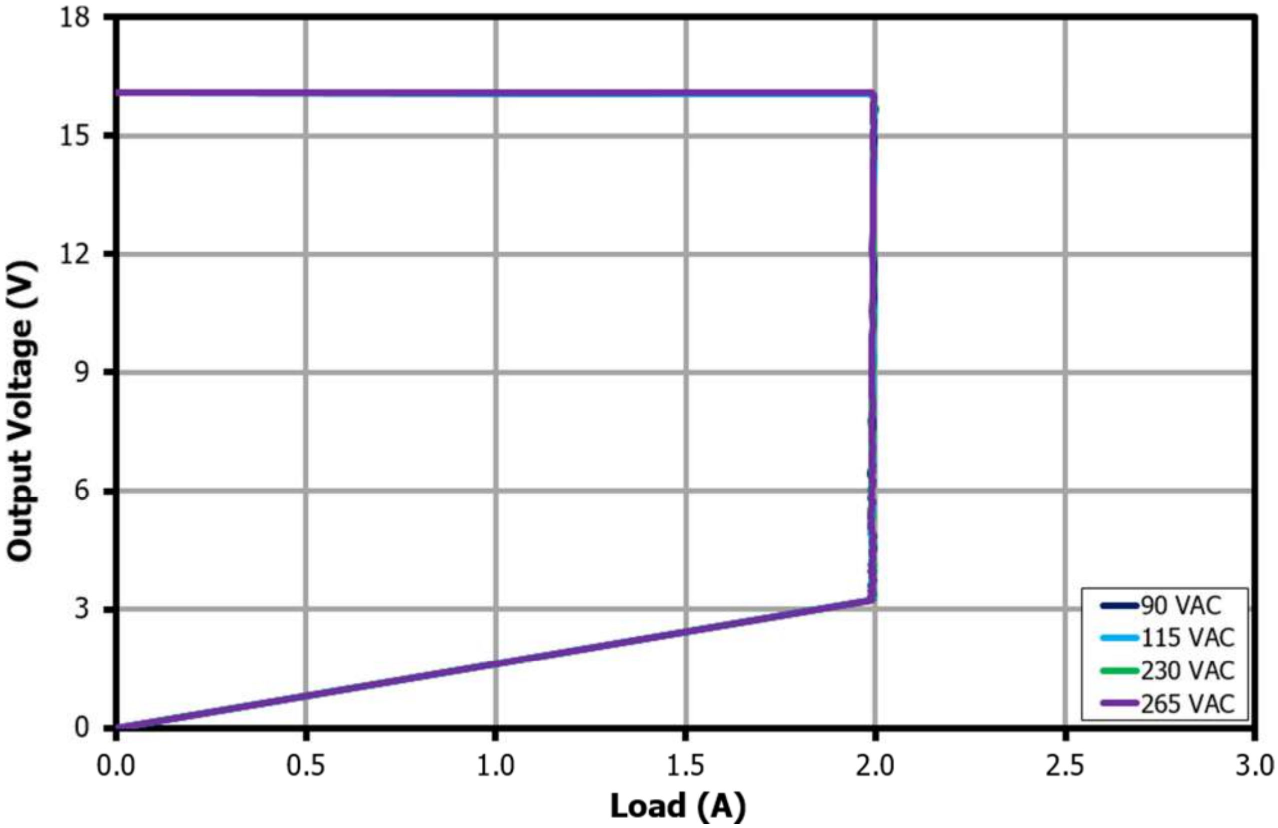


Figure 160 – CV/CC Profile for 16 V / 2 A PPS Request.

15 Voltage Step and Current Limit Test using Quadramax and Total Phase Analyzer

15.1 *Voltage Step Test (VST)*

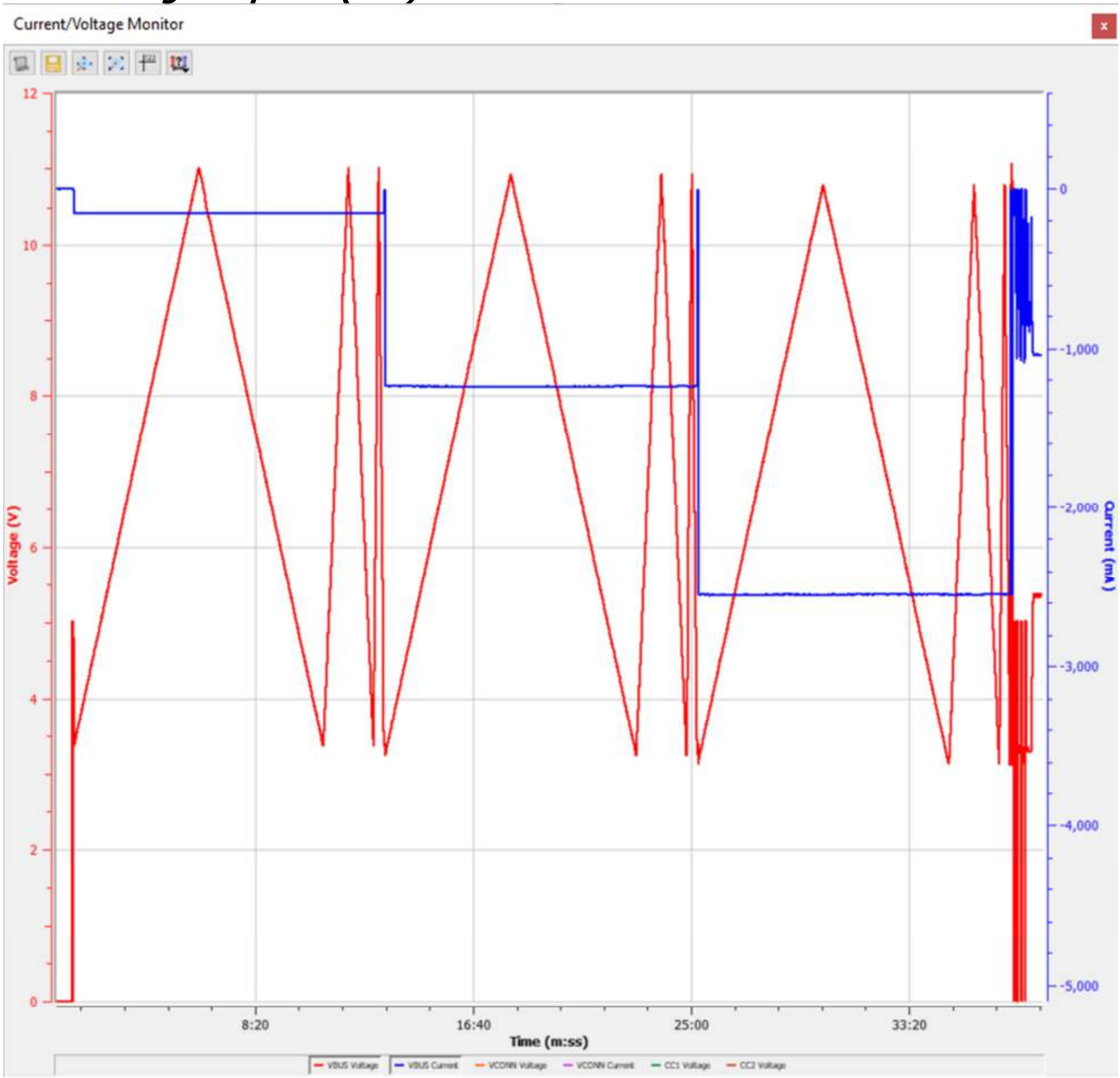


Figure 161 – Plot of SPT.6 VST from Total Phase Analyzer.

15.2 ***Current Limit Test (CLT)***

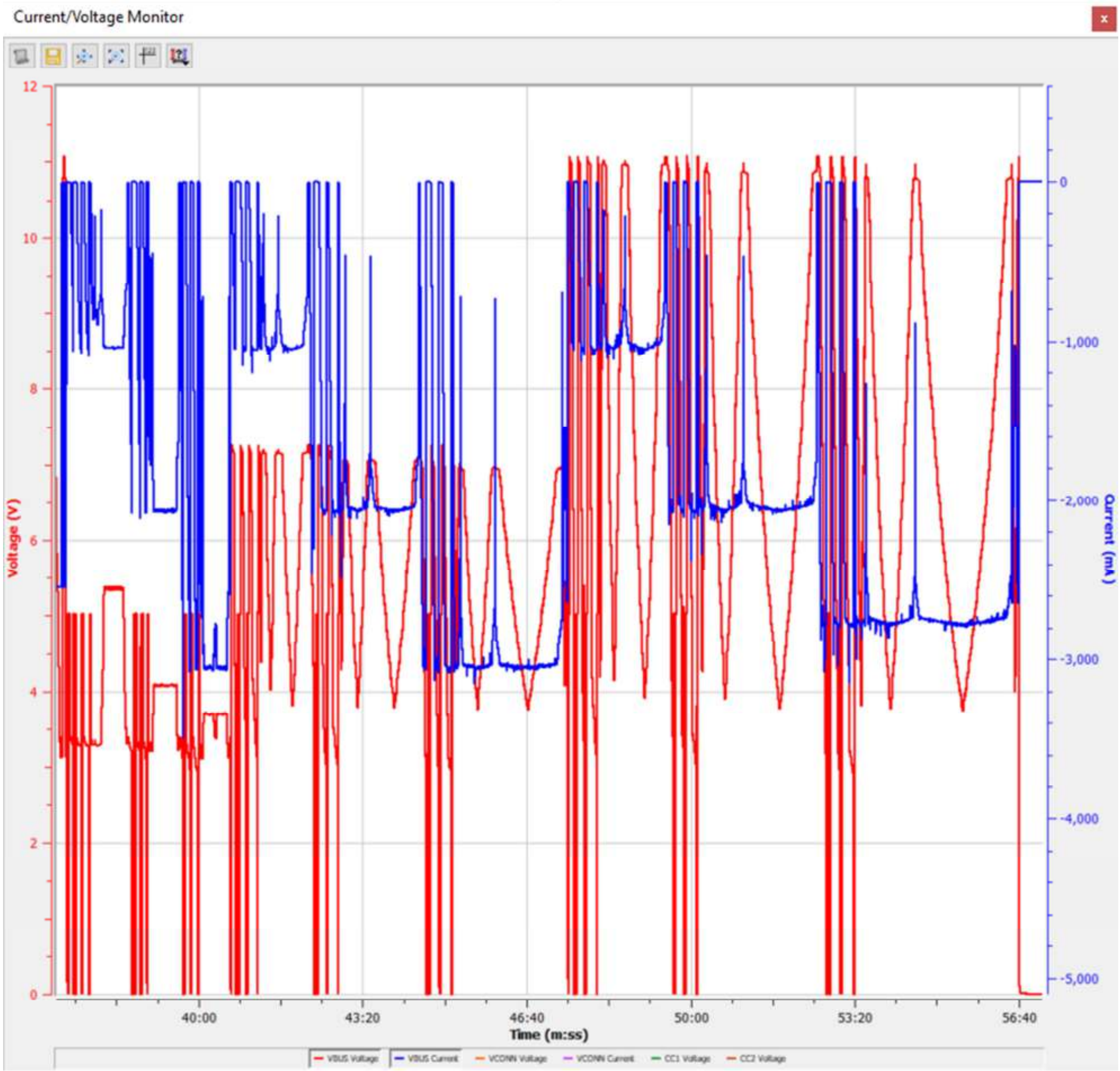
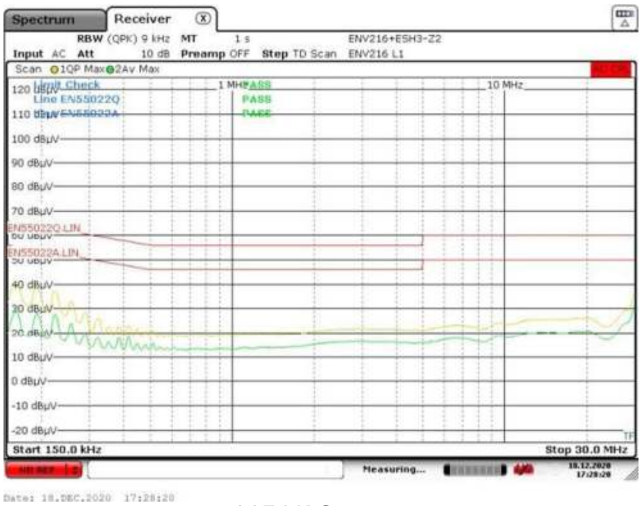


Figure 162 – Plot of SPT.7 CLT from Total Phase Analyzer.

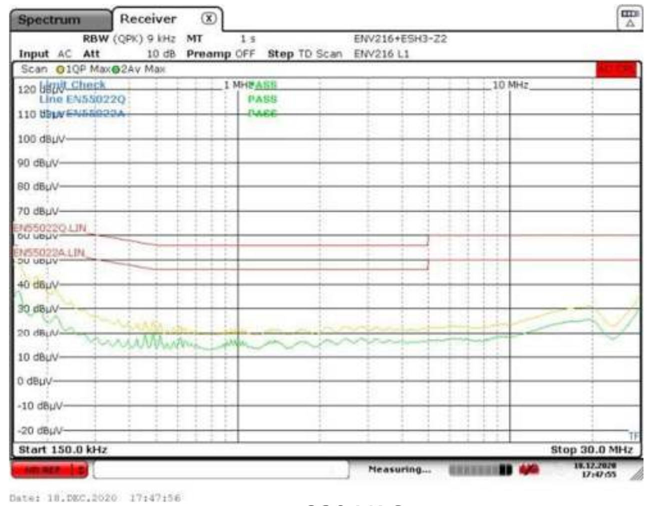
16 Conducted EMI

16.1 ***Floating Ground (QPK / AV)***

16.1.1 Output: 5 V / 3 A

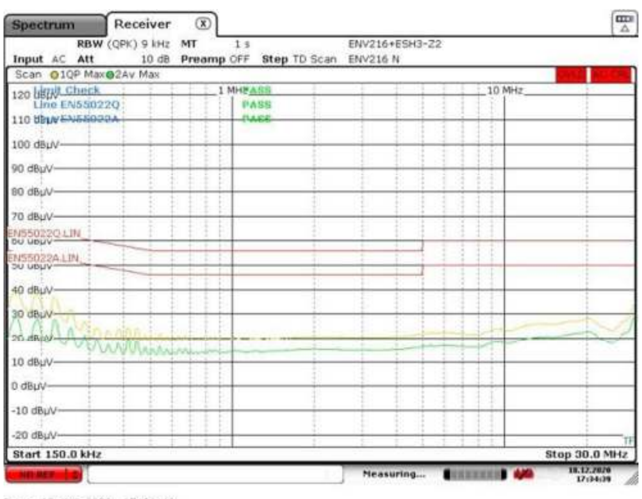


115 VAC.

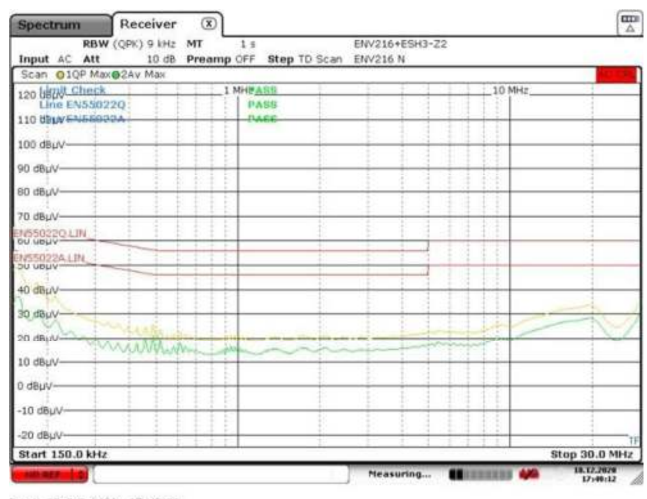


230 VAC.

Figure 163 – Floating Ground EMI, 5 V / 3 A Load [Line Scan].



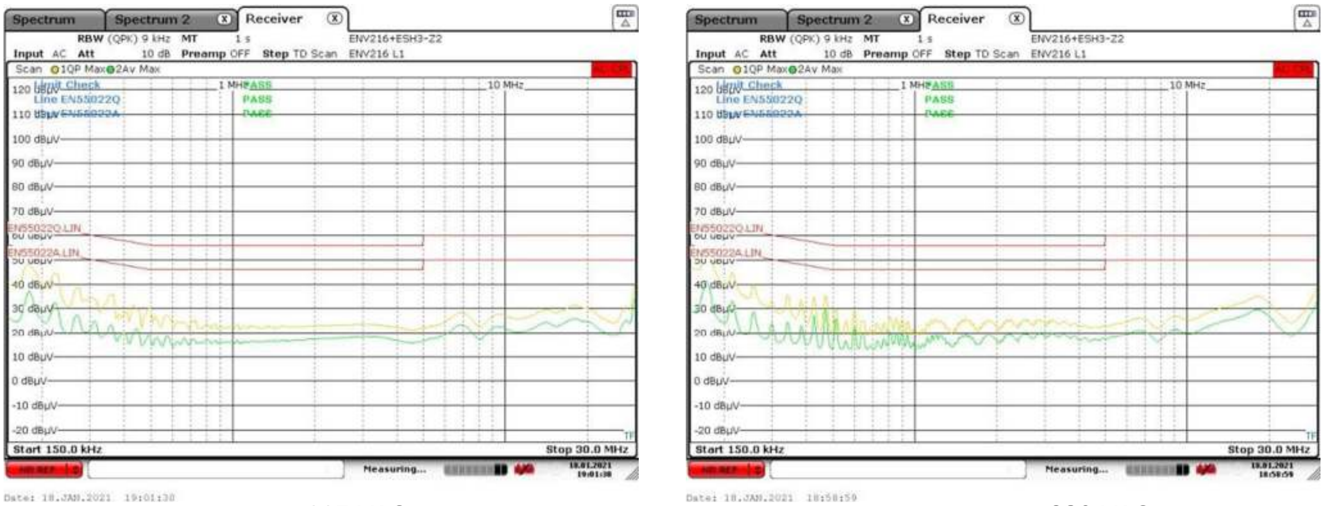
115 VAC.



230 VAC.

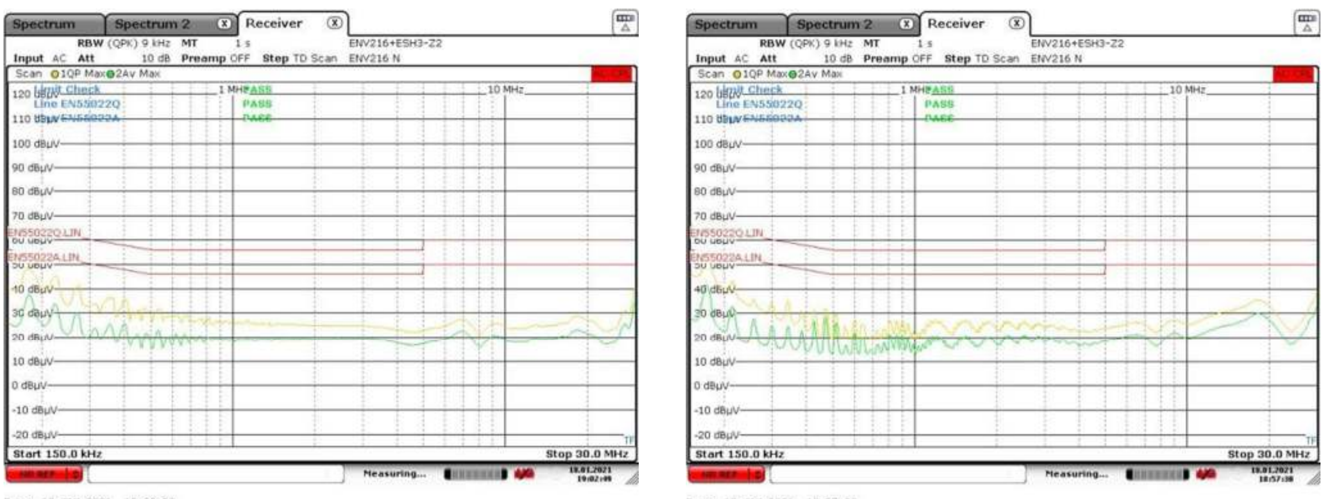
Figure 164 – Floating Ground EMI, 5 V / 3 A Load [Neutral Scan].

16.1.2 Output: 9 V / 3 A



115 VAC. 230 VAC.

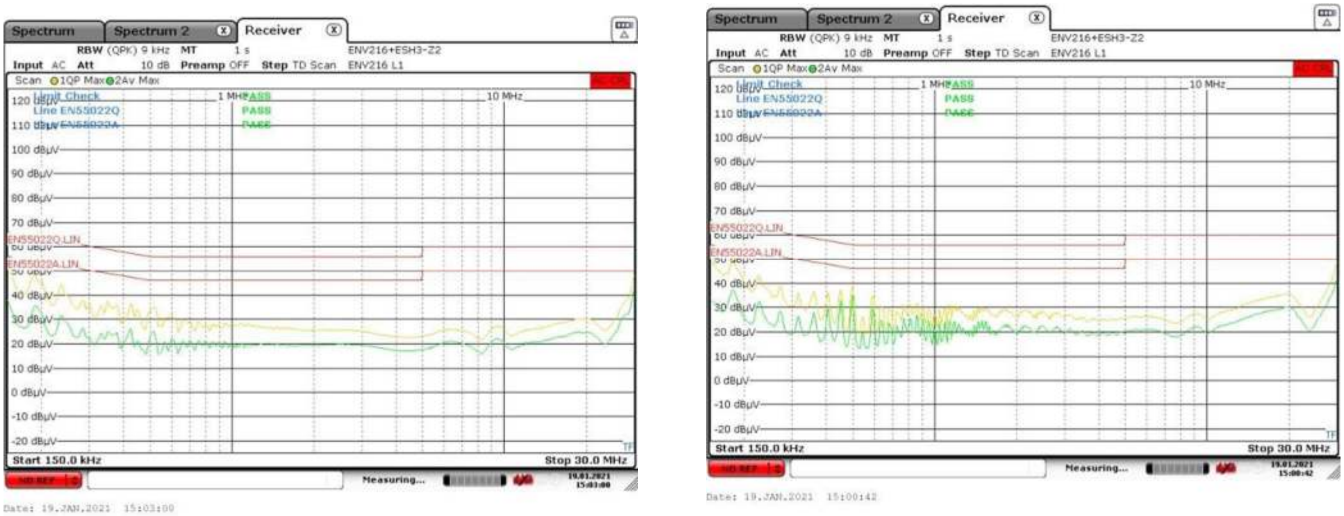
Figure 165 – Floating Ground EMI, 9 V / 3 A Load [Line Scan].



115 VAC. 230 VAC.

Figure 166 – Floating Ground EMI, 9 V / 3 A Load [Neutral Scan].

16.1.3 Output: 12 V / 2.5 A



115 VAC. 230 VAC.

Figure 167 – Floating Ground EMI, 15 V / 2 A Load [Line Scan].

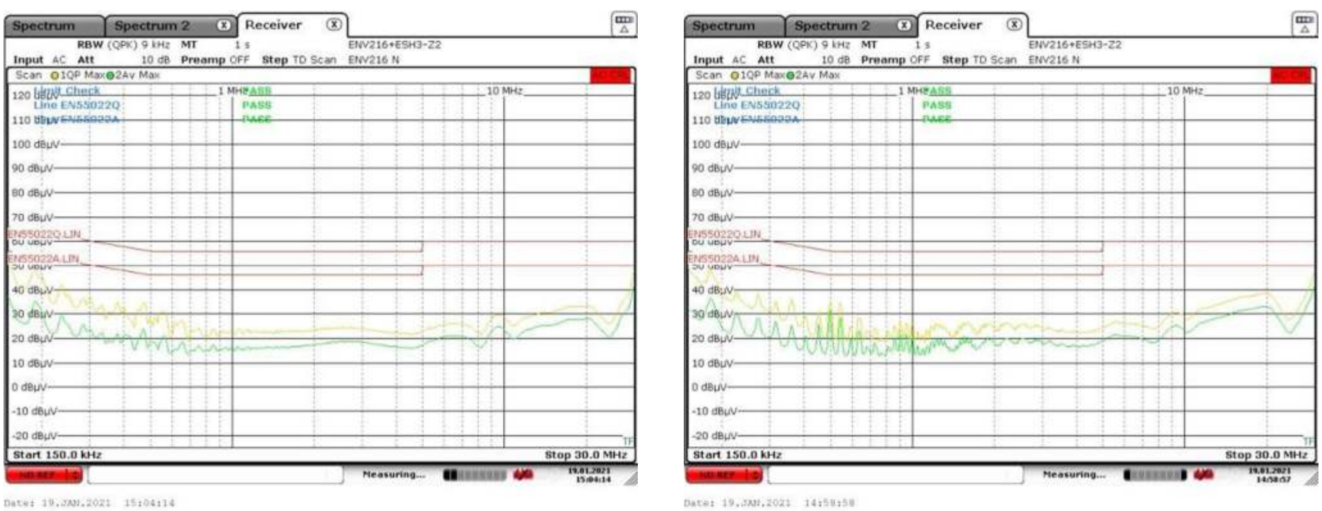
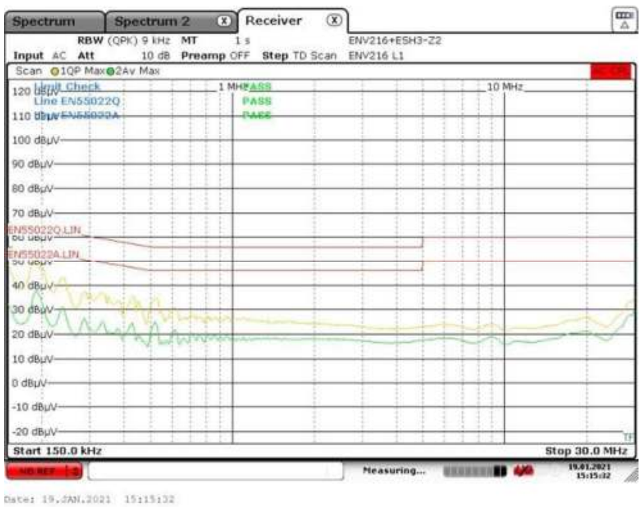
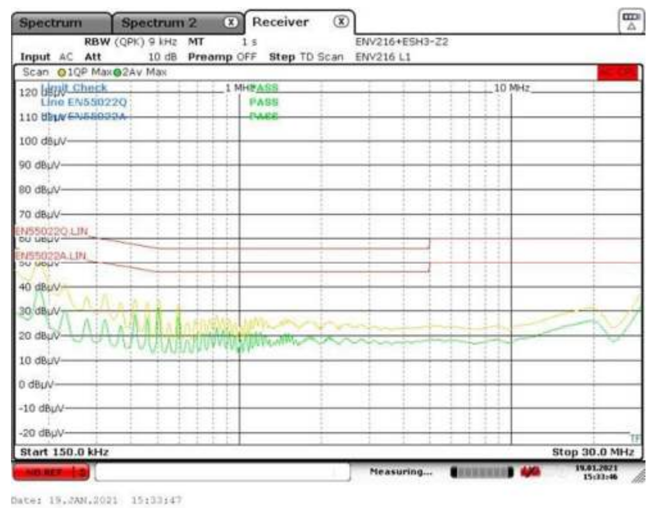


Figure 168 – Floating Ground EMI, 15 V / 2 A Load [Neutral Scan].

16.1.4 Output: 15 V / 2 A

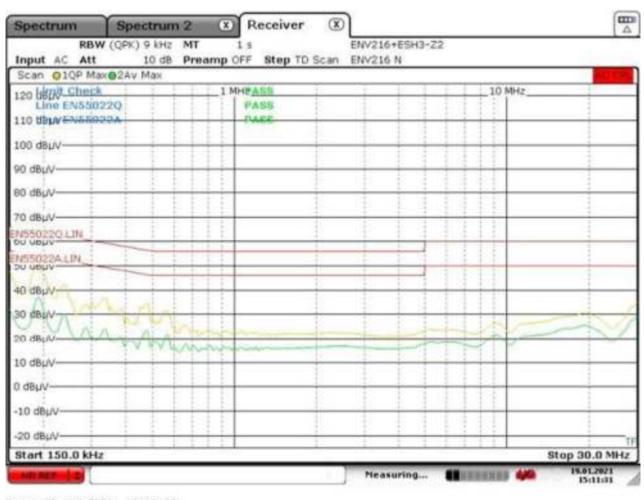


115 VAC.

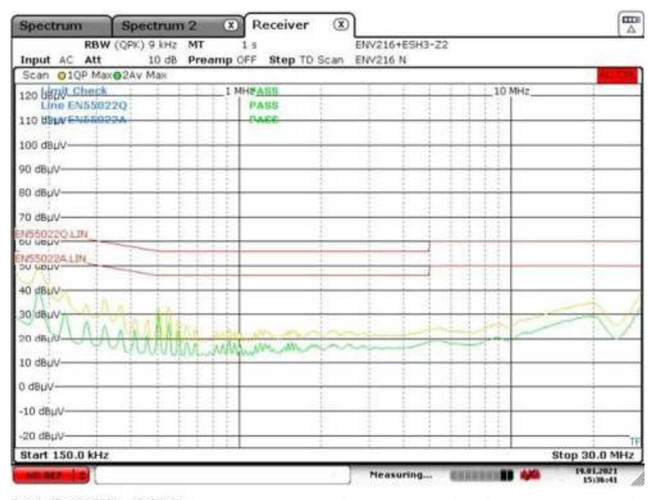


230 VAC.

Figure 169 – Floating Ground EMI, 15 V / 2 A Load [Line Scan].



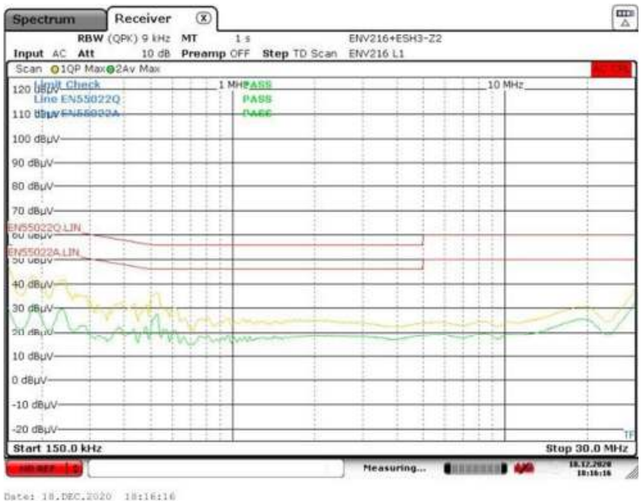
115 VAC.

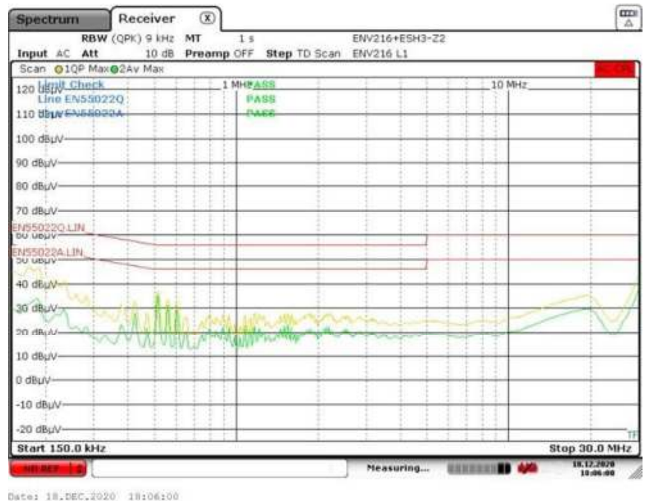


230 VAC.

Figure 170 – Floating Ground EMI, 15 V / 2 A Load [Neutral Scan].

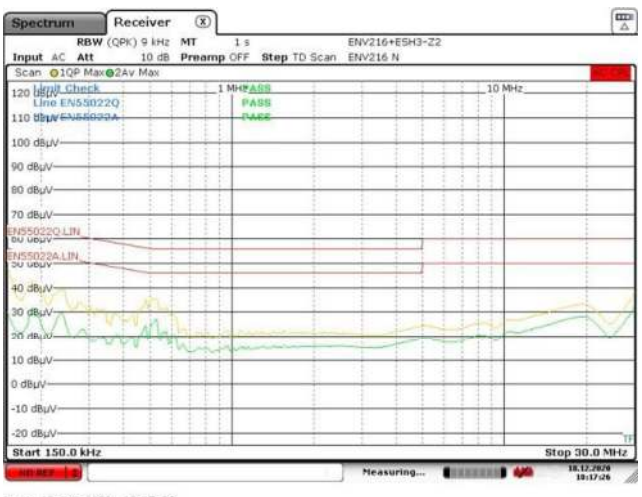
16.1.5 Output: 20 V / 1.5 A

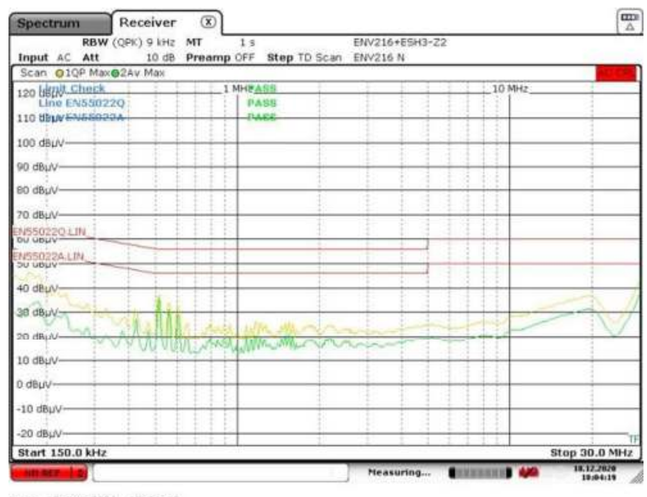




115 VAC. 230 VAC.

Figure 171 – Floating Ground EMI, 20 V / 1.5 A Load [Line Scan].





115 VAC. 230 VAC.

Figure 172 – Floating Ground EMI, 20 V / 1.5 A Load [Neutral Scan].

17 Combination Wave Surge

The unit was subjected to ±1000 V differential mode and ±2000 V common mode combination wave surge at several line phase angles with 10 strikes for each condition.

A test failure was defined as an output latch-off that needs operator intervention to recover, or a complete loss of function that is not recoverable.

17.1 *Differential Mode Surge (L1 to L2), 230 VAC Input*

Surge Level (V)	Injection Phase (°)	Test Result 5 V / 3 A	Test Result 9 V / 3 A	Test Result 12 V / 2.5 A	Test Result 15 V / 2 A	Test Result 20 V / 1.5 A
+1000	0	PASS	PASS	PASS	PASS	PASS
-1000	0	PASS	PASS	PASS	PASS	PASS
+1000	90	PASS	PASS	PASS	PASS	PASS
-1000	90	PASS	PASS	PASS	PASS	PASS
+1000	180	PASS	PASS	PASS	PASS	PASS
-1000	180	PASS	PASS	PASS	PASS	PASS
+1000	270	PASS	PASS	PASS	PASS	PASS
-1000	270	PASS	PASS	PASS	PASS	PASS

17.2 *Common Mode Surge (L1, L2 to PE), 230 VAC Input*

Surge Level (V)	Injection Phase (°)	Test Result 5 V / 3 A	Test Result 9 V / 3 A	Test Result 12 V / 2.5 A	Test Result 15 V / 2 A	Test Result 20 V / 1.5 A
+2000	0	PASS	PASS	PASS	PASS	PASS
-2000	0	PASS	PASS	PASS	PASS	PASS
+2000	90	PASS	PASS	PASS	PASS	PASS
-2000	90	PASS	PASS	PASS	PASS	PASS
+2000	180	PASS	PASS	PASS	PASS	PASS
-2000	180	PASS	PASS	PASS	PASS	PASS
+2000	270	PASS	PASS	PASS	PASS	PASS
-2000	270	PASS	PASS	PASS	PASS	PASS

17.3 *Common Mode Surge (L1 to PE), 230 VAC Input*

Surge Level (V)	Injection Phase (°)	Test Result 5 V / 3 A	Test Result 9 V / 3 A	Test Result 12 V / 2.5 A	Test Result 15 V / 2 A	Test Result 20 V / 1.5 A
+2000	0	PASS	PASS	PASS	PASS	PASS
-2000	0	PASS	PASS	PASS	PASS	PASS
+2000	90	PASS	PASS	PASS	PASS	PASS
-2000	90	PASS	PASS	PASS	PASS	PASS
+2000	180	PASS	PASS	PASS	PASS	PASS
-2000	180	PASS	PASS	PASS	PASS	PASS
+2000	270	PASS	PASS	PASS	PASS	PASS
-2000	270	PASS	PASS	PASS	PASS	PASS

17.4 *Common Mode Surge (L2 to PE), 230 VAC Input*

Surge Level (V)	Injection Phase (°)	Test Result 5 V / 3 A	Test Result 9 V / 3 A	Test Result 12 V / 2.5 A	Test Result 15 V / 2 A	Test Result 20 V / 1.5 A
+2000	0	PASS	PASS	PASS	PASS	PASS
-2000	0	PASS	PASS	PASS	PASS	PASS
+2000	90	PASS	PASS	PASS	PASS	PASS
-2000	90	PASS	PASS	PASS	PASS	PASS
+2000	180	PASS	PASS	PASS	PASS	PASS
-2000	180	PASS	PASS	PASS	PASS	PASS
+2000	270	PASS	PASS	PASS	PASS	PASS
-2000	270	PASS	PASS	PASS	PASS	PASS

18 Electrostatic Discharge

The unit was tested with ±16.5 kV air discharge and ±8.8 kV contact discharge with 10 strikes for each condition at the following locations:

- End of cable +VOUT
- End of cable GND
- On-board +VOUT
- On-board GND
- End of cable CC1
- End of cable CC2

A test failure was defined as an output latch-off that needs operator intervention to recover, or a complete loss of function that is not recoverable.

18.1 *Contact Discharge 8.8kV, USB-C Cable Connected*

<table>
<tr><th>Zap Terminal</th><th>Zap Point</th><th>VOUT (V)</th><th>Load (A)</th><th># of Strikes</th><th>Positive</th><th>Negative</th></tr>
<tr><td rowspan="8">End of Cable</td><td rowspan="2">CC1</td><td rowspan="8">5</td><td>0</td><td rowspan="8">10</td><td>PASS</td><td>PASS</td></tr>
<tr><td>3</td><td>PASS</td><td>PASS</td></tr>
<tr><td rowspan="2">CC2</td><td>0</td><td>PASS</td><td>PASS</td></tr>
<tr><td>3</td><td>PASS</td><td>PASS</td></tr>
<tr><td rowspan="2">VBUS</td><td>0</td><td>PASS</td><td>PASS</td></tr>
<tr><td>3</td><td>PASS</td><td>PASS</td></tr>
<tr><td rowspan="2">Return</td><td>0</td><td>PASS</td><td>PASS</td></tr>
<tr><td>3</td><td>PASS</td><td>PASS</td></tr>
</table>

18.2 *Air Discharge 16.5 kV, USB-C Cable Connected*

<table>
<tr><th>Zap Terminal</th><th>Zap Point</th><th>VOUT (V)</th><th>Load (A)</th><th># of Strikes</th><th>Positive</th><th>Negative</th></tr>
<tr><td rowspan="8">End of Cable</td><td rowspan="2">CC 1</td><td rowspan="10">5</td><td>0</td><td rowspan="10">10</td><td>PASS</td><td>PASS</td></tr>
<tr><td>3</td><td>PASS</td><td>PASS</td></tr>
<tr><td rowspan="2">CC 2</td><td>0</td><td>PASS</td><td>PASS</td></tr>
<tr><td>3</td><td>PASS</td><td>PASS</td></tr>
<tr><td rowspan="2">VBUS</td><td>0</td><td>PASS</td><td>PASS</td></tr>
<tr><td>3</td><td>PASS</td><td>PASS</td></tr>
<tr><td rowspan="4">Return</td><td>0</td><td>PASS</td><td>PASS</td></tr>
<tr><td>3</td><td>PASS</td><td>PASS</td></tr>
<tr><td rowspan="2">On Board</td><td>0</td><td>PASS</td><td>PASS</td></tr>
<tr><td>3</td><td>PASS</td><td>PASS</td></tr>
</table>

18.3 *Air Discharge 16.5 kV, USB-C Cable Not Connected*

<table>
<tr><th>Zap Point</th><th>VOUT (V)</th><th>Load (A)</th><th># of Strikes</th><th>Positive</th><th>Negative</th></tr>
<tr><td>CC1</td><td rowspan="4">5</td><td rowspan="4">0</td><td rowspan="4">10</td><td>PASS</td><td>PASS</td></tr>
<tr><td>CC2</td><td>PASS</td><td>PASS</td></tr>
<tr><td>VBUS</td><td>PASS</td><td>PASS</td></tr>
<tr><td>Return</td><td>PASS</td><td>PASS</td></tr>
</table>

19 Revision History

Date	Author	Revision	Description & Changes	Reviewed
22-Jul-21	Norberto Sánchez-Dichi	1.0	Initial Release.	Apps & Mktg

For the latest updates, visit our website: www.power.com

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