



**HIGH-SPEED 3.3V 256K x 36  
SYNCHRONOUS  
BANK-SWITCHABLE  
DUAL-PORT STATIC RAM  
WITH 3.3V OR 2.5V INTERFACE**

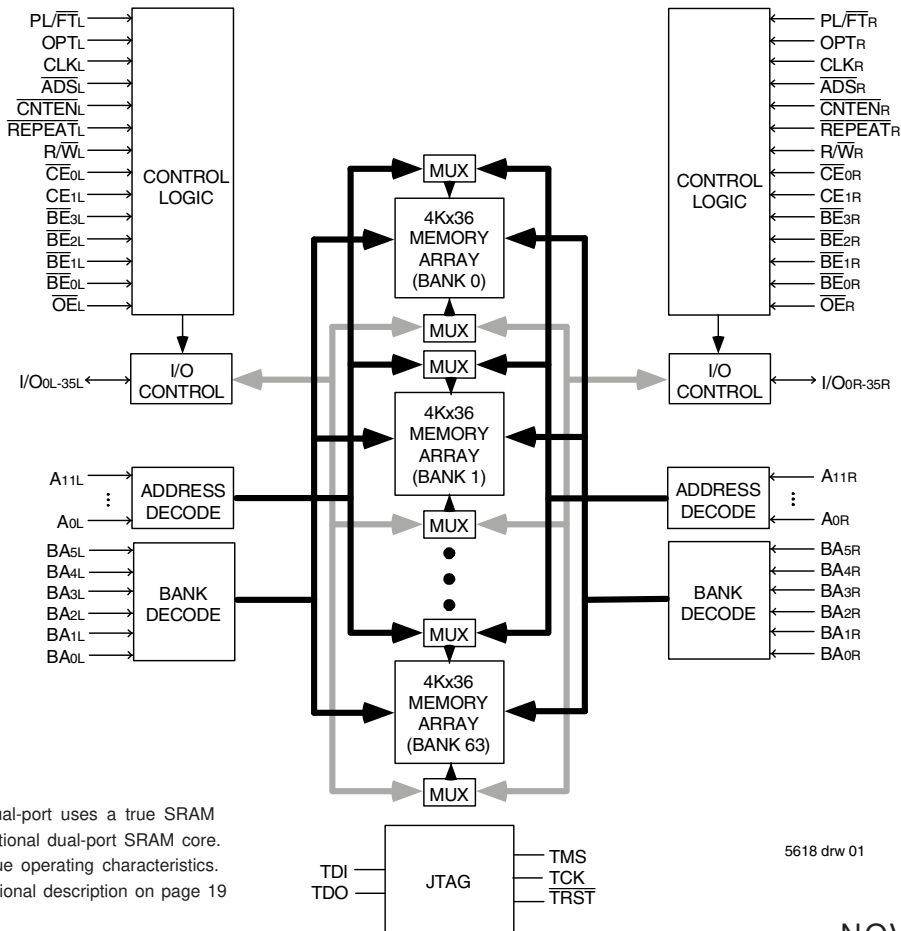
**70V7519S**

**Features:**

- ◆ 256K x 36 Synchronous Bank-Switchable Dual-ported SRAM Architecture
  - 64 independent 4K x 36 banks
  - 9 megabits of memory on chip
- ◆ Bank access controlled via bank address pins
- ◆ High-speed data access
  - Commercial: 3.4ns(200MHz)/3.6ns(166MHz)/4.2ns(133MHz) (max.)
  - Industrial: 3.6ns(166MHz)/4.2ns(133MHz) (max.)
- ◆ Selectable Pipelined or Flow-Through output mode
- ◆ Counter enable and repeat features
- ◆ Dual chip enables allow for depth expansion without additional logic
- ◆ Full synchronous operation on both ports
  - 5ns cycle time, 200MHz operation (14Gbps bandwidth)
  - Fast 3.4ns clock to data out

- 1.5ns setup to clock and 0.5ns hold on all control, data, and address inputs @ 200MHz
- Data input, address, byte enable and control registers
- Self-timed write allows fast cycle time
- ◆ Separate byte controls for multiplexed bus and bus matching compatibility
- ◆ LVTTTL-compatible, 3.3V (±150mV) power supply for core
- ◆ LVTTTL compatible, selectable 3.3V (±150mV) or 2.5V (±100mV) power supply for I/Os and control signals on each port
- ◆ Industrial temperature range (-40°C to +85°C) is available at 166MHz and 133MHz
- ◆ Available in a 208-pin fine pitch Ball Grid Array (fpBGA) and 256-pin Ball Grid Array (BGA)
- ◆ Supports JTAG features compliant with IEEE 1149.1
- ◆ Green parts available, see ordering information

**Functional Block Diagram**



**NOTE:**

1. The Bank-Switchable dual-port uses a true SRAM core instead of the traditional dual-port SRAM core. As a result, it has unique operating characteristics. Please refer to the functional description on page 19 for details.

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NOVEMBER 2019

## Description:

The IDT70V7519 is a high-speed 256Kx36 (9Mbit) synchronous Bank-Switchable Dual-Ported SRAM organized into 64 independent 4Kx36 banks. The device has two independent ports with separate control, address, and I/O pins for each port, allowing each port to access any 4Kx36 memory block not already accessed by the other port. Accesses by the ports into specific banks are controlled via the bank address pins under the user's direct control.

Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data

register, the IDT70V7519 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by CE<sub>0</sub> and CE<sub>1</sub>, permits the on-chip circuitry of each port to enter a very low standby power mode. The dual chip enables also facilitate depth expansion.

The 70V7519 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (V<sub>DD</sub>) remains at 3.3V. Please refer also to the functional description on page 19.

## Pin Configuration<sup>(1,2,3,4)</sup>

A1 IO19L	A2 IO18L	A3 VSS	A4 TDO	A5 NC	A6 BA4L	A7 BA0L	A8 A8L	A9 BE1L	A10 VDD	A11 CLKL	A12 CNTENL	A13 A4L	A14 A0L	A15 OPTL	A16 IO17L	A17 VSS	
B1 IO20R	B2 VSS	B3 IO18R	B4 TDI	B5 BA5L	B6 BA1L	B7 A9L	B8 BE2L	B9 CE0L	B10 VSS	B11 ADSL	B12 A5L	B13 A1L	B14 VSS	B15 VDDQR	B16 IO16L	B17 IO15R	
C1 VDDQL	C2 IO19R	C3 VDDQR	C4 PL/FTL	C5 NC	C6 BA2L	C7 A10L	C8 BE3L	C9 CE1L	C10 VSS	C11 R/WL	C12 A6L	C13 A2L	C14 VDD	C15 IO16R	C16 IO15L	C17 VSS	
D1 IO22L	D2 VSS	D3 IO21L	D4 IO20L	D5 BA3L	D6 A11L	D7 A7L	D8 BE0L	D9 VDD	D10 OEL	D11 REPEATL	D12 A3L	D13 VDD	D14 IO17R	D15 VDDQL	D16 IO14L	D17 IO14R	
E1 IO23L	E2 IO22R	E3 VDDQR	E4 IO21R	<b>70V7519</b> <b>BF208<sup>(5)</sup></b>  <b>208-Pin fpBGA</b> <b>Top View<sup>(6)</sup></b>										E14 IO12L	E15 IO13R	E16 VSS	E17 IO13L
F1 VDDQL	F2 IO23R	F3 IO24L	F4 VSS											F14 VSS	F15 IO12R	F16 IO11L	F17 VDDQR
G1 IO26L	G2 VSS	G3 IO25L	G4 IO24R											G14 IO9L	G15 VDDQL	G16 IO10L	G17 IO11R
H1 VDD	H2 IO26R	H3 VDDQR	H4 IO25R											H14 VDD	H15 IO9R	H16 VSS	H17 IO10R
J1 VDDQL	J2 VDD	J3 VSS	J4 VSS											J14 VSS	J15 VDD	J16 VSS	J17 VDDQR
K1 IO28R	K2 VSS	K3 IO27R	K4 VSS											K14 IO7R	K15 VDDQL	K16 IO8R	K17 VSS
L1 IO29R	L2 IO28L	L3 VDDQR	L4 IO27L											L14 IO6R	L15 IO7L	L16 VSS	L17 IO8L
M1 VDDQL	M2 IO29L	M3 IO30R	M4 VSS											M14 VSS	M15 IO6L	M16 IO5R	M17 VDDQR
N1 IO31L	N2 VSS	N3 IO31R	N4 IO30L											N14 IO3R	N15 VDDQL	N16 IO4R	N17 IO5L
P1 IO32R	P2 IO32L	P3 VDDQR	P4 IO35R											P5 TRST	P6 BA4R	P7 BA0R	P8 A8R
R1 VSS	R2 IO33L	R3 IO34R	R4 TCK	R5 BA5R	R6 BA1R	R7 A9R	R8 BE2R	R9 CE0R	R10 VSS	R11 ADSR	R12 A5R	R13 A1R	R14 VSS	R15 VDDQL	R16 IO1R	R17 VDDQR	
T1 IO33R	T2 IO34L	T3 VDDQL	T4 TMS	T5 NC	T6 BA2R	T7 A10R	T8 BE3R	T9 CE1R	T10 VSS	T11 R/WR	T12 A6R	T13 A2R	T14 VSS	T15 IO0R	T16 VSS	T17 IO2R	
U1 VSS	U2 IO35L	U3 PL/FTL	U4 NC	U5 BA3R	U6 A11R	U7 A7R	U8 BE0R	U9 VDD	U10 OER	U11 REPEATR	U12 A3R	U13 A0R	U14 VDD	U15 OPTR	U16 IO0L	U17 IO1L	

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### NOTES:

1. All V<sub>DD</sub> pins must be connected to 3.3V power supply.
2. All V<sub>DDQ</sub> pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V<sub>IH</sub> (3.3V), and 2.5V if OPT pin for that port is set to V<sub>IL</sub> (0V).
3. All V<sub>SS</sub> pins must be connected to ground supply.
4. Package body is approximately 15mm x 15mm x 1.4mm with 0.8mm ball pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration<sup>(1,2,3,4)</sup> (con't.)

70V7519  
BC256<sup>(5)</sup>

256-Pin BGA  
Top View<sup>(6)</sup>

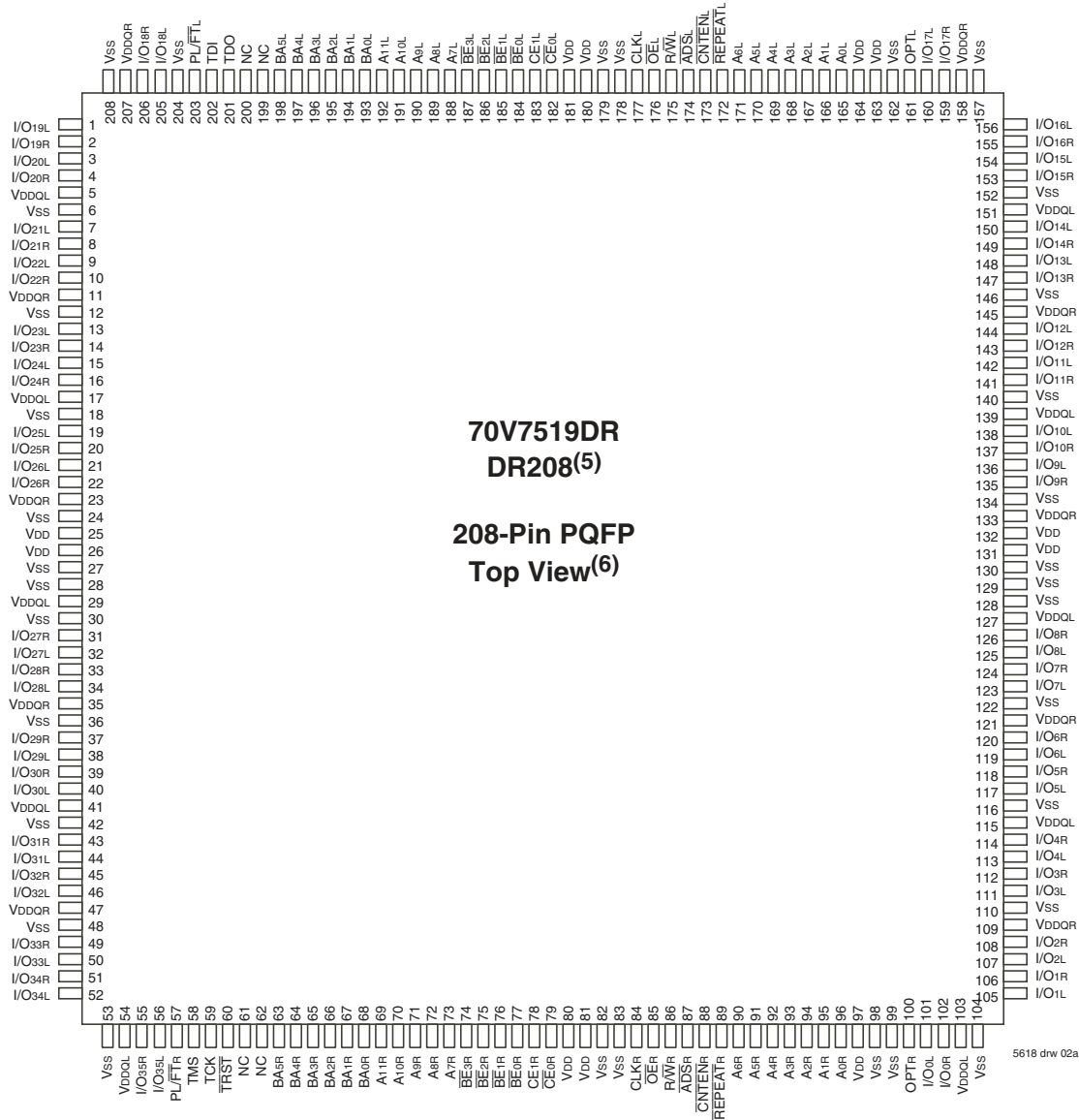
A1 NC	A2 TDI	A3 NC	A4 BA5L	A5 BA2L	A6 A11L	A7 A8L	A8 $\overline{BE}2L$	A9 CE1L	A10 $\overline{OE}L$	A11 $\overline{CNTEN}L$	A12 A5L	A13 A2L	A14 A0L	A15 NC	A16 NC
B1 I/O18L	B2 NC	B3 TDO	B4 NC	B5 BA3L	B6 BA0L	B7 A9L	B8 $\overline{BE}3L$	B9 $\overline{CE}0L$	B10 R/WL	B11 $\overline{REPEAT}L$	B12 A4L	B13 A1L	B14 VDD	B15 I/O17L	B16 NC
C1 I/O18R	C2 I/O19L	C3 VSS	C4 BA4L	C5 BA1L	C6 A10L	C7 A7L	C8 $\overline{BE}1L$	C9 $\overline{BE}0L$	C10 CLKL	C11 $\overline{ADS}L$	C12 A6L	C13 A3L	C14 OPTL	C15 I/O17R	C16 I/O16L
D1 I/O20R	D2 I/O19R	D3 I/O20L	D4 PL/FTL	D5 VDDQL	D6 VDDQL	D7 VDDQRL	D8 VDDQRL	D9 VDDQL	D10 VDDQL	D11 VDDQRL	D12 VDDQRL	D13 VDD	D14 I/O15R	D15 I/O15L	D16 I/O16R
E1 I/O21R	E2 I/O21L	E3 I/O22L	E4 VDDQL	E5 VDD	E6 VDD	E7 VSS	E8 VSS	E9 VSS	E10 VSS	E11 VDD	E12 VDD	E13 VDDQRL	E14 I/O13L	E15 I/O14L	E16 I/O14R
F1 I/O23L	F2 I/O22R	F3 I/O23R	F4 VDDQL	F5 VDD	F6 VSS	F7 VSS	F8 VSS	F9 VSS	F10 VSS	F11 VSS	F12 VDD	F13 VDDQRL	F14 I/O12R	F15 I/O13R	F16 I/O12L
G1 I/O24R	G2 I/O24L	G3 I/O25L	G4 VDDQRL	G5 VSS	G6 VSS	G7 VSS	G8 VSS	G9 VSS	G10 VSS	G11 VSS	G12 VSS	G13 VDDQL	G14 I/O10L	G15 I/O11L	G16 I/O11R
H1 I/O26L	H2 I/O25R	H3 I/O26R	H4 VDDQRL	H5 VSS	H6 VSS	H7 VSS	H8 VSS	H9 VSS	H10 VSS	H11 VSS	H12 VSS	H13 VDDQL	H14 I/O9R	H15 I/O9L	H16 I/O10R
J1 I/O27L	J2 I/O28R	J3 I/O27R	J4 VDDQL	J5 VSS	J6 VSS	J7 VSS	J8 VSS	J9 VSS	J10 VSS	J11 VSS	J12 VSS	J13 VDDQRL	J14 I/O8R	J15 I/O7R	J16 I/O8L
K1 I/O29R	K2 I/O29L	K3 I/O28L	K4 VDDQL	K5 VSS	K6 VSS	K7 VSS	K8 VSS	K9 VSS	K10 VSS	K11 VSS	K12 VSS	K13 VDDQRL	K14 I/O6R	K15 I/O6L	K16 I/O7L
L1 I/O30L	L2 I/O31R	L3 I/O30R	L4 VDDQRL	L5 VDD	L6 VSS	L7 VSS	L8 VSS	L9 VSS	L10 VSS	L11 VSS	L12 VDD	L13 VDDQL	L14 I/O5L	L15 I/O4R	L16 I/O5R
M1 I/O32R	M2 I/O32L	M3 I/O31L	M4 VDDQRL	M5 VDD	M6 VDD	M7 VSS	M8 VSS	M9 VSS	M10 VSS	M11 VDD	M12 VDD	M13 VDDQL	M14 I/O3R	M15 I/O3L	M16 I/O4L
N1 I/O33L	N2 I/O34R	N3 I/O33R	N4 PL/FTL	N5 VDDQRL	N6 VDDQRL	N7 VDDQL	N8 VDDQL	N9 VDDQRL	N10 VDDQRL	N11 VDDQL	N12 VDDQL	N13 VDD	N14 I/O2L	N15 I/O1R	N16 I/O2R
P1 I/O35R	P2 I/O34L	P3 TMS	P4 BA4R	P5 BA1R	P6 A10R	P7 A7R	P8 $\overline{BE}1R$	P9 $\overline{BE}0R$	P10 CLKR	P11 $\overline{ADS}R$	P12 A6R	P13 A3R	P14 I/O0L	P15 I/O0R	P16 I/O1L
R1 I/O35L	R2 NC	R3 $\overline{TRST}$	R4 NC	R5 BA3R	R6 BA0R	R7 A9R	R8 $\overline{BE}3R$	R9 $\overline{CE}0R$	R10 R/WL	R11 $\overline{REPEAT}R$	R12 A4R	R13 A1R	R14 OPTR	R15 NC	R16 NC
T1 NC	T2 TCK	T3 NC	T4 BA5R	T5 BA2R	T6 A11R	T7 A8R	T8 $\overline{BE}2R$	T9 CE1R	T10 $\overline{OE}R$	T11 $\overline{CNTEN}R$	T12 A5R	T13 A2R	T14 A0R	T15 NC	T16 NC

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NOTES:

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration<sup>(1,2,3,4)</sup> (con't.)



NOTES:

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 28mm x 28mm x 3.5mm.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

## Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$ , CE <sub>1L</sub>	$\overline{CE}_{0R}$ , CE <sub>1R</sub>	Chip Enables
R $\overline{WL}$	R $\overline{WR}$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
BA <sub>0L</sub> - BA <sub>5L</sub>	BA <sub>0R</sub> - BA <sub>5R</sub>	Bank Address <sup>(4)</sup>
A <sub>0L</sub> - A <sub>11L</sub>	A <sub>0R</sub> - A <sub>11R</sub>	Address
I/O <sub>0L</sub> - I/O <sub>35L</sub>	I/O <sub>0R</sub> - I/O <sub>35R</sub>	Data Input/Output
CLK <sub>L</sub>	CLK <sub>R</sub>	Clock
PL/ $\overline{FT}_L$	PL/ $\overline{FT}_R$	Pipeline/Flow-Through
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Enable
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable
$\overline{REPEAT}_L$	$\overline{REPEAT}_R$	Counter Repeat <sup>(9)</sup>
$\overline{BE}_{0L}$ - $\overline{BE}_{3L}$	$\overline{BE}_{0R}$ - $\overline{BE}_{3R}$	Byte Enables (9-bit bytes)
V <sub>DDQL</sub>	V <sub>DDQR</sub>	Power (I/O Bus) (3.3V or 2.5V) <sup>(1)</sup>
OPT <sub>L</sub>	OPT <sub>R</sub>	Option for selecting V <sub>DDQx</sub> <sup>(1,2)</sup>
V <sub>DD</sub>		Power (3.3V) <sup>(1)</sup>
V <sub>SS</sub>		Ground (0V)
TDI		Test Data Input
TDO		Test Data Output
TCK		Test Logic Clock (10MHz)
TMS		Test Mode Select
$\overline{TRST}$		Reset (Initialize TAP Controller)

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### NOTES:

1. V<sub>DD</sub>, OPT<sub>x</sub>, and V<sub>DDQx</sub> must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
2. OPT<sub>x</sub> selects the operating voltage levels for the I/Os and controls on that port. If OPT<sub>x</sub> is set to VIH (3.3V), then that port's I/Os and controls will operate at 3.3V levels and V<sub>DDQx</sub> must be supplied at 3.3V. If OPT<sub>x</sub> is set to VIL (0V), then that port's I/Os and address controls will operate at 2.5V levels and V<sub>DDQx</sub> must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.
3. When  $\overline{REPEAT}_x$  is asserted, the counter will reset to the last valid address loaded via  $\overline{ADS}_x$ .
4. Accesses by the ports into specific banks are controlled by the bank address pins under the user's direct control: each port can access any bank of memory with the shared array that is not currently being accessed by the opposite port (i.e., BA<sub>0L</sub> - BA<sub>5L</sub> ≠ BA<sub>0R</sub> - BA<sub>5R</sub>). In the event that both ports try to access the same bank at the same time, neither access will be valid, and data at the two specific addresses targeted by the ports within that bank may be corrupted (in the case that either or both ports are writing) or may result in invalid output (in the case that both ports are trying to read).

Truth Table I—Read/Write and Enable Control<sup>(1,2,3,4)</sup>

$\overline{OE}^3$	CLK	$\overline{CE}_0$	$CE_1$	$\overline{BE}_3$	$\overline{BE}_2$	$\overline{BE}_1$	$\overline{BE}_0$	R $\overline{W}$	Byte 3 I/O <sub>27-35</sub>	Byte 2 I/O <sub>18-26</sub>	Byte 1 I/O <sub>9-17</sub>	Byte 0 I/O <sub>0-8</sub>	MODE
X	↑	H	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Deselected—Power Down
X	↑	X	L	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Deselected—Power Down
X	↑	L	H	H	H	H	H	X	High-Z	High-Z	High-Z	High-Z	All Bytes Deselected
X	↑	L	H	H	H	H	L	L	High-Z	High-Z	High-Z	D <sub>IN</sub>	Write to Byte 0 Only
X	↑	L	H	H	H	L	H	L	High-Z	High-Z	D <sub>IN</sub>	High-Z	Write to Byte 1 Only
X	↑	L	H	H	L	H	H	L	High-Z	D <sub>IN</sub>	High-Z	High-Z	Write to Byte 2 Only
X	↑	L	H	L	H	H	H	L	D <sub>IN</sub>	High-Z	High-Z	High-Z	Write to Byte 3 Only
X	↑	L	H	H	H	L	L	L	High-Z	High-Z	D <sub>IN</sub>	D <sub>IN</sub>	Write to Lower 2 Bytes Only
X	↑	L	H	L	L	H	H	L	D <sub>IN</sub>	D <sub>IN</sub>	High-Z	High-Z	Write to Upper 2 bytes Only
X	↑	L	H	L	L	L	L	L	D <sub>IN</sub>	D <sub>IN</sub>	D <sub>IN</sub>	D <sub>IN</sub>	Write to All Bytes
L	↑	L	H	H	H	H	L	H	High-Z	High-Z	High-Z	D <sub>OUT</sub>	Read Byte 0 Only
L	↑	L	H	H	H	L	H	H	High-Z	High-Z	D <sub>OUT</sub>	High-Z	Read Byte 1 Only
L	↑	L	H	H	L	H	H	H	High-Z	D <sub>OUT</sub>	High-Z	High-Z	Read Byte 2 Only
L	↑	L	H	L	H	H	H	H	D <sub>OUT</sub>	High-Z	High-Z	High-Z	Read Byte 3 Only
L	↑	L	H	H	H	L	L	H	High-Z	High-Z	D <sub>OUT</sub>	D <sub>OUT</sub>	Read Lower 2 Bytes Only
L	↑	L	H	L	L	H	H	H	D <sub>OUT</sub>	D <sub>OUT</sub>	High-Z	High-Z	Read Upper 2 Bytes Only
L	↑	L	H	L	L	L	L	H	D <sub>OUT</sub>	D <sub>OUT</sub>	D <sub>OUT</sub>	D <sub>OUT</sub>	Read All Bytes
H	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Outputs Disabled

NOTES:

- "H" = V<sub>IH</sub>, "L" = V<sub>IL</sub>, "X" = Don't Care.
- $\overline{ADS}$ ,  $\overline{CNTEN}$ ,  $\overline{REPEAT}$  are set as appropriate for address access. Refer to Truth Table II for details.
- $\overline{OE}$  is an asynchronous input signal.
- It is possible to read or write any combination of bytes during a given access. A few representative samples have been illustrated here.

5618 tbl 02

Truth Table II—Address and Address Counter Control<sup>(1,2,7)</sup>

Address	Previous Address	Addr Used	CLK	$\overline{ADS}$	$\overline{CNTEN}$	$\overline{REPEAT}^{(6)}$	I/O <sup>(3)</sup>	MODE
A <sub>n</sub>	X	A <sub>n</sub>	↑	L <sup>(4)</sup>	X	H	D <sub>I/O</sub> (n)	External Address Used
X	A <sub>n</sub>	A <sub>n</sub> + 1	↑	H	L <sup>(5)</sup>	H	D <sub>I/O</sub> (n+1)	Counter Enabled—Internal Address generation
X	A <sub>n</sub> + 1	A <sub>n</sub> + 1	↑	H	H	H	D <sub>I/O</sub> (n+1)	External Address Blocked—Counter disabled (A <sub>n</sub> + 1 reused)
X	X	A <sub>n</sub>	↑	X	X	L <sup>(4)</sup>	D <sub>I/O</sub> (0)	Counter Set to last valid $\overline{ADS}$ load

NOTES:

- "H" = V<sub>IH</sub>, "L" = V<sub>IL</sub>, "X" = Don't Care.
- Read and write operations are controlled by the appropriate setting of R $\overline{W}$ ,  $\overline{CE}_0$ ,  $CE_1$ ,  $\overline{BE}_n$  and  $\overline{OE}$ .
- Outputs configured in flow-through output mode: if outputs are in pipelined mode the data out will be delayed by one cycle.
- $\overline{ADS}$  and  $\overline{REPEAT}$  are independent of all other memory control signals including  $\overline{CE}_0$ ,  $CE_1$  and  $\overline{BE}_n$ .
- The address counter advances if  $\overline{CNTEN}$  = V<sub>IL</sub> on the rising edge of CLK, regardless of all other memory control signals including  $\overline{CE}_0$ ,  $CE_1$ ,  $\overline{BE}_n$ .
- When  $\overline{REPEAT}$  is asserted, the counter will reset to the last valid address loaded via  $\overline{ADS}$ . This value is not set at power-up: a known location should be loaded via  $\overline{ADS}$  during initialization if desired. Any subsequent  $\overline{ADS}$  access during operations will update the  $\overline{REPEAT}$  address location.
- The counter includes bank address and internal address. The counter will advance across bank boundaries. For example, if the counter is in Bank 0, at address FFFh, and is advanced one location, it will move to address 0h in Bank 1. By the same token, the counter at FFFh in Bank 63 will advance to 0h in Bank 0. Refer to Timing Waveform of Counter Repeat, page 18. Care should be taken during operation to avoid having both counters point to the same bank (i.e., ensure BA<sub>0L</sub> - BA<sub>5L</sub> ≠ BA<sub>0R</sub> - BA<sub>5R</sub>), as this condition will invalidate the access for both ports. Please refer to the functional description on page 19 for details.

5618 tbl 03

### Recommended Operating Temperature and Supply Voltage<sup>(1)</sup>

Grade	Ambient Temperature	GND	VDD
Commercial	0°C to +70°C	0V	3.3V ± 150mV
Industrial	-40°C to +85°C	0V	3.3V ± 150mV

5618 tbl 04

NOTE:

1. This is the parameter TA. This is the "instant on" case temperature.

### Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Commercial & Industrial	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	50	mA

5618 tbl 06

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed VDD + 150mV for more than 25% of the cycle time or 4ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ VDD + 150mV.

### Recommended DC Operating Conditions with VDDQ at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Core Supply Voltage	3.15	3.3	3.45	V
VDDQ	I/O Supply Voltage <sup>(3)</sup>	2.4	2.5	2.6	V
VSS	Ground	0	0	0	V
VIH	Input High Voltage (Address & Control Inputs)	1.7	—	VDDQ + 100mV <sup>(2)</sup>	V
VIH	Input High Voltage - I/O <sup>(3)</sup>	1.7	—	VDDQ + 100mV <sup>(2)</sup>	V
VIL	Input Low Voltage	-0.3 <sup>(1)</sup>	—	0.7	V

5618 tbl 05a

NOTES:

1. Undershoot of VIL ≥ -1.5V for pulse width less than 10ns is allowed.
2. VTERM must not exceed VDDQ + 100mV.
3. To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to VIL (0V), and VDDQx for that port must be supplied as indicated above.

### Recommended DC Operating Conditions with VDDQ at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Core Supply Voltage	3.15	3.3	3.45	V
VDDQ	I/O Supply Voltage <sup>(3)</sup>	3.15	3.3	3.45	V
VSS	Ground	0	0	0	V
VIH	Input High Voltage (Address & Control Inputs) <sup>(3)</sup>	2.0	—	VDDQ + 150mV <sup>(2)</sup>	V
VIH	Input High Voltage - I/O <sup>(3)</sup>	2.0	—	VDDQ + 150mV <sup>(2)</sup>	V
VIL	Input Low Voltage	-0.3 <sup>(1)</sup>	—	0.8	V

5618 tbl 05b

NOTES:

1. Undershoot of VIL ≥ -1.5V for pulse width less than 10ns is allowed.
2. VTERM must not exceed VDDQ + 150mV.
3. To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to VIH (3.3V), and VDDQx for that port must be supplied as indicated above.

## Capacitance<sup>(1)</sup>

(TA = +25°C, F = 1.0MHz) PQFP ONLY

Symbol	Parameter	Conditions <sup>(2)</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	8	pF
C <sub>OUT</sub> <sup>(3)</sup>	Output Capacitance	V <sub>OUT</sub> = 3dV	10.5	pF

5618 tbl 07

NOTES:

1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. C<sub>OUT</sub> also references C<sub>I/O</sub>.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V<sub>DD</sub> = 3.3V ± 150mV)

Symbol	Parameter	Test Conditions	70V7519S		Unit
			Min.	Max.	
I <sub>LI</sub>	Input Leakage Current <sup>(1)</sup>	V <sub>DDQ</sub> = Max., V <sub>IN</sub> = 0V to V <sub>DDQ</sub>	—	10	μA
I <sub>LO</sub>	Output Leakage Current <sup>(1)</sup>	$\overline{CE_0}$ = V <sub>IH</sub> or CE <sub>1</sub> = V <sub>IL</sub> , V <sub>OUT</sub> = 0V to V <sub>DDQ</sub>	—	10	μA
V <sub>OL</sub> (3.3V)	Output Low Voltage <sup>(2)</sup>	I <sub>OL</sub> = +4mA, V <sub>DDQ</sub> = Min.	—	0.4	V
V <sub>OH</sub> (3.3V)	Output High Voltage <sup>(2)</sup>	I <sub>OH</sub> = -4mA, V <sub>DDQ</sub> = Min.	2.4	—	V
V <sub>OL</sub> (2.5V)	Output Low Voltage <sup>(2)</sup>	I <sub>OL</sub> = +2mA, V <sub>DDQ</sub> = Min.	—	0.4	V
V <sub>OH</sub> (2.5V)	Output High Voltage <sup>(2)</sup>	I <sub>OH</sub> = -2mA, V <sub>DDQ</sub> = Min.	2.0	—	V

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NOTES:

1. At V<sub>DD</sub> ≤ 2.0V leakages are undefined.
2. V<sub>DDQ</sub> is selectable (3.3V/2.5V) via OPT pins. Refer to p.5 for details.



## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(5)</sup> ( $V_{DD} = 3.3V \pm 150mV$ )

Symbol	Parameter	Test Condition	Version	70V7519S200 <sup>(7)</sup> Com'l Only		70V7519S166 <sup>(6)</sup> Com'l & Ind		70V7519S133 Com'l & Ind		Unit
				Typ. <sup>(4)</sup>	Max.	Typ. <sup>(4)</sup>	Max.	Typ. <sup>(4)</sup>	Max.	
IDD	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R = V_{IL}$ , Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L S	815	950	675	790	550	645	mA
			IND S	—	—	675	830	550	675	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L S	340	410	275	340	250	295	mA
			IND S	—	—	275	355	250	310	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^{*A} = V_{IL}$ and $\overline{CE}^{*B} = V_{IH}^{(3)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L S	690	770	515	640	460	520	mA
			IND S	—	—	515	660	460	545	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DDQ} - 0.2V$ , $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0^{(2)}$	COM'L S	10	30	10	30	10	30	mA
			IND S	—	—	10	40	10	40	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^{*A} \leq 0.2V$ and $\overline{CE}^{*B} \geq V_{DDQ} - 0.2V^{(5)}$ $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$ , Active Port, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L S	690	770	515	640	460	520	mA
			IND S	—	—	515	660	460	545	

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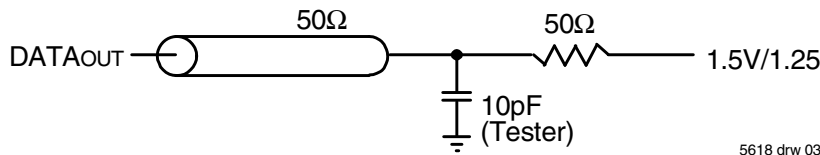
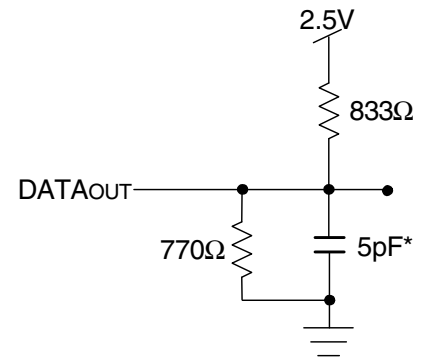
NOTES:

- At  $f = f_{MAX}$ , address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of  $1/t_{CYC}$ , using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$  means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 3.3V$ ,  $T_A = 25^\circ C$  for Typ, and are not production tested.  $IDD DC(f=0) = 120mA$  (Typ).
- $\overline{CE}_X = V_{IL}$  means  $\overline{CE}_{0X} = V_{IL}$  and  $CE_{1X} = V_{IH}$   
 $\overline{CE}_X = V_{IH}$  means  $\overline{CE}_{0X} = V_{IH}$  or  $CE_{1X} = V_{IL}$   
 $\overline{CE}_X \leq 0.2V$  means  $\overline{CE}_{0X} \leq 0.2V$  and  $CE_{1X} \geq V_{DDQ} - 0.2V$   
 $\overline{CE}_X \geq V_{DDQ} - 0.2V$  means  $\overline{CE}_{0X} \geq V_{DDQ} - 0.2V$  or  $CE_{1X} \leq 0.2V$   
"X" represents "L" for left port or "R" for right port.
- 166MHz Industrial Temperature not available in BF208 package.
- This speed grade available when  $V_{DDQ} = 3.3V$  for a specific port (i.e.,  $OPTx = V_{IH}$ ). This speed grade available in BC-256 package only.

AC Test Conditions (VDDQ - 3.3V/2.5V)

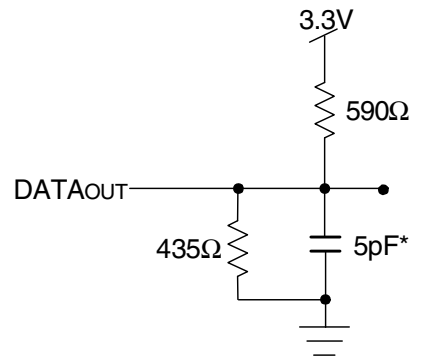
Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.4V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.4V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figures 1 and 2

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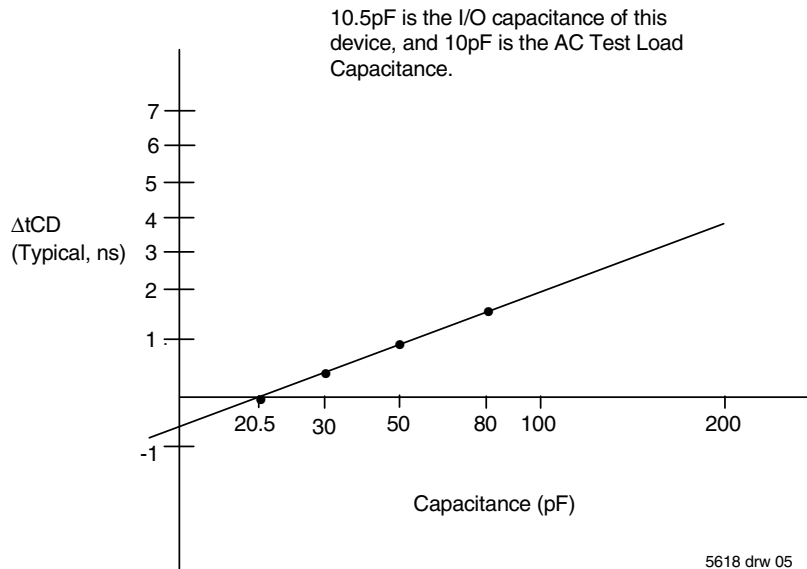
5618 drw 03

Figure 1. AC Output Test load.



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Figure 2. Output Test Load  
(For tCKLZ, tCKHZ, tOLZ, and tOHZ).  
\*Including scope and jig.



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Figure 3. Typical Output Derating (Lumped Capacitive Load).

## AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)<sup>(2,3)</sup> ( $V_{DD} = 3.3V \pm 150mV$ , $T_A = 0^\circ C$ to $+70^\circ C$ )

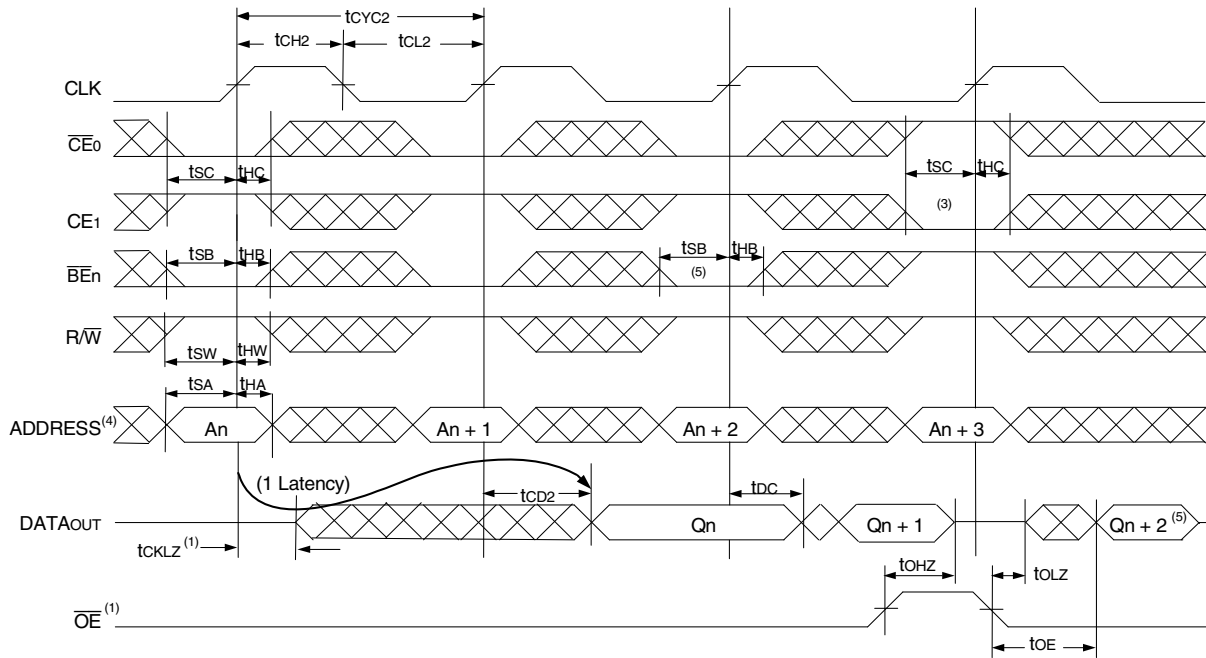
Symbol	Parameter	70V7519S200 <sup>(5)</sup> Com1 Only		70V7519S166 <sup>(3,4)</sup> Com1 & Ind		70V7519S133 <sup>(3)</sup> Com1 & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>CYC1</sub>	Clock Cycle Time (Flow-Through) <sup>(1)</sup>	15	—	20	—	25	—	ns
t <sub>CYC2</sub>	Clock Cycle Time (Pipelined) <sup>(1)</sup>	5	—	6	—	7.5	—	ns
t <sub>CH1</sub>	Clock High Time (Flow-Through) <sup>(1)</sup>	5	—	6	—	7	—	ns
t <sub>CL1</sub>	Clock Low Time (Flow-Through) <sup>(1)</sup>	5	—	6	—	7	—	ns
t <sub>CH2</sub>	Clock High Time (Pipelined) <sup>(2)</sup>	2.0	—	2.1	—	2.6	—	ns
t <sub>CL2</sub>	Clock Low Time (Pipelined) <sup>(1)</sup>	2.0	—	2.1	—	2.6	—	ns
t <sub>R</sub>	Clock Rise Time	—	1.5	—	1.5	—	1.5	ns
t <sub>F</sub>	Clock Fall Time	—	1.5	—	1.5	—	1.5	ns
t <sub>SA</sub>	Address Setup Time	1.5	—	1.7	—	1.8	—	ns
t <sub>HA</sub>	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>SC</sub>	Chip Enable Setup Time	1.5	—	1.7	—	1.8	—	ns
t <sub>HC</sub>	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>SB</sub>	Byte Enable Setup Time	1.5	—	1.7	—	1.8	—	ns
t <sub>HB</sub>	Byte Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>SW</sub>	R/W Setup Time	1.5	—	1.7	—	1.8	—	ns
t <sub>HW</sub>	R/W Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>SD</sub>	Input Data Setup Time	1.5	—	1.7	—	1.8	—	ns
t <sub>HD</sub>	Input Data Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>SAD</sub>	$\overline{ADS}$ Setup Time	1.5	—	1.7	—	1.8	—	ns
t <sub>HAD</sub>	$\overline{ADS}$ Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>SCN</sub>	$\overline{CNTEN}$ Setup Time	1.5	—	1.7	—	1.8	—	ns
t <sub>HCN</sub>	$\overline{CNTEN}$ Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>SRPT</sub>	$\overline{REPEAT}$ Setup Time	1.5	—	1.7	—	1.8	—	ns
t <sub>HRPT</sub>	$\overline{REPEAT}$ Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>OE</sub>	Output Enable to Data Valid	—	4.0	—	4.0	—	4.2	ns
t <sub>OLZ</sub>	Output Enable to Output Low-Z	0.5	—	0.5	—	0.5	—	ns
t <sub>OHZ</sub>	Output Enable to Output High-Z	1	3.4	1	3.6	1	4.2	ns
t <sub>CD1</sub>	Clock to Data Valid (Flow-Through) <sup>(1)</sup>	—	10	—	12	—	15	ns
t <sub>CD2</sub>	Clock to Data Valid (Pipelined) <sup>(1)</sup>	—	3.4	—	3.6	—	4.2	ns
t <sub>DC</sub>	Data Output Hold After Clock High	1	—	1	—	1	—	ns
t <sub>CKHZ</sub>	Clock High to Output High-Z	1	3.4	1	3.6	1	4.2	ns
t <sub>CKLZ</sub>	Clock High to Output Low-Z	0.5	—	0.5	—	0.5	—	ns
Port-to-Port Delay								
t <sub>CO</sub>	Clock-to-Clock Offset	5.0	—	6.0	—	7.5	—	ns

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NOTES:

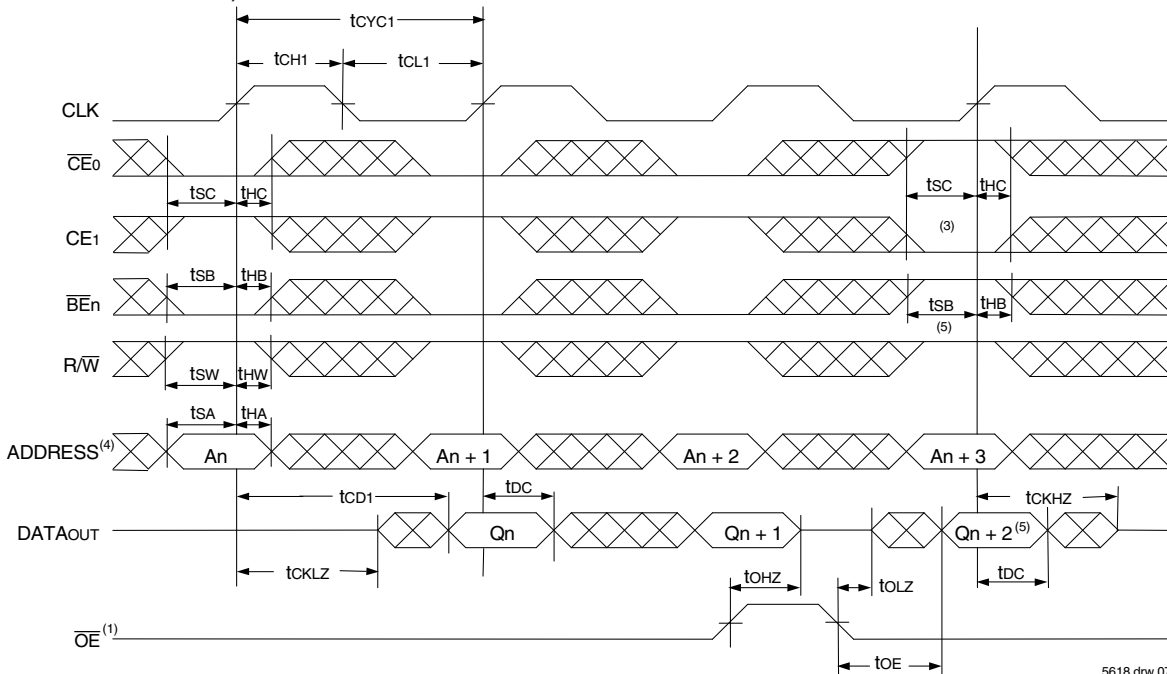
- The Pipelined output parameters (t<sub>CYC2</sub>, t<sub>CD2</sub>) apply to either or both left and right ports when  $\overline{FT}/PIPEX = V_{IH}$ . Flow-through parameters (t<sub>CYC1</sub>, t<sub>CD1</sub>) apply when  $\overline{FT}/PIPEX = V_{IL}$  for that port.
- All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ( $\overline{OE}$ ) and  $\overline{FT}/PIPE$ .  $\overline{FT}/PIPE$  should be treated as a DC signal, i.e. steady state during operation.
- These values are valid for either level of V<sub>DDQ</sub> (3.3V/2.5V). See page 5 for details on selecting the desired operating voltage levels for each port.
- 166MHz Industrial Temperature not available in BF208 package.
- This speed grade available when V<sub>DDQ</sub> = 3.3V for a specific port (i.e., OPTx = V<sub>IH</sub>). This speed grade available in BC256 package only.

### Timing Waveform of Read Cycle for Pipelined Operation (**ADS** Operation) (**FT/PIPE**'x' = $V_{IH}$ )<sup>(2)</sup>



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### Timing Waveform of Read Cycle for Flow-through Output (**FT/PIPE**"x" = $V_{IL}$ )<sup>(2,6)</sup>

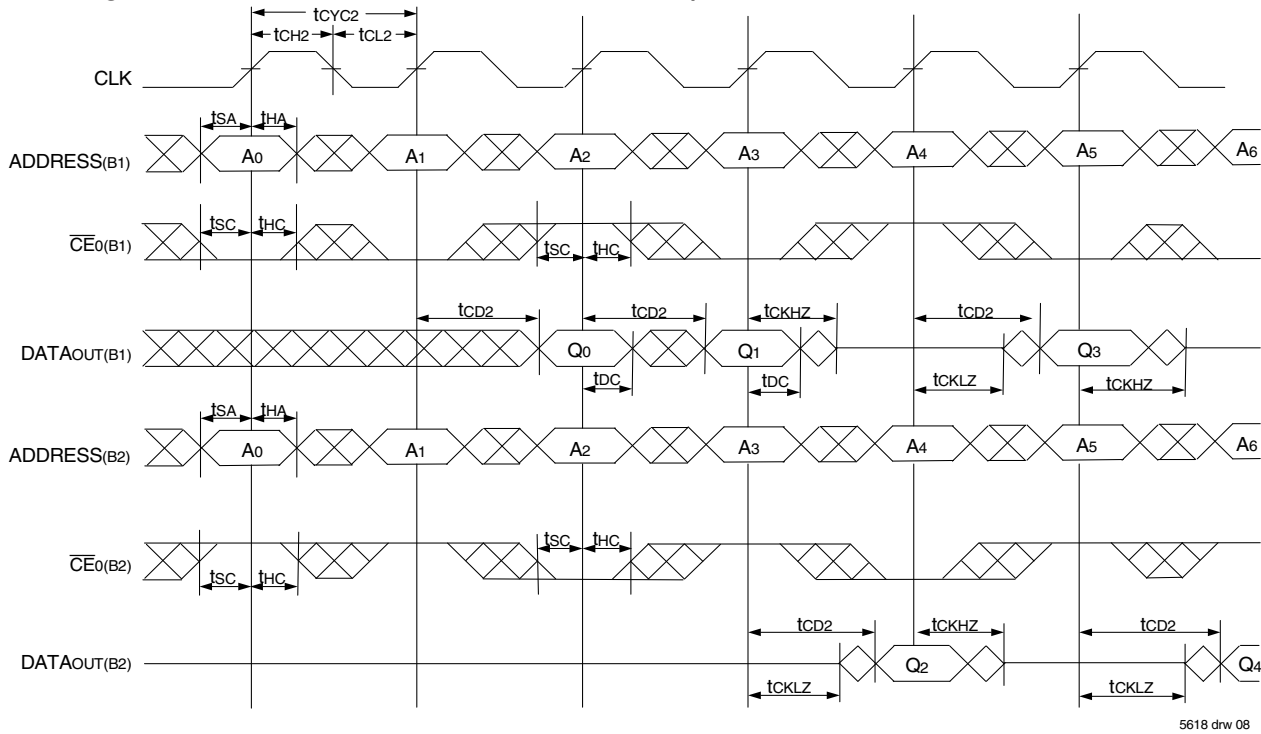


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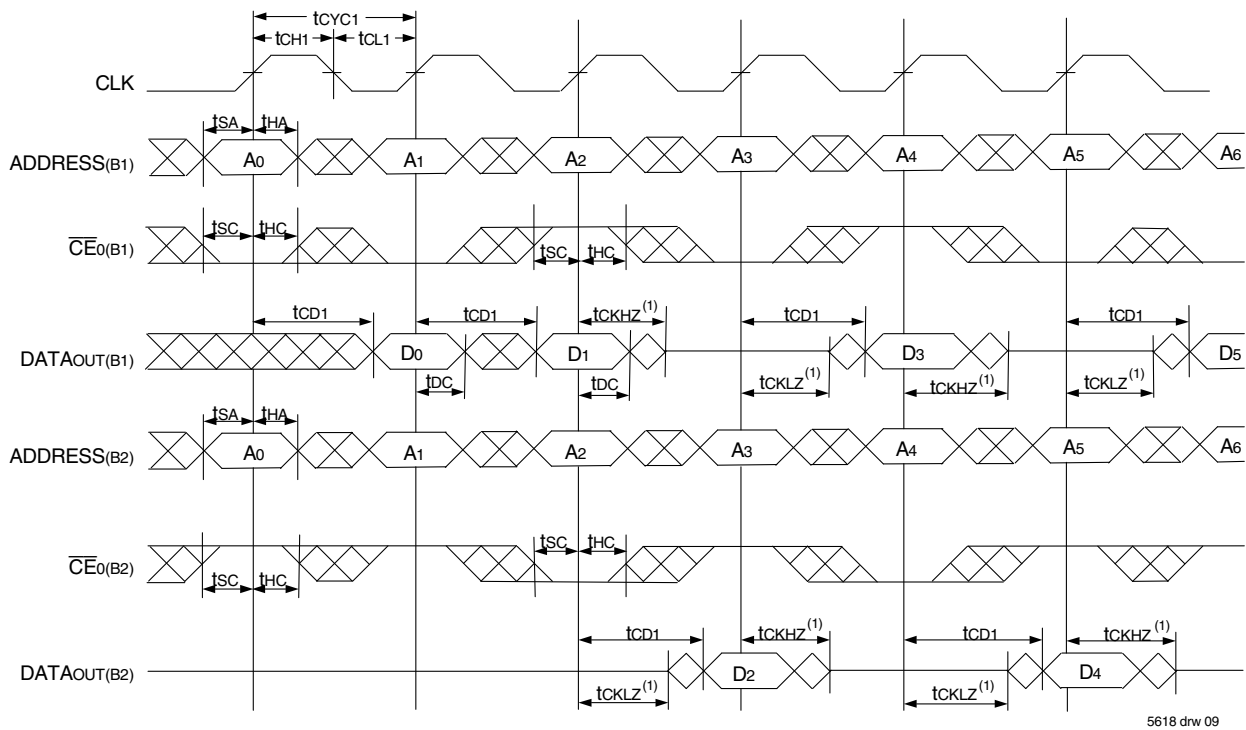
NOTES:

1.  $\overline{OE}$  is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
2.  $\overline{ADS} = V_{IL}$ ,  $\overline{CNTEN}$  and  $\overline{REPEAT} = V_{IH}$ .
3. The output is disabled (High-Impedance state) by  $\overline{CE}_0 = V_{IH}$ ,  $CE_1 = V_{IL}$ ,  $\overline{BE}_n = V_{IH}$  following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If  $\overline{BE}_n$  was HIGH, then the appropriate Byte of DATAout for  $Q_n + 2$  would be disabled (High-Impedance state).
6. "x" denotes Left or Right port. The diagram is with respect to that port.

### Timing Waveform of a Multi-Device Pipelined Read<sup>(1,2)</sup>



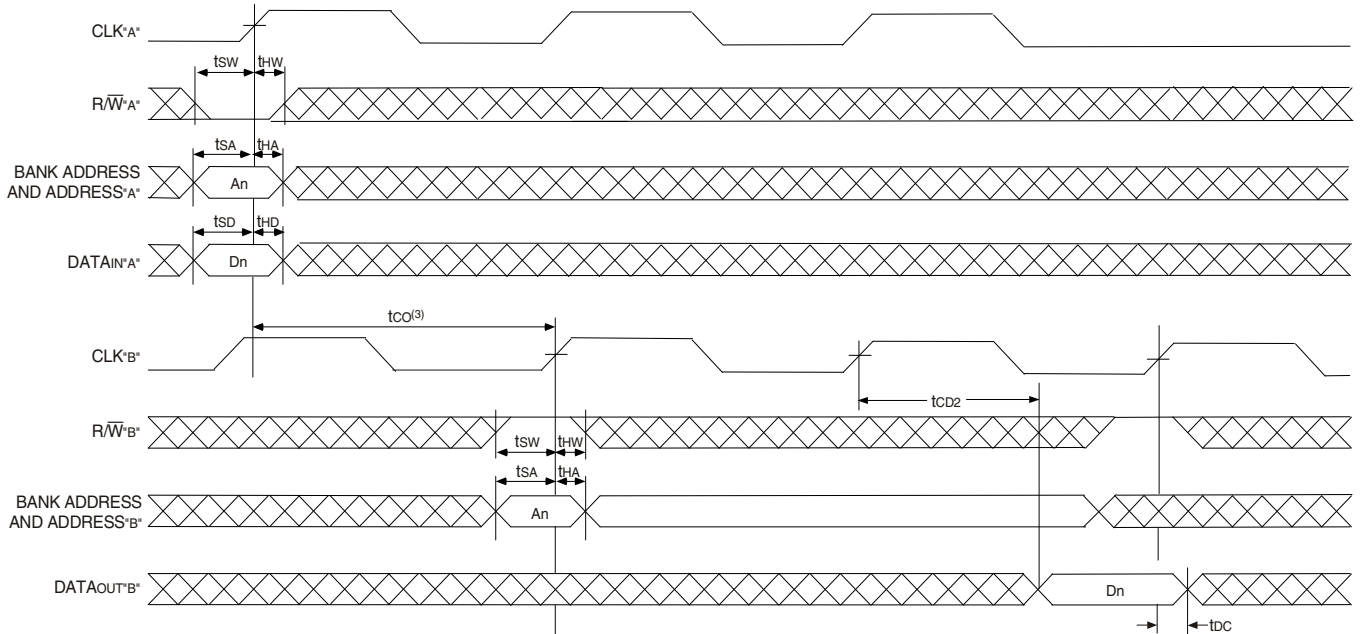
### Timing Waveform of a Multi-Device Flow-Through Read<sup>(1,2)</sup>



**NOTES:**

1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70V7519 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. BE<sub>n</sub>, OE, and ADS = VIH; CE1(B1), CE1(B2), R/W, CNTEN, and REPEAT = VIH.

### Timing Waveform of Port A Write to Pipelined Port B Read<sup>(1,2,4)</sup>

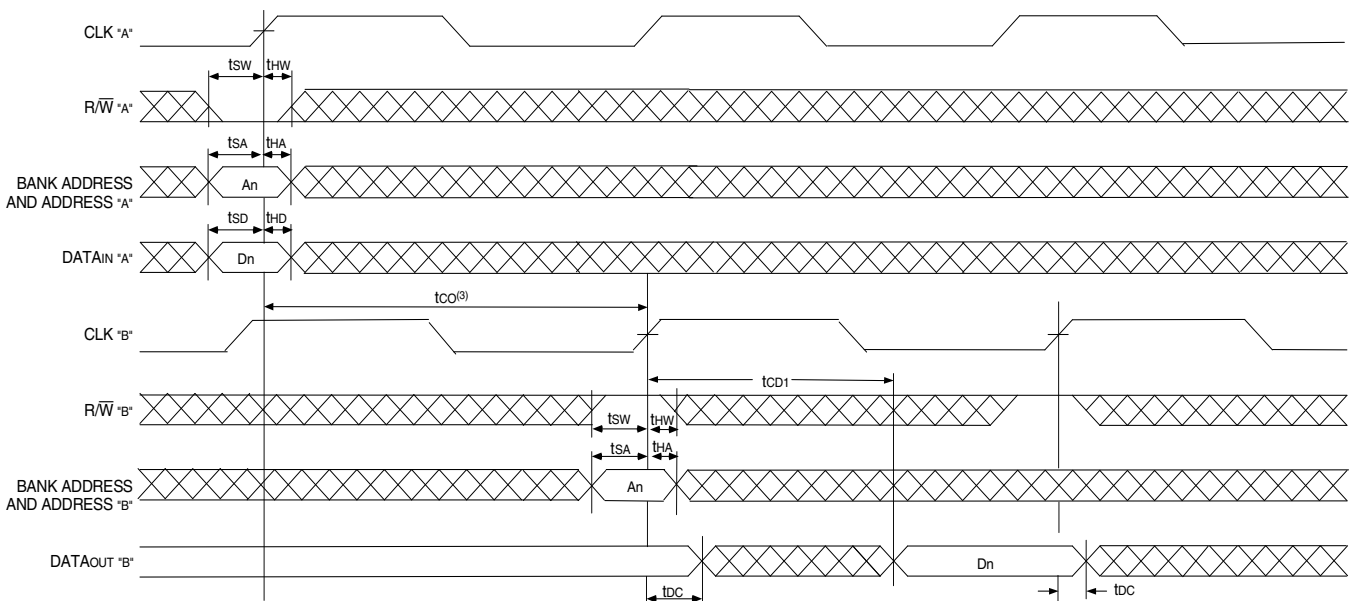


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NOTES:

1.  $\overline{CE}_0$ ,  $\overline{BE}_n$ , and  $\overline{ADS} = V_{IL}$ ;  $\overline{CE}_1$ ,  $\overline{CNTEN}$ , and  $\overline{REPEAT} = V_{IH}$ .
2.  $\overline{OE} = V_{IL}$  for Port "B", which is being read from.  $\overline{OE} = V_{IH}$  for Port "A", which is being written to.
3. If  $t_{CO} <$  minimum specified, then operations from both ports are INVALID. If  $t_{CO} \geq$  minimum, then data from Port "B" read is available on first Port "B" clock cycle (ie, time from write to valid read on opposite port will be  $t_{CO} + t_{CYC2} + t_{CD2}$ ).
4. All timing is the same for Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite of Port "A"

### Timing Waveform with Port-to-Port Flow-Through Read<sup>(1,2,4)</sup>

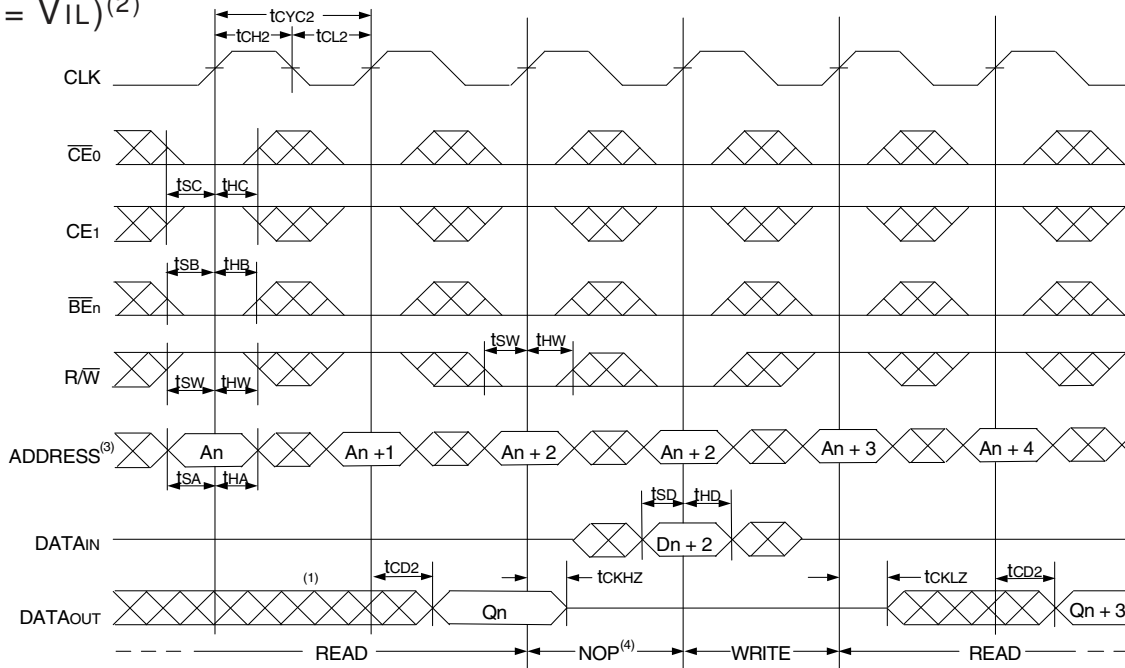


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NOTES:

1.  $\overline{CE}_0$ ,  $\overline{BE}_n$ , and  $\overline{ADS} = V_{IL}$ ;  $\overline{CE}_1$ ,  $\overline{CNTEN}$ , and  $\overline{REPEAT} = V_{IH}$ .
2.  $\overline{OE} = V_{IL}$  for the Right Port, which is being read from.  $\overline{OE} = V_{IH}$  for the Left Port, which is being written to.
3. If  $t_{CO} <$  minimum specified, then operations from both ports are INVALID. If  $t_{CO} \geq$  minimum, then data from Port "B" read is available on first Port "B" clock cycle (i.e., time from write to valid read on opposite port will be  $t_{CO} + t_{CD1}$ ).
4. All timing is the same for both left and right ports. Port "A" may be either left or right port. Port "B" is the opposite of Port "A".

### Timing Waveform of Pipelined Read-to-Write-to-Read ( $\overline{OE} = V_{IL}$ )<sup>(2)</sup>

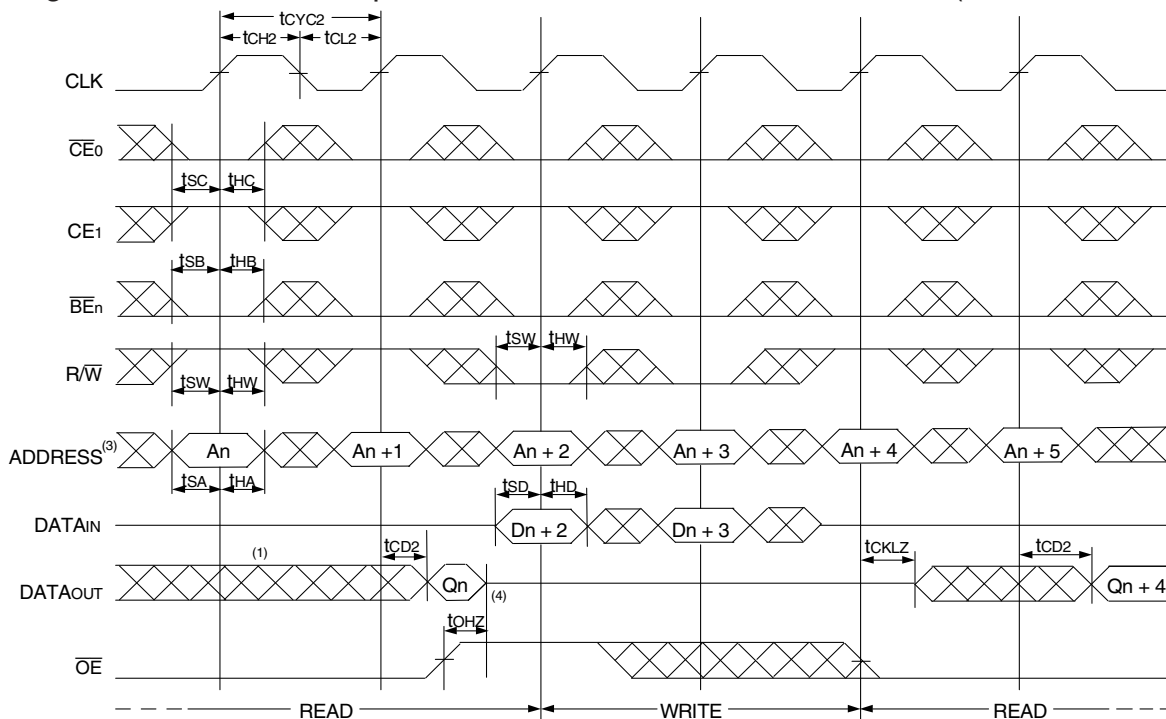


NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2.  $\overline{CE}_0$ ,  $\overline{BE}_n$ , and  $\overline{ADS} = V_{IL}$ ;  $CE_1$ ,  $CNTEN$ , and  $REPEAT = V_{IH}$ . "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be rewritten to guarantee data integrity.

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### Timing Waveform of Pipelined Read-to-Write-to-Read ( $\overline{OE}$ Controlled)<sup>(2)</sup>

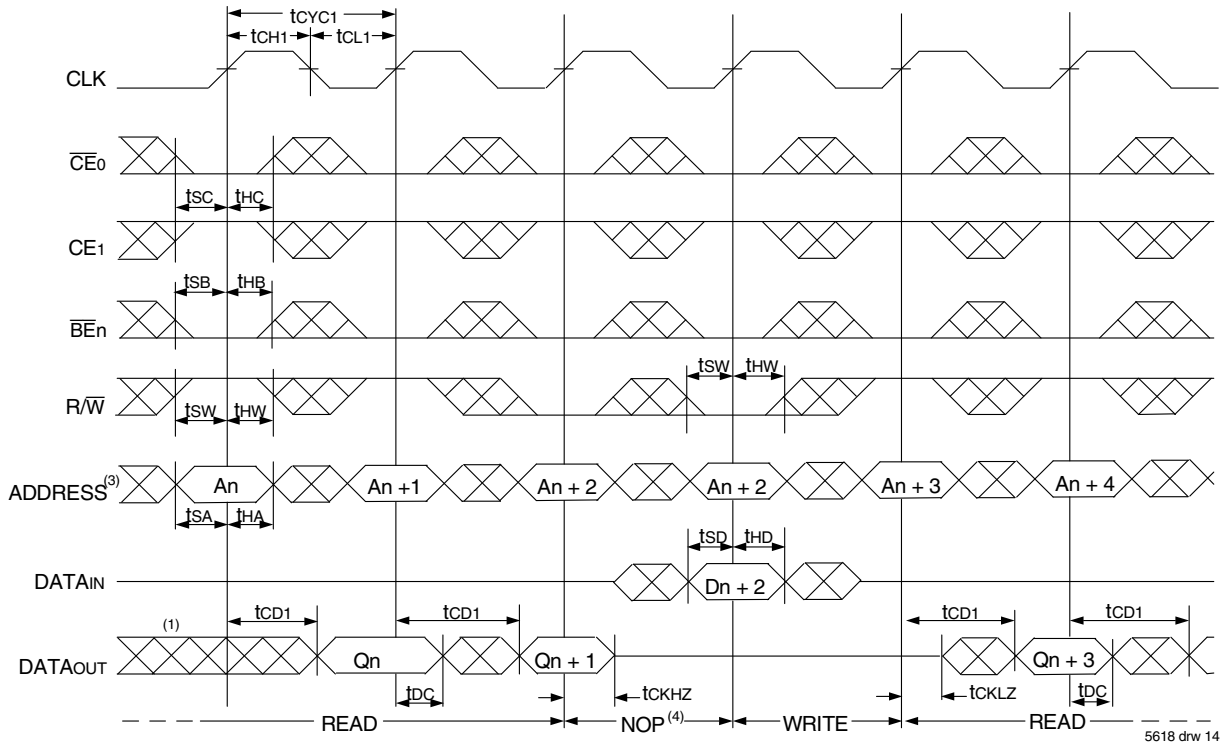


NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2.  $\overline{CE}_0$ ,  $\overline{BE}_n$ , and  $\overline{ADS} = V_{IL}$ ;  $CE_1$ ,  $CNTEN$ , and  $REPEAT = V_{IH}$ .
3. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

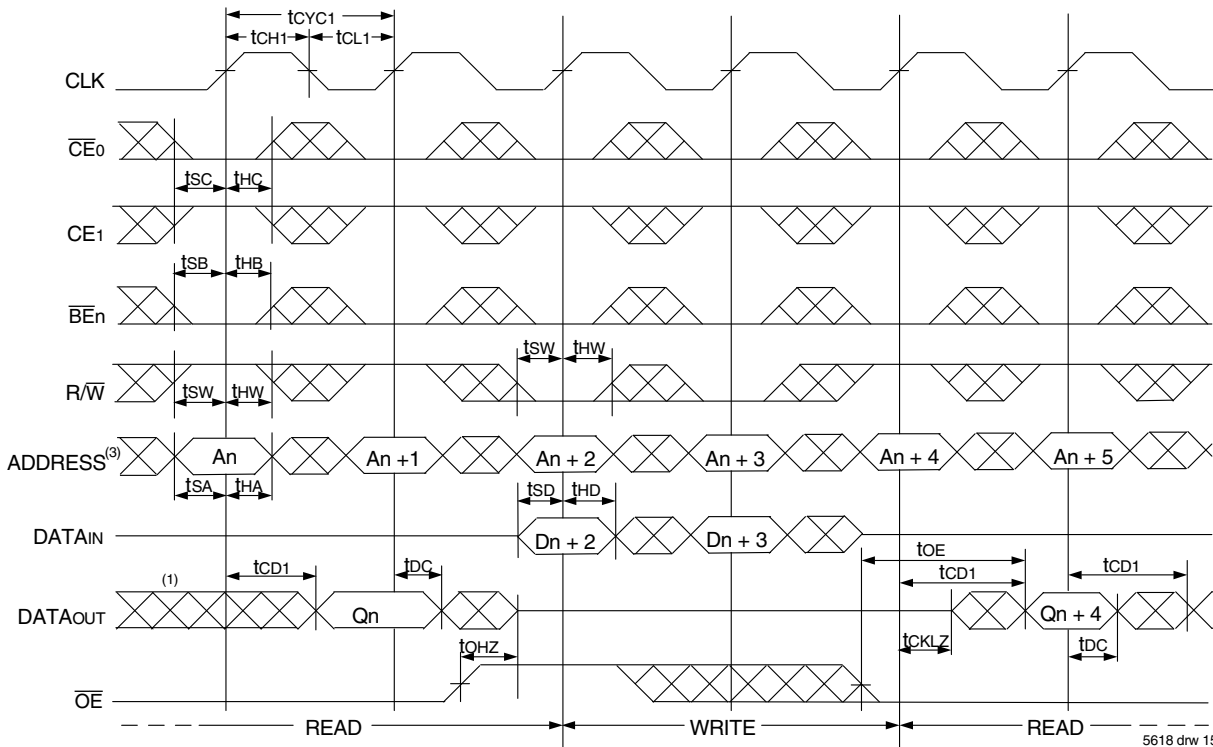
5618 drw 13

Timing Waveform of Flow-Through Read-to-Write-to-Read ( $\overline{OE} = V_{IL}$ )<sup>(2)</sup>



5618 drw 14

Timing Waveform of Flow-Through Read-to-Write-to-Read ( $\overline{OE}$  Controlled)<sup>(2)</sup>



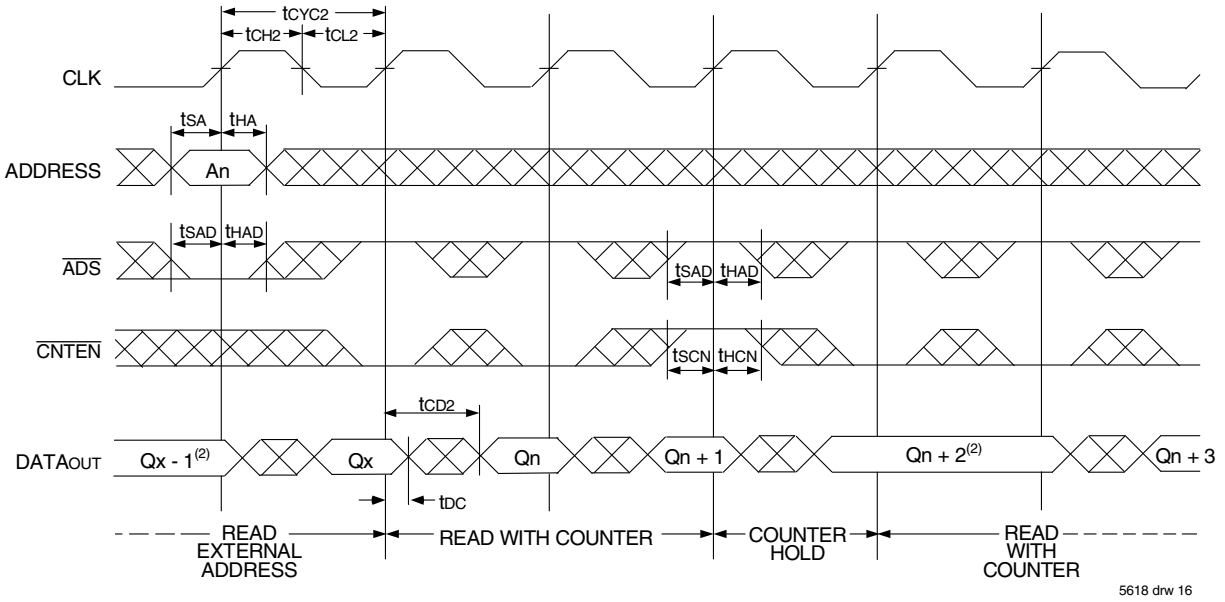
5618 drw 15

NOTES:

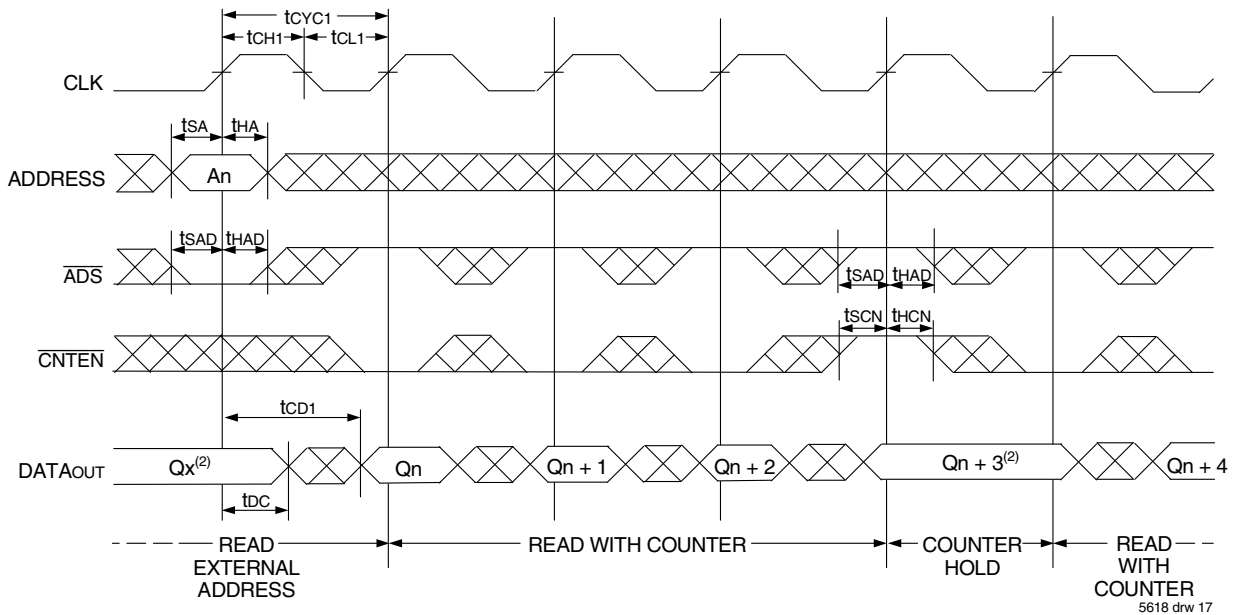
1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2.  $\overline{CE0}$ ,  $\overline{BEn}$ , and  $\overline{ADS} = V_{IL}$ ;  $\overline{CE1}$ ,  $\overline{CNTEN}$ , and  $\overline{REPEAT} = V_{IH}$ .
3. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be rewritten to guarantee data integrity.



### Timing Waveform of Pipelined Read with Address Counter Advance<sup>(1)</sup>



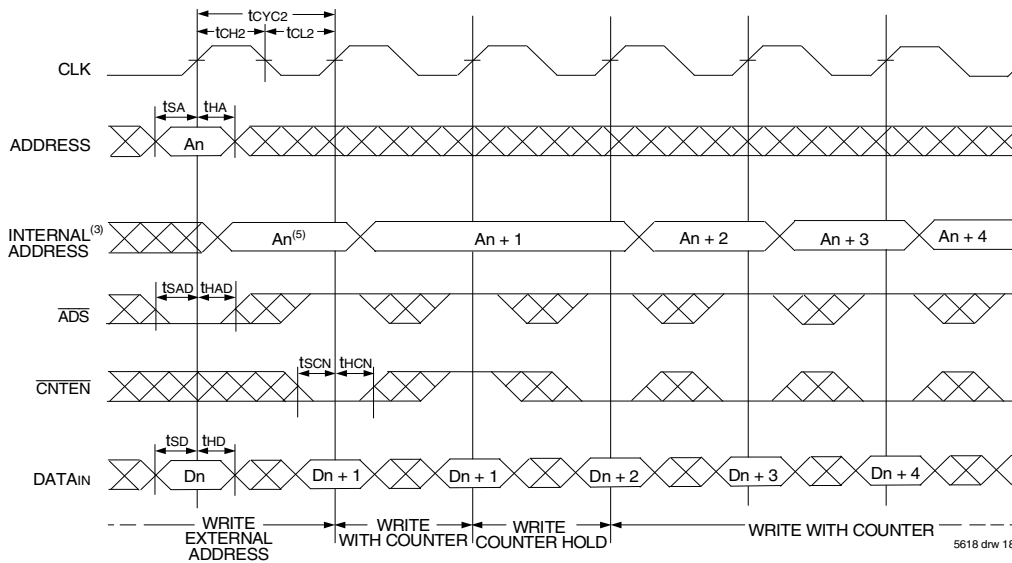
### Timing Waveform of Flow-Through Read with Address Counter Advance<sup>(1)</sup>



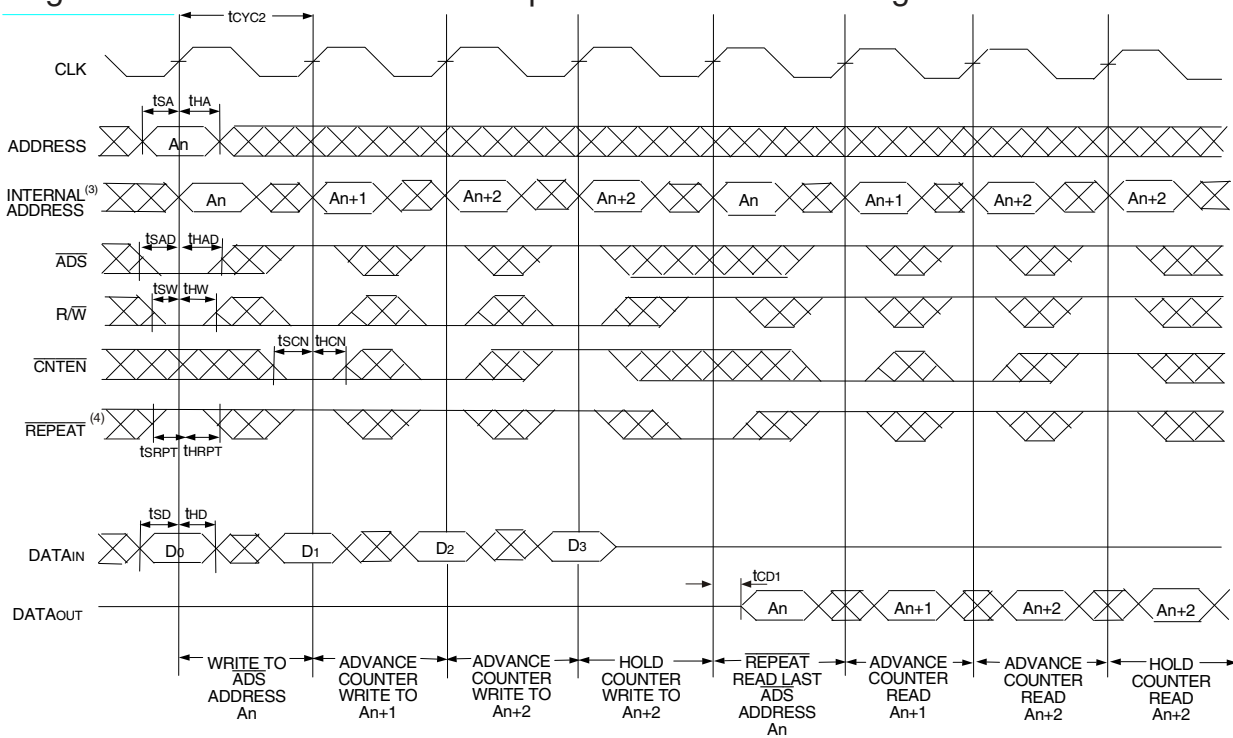
**NOTES:**

1.  $\overline{CE}_0, \overline{OE}, \overline{BE}_n = V_{IL}; CE_1, R\overline{W}, \text{ and } \overline{REPEAT} = V_{IH}.$
2. If there is no address change via  $\overline{ADS} = V_{IL}$  (loading a new address) or  $\overline{CNTEN} = V_{IL}$  (advancing the address), i.e.  $\overline{ADS} = V_{IH}$  and  $\overline{CNTEN} = V_{IH}$ , then the data output remains constant for subsequent clocks.

## Timing Waveform of Write with Address Counter Advance (Flow-through or Pipelined Inputs)<sup>(1,6)</sup>



## Timing Waveform of Counter Repeat for Flow Through Mode<sup>(2,6,7)</sup>



NOTES:

1.  $\overline{CE}_0$ ,  $\overline{BE}_n$ , and  $R/\overline{W} = V_{IL}$ ;  $CE_1$  and  $\overline{REPEAT} = V_{IH}$ .
2.  $\overline{CE}_0$ ,  $\overline{BE}_n = V_{IL}$ ;  $CE_1 = V_{IH}$ .
3. The "Internal Address" is equal to the "External Address" when  $\overline{ADS} = V_{IL}$  and equals the counter output when  $\overline{ADS} = V_{IH}$ .
4. No dead cycle exists during  $\overline{REPEAT}$  operation. A READ or WRITE cycle may be coincidental with the counter  $\overline{REPEAT}$  cycle: Address loaded by last valid  $\overline{ADS}$  load will be accessed. For more information on  $\overline{REPEAT}$  function refer to Truth Table II.
5.  $\overline{CNTEN} = V_{IL}$  advances Internal Address from 'An' to 'An + 1'. The transition shown indicates the time required for the counter to advance. The 'An + 1' Address is written to during this cycle.
6. The counter includes bank address and internal address. The counter will advance across bank boundaries. For example, if the counter is in Bank 0, at address FFFh, and is advanced one location, it will move to address 0h in Bank 1. By the same token, the counter at FFFh in Bank 63 will advance to 0h in Bank 0.
7. For Pipelined Mode user should add 1 cycle latency for outputs as per timing waveform of read cycle for pipelined operations.

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## Functional Description

The IDT70V7519 is a high-speed 256Kx36 (9 Mbit) synchronous Bank-Switchable Dual-Ported SRAM organized into 64 independent 4Kx36 banks. Based on a standard SRAM core instead of a traditional true dual-port memory core, this bank-switchable device offers the benefits of increased density and lower cost-per-bit while retaining many of the features of true dual-ports. These features include simultaneous, random access to the shared array, separate clocks per port, 166 MHz operating speed, full-boundary counters, and pinouts compatible with the IDT70V3599 (128Kx36) dual-port family.

The two ports are permitted independent, simultaneous access into separate banks within the shared array. Access by the ports into specific banks are controlled by the bank address pins under the user's direct control: each port can access any bank of memory with the shared array that is not currently being accessed by the opposite port (i.e., BA0L - BA5L ≠ BA0R - BA5R). In the event that both ports try to access the same bank at the same time, neither access will be valid, and data at the two specific addresses targeted by the ports within that bank may be corrupted (in the case that either or both ports are writing) or may result in invalid output (in the case that both ports are trying to read).

The IDT70V7519 provides a true synchronous Dual-Port Static RAM

interface. Registered inputs provide minimal setup and hold times on address, data and all critical control inputs.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on  $\overline{CE_0}$  or a LOW on CE1 for one clock cycle will power down the internal circuitry on each port (individually controlled) to reduce static power consumption. Dual chip enables allow easier banking of multiple IDT70V7519s for depth expansion configurations. Two cycles are required with  $\overline{CE_0}$  LOW and CE1 HIGH to read valid data on the outputs.

## Depth and Width Expansion

The IDT70V7519 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V7519 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 72-bits or wider.

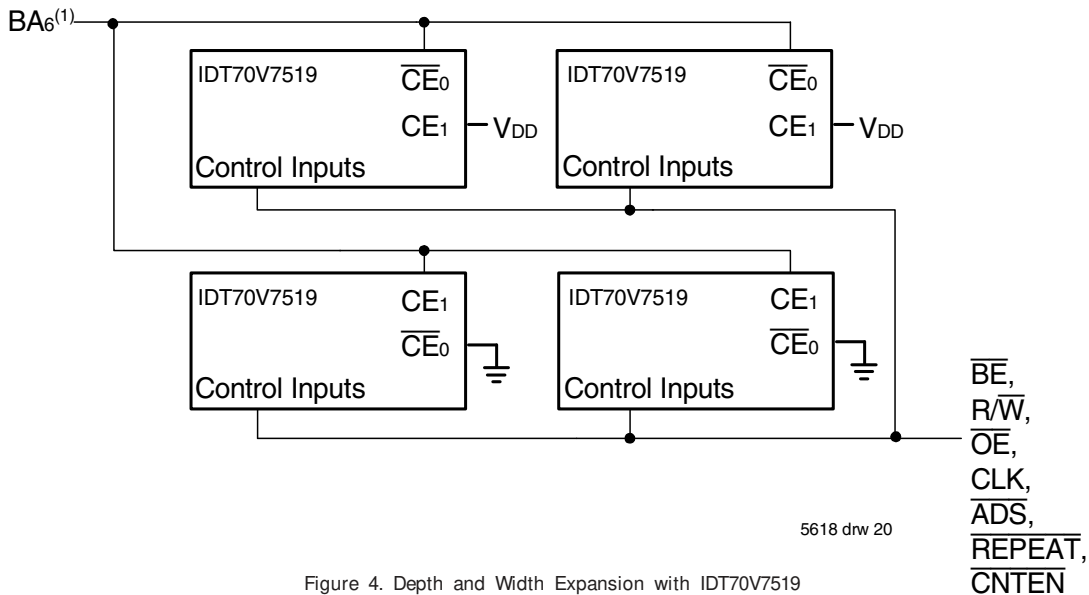
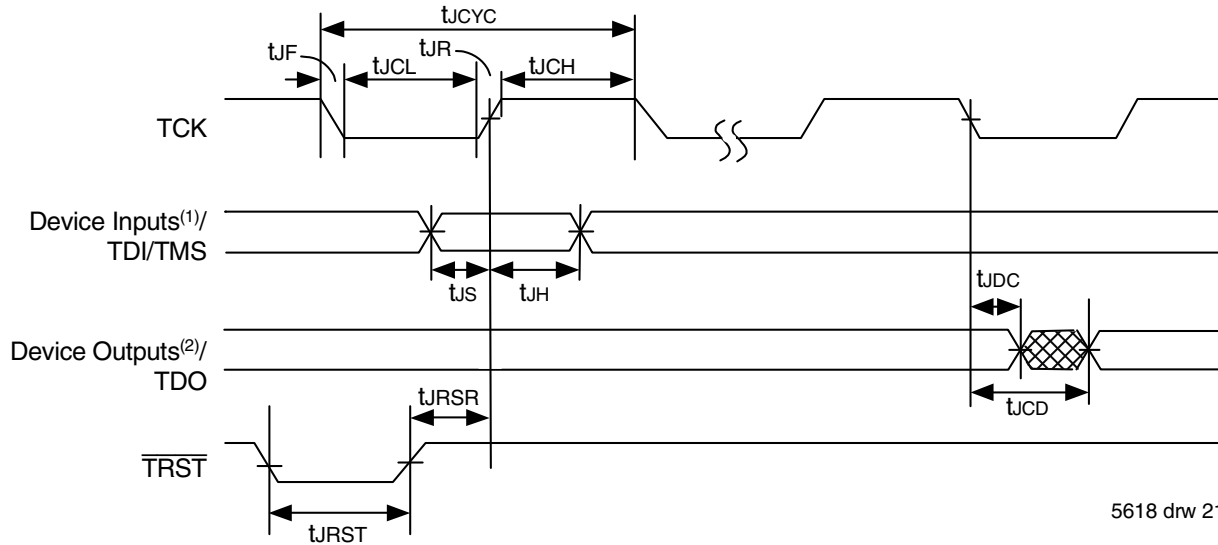


Figure 4. Depth and Width Expansion with IDT70V7519

NOTE:

1. In the case of depth expansion, the additional address pin logically serves as an extension of the bank address. Accesses by the ports into specific banks are controlled by the bank address pins under the user's direct control: each port can access any bank of memory within the shared array that is not currently being accessed by the opposite port (i.e., BA0L - BA6L ≠ BA0R - BA6R). In the event that both ports try to access the same bank at the same time, neither access will be valid, and data at the two specific addresses targeted by the parts within that bank may be corrupted (in the case that either or both parts are writing) or may result in invalid output (in the case that both ports are trying to read).

## JTAG Timing Specifications



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Figure 5. Standard JTAG Timing

NOTES:

1. Device inputs = All device inputs except TDI, TMS, TRST, and TCK.
2. Device outputs = All device outputs except TDO.

## JTAG AC Electrical Characteristics<sup>(1,2,3,4)</sup>

Symbol	Parameter	70V7519		
		Min.	Max.	Units
t <sub>JCYC</sub>	JTAG Clock Input Period	100	—	ns
t <sub>JCH</sub>	JTAG Clock HIGH	40	—	ns
t <sub>JCL</sub>	JTAG Clock Low	40	—	ns
t <sub>JR</sub>	JTAG Clock Rise Time	—	3 <sup>(1)</sup>	ns
t <sub>JF</sub>	JTAG Clock Fall Time	—	3 <sup>(1)</sup>	ns
t <sub>JRST</sub>	JTAG Reset	50	—	ns
t <sub>JRSR</sub>	JTAG Reset Recovery	50	—	ns
t <sub>JCD</sub>	JTAG Data Output	—	25	ns
t <sub>JDC</sub>	JTAG Data Output Hold	0	—	ns
t <sub>JS</sub>	JTAG Setup	15	—	ns
t <sub>JH</sub>	JTAG Hold	15	—	ns

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NOTES:

1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

## Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	0x0	Reserved for version number
IDT Device ID (27:12)	0x300	Defines IDT part number
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register

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## Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
Identification (IDR)	32
Boundary Scan (BSR)	Note (3)

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## System Interface Parameters

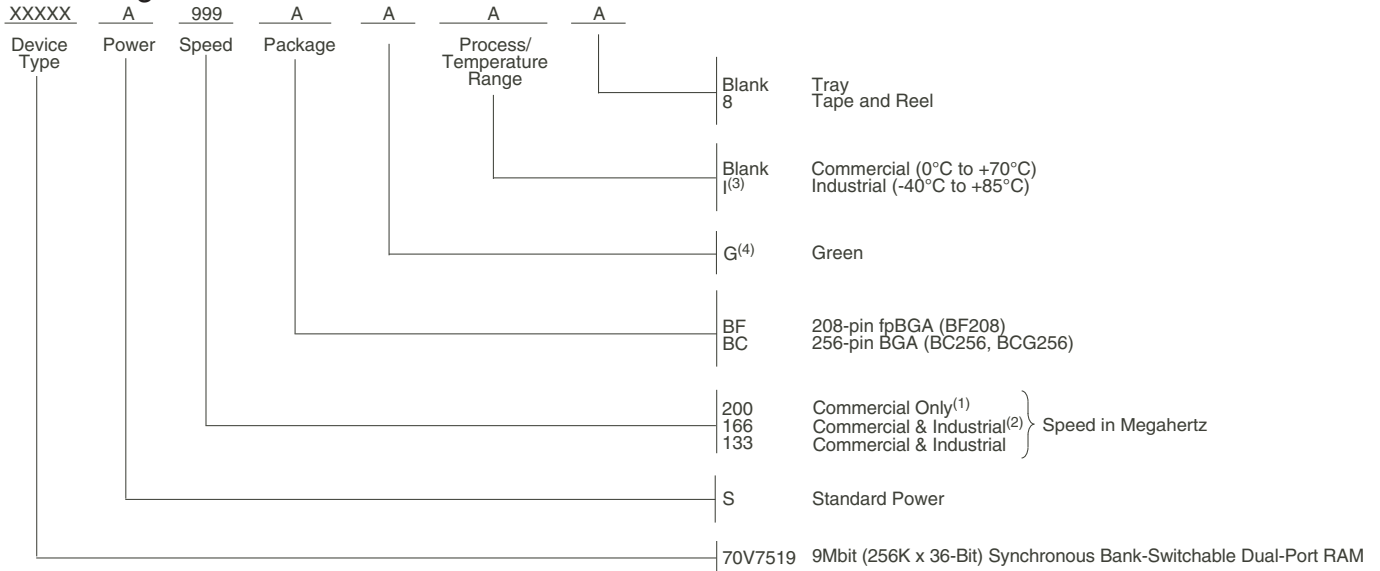
Instruction	Code	Description
EXTEST	0000	Forces contents of the boundary scan cells onto the device outputs <sup>(1)</sup> . Places the boundary scan register (BSR) between TDI and TDO.
BYPASS	1111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	0010	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0100	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state.
CLAMP	0011	Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO.
SAMPLE/PRELOAD	0001	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs <sup>(2)</sup> and outputs <sup>(1)</sup> to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.
RESERVED	All other codes	Several combinations are reserved. Do not use codes other than those identified above.

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### NOTES:

1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, TRST, and TCK.
3. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website ([www.idt.com](http://www.idt.com)), or by contacting your local IDT sales representative.

## Ordering Information



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### NOTES:

1. Available in BC256 package only.
2. Industrial Temperature at 166Mhz not available in BF208 package.
3. Contact your local sales office for industrial temp range for other speeds, packages and powers.
4. Green parts available. For specific speeds, packages and powers contact your local sales office.

**LEAD FINISH (SnPb) parts are Obsolete excluding BGA & fpBGA. Product Discontinuation Notice - PDN# SP-17-02**  
 Note that information regarding recently obsoleted parts are included in this datasheet for customer convenience.

## Orderable Part Information

Speed (MHz)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
133	70V7519S133BC	BC256	CABGA	C
	70V7519S133BC8	BC256	CABGA	C
	70V7519S133BCI	BC256	CABGA	I
	70V7519S133BCI8	BC256	CABGA	I
	70V7519S133BF	BF208	CABGA	C
	70V7519S133BF8	BF208	CABGA	C
	70V7519S133BFI	BF208	CABGA	I
	70V7519S133BFI8	BF208	CABGA	I
166	70V7519S166BC	BC256	CABGA	C
	70V7519S166BC8	BC256	CABGA	C
	70V7519S166BCI	BC256	CABGA	I
	70V7519S166BCI8	BC256	CABGA	I
	70V7519S166BF	BF208	CABGA	C
	70V7519S166BF8	BF208	CABGA	C
200	70V7519S200BC	BC256	CABGA	C
	70V7519S200BC8	BC256	CABGA	C
	70V7519S200BCG	BCG256	CABGA	C
	70V7519S200BCG8	BCG256	CABGA	C

## Datasheet Document History:

01/05/00:	Initial Public Offering
10/19/01:	<p>Page 2, 3 &amp; 4 Added date revision for pin configurations</p> <p>Page 9 Changed I<sub>SB3</sub> values for commercial and industrial DC Electrical Characteristics</p> <p>Page 11 Changed t<sub>OE</sub> value in AC Electrical Characteristics, please refer to Errata #SMEN-01-05</p> <p>Page 20 Increased t<sub>UCD</sub> from 20ns to 25ns, please refer to Errata #SMEN-01-04</p> <p>Page 1 &amp; 22 Replaced ™ logo with ® logo</p>
01/11/02:	Page 2 Corrected BF-208 pinout configuration fpBGA A15
03/18/02:	<p>Page 1, 9, 11 &amp; 22 Added 200MHz specification</p> <p>Page 9 Tightened power numbers in DC Electrical Characteristics</p> <p>Page 14 Changed waveforms to show INVALID operation from opposite ports if t<sub>CO</sub> &lt; minimum specified</p> <p>Page 1 - 22 Removed "Preliminary" status</p>
12/04/02:	Page 9, 11 & 22 Designated 200Mhz speed grade available in BC-256 package only
01/16/04:	Page 11 Added byte enable setup time and byte enable hold time parameters and values to all speed grades in the AC Electrical Characteristics Table
07/25/08:	Page 9 Corrected a typo in the DC Chars table
01/29/09:	Page 22 Removed "IDT" from orderable part number
06/04/15:	<p>Page 1 Added Green availability to Features</p> <p>Page 2, 3, 4 &amp; 22 The package codes for BF-208 changed to BF208, BC-256 changed to BC256, and DR-208 changed to DR208 respectively to match the standard package codes</p> <p>Page 2, 3 &amp; 4 Removed the date from all of the pin configurations BF208, BC256 &amp; DR208</p> <p>Page 22 Added Green and T&amp;R indicators and the correlating footnotes to Ordering Information</p>
06/22/18:	<p>Product Discontinuation Notice - PDN# SP-17-02</p> <p>Last time buy expires June 15, 2018</p>
10/16/19:	<p>Page 1 &amp; 22 Deleted obsolete DR208 PQFP package code</p> <p>Page 2 &amp; 3 Updated package codes</p> <p>Page 22 Added Orderable Part Information table</p>
11/01/19:	Page 22 Corrected "ns" to "MHz" in the header of the Orderable Part Information table

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